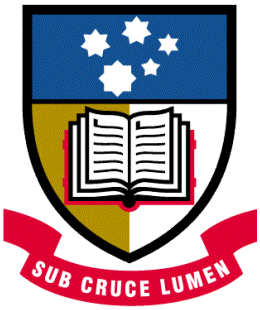

THE UNIVERSITY OF ADELAIDE

School of Electrical and Electronic Engineering

Investigation and Analysis of Decentralised Multilevel Modular Integrated Converters in Small Scale Grid-Tied PV Systems

A Thesis Submitted for the
Degree of Doctor of Philosophy

By

David Matthew Scholten

Submitted: March 2017

Principal Supervisor:
Associate Professor Nesimi Ertugrul
Co-Supervisor:
Associate Professor Wen Soong

I dedicate this thesis to Yuli Chen.

Table of Contents

I. Abstract

This research focuses on the analysis of multilevel voltage interleaving for decentralised cascaded micro inverters in small scale photovoltaic (PV) grid tied applications. These decentralised cascaded micro inverters, otherwise known and modular integrated converters (MICs), have previously been implemented both with multilevel voltage interleaving (requires fast and reliable communications for PV power tracking) and without (requires no communications). The approach proposed by this research utilises a hybrid of both multilevel and non-multilevel switching, which reduces the communications requirement down to less than one system-wide update per second (whilst still allowing for a reduced filter size and lower switching frequency). In addition to the benefits of multilevel switching, the cascaded topology does not require a high gain DC-DC boost stage and maintains the ability to track the power of each PV panel independently.

It was found that the optimal number of MICs for a cascaded system should be between 4 and 8 and that such a system should utilise a 1st order inductive filter. Prototype MICs were developed and a comparison was made between a parallel and 2-MIC cascaded system that found an increase in both the efficiency (94.8% to 95.9%) and the total harmonic distortion (THD) (4.8% to 5.2%) for the cascaded system. Additionally, a grid zero-crossing detection error of just 4° in the cascaded system generated enough harmonics to exceed allowable THD limits. The implemented 4-MIC decentralised cascaded system utilised a round robin greedy sorting algorithm to sort power blocks for PV multilevel power tracking with an allocation error generally below 2%. Accounting for typical solar irradiance transient conditions and harmonic standards, it was found that a communications update rate of 0.7Hz is required. Additionally, it was found that grid-tied cascaded MICs have fundamental power sharing ratio limitations that restrict the maximum shading of one MIC to 74% in the 4-MIC system.

II. Statement of Originality

I certify that this work contains no material which has been accepted for the award of any other degree or diploma in my name, in any university or other tertiary institution and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text. In addition, I certify that no part of this work will, in the future, be used in a submission in my name, for any other degree or diploma in any university or other tertiary institution without the prior approval of the University of Adelaide and where applicable, any partner institution responsible for the joint-award of this degree.

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I acknowledge the support I have received for my research through the provision of an Australian Government Research Training Program Scholarship.

Signed: David Scholten **Date**: 26/03/17

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IV. Publications

[1] D. Scholten, N. Ertugrul, Wen L. Soong, "Micro-Inverters in Small Scale PV Systems: A Review and Future Directions", Australasian Universities Power Engineering Conference, (AUPEC 2013), 29th September, 2013.

[2] D. Scholten, N. Ertugrul, Wen L. Soong, "Analysis and Control of Decentralized PV Cascaded Multilevel Modular Integrated Converters", IEEE Energy Conversion Congress and Exposition (ECCE 2016).

Pending Publications:

[3] D. Scholten, N. Ertugrul, Wen L. Soong, "Detailed Analysis of Decentralised Multilevel Cascaded and Parallel Photovoltaic Converters", International Journal of Electrical Power & Energy Systems (2016).

[4] D. Scholten, N. Ertugrul, Wen L. Soong, "Analysis and Control of Decentralized PV Cascaded Multilevel Modular Integrated Converters", Journal of Emerging and Selected Topics in Power Electronics (2017).

V. List of Figures

VI. List of Tables

VII. Abbreviations & Acronyms

AC	Alternating Current
ADC	Analogue to Digital Converter
BOM	Bill Of Materials
CEC	California Energy Commission
CHB	Cascaded H-Bridge
DAC	Digital to Analogue Converter
DC	Direct Current
DMC	Decentralised Multilevel Cascaded
DIP	Dual In-line Package
DPP	Differential Power Processing
EOP	Ethernet Over Power
FC	Flying Capacitor
HF	High Frequency
HVDC	High Voltage Direct Current
IDE	Interactive Development Environment
IEEE	Institute of Electrical & Electronic Engineers
MIC	Modular Integrated Converter
MPP	Maximum Power Point
MPPT	Maximum Power Point Tracking
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
PF	Power Factor
PLC	Power Line Communications
PV	Photo-Voltaic
PWM	Pulse Width Modulation
RMS	Root Mean Squared
SPWM	Sinusoidal Pulse Width Modulation
THD	Total Harmonic Distortion

VIII. Symbols

C	Capacitance
f	Frequency
I_D	Diode Current
I_{DC}	Average Current (DC)
I_{MPP}	Maximum Power Point Current
I_{photon}	Photon-Influenced Current
$I_{Ripple(pp)}$	Peak-to-Peak Current (AC)
I_{RMS}	Root Mean Squared Current
I_{SC}	Short Circuit Current
IV	Current-Voltage
L	Inductance
P_{Avg}	Average Power
φ	Phase Angle
P_{Max}	Maximum Power
p-n	Positive-Negative
R_s	Series Resistance
R_{sh}	Shunt Resistance
V_{DC}	Average Voltage (DC)
V_{MPP}	Maximum Power Point Voltage
V_{OC}	Open Circuit Voltage
$V_{Ripple(pp)}$	Peak-to-Peak Voltage (AC)
V_{RMS}	Root Mean Squared Voltage
ω	Angular Velocity
Z_C	Capacitive Impedance
Z_g	Grid Impedance
Z_L	Inductive Impedance
Z_{th}	Thevenin's Equivalent Impedance

1 Introduction

Small scale photovoltaic (PV) systems (residential rooftop systems with 25 or fewer PV panels totalling less than 5kW) are widely used to generate, store and share power with the grid. In order to increase inverter system efficiencies, it is desirable to utilise cascaded multilevel waveform converters that take advantage of the multi-source nature of PV arrays to reduce switching frequencies, filter sizes and PV utilisation losses from non-uniform shading. However, small rooftop applications favour decentralised systems that do not require complex wiring between a central controller and multiple PV sources. Thus, there is an incentive to develop simple decentralised cascaded multilevel converters for small scale residential application. Fig 1-1 shows a block diagram of the functionality of the modern rooftop inverter system, which ultimately tries to maximise the power extracted from the PV panels (PV utilisation) and minimise the conversion losses in the actual inverter (inverter efficiency).

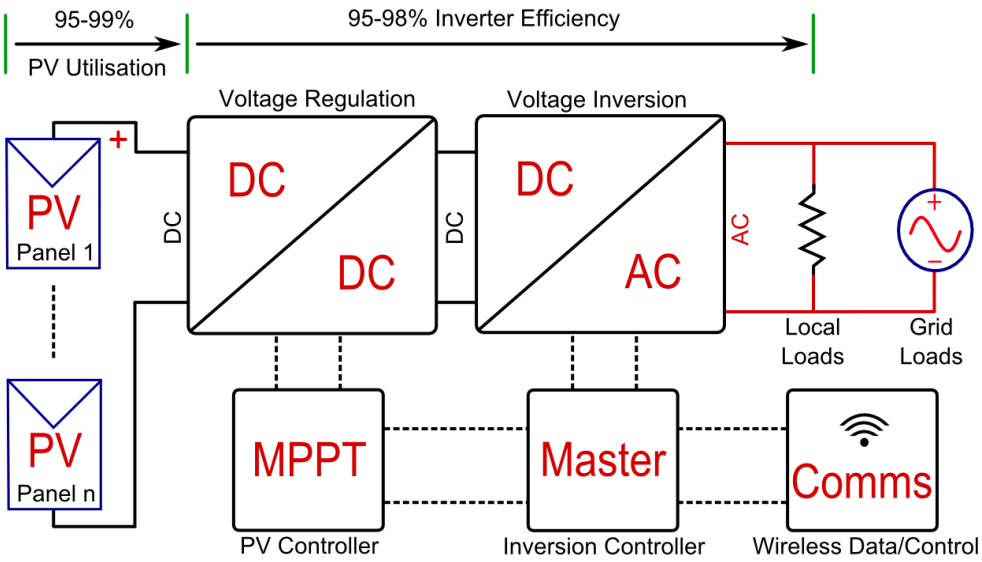

Fig 1-1. The functional components of a modern grid-tied inverter system.

1.1 PV System Basics

Since the industrial revolution, humanity's demand for energy has been increasing at an astounding rate. Fossil fuels are currently the primary source of energy and will continue to be so until a convenient alternative is found. Solar energy is nearly limitless and its direct

utilisation is limited by only by our ability to capture it with current PV technology. Comprehensively described by Einstein's 1905 paper on the photoelectric effect [1], the energy of an incoming photon can be transferred to an electron, converting sunlight into useful electricity. This is typically accomplished today in PV cells through the use of the positive-type to negative-type doped silicon junction seen in Fig 1-2a. Incoming photons strike electrons, liberating them from the silicon lattice and into the conduction band, allowing them to cross the interfacing depletion layer. This forms a potential difference, which when connected to a load, creates a current that can be utilised to generate electrical power.

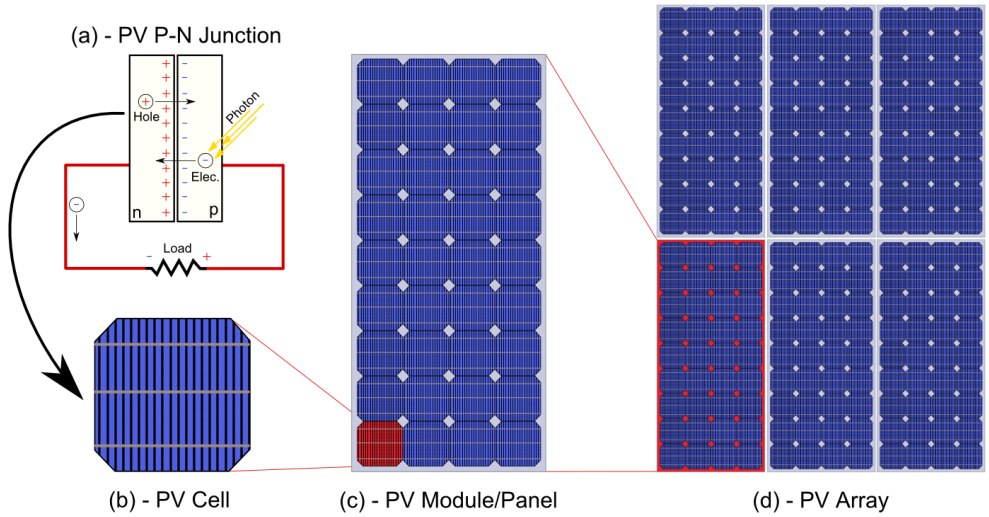

Fig 1-2. The PV p-n junction (a) and its implementation as a PV cell (b), a module (c) and as an array (d).

As shown in Fig 1-2b, a PV cell is a high surface area PV p-n junction. These modern commercial cells will have an open-circuit voltage of 600mV with a typical working photo-electrical efficiency of 10-20%. These PV cells are usually connected in series to form PV modules (Fig 1-2c) with higher voltages and rated life spans of 20-25 years. For mass power generation, these PV modules are then again connected in series to form PV arrays (Fig 1-2d) with mains level voltages (100V+) for interfacing with the grid. From the solar powered calculators of 1978 to the modern household inverter system of today, silicon PV cells have dropped from over $50 USD per Watt down to less than $0.30 USD per Watt [2], becoming a serious cost competitor to traditional fossil fuel sources.

A PV cell or module on its own is only capable of producing a power in the presence of sunlight. Practically, to make good use of PV technology, a battery is needed to store the produced electrical energy for use when sunlight is insufficient. Traditionally, lead acid batteries have been used in the past to safely store mass quantities of energy. Recently, this role has been replaced by more modern lithium battery chemistries, with Lithium-Iron (LiFe) being one of the safest and most suited to the task. To then use this energy, an inverter converts power from the DC battery to an AC voltage at mains magnitudes, which can then be utilised by typical household appliances. These inverter systems (Fig 1-3a) are known as stand-alone inverters as they cannot connect to the electrical grid and therefore operate as isolated generators only.

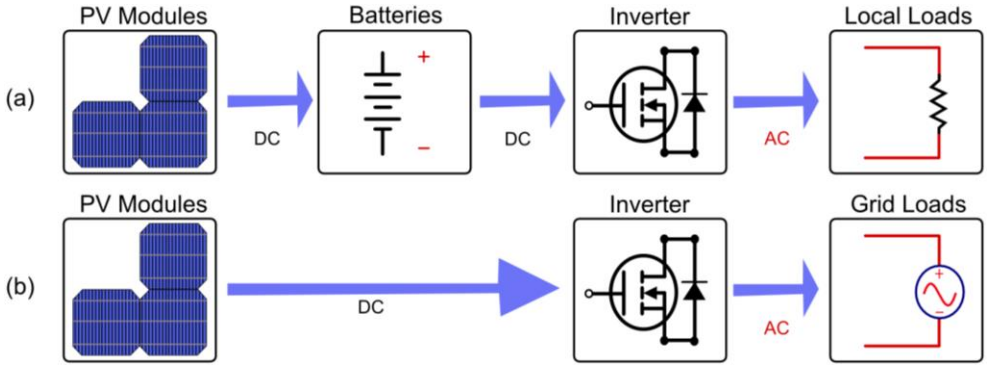

Fig 1-3. Stand-alone (a) and grid-tied (b) inverters systems. See Fig 1-1 for details on (b).

However, the grid-tied inverter (Fig 1-3b), which is the most common inverter system as of 2016, connects directly to the electrical grid to inject power into the transmission system. By doing this, the inverter now supplies energy not only to local loads within the household, but can supply power to distant loads connected elsewhere on the electrical grid. This occurs when there is a surplus of generated energy (net export). Critically though, when the PV power generation runs short of supplying the local household, power is instead sourced from the grid to supply difference for the local loads (net import). Effectively, the grid now acts as a battery with an infinite capacity that absorbs the fluctuating difference between the local PV power generated and local power consumed. However, in the absence of a grid voltage (i.e. an electrical blackout) a conventional grid-tied inverter system shuts down. This is to protect personnel working on power lines that

are assumed to not be live. Thus, the grid-tied inverter acts as a standalone (but dependant) power generation system on the grid as seen in Fig 1-1.

1.2 PV Maximum Power Point

Typical PV cells exhibit the current-voltage (IV) characteristic curve as seen in Fig 1-4a. From this curve, five basic characteristics that are critical to the design of any inverter system can be derived. These characteristics are the open-circuit voltage (V_{OC}), the short circuit current (I_{SC}), the voltage/current at the maximum power point (V_{MPP} & I_{MPP}) and the maximum power itself (P_{Max}). It is the goal of any inverter system to operate the PV cell at its maximum power point (MPP) in any situation, as any other operating point is wasting possible energy (i.e. poor utilisation).

The single diode electrical equivalent model of the PV cell is seen in Fig 1-4b, which is made up of a photon and temperature sensitive current source, a characterised thermally sensitive diode, a shunting resistor (R_{Sh}) and a series source resistor (R_S). Given the key variables of Fig 1-4a (and thermal coefficients), it is possible to characterise the model components of Fig 1-4b and simulate any typical PV cell with a fairly high degree of accuracy [3, 4].

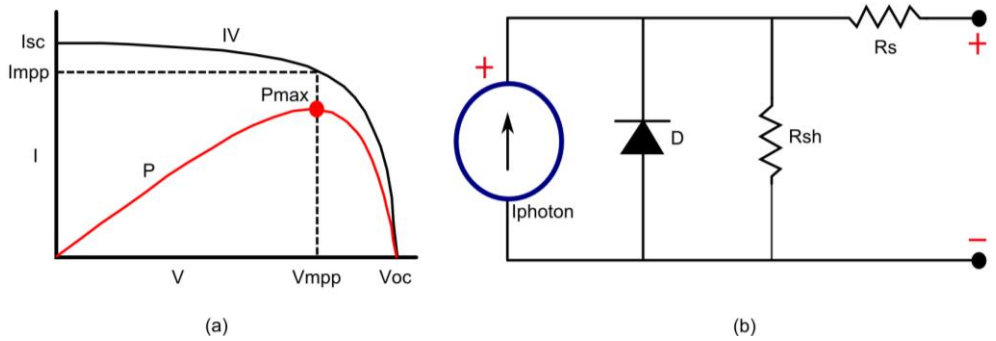

Fig 1-4. The IV characteristic curve (a) and the single diode equivalent electrical model (b) for a photovoltaic cell.

In an operational PV system, a PV panel's IV characteristics is primarily affected by two prevailing factors, which is the solar irradiance (Fig 1-5a) and the cell temperature (Fig 1-5b). As the solar irradiance increases it is primarily the I_{MPP} of the cell that increases with it, greatly boosting P_{Max} (Fig 1-5c). Conversely, as the temperature increases the general operating voltage decreases, significantly left shifting the V_{MPP} and

decreasing P_{Max} (Fig 1-5d). Ultimately, the V_{MPP}, I_{MPP} and P_{Max} of a PV panel will vary significantly in operation, requiring a constant readjustment of the applied load to track the MPP. This load manipulation to follow the MPP is known as maximum power point tracking (MPPT).

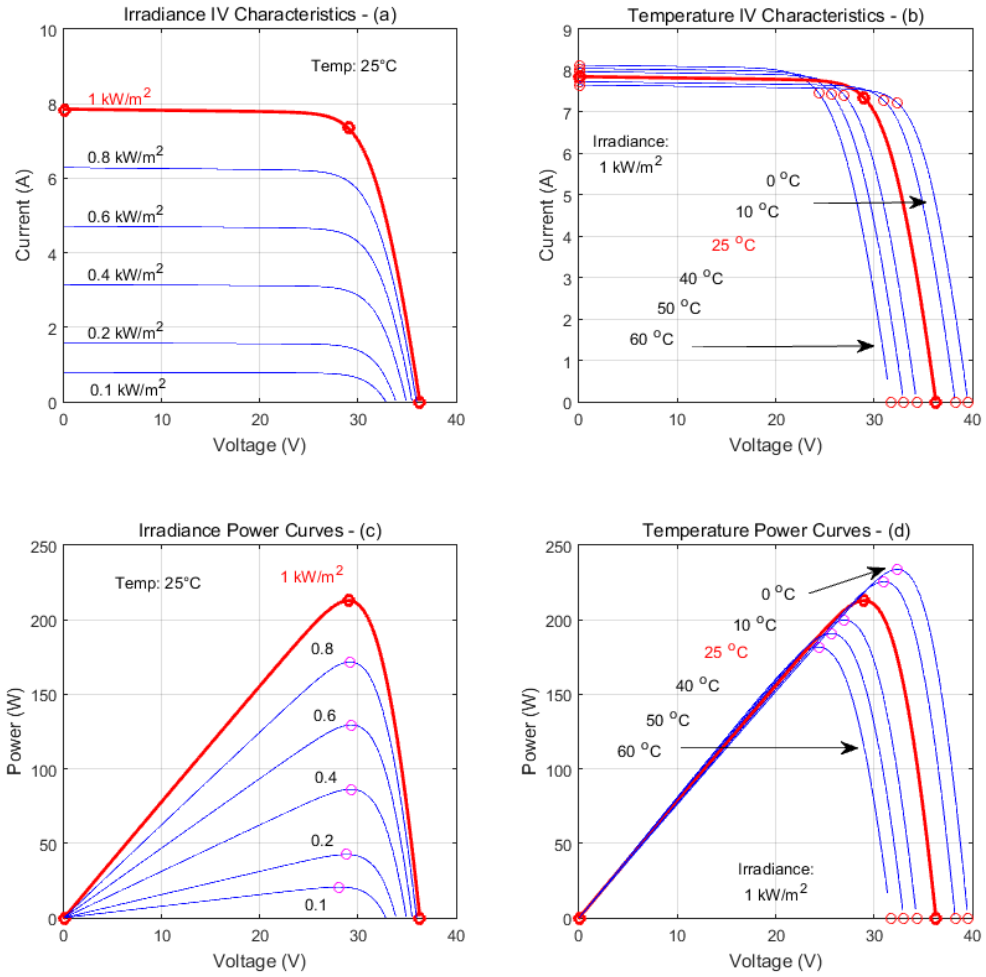

Fig 1-5. The IV characteristic curves for different solar irradiances (a), temperatures (b) and the power curves for different solar irradiances (c) and temperatures (d). Generated from a characterised single diode PV model for the Soltech 250W Panel (1Soltech 1STH-250-WH).

By constantly readjusting the load applied to a PV panel in response to a changing measured power level, it is possible to operate at a varying MPP. For a grid-connected inverter system with a PV panel, the load adjustment means changing the amount of current injected into the grid through the inverter. The Perturb and Observe algorithm (P&O) is the most widely used form of MPPT due to its simplicity and minimal parameter requirements. A grid-connected inverter using P&O periodically perturbs the PV panel's

operating point (i.e. grid current) and then compares the measured power before and after the perturbation (Fig 1-6). However, P&O and other similar algorithms [5] make assumptions that the IV characteristic curve of the PV module has only one obvious MPP.

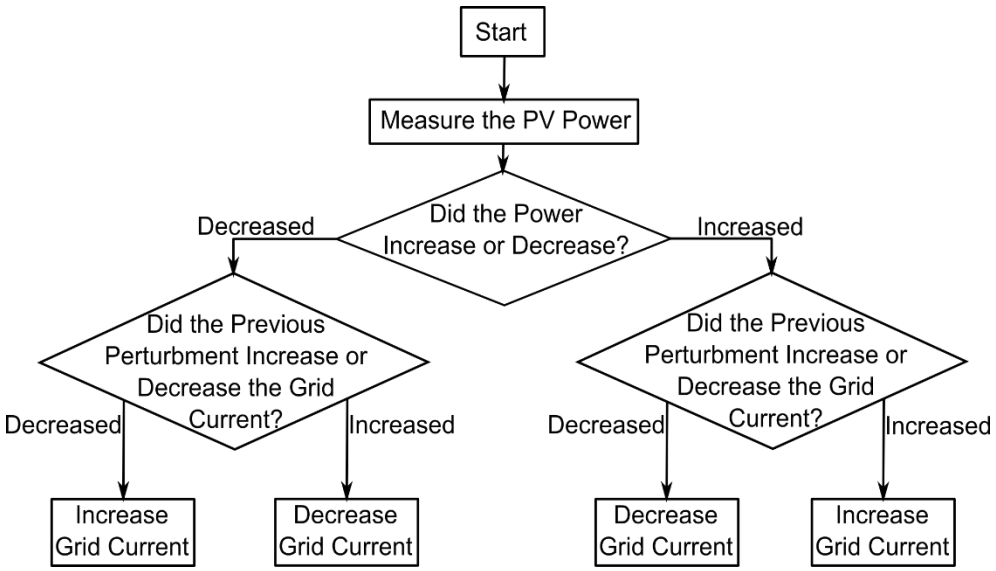

Fig 1-6. The periodic "Perturb and Observe" (P&O) algorithm flow diagram for a grid-tied inverter.

In a practical system, series connected PV modules may experience power mismatches between themselves due to non-uniform shading (trees) and other factors that can mimic non-uniform PV power distribution (i.e. dirt, manufacturing mismatch, age, angling, etc.). Shaded (or under-powered) PV modules will dissipate power from the non-shaded/over-powered modules, causing them to quickly heat up and create hot spots in a PV array. To help alleviate this, bypass diodes are connected in parallel with each PV module in an array (Fig 1-7a), allowing current to pass around shaded modules, but only in the most in extreme circumstances. Typically, these bypass diodes are not active and non-uniform shading produces multiple power peaks [6, 7] that are hard to differentiate from each other with simple MPPT techniques. As a result, simple algorithms like P&O may become stuck on a power peak that is not the true system MPP during non-uniform shading conditions in a PV array as shown in Fig 1-7b.

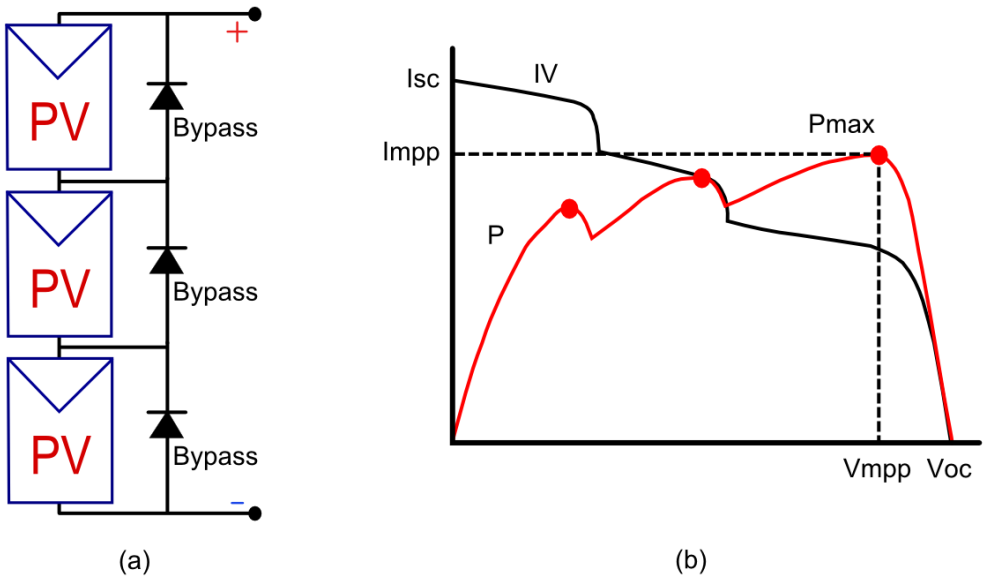

Fig 1-7. Series connected PV modules with extreme-case bypass diodes (a) and the typical IV characteristics of series connected PV modules with moderate non-uniform shading (b).

To account for the non-uniform shading across series connected PV modules (arrays), MPPT algorithms must take an approach that falls in the spectrum between two fundamental techniques: Either an MPPT algorithm makes no assumptions about the shape of PV IV characteristics (i.e. the entire IV curve is scanned periodically for the MPP) or instead the series connected PV modules are modelled in their entirety based on inferred parameters [8].

It should be noted that non-uniform shading conditions can actually occur between the PV cells of a PV module itself, forcing a smaller localised iteration of the same series connected MPPT issues. However, due to the physically close proximity of the PV cells to each other in the PV module itself, any of the conditions that would affect one cell would likely affect the whole module regardless. Additionally, the PV module would have been manufactured from a batch of electrically matching PV cells, which is not the case when comparing entire modules within PV arrays. Thus, a practical compromise is to only utilise bypassing techniques for entire PV modules and not PV cells.

1.3 Grid Requirements

A traditional electrical grid is comprised of interconnected generators, transmission/distribution lines and commercial/residential loads. However, the advent of

distributed generation (from both commercial PV/wind and residential PV sources) is changing the standard model of the electrical grid. In PV systems, specifically residential, this results in customers rapidly switching between consuming and producing electrical power as the solar irradiance changes throughout the day.

For the influx of the low voltage grid-tied residential inverters, specific standards have been developed. In Australia (as of 2016), a typical residential PV system is governed by the requirements as set out by AS/NZS 4777.2 [9]. As described by the standards, total harmonic distortion (THD) is a measure of a waveform's distortion in relation to the magnitude of the intended fundamental frequency. A low THD value indicates a pure waveform that is mostly composed of a sinusoid at the fundamental frequency. The Institute of Electrical and Electronic Engineers (IEEE) defines the THD as the ratio of the sum of all the root mean square (RMS) magnitudes of harmonic (H_n) content of a signal to the fundamental content (H_1), expressed as a percentage:

$$\mathrm{THD\%} = 100 \cdot \frac{\sqrt{\sum_{n=2}^{\infty} H_n^2}}{H_1} \qquad \textit{(1-1)}$$

For the Australian grid standards [9] relating to residential grid-tied inverters, the THD of the injected current must be no more than 5% at the rated inverter output power. However, this only takes into consideration the first 50 harmonic frequencies. Additionally, there are specific harmonic restrictions within the overall 5% limitation as given in Table 1-1.

Table 1-1. Harmonic restrictions for a grid-tied inverter [9].

Harmonic Order Number	**Limit of Each Harmonic as a Percentage of the Fundamental**
2 - 50	5%
3, 5 & 7	4%
9, 11 & 13	2%
15, 17 & 19	1%
2, 4, 6 & 8	1%
21, 23, 25, 27, 29, 31 & 33	0.6%
10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, & 32	0.5%

Similarly, power factor (PF) is also defined in sinusoidal systems as the ratio of the real power of a circuit to the apparent power. Therefore, for the electrical grid, it is indicative of the phase angle (ϕ) between the voltage and current waveforms as given below:

$$\text{PF} = \frac{\text{Real Power}}{\text{Apparent Power}} = \cos(\phi) \qquad (1\text{-}2)$$

For a grid-tied inverter (operating between 25% and 100% power) the PF of the generation must not fall below 0.95 (lagging or leading), which translates to a voltage-current phase angle of +/-18.2°. This assumes the inverter is operating in static and stable conditions (at a steady power output, grid voltage and grid frequency). There are various transient situations specified in [9] that allow or demand the power factor be reduced below 0.95.

In addition, the grid-tied inverter must also be aware of the operating status of the grid during operation. If the voltage or frequency exceeds certain bounds then the grid-tied inverter must disconnect. This is known as anti-islanding, which is a technique to avoid the situation of having active live islands of the grid that may electrocute unsuspecting line workers. According to [9] the allowed sustained operating voltage range is 180-258Vrms for Australia. However, as the grid-tied inverter approaches the voltages limits, the standards demand that the PF be adjusted to assist in regulating the grid voltage. Similarly, there is a restricted allowable band of operation for frequency (47-52Hz), which the inverter must help to regulate (with its real power) near the edge of the band. The requirements for a residential grid-tied inverter (summarised in Table 1-2) provide a useful guide for the development of inverter prototypes, which are considered in this research.

Table 1-2. Summary of AS/NZS 4777.2 [9] for residential grid-tied inverters.

Grid Parameter	**Requirement**
THD Limit	5% of Rated Output
Power Factor	0.95-1.0 Lagging/Leading
Voltage Range	180-258Vrms
Frequency Range	47-52Hz
Anti-Islanding	Disconnect Within 2 Seconds & Reconnect After 60 Seconds
DC Injection	0.5% of Rated Output Current or 5mA (Whichever is Greater)

1.4 The Grid-Tied Inverter

It is the function of the grid-tied inverter (e.g. Fig 1-1) to convert energy from a photovoltaic source and inject it into the electrical grid. More specifically, the grid-tied inverter needs to apply MPPT techniques to a DC PV array whilst generating an AC current that meets the grid standards. The challenges facing grid-tied inverters are summarised in Fig 1-8, which show not only the PV/grid requirements from sections 1.2/1.3, but also the other requirements of the inverter. PV panels have unique characteristics that are at odds with the demands of the electrical grid and it is the responsibility of the inverter to interface the two together as efficiently as possible.

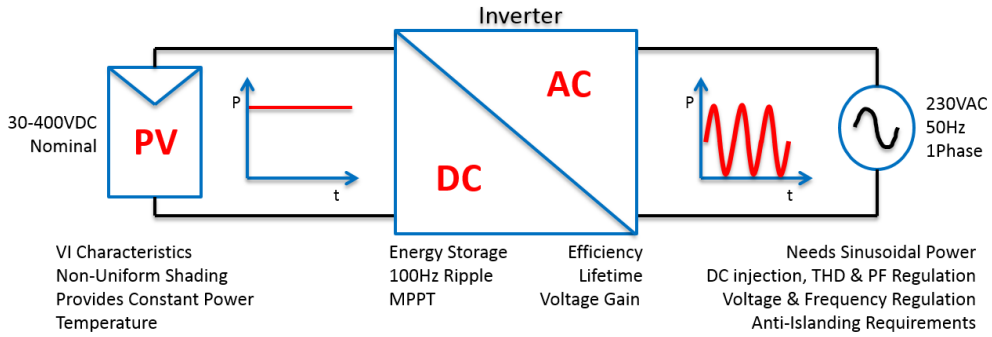

Fig 1-8. The grid-tied inverter with its competing PV and grid requirements.

Ideally, the grid-tied inverter needs to match the 20-25 year lifespan of the PV panels and should have a high conversion efficiency to maximise energy yield over its lifetime. Additionally, the inverter needs to not only provide MPPT, but may also need to step up the PV voltage if it is too low (i.e. not enough panels in series). Finally, the inverter needs to buffer the rate of power flow between the PV panels (constant power) and the 50Hz grid (100Hz sinusoidal power). This power decoupling is achieved with a capacitor (typically) for energy storage. Without this, power drawn from the PV panels would be sinusoidal, rendering PV MPPT impossible.

Fig 1-9 shows the simplified circuit schematics of the four power stages of a standard grid-tied inverter. The voltage gain stage in the circuit is responsible for boosting the input PV panel voltage to a voltage higher than the peak of the grid whilst considering MPPT. Ideally, the low DC voltage of the PV panel is boosted straight to an output AC voltage that provides a sinusoidal output current to the grid. However, this can be difficult due to

the control complexity of such a dynamic conversion [10, 11]. A simpler approach is to break up the DC-AC conversion into a separate DC-DC and simplified DC-AC stage, which reduces the control intricacies of sub-systems (such as MPPT) via complexity abstraction and lowers the THD [12, 13]. The circuit given in Fig 1-9 would only be useful for low voltage gains due to a poor efficiency at high voltage ratios [14]. When the designed PV array voltage is very low with respect to the grid, a high frequency transformer in the voltage gain stage can be utilised [11] to improve efficiency.

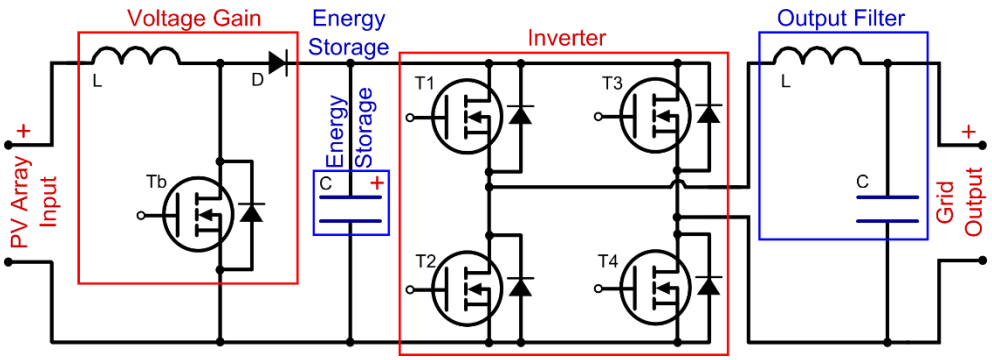

Fig 1-9. The four primary power stages of a grid-tied inverter.

The capacitive energy storage of Fig 1-9 acts as a power decoupling buffer between the voltage gain (DC-DC) and inverter (DC-AC) stages. The DC-DC stage provides a near constant power (neglecting MPPT transients) that charges the capacitor whilst the DC-AC stages draws a sinusoidally power according to the equation given below.

$$P_{(t)} = P_{Avg} \cdot (1 - \cos 2\omega t) \qquad (1\text{-}3)$$

Where P_{Avg} is the average inverter power and ω is the angular velocity of the grid. The power drawn from the capacitor corresponds to the AC component of equation (1-3) above and thus will oscillate between plus and minus two times the average power at a frequency of 100Hz (for a 50Hz grid). This difference in instantaneous power between charging and discharging results in a ripple voltage (V_{Ripple}) across the DC-link capacitor, which can be calculated [15] as equation (1-4):

$$V_{Ripple} = \frac{P_{Avg}}{\omega \cdot V_{DC} \cdot C} \qquad (1\text{-}4)$$

Where V_{DC} is the average DC-link voltage (i.e. an indicator of the capacitor's voltage rating) and C is the capacitance. A well-defined limit on the ripple voltage is given in [15] as 8.5% ripple for 98% utilisation of the PV panel. Thus, to reduce the required capacitance, it is desirable to decouple power at high voltages in order to minimise the use of shorter-lived electrolytic capacitors. It should be noted that inductive energy storage can also be utilised in a similar manner, effectively turning the DC-link from a voltage source into a current source. This allows for electrolytic capacitors to be completely eliminated from the inverter design, increasing reliability. However, for the same level of energy storage, inductors are larger, more expensive and less efficient.

The inverter (DC-AC H-bridge) stage of the inverter in Fig 1-9 is fed a series of high frequency gating pulses to control the exported sinusoidal grid current. The most basic form of current control is known as "bang-bang" control, which alternates between applying positive/negative voltages as the grid current undershoots/overshoots its target. Such methods of DC-AC conversion are simple, effective and do not require much processing power. To keep the switching frequency of such control methods at realistic levels, there must always be an output filter (see Fig 1-9) to add a slew-limiting affect to the grid current. Without this, the di/dt of the grid current would be near-infinite in response to a change in the applied voltage from the H-bridge. Filters are typically first order (L), second order (LC) or third order (LCL), with a higher order further reducing the di/dt. As the filter order rises, so too does the control complexity requirement. This makes stable operation of simplified control schemes such as "bang-bang" difficult with high-order filters. Ultimately, efficient operation of the DC-AC stage is a tradeoff between switching losses and filter losses, with the maximum efficiency achieved when they are in equilibrium.

1.5 Residential Inverter System Topologies

The "String Inverter" [15], which is an inverter connected to a group of series connected PV panels, is the most common inverter system installed in the residential setting. Seen in Fig 1-10a, the string inverter generates the grid-level DC voltages needed by connecting PV panels in series, the output of which is then inverted to AC by a centrally controlled inverter. This system topology is simple, well tested and in theory, perfect. However, due to the IV characteristic mismatch of real PV panels, it is very unlikely for the current

flowing through the series string to be at the MPP for each panel. Thus, the MPPT process is lossy and not all potential PV power is utilised the string topology.

By connecting a DC-DC converter to each PV panel, it is possible to control each panel independently. Seen in Fig 1-10b, "Smart DC-DC Optimisers" [16] are usually installed within the terminal boxes of the PV panels themselves. Although optimisers do not increase the power rating of the PV panels, it does allow the true MPP of each PV panel to be tracked in a mismatched string. These smart DC-DC optimisers vary the effective PV panel output voltages, allowing different currents to flow through each of the PV panels in the system. Thus, the MPP of each PV panel can be tracked through a simple algorithm within each smart DC-DC optimiser that performs "local" MPPT. The downside to this system topology is the increased cost and reduced conversion efficiency associated with using multiple lower power converters. Additionally, the operating temperature of the back of the PV panels (a common optimiser mounting location) can often exceed 60° Celsius [17], which increases the design costs of the optimisers if they are going to be rated to match the 20-25 year PV lifespan. Regardless, the conversion losses and increased design costs may be offset by the increase in energy yield due to the higher overall system MPP.

The "Differential Power Processing" (DPP) [18] system, seen in Fig 1-10c, is principally the same as the smart DC-DC optimiser system, but power is instead bypassed around weaker PV panels. As seen in the figure, the DC-DC converters have the significant advantage that they do not need to perform the conversion of the full power output of each PV panel. Instead, each DPP DC-DC converter only converts the mismatched power (difference in power) between the different PV panels. As a result, there is a small increase to the cost and complexity of the system. There is also the significantly reduced conversion losses of the DC-DC converters, which are now processing less than 20% of the power that they were in the case of Fig 1-10b as "Smart DC-DC Optimisers".

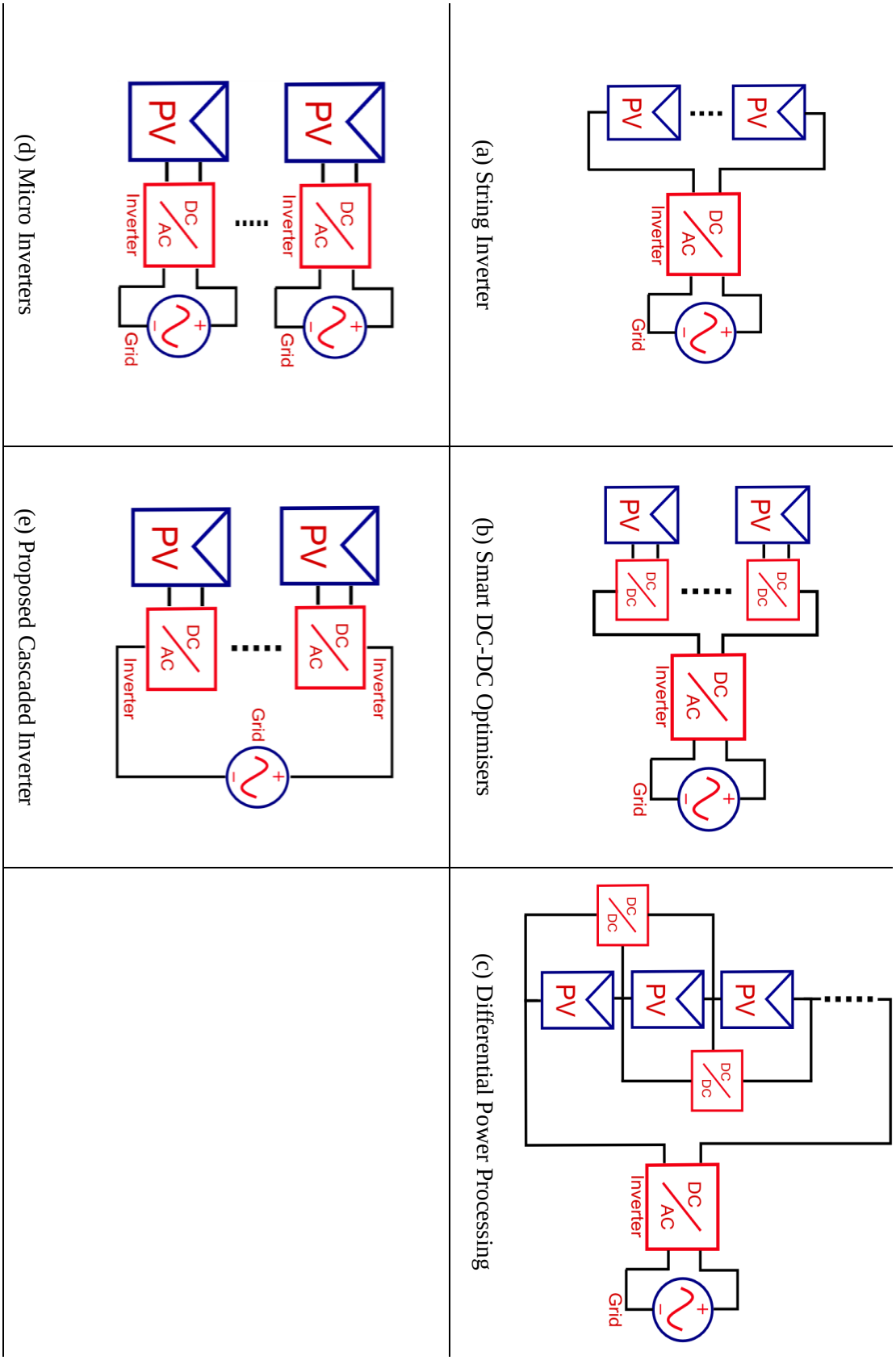

Fig 1-10. The five fundamental inverter systems suited for MPPT in residential installations.

To reduce the complexity of the DC-DC based modular systems of Fig 1-10b and Fig 1-10c, it is necessary to remove the central DC-AC converter that ties everything to a common point. Micro inverters [19, 20] are PV integrated, fully functional miniature inverters that operate in isolation from each other. Seen in Fig 1-10d, each micro inverter is fed by a single PV panel (usually under 250W) and connects directly to the grid. This allows for each micro inverter to accurately track the MPP of a PV panel and eliminate power mismatch issues in series strings. For example, one micro inverter can be 100% shaded whilst another functions normally. Micro inverters are completely independent and the system is completely fault tolerant as a result. Additionally, the modular nature of the system topology allows for quick, cheap and easy residential rooftop installation. However, micro inverters (per rated watt) are more expensive in part due to their own modularity, the economies of scale and the panel-mounted temperature requirements. It is cheaper to (per rated watt) have a larger central inverter on the side of the house rather than several panel-mounted micro inverters. Therefore, only on the residential scale, where installation cost is a large proportion of the total cost, is it viable to have a micro inverter system.

However, a significant drawback to micro inverters is the conversion efficiency, which is reduced due to the requirement to step up the low voltage of a single PV panel (under 50V) to the DC-link voltages required (over 400V) to interface with the Australian grid. Boost/flyback converters of such a high voltage gain are inefficient compared with their lower gain equivalents [14]. Due to the low MPP voltage (0.5V) of individual silicon PV cells, it is impractical and cost inefficient to manufacture 250W PV panels with voltages over 400V, thus making the high gain voltage boosting stage a necessity. Although high voltage PV panels would solve the high gain boost converter problem, a 400V 1.6m x 1.0m PV panel would have 571 PV cells each with a low surface area of 28cm² (5.3cm² x 5.3cm²). Such PV panels would be far too unreliable and cost ineffective for mass production.

A hybrid of the central inverter and the micro inverter is known as the cascaded inverter, which is effectively multiple H-bridges in a cascaded configuration with the grid. Seen in Fig 1-10e, cascaded inverters have been widely used in industry for the handling of “medium” voltage (13.8kV) power system conversions as they make possible the use of low-voltage and mature semiconductor switches in easily serviceable modules [21]. By

connecting the AC outputs of the DC-AC converters in series, it is possible to eliminate the micro inverter's high gain boost requirements whilst simultaneously allowing for the DC-AC converters to perform per-panel level MPPT. A detailed visualisation of the standard cascaded inverter with 'n' PV panels is given in Fig 1-11. The major unavoidable drawback to this circuit topology is the lower DC-link voltages, which requires the use of electrolytic capacitors to fulfil the energy storage requirements and potentially reduce the lifespan of the system. In addition, some modularity of the system is sacrificed (DC-AC converters in series rely on each other), which also has flow on effects to the fault tolerance of the entire series connected system. Regardless, the low voltage gain requirements allow for an increased conversion efficiency. Thus, for the systems of Fig 1-10, it is the cascaded inverter configuration of Fig 1-10e that will likely result in the highest overall PV energy yield for the small scale rooftop setting under real world conditions including shading.

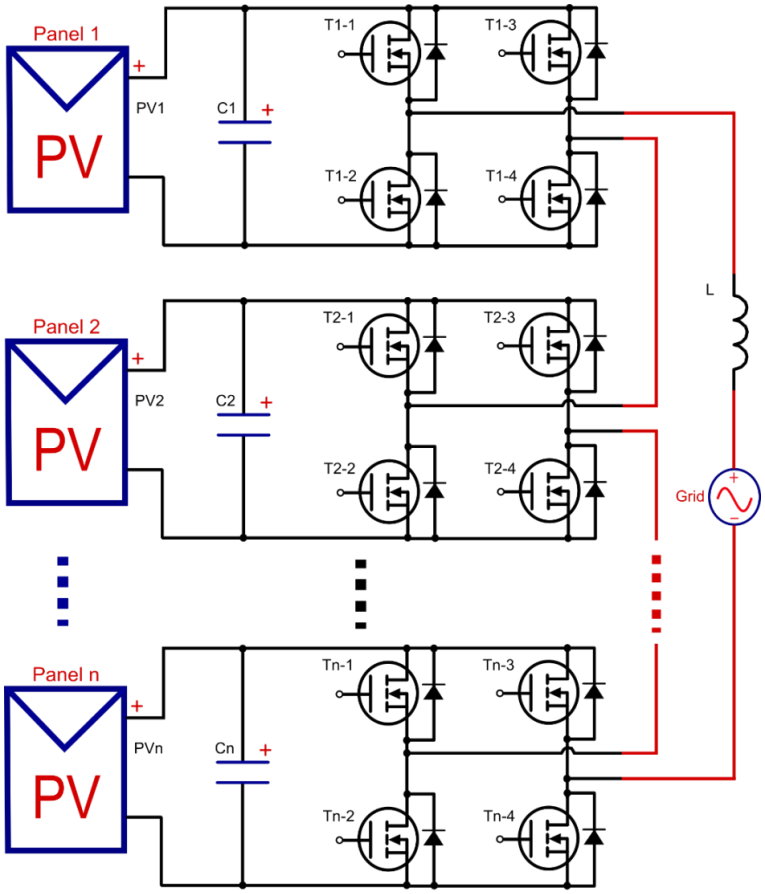

Fig 1-11. Standard PV single-phase centralised cascaded inverter system.

1.6 Cascaded Decentralisation and Multilevel Operation

The problem with cascaded operation (Fig 1-10e & Fig 1-11), within the small scale setting, is that each DC-AC converter (H-bridge) is controlled from a centralised location. Practically, this means that a centralised inverter installation (containing all of the cascaded DC-AC converters) will be mounted on the side of a residence with pairs of power cables going to each rooftop mounted PV panel. However, for the largest of the small scale systems (containing up to 25 200W PV panels), this would involve 25 pairs of conductors rated for at least 4A each (assuming the best case use of higher voltage 96 cell, 200W PV panels). Such cabling is impractical and proportionately costly. Thus, the system must be decentralised by placing a self-contained DC-AC converter module into each PV panel, turning them each into Modular Integrated Converters (MICs). These MICs each contain the functionality of Fig 1-9 such as a low gain boost converter, DC-link energy storage, an H-bridge and an output filter. Each MIC also contains voltage sensors, current sensors and an embedded micro controller. These standalone cascaded MICs require no centralised controller and only need access to the grid voltage waveform for zero crossing timing and to communicate with each other (with the latter only being a requirement if multilevel switching is to be utilised).

Multilevel switching, or voltage interleaving, is the process of switching "on" various voltage levels in a timed sequence to form a staircase waveform as seen in Fig 1-12a. The three fundamental multilevel converter topologies are the Neutral Point Clamped (NPC), the Flying Capacitor (FC) and the Cascaded H-Bridge (CHB) converter [22]. While the NPC and FC topologies utilise diodes and capacitors to artificially create additional voltage levels, the CHB topology (i.e. Fig 1-11) instead simply makes use the multiple sources available (i.e. PV panels) to generate the multilevel waveform (Fig 1-12a). Due to the modular nature of the CHB topology, decentralised operation of MICs in cascade is ideal.

In a decentralised multilevel cascaded MIC system, as the sinusoidal grid voltage increases, only the necessary numbers of voltage levels are switched on to match the instantaneous grid voltage to control the current. This ensures that the voltage difference between the system and the grid (i.e. the filter voltage) is minimised. This serves to reduce the di/dt of the grid current, which in turn reduces the switching frequency required to control the current. For the decentralised cascaded system, a greater number of MICs

would increase the number of multilevel steps that are possible. In addition, as only a single MIC needs to be actively modulating its output voltage to control the current, the other MICs can simply stay switched in the "on" or "off" state. This results in the already reduced switching frequency of the system being "spread out" amongst all of the MICs in the system as seen in Fig 1-12b and Fig 1-12c. Thus, the primary two benefits of using multilevel switching over normal switching within a cascaded (decentralised or not) system are as follows (whilst maintaining the same filter energy per watt):

1. The switching frequency is decreased due to a reduced average filter voltage (smaller voltage steps results in a lower di/dt).
2. The switching that does occur is spread out between the MICs in the system (only one MIC needs to modulate its voltage at any one time).

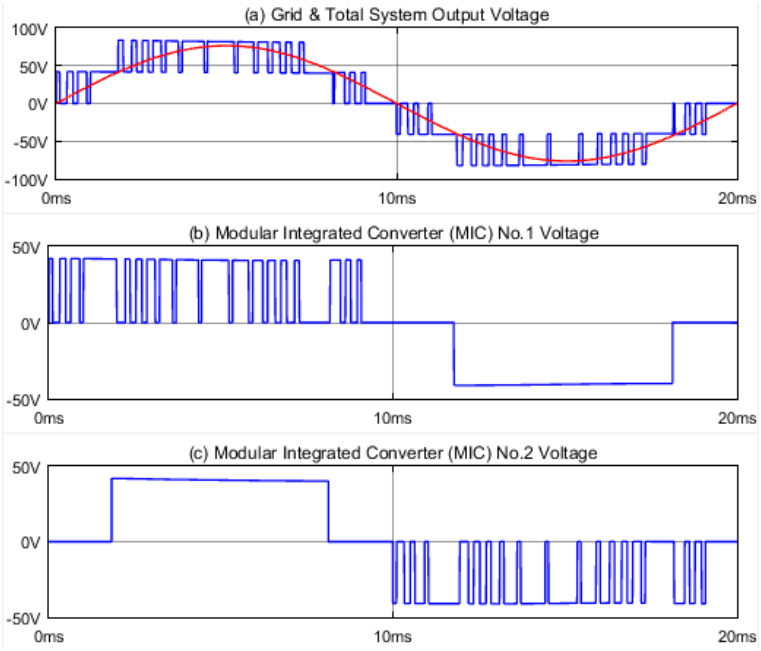

Fig 1-12. Principle waveforms of 2-MIC multilevel system. Voltages are seen in blue and current in red for the (a) total system output, (b) first MIC output and (c) second MIC output. See Fig. 6-10 for a 4-MIC simulation.

As an example, if an existing 8-MIC system were to use multilevel switching, the switching frequency for each MIC would be reduced to $1/8^{th}$ (due to the $1/8^{th}$ voltage steps) and then reduced to $1/8^{th}$ again due to the requirement for only a single MIC to perform voltage modulation at any one time. Thus, the switching frequency would be reduced to

$1/64^{th}$ of what it was without multilevel switching. A cascaded system with a higher number of MICs would therefore see an even greater switching frequency reduction.

1.7 Research Gap and Objective

Standard string inverter PV systems rely on the series connection of PV panels to create the high DC-link voltages required for interfacing with the grid. However, series strings of PV panels have IV characteristic mismatches between them, making it impossible to accurately track the MPP of each individual panel. Cascaded inverter systems instead connect the output of multiple PV-inverter pairs in series, allowing the MPP of each PV panel to be accurately tracked. Having multiple inverters in cascade also allows for multilevel switching, which can greatly reduce the inverters' switching frequencies. However, cascaded systems require decentralisation to reduce the relative cost of installation in small scale systems.

The most popular approach used in the literature to implement a decentralised cascaded small scale system is to forego multilevel switching in order to simplify operation [23-26]. In this way, there is no advanced coordination of the MICs and the system is simplified. This approach does not require a communications link between MICs, but still requires a grid reference for zero crossing information. However, as the switching frequency reduction provided by multilevel switching is highly desirable, it is necessary to find a method to implement it for the decentralised cascaded small scale system topology. A significant hurdle for this objective is the is the requirement of a communications link between the MICs for multilevel switching [27], which complicates the small scale system and can potentially raise installation costs compared with a standard micro inverter system. One solution to this wiring complexity is wireless communications between MICs. However, due to the limitations of desirable cheap wireless links (unreliable or intermittent), economic wireless communication may not be suitable for the time-critical interleaving involved in multilevel switching.

The research gap is therefore the implementation of multilevel switching in a small scale decentralised cascaded MIC system with a reduced or eliminated MIC-to-MIC communications requirement. An exploration of this research gap will allow for the development of a decentralised multilevel cascaded system that can cope with the limitations of unreliable or intermittent wireless links. Thus, such a decentralised system

would bring the benefits of multilevel switching, low voltage gain requirements, per-panel MPPT, and a reduced installation cost; with the whole system utilising only a cheap wireless link for communications. The objective of this thesis is therefore the analysis, justification and implementation of this small scale decentralised multilevel cascaded MIC system with reduced MIC-to-MIC communication requirements.

1.8 Original Contributions

The primary contributions of this thesis are related to the analysis, design and implementation of the 4-MIC decentralised system utilising intermittent communications. These contributions are detailed below:

- In a detailed analysis of the decentralised MIC concept it was found that the optimal number of MICs in a decentralised multilevel system is between 4 and 8 modules utilising a 1st order decentralised inductive grid filter. Four 200W MICs were then designed and prototyped to implement the proposed system.
- A detailed comparison analysis between a parallel and 2-MIC cascaded decentralised system found that although the CEC efficiency rose when moving to the 2-MIC cascaded configuration (94.8% to 95.9%), so too did the THD (4.8% to 5.2%). This analysis also found that a zero-crossing error of just 4° was enough to exceed grid harmonic limits.
- A detailed analysis of the power distribution limit between cascaded MICs found that a single MIC in the 4-MIC prototype system could be shaded by 74% before the power utilisation of the other MIC's were affected. Analytical equations were derived and verified experimentally for different shading configurations.
- The proposed decentralised multilevel MPPT algorithm was presented and analysed. It successfully allocated power between the four MICs in the prototype system (below 2% error) with a CEC conversion efficiency of 94.1% (compared with 94.8% for centralised multilevel control and 92.1% for non-multilevel control).
- A detailed analysis of the speed of the decentralised MPPT algorithm found that it was limited by the grid harmonic current limit, the shared region width and the global communications update rate of the system. Analytical equations were derived and verified experimentally to describe the limit of the decentralised MPPT

speed. It was found that a communications update rate as low as 0.7Hz was plausible to cover almost all solar irradiance transients.

The proposed decentralised multilevel cascaded MIC system requires only an additional intermittent communications link to implement multilevel switching (compared with a non-multilevel cascaded system). Thus, in small scale systems (where installation is a significant cost), complete decentralisation/modularity of the multilevel MICs is possible as the communications requirement can now be achieved with only a cheap/intermittent wireless link.

1.9 Thesis Structure

The outline of the thesis is as follows:

Chapter 2 presents an analysis of the cascaded inverter concept relating to its installation issues and the optimal number of MICs that should be placed in a decentralised system. Additionally, the concept of a distributed filter is discussed and analysed. Finally, the MIC themselves are designed and implemented.

Chapter 3 presents a comparative analysis that quantifies the differences between a single-MIC and two-MIC decentralised system. Variables such as the filter magnitude, THD, switching frequency and efficiency are compared. Additionally, further analysis of zero crossing error is made for the two-MIC system, quantifying the error limit that can be tolerated. Finally, the ratio of power between the MICs in the two-MIC system is analysed.

Chapter 4 presents the intermittent decentralised MPPT of the final 4-MIC system. The proposed hybrid partial-multilevel waveform is discussed along with the concepts of global and local MPPT through the greedy round-robin power sorting algorithm. Analytical expressions are presented for both the partial shading capabilities of the system and the MPPT speed limit imposed by intermittent communications. These equations and the operation of the entire algorithm are verified by the decentralised 4-MIC prototype system.

Chapter 5 contains a summarisation of the major results and findings from the thesis, as well as some suggestions for future work.

2 Analysis and Design of the Cascaded MIC

Cascaded multilevel MICs, whether decentralised or not, have a multitude of various factors affecting their performance. Changing the number of MICs in a cascaded system has an effect on the transistor efficiency, capacitor reliability, switching frequency, fault tolerance, modularity, MPPT capability, voltage gain requirements and ease of installation. The filter design is also affected by the cascaded nature of the system. The entire "n-sized" decentralised cascaded multilevel MIC inverter system can be seen in Fig. 2-1.

By using simulations of the ideally sized cascaded system, the theoretical benefits of a decentralised multilevel cascaded MIC system are explored in this chapter. The design and theory behind designing functional MIC prototypes is also explored through circuit diagrams, printed circuit board (PCB) layouts, hardware testing and software coding.

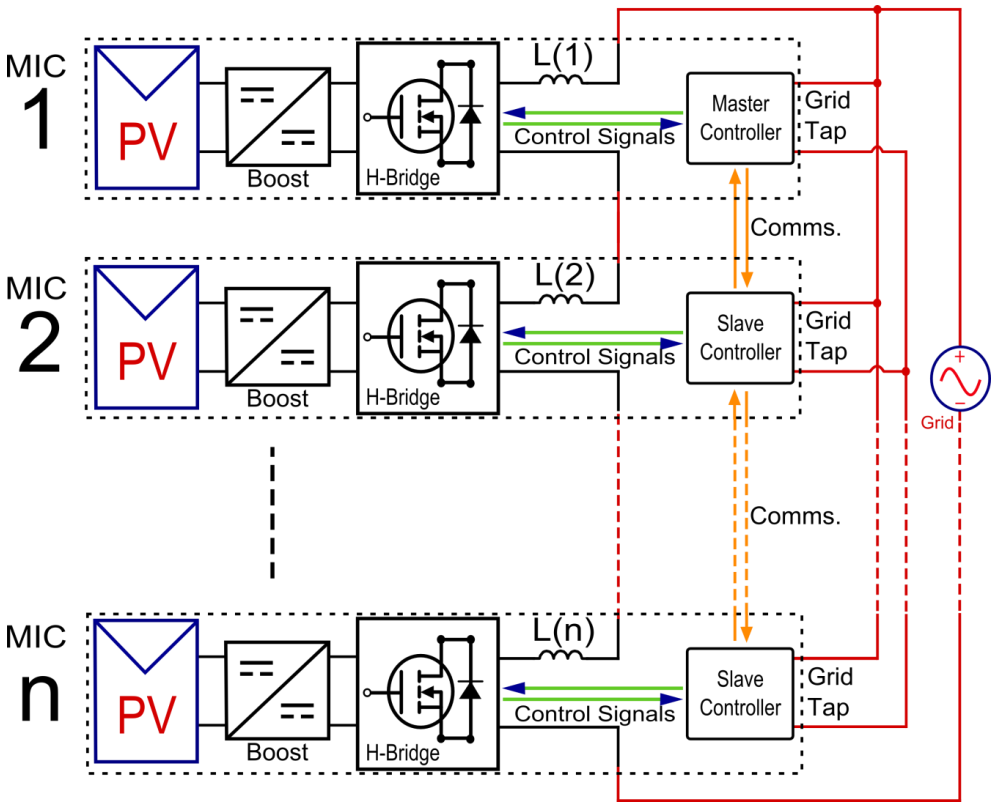

Fig. 2-1. The decentralised cascaded multilevel MIC inverter system.

2.1 The Practical Decentralisation Concepts

As it can be seen in Fig. 2-1, each MIC has five primary components which are the PV panel, boost converter, H-bridge, output filter and controller. The PV panel, when paired with the boost converter, produces a constant DC output voltage whilst allowing for MPPT. The controller, which controls the boost converter, also coordinates the transistors of the H-bridge to inject the correct amount of power through the filter and into the grid to satisfy the PV MPPT and grid harmonic requirements. Therefore, as it can be seen in this topology, each MIC requires knowledge of its own DC-link voltage/current (for MPPT), its grid current (for injecting grid power) and its grid voltage (zero-crossing synchronisation).

Connecting the MICs in cascade requires three primary connections:

- The outputs of each MIC are connected in series (through their filters) to the grid.
- Each MIC has a separate grid connection for measurement purposes.
- Each MIC has a communications link to the neighbouring MIC which may occur through either power line communications (PLC), an additional wired link or through a wireless connection (Bluetooth, Wi-Fi, etc.).

In a centralised cascaded inverter system, the output filter is connected solely at the output as seen in Fig 1-11, which shows a 1st order filter (inductor only). To implement a centralised 2nd order filter, a capacitor is simply added across the grid connection after the inductor. Conversely, for a decentralised cascaded system, it is desirable to distribute the total system filter across each MIC in cascade as seen in Fig. 2-1 (reducing installation costs). Cascading 1st order inductive filters is simple as the total filtering impedance adds in series. However, cascading multiple 2nd order filters in series does not result in a centralised equivalent 2nd order filter due to the interactions between the neighbouring cascaded filter stages. A full analysis of cascaded 1st, 2nd and 3rd order filters will be discussed in section 2.3. It was decided that to reduce complexity only 1st order cascaded filters would be considered and analysed for MICs in this thesis.

2.1.1 MPPT of MICs

The series connected nature of cascaded systems ensures that there is a reliance of each MIC on one another for voltage, current and therefore power. Unlike the parallel connected

micro inverter, each MIC in a cascaded chain shares a common grid current, but not a common voltage. In a non-multilevel system, if one MIC increases its AC output voltage (PV power increase) then this will increase the grid current, satisfying its power increase requirements. In turn this will then instantaneously increase the average power being drawn from the other MICs to the grid. The other MICs will then correct for this by reducing their output voltages, thereby reducing the grid current. Once more the first MIC will respond by increasing its output voltage by a further amount. This process will repeat until the system converges on steady state conditions where the voltage balance between the MICs is correct for both the grid current and the overall MIC power distribution. This push-pull behaviour is perfect for a decentralised system as no communications between the MICs is required. An individual MIC in a non-multilevel cascaded system that aims to perform MPPT need only follow the logic described below:

1. Input power increasing?
    - → Increase output voltage.
2. Input power decreasing?
    - → Decrease output voltage.
3. Output current increasing?
    - → Decrease output voltage.
4. Output current decreasing?
    - → Increase output voltage.

However, if we wish to utilise multilevel switching in the cascaded system then the approach above is impossible as only a single MIC is in control of the current at any one time (i.e. Fig 1-12). In a multilevel waveform, if the MIC that is in control of the current tries to reduce its power, then the current will be reduced without the other MICs doing anything to instantaneously respond. However, later in the waveform when the affected MICs are finally in control of the current, only then can they modify the current compensate for the other original MIC's earlier actions. This then affects additional MICs as a carry on effect. As a result, there are regions of different current references from all of the MICs and the current ultimately becomes non-sinusoidal. To make multilevel MPPT a possibility, communications is therefore required between the MICs to accurately coordinate the entire multilevel MPPT process. Instead of current references fighting

against each other, segments of the multilevel waveform are reallocated between the MICs (with different weightings), reflecting the changing power targets of each PV panel.

2.1.2 Practical MIC Installation Issues

In a typical micro inverter system, each inverter may be electrically connected in parallel, but the practical mains wiring results in an apparent physical cascaded connection. Each micro inverter connects (in parallel) to a high gauge (low resistance) multi-core linking cable that contains active, neutral and earth. This linking cable runs from inverter to inverter, connecting them in parallel, until the current carrying capacity of the linking cable is reached. Some micro inverters are designed with integrated male/female linking cable plugs to allow the unit to be part of the linking cable itself. A decentralised multilevel cascaded system may be installed in the same way, but with an additional fourth cascade wire in the linking cable as shown in Fig. 2-2 to create and electrically true cascaded connection. This assumes either wireless or power line communications for any multilevel operations.

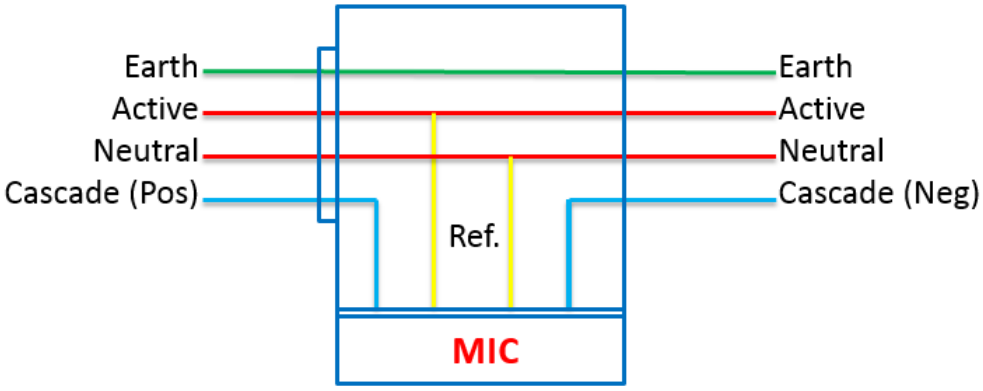

Fig. 2-2. Wiring of a single MIC for installation into a decentralised cascaded multilevel system.

By combining the installation technique of Fig. 2-2 with the linking cable lug of Fig. 2-3, it is possible to form modular cascaded systems. An example system can be seen in Fig. 2-4, where a decentralised cascaded system operates using the proposed cable arrangement.

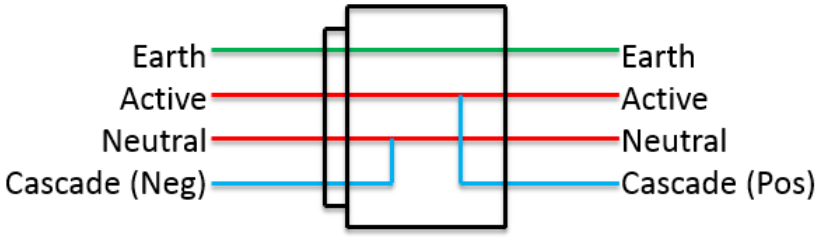

Fig. 2-3. The wiring configuration of a termination lug to allow for multiple parallel cascaded systems on the same linking cable.

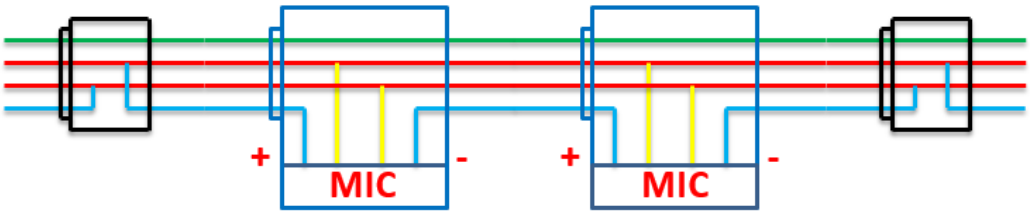

Fig. 2-4. A decentralised cascaded multilevel 2-MIC system based on Fig. 2-2 and Fig. 2-3, which can easily be repeated to parallel more cascaded systems on the same linking cable.

Looking at the cascaded linking cable lug in Fig. 2-3 and Fig. 2-4, it can be seen that one side of the linking lug is designed to be the negative end of a cascaded chain (male side, neutral tap) and the other side is designed to be at the positive end of a cascaded chain (female side, active tap). Active, neutral and earth are passed through the inverters, but the cascade conductor is not (i.e. it is the cascaded power output). Ultimately, this cabling arrangement allows for multiple decentralised multilevel cascaded MICs to be installed in small scale PV environments in almost the exact same way that micro inverters are. Effectively, the installation costs are unaffected by the shift from a parallel to a decentralised multilevel cascaded system.

2.2 Sizing the Decentralised Cascaded System

A decentralised multilevel cascaded system can be constructed out of any number of MICs and through nearly any cascaded-parallel combination (i.e. multiple cascaded systems on one rooftop). A system can contain any number of MICs, so long as there are at least two. However, factors such as MOSFET efficiency, DC-link film capacitor viability, achieved multilevel switching frequency, partial shading resilience, DC-link voltage gain requirements and fault tolerance are all affected by the number of MICs connected in

cascade. As a result, there exists an optimally sized cascaded system that should be utilised in order to maximise the overall system effectiveness.

2.2.1 MOSFET Conduction Efficiency

For residential PV grid-tied applications with at least two MICs connected in cascade, the voltage rating of the transistors utilised will be at least 200Vdc for a 230Vrms grid and 100Vdc for an 110Vrms grid. Devices below these voltages are certainly the domain of MOSFET transistors (with on-state resistive losses) and not that of the IGBT transistors (near constant on-state voltage drop). Assuming that the desired switching frequency is not high (i.e. under 20kHz) then the primary indicator of performance for a MOSFET is the on-state resistance, which changes with the breakdown voltage.

For a given MIC at 200W, if the voltage rating were to double then the current rating would halve. As the conduction losses are proportional to the square of the current this means that they would be reduced to a quarter of what they were. Thus, to maintain the same conduction losses, the on-state resistance would need to quadruple. For a MOSFET, doubling the voltage rating is analogous to removing one of two parallel connected MOSFETs (doubling the resistance) and then placing that MOSFET in series with the other (again doubling the resistance). Effectively, this is what is happening, but on a substrate level within the MOSFET package. However, this is not always the case for actual MOSFETs available on the market. Fig. 2-5 shows a plot of the on-state resistances in proportion to the squared breakdown voltages for a selection of commercially available MOSFETs. Note that as this graph is based on available commercial MOSFETs within a restricted price range (<$5USD), it also reflects trends in consumer demands for different device ratings. Lower is better and theoretically the plot should be a straight line that indicates an adherence to the square voltage rule (i.e. a constant specific resistance of the substrate across all voltage ratings).

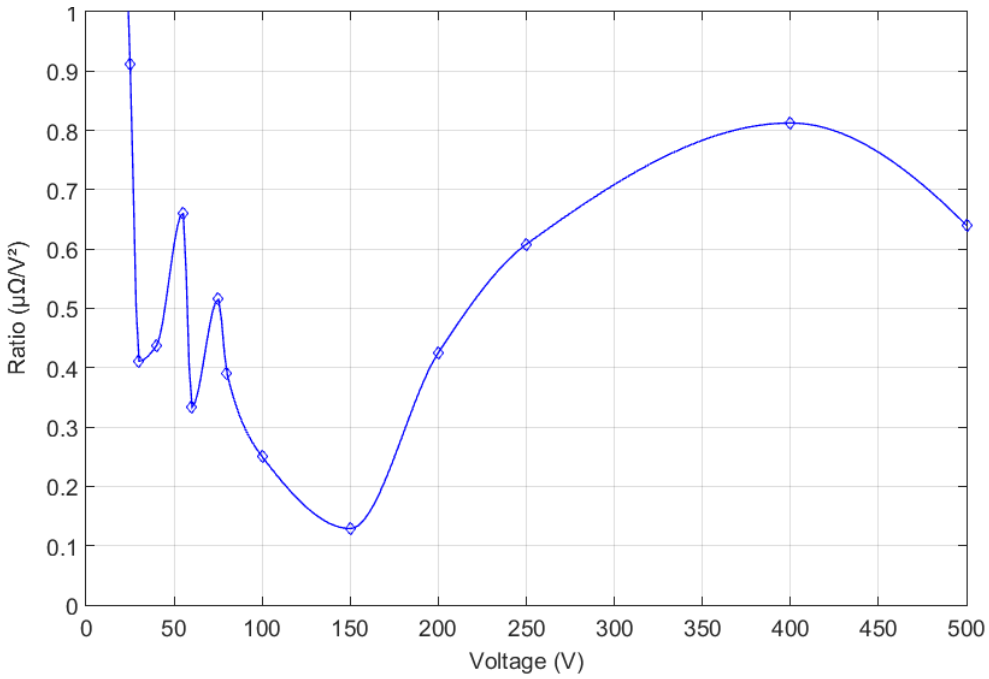

Fig. 2-5. The ratio of the on-state resistance to the square of the breakdown voltage for commercially available MOSFETs. Based on the best MOSFET (<$5USD) for each voltage category that contained at least 60 different stocked items (element14, November, 2016).

It can be seen in Fig. 2-5 that although there are fluctuations in the obtained data, the resistance ratio shows a trend indicating a clear minimum around the 150V breakdown voltage. As the MOSFET resistance seems to increase at a rate greater than the square of the voltage, the resistance ratio can be seen to be increasing at voltages beyond 150V. Conversely, at low voltages, the resistance cannot be reduced much further due to MOSFET package restraints, which increases the MOSFET resistance ratio at low voltages. Regardless, if we ignore the higher frequency ratio fluctuations around the 50V region, it can generally be concluded that to minimise the on-state resistive conduction losses it is best to utilise MOSFETs with breakdown voltages between 30V and 200V.

2.2.2 The Viability of a Film Capacitor DC-Link

The DC-link capacitor of an MIC is critical in decoupling the AC power of the grid from the DC power flow of a PV panel. As explained in section 1.4, if this capacitor is too small then the power ripple of the PV panel begins to affect the MIC's MPPT capability. Conversely, it is not cost effective if the capacitor is too large due to diminishing MPPT returns from the additional DC-link energy storage. This relationship was described by

equation (1-4), indicating that for a given ripple voltage, grid frequency and average grid power, the required capacitance is dependent on its DC-link voltage. In addition, as discussed in section 1.4, [15] states that 98% PV power utilisation can be achieved with a ripple voltage of 8.5%. For a 200W MIC with a 50V DC-link, this results in a capacitance of 3mF. According to the capacitive energy storage equation of equation (2-1), this is an energy capacity of 3.75J.

$$E = \frac{1}{2} \cdot C \cdot V^2 \qquad (2\text{-}1)$$

However, as the voltage ripple is defined as a proportion of the DC-link voltage, the energy content of the capacitor stays constant for all DC-link voltages. Therefore, to normalise the energy storage of the capacitor for all MIC power ratings, the unit is given as milli joules per rated watt of output power. Thus, for a 50Hz grid with 98% PV utilisation, any DC-link capacitor must have an energy storage capacity of 18.75mJ/W.

Critically, a DC-link energy storage of 18.75mJ/W (or 3.75J for the 200W standard MIC) is a significant hurdle as this requirement mandates electrolytic capacitors be used for lower DC link voltages. Electrolytic capacitors, as opposed to reliable film capacitors, have very large energy storage densities that make their use very attractive. However, due to the requirements of long life, the DC-links of MIC should use film capacitors where viable. As energy storage using film capacitors is the most economically viable at high voltages, it is only natural to conclude that a DC-link should maximise its voltage. Unfortunately, for the cascaded system, the aim is to have low voltage DC-links to allow for multilevel operations.

To explore the viability of film capacitors at lower voltages, Fig. 2-6 reveals the cost of designing a DC-link using only film capacitors for a 200W MIC (3.75J energy storage). Fig. 2-6a shows the capacitance required for the necessary 3.75J energy storage and Fig. 2-6b shows the cost of purchasing enough film capacitors to meet that capacitance requirement. Since the capacitance required is reduced with the square of the DC-link voltage (and film capacitors are generally much smaller in capacitance), the price of the required film capacitors quickly drops as the DC-link voltage increases. For a 230Vrms grid, the DC-link of the minimum cascaded system size (2 MICs) is 200V. Unfortunately,

the cost of the film capacitor based DC-link at 200V exceeds $100USD, which is impractical. Although these price points are based on the 'single item' costs and not the reduced bulk quantity purchase costs, it can be concluded that film capacitors are not viable at any cascaded system size other the 2-MIC minimum.

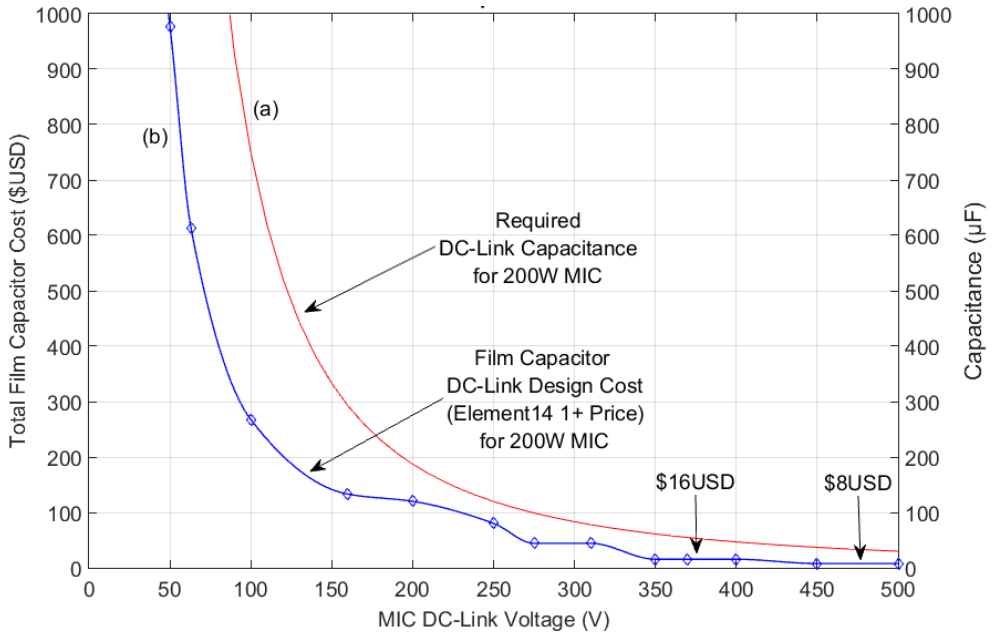

Fig. 2-6. The cost of commercially available film DC-link capacitors (3.75J energy storage) as a function of the DC-link voltage for 200W cascaded MICs with 98% PV power utilisation (8.5% ripple voltage). Each "capacitor" may be made up of multiple paralleled capacitors. Based on the single unit price of film capacitors listed on element14, December, 2016.

Although electrolytic capacitor DC-links are undesirable, they are not completely unviable. Beneficially, electrolytic capacitors that fail from age typically do so in a non-destructive way (i.e. open circuit fault). This allows for inclusion of additional parallel electrolytic capacitors that decrease the chances of the total capacitance falling below the 98% PV utilisation threshold. Additionally, if film capacitors are used in conjunction with electrolytic capacitors then at least some % utilisation of the PV panel can be guaranteed over the MIC lifespan (long after the electrolytics have failed).

2.2.3 Switching Frequency Reduction

As discussed in section 1.6, operating a system with multilevel voltage interleaving allows for a switching frequency reduction that increases with the square of the number of cascaded MICs (compared with an equivalent centralised inverter that is not multilevel

interleaving). Seen in Fig. 2-7, the multilevel switching frequency reduction is significant in systems with a large numbers of MICs. Thus, it is beneficial to operate a cascaded system with the maximum number of MICs possible.

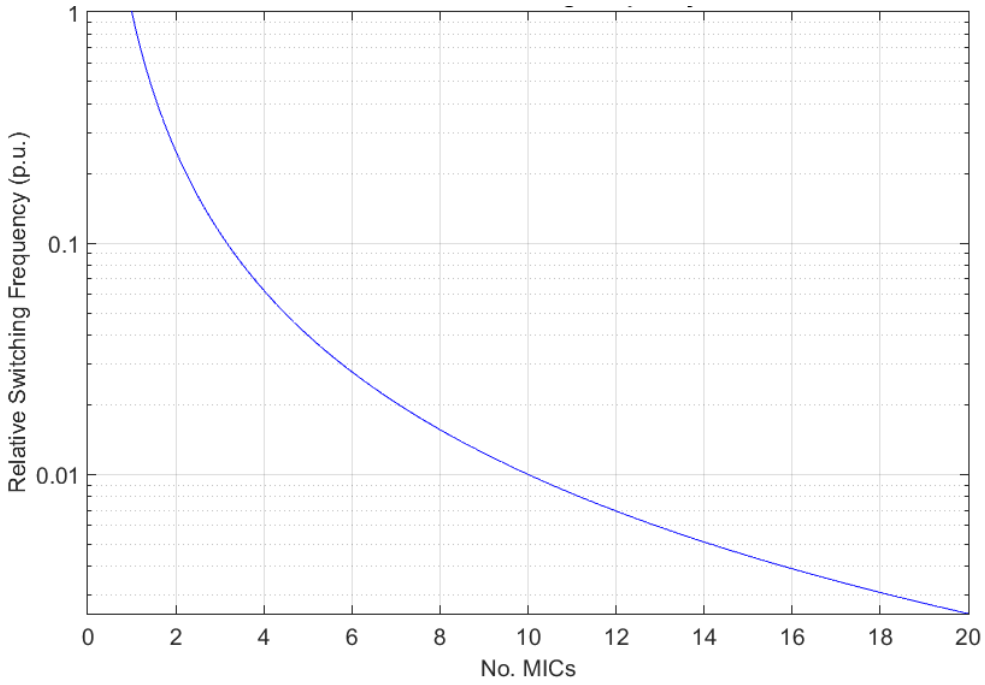

Fig. 2-7. The relative switching frequency of a multilevel cascaded inverter system compared with a centralised (non-multilevel) inverter equivalent.

As it is hard to comment on the absolute switching frequencies of an MIC system without mentioning the specific hardware arrangement, it is far simpler to generalise. It could be said that to justify the added complexity of a decentralised cascaded multilevel system over a micro inverter system, a switching frequency reduction of at least 90% (i.e. $1/10^{th}$) is necessary. Based on the multilevel switching frequency reduction plot of Fig. 2-7, it can therefore be concluded that there should be a minimum of 4 MICs in a decentralised multilevel cascaded system.

2.2.4 Partial Shading Resilience

Discussed in detail in section 4.4, partial shading in cascaded MIC inverter systems have a limit to the power distribution ratios that is possible between PV panels. If one PV panel falls below a critical minimum power threshold, the entire cascaded inverter system cannot function correctly. As the number of MICs in the cascaded system is increased, the

maximum shading that can occur across a single PV panel increases (as one PV panel now represents a smaller proportion of the entire cascaded system's power). Thus, to enhance partial shading resilience, the number of MICs in a cascaded system should be maximised. For example, a cascaded system with 4 MICs or more would allow for at least a 50% shading of an MIC (see Fig. 4-11).

2.2.5 DC-Link Voltage Gain Requirements

The higher the number of MICs in a cascaded system, the smaller the voltage gain that is required by each MIC to meet the DC-link voltage (400Vdc or 200Vdc) that is necessary to safely interface with the grid (230Vrms or 110Vrms). However, there are a set number of standard mass-produced PV panel sizes available which are 36 cells (18-23.4V), 60 cells (30-39V), 72 cells (36-46.8V) and 96 cells (48-62.5V). The maximum voltage ranges are due to the difference between the per-cell MPP (0.5V) and the open circuit voltage (0.65V). Additionally, since PV panel working voltages can drop significantly with solar irradiance, a step-up (boost) converter is always required for the DC-link. As such, step-down (buck) voltage conversion is not considered, as this would require buck/boost operation, decreasing the efficiency of the DC-link. Thus, given these constraints, this creates combinations of PV panels and voltages gains that fluctuate with the number of cascaded MICs, which can be seen in Table 2-1.

Table 2-1 was produced by selecting the largest PV panel that could work with an MIC of a cascaded system of 'n' size without exceeding the standard total DC-link voltage requirement to interface with the grid (200Vdc for a 110Vrms grid and 400Vdc for a 230Vrms grid). The open circuit voltages (V_{OC}) of the PV panels were used to find the largest PV panels that would not require any voltage step-down. The displayed voltage step-up boost gain was then calculated based on the PV maximum power point voltage (V_{MPP}), as this is the most critical operating point. It should be noted that PV panels with larger numbers of cells typically will have higher power ratings, but cell efficiencies can alter this fact. Additionally, it is possible to have parallel/series arrangements of cells within the same panel (i.e. 72 cells may be two sets of 36 cells in parallel).

Table 2-1. Voltage gain requirements for cascaded systems of different sizes with optimally matched standard PV panels based on their open circuit voltages for 110Vrms and 230Vrms grids.

No. MICs	Optimal PV Panels for MICs on a 110rms Grid (200V Total DC-Link)	MPP Boost Gain	Optimal PV Panels for MICs on a 230Vrms Grid (400V Total DC-Link)	MPP Boost Gain
1	62.5Voc/48Vmpp (96 Cell)	4.16	62.5Voc/48Vmpp (96 Cell)	8.33
2	62.5Voc/48Vmpp (96 Cell)	2.08	62.5Voc/48Vmpp (96 Cell)	4.17
3	62.5Voc/48Vmpp (96 Cell)	1.39	62.5Voc/48Vmpp (96 Cell)	2.78
4	46.8Voc/36Vmpp (72 Cell)	1.39	62.5Voc/48Vmpp (96 Cell)	2.08
5	39Voc/30Vmpp (60 Cell)	1.33	62.5Voc/48Vmpp (96 Cell)	1.67
6	23.4Voc/18Vmpp (36 Cell)	1.85	62.5Voc/48Vmpp (96 Cell)	1.39
7	23.4Voc/18Vmpp (36 Cell)	1.59	46.8Voc/36Vmpp (72 Cell)	1.59
8	23.4Voc/18Vmpp (36 Cell)	1.39	46.8Voc/36Vmpp (72 Cell)	1.39
9	Boost/Buck Required		39Voc/30Vmpp (60 Cell)	1.48
10	Boost/Buck Required		39Voc/30Vmpp (60 Cell)	1.33
11	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	2.02
12	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	1.85
13	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	1.71
14	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	1.59
15	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	1.48
16	Boost/Buck Required		23.4Voc/18Vmpp (36 Cell)	1.06

Table 2-1 reveals that the practical gain requirements of a cascaded system do fluctuate as the number of MICs increases. However, by only focussing on the configurations with a gain under 2.0 (green/yellow), it can be concluded that so long as there are at least 3 cascaded MICs for a 110Vrms grid or 5 MICs for a 230Vrms grid, the voltage gain requirements are minimised. This is because there is a large voltage gap between the highest voltage PV panel (96 cells – 48Vmpp) and the 200Vdc/400Vdc voltage required to interface with the grid (as discussed previously in section 1.5). Therefore, as long as there are enough PV panels in the cascaded system to come close to (or exceed) the grid voltage requirements, then there are many smaller PV panel cell configurations to meet low voltage gain requirement arrangements. Still, it is ideal if the number of MICs in a system allows for a voltage gain below 1.5 (green).

2.2.6 Total Installation Fault Tolerance

Unlike the previously mentioned factors that affect the ideal size of a cascaded system, fault tolerance is hard to quantify. In a cascaded system, the failure of one MIC can easily

affect the rest of the system and interfere with operation. However, if we allow for a higher than required total DC-link voltage, the system can meet the grid interface voltage requirements without all of the MICs functioning (i.e. one MIC can fail and bypass itself). Regardless, if a cascaded system has a lower number of MICs then there will be more cascaded systems connected in parallel (see Fig. 2-4) to meet the total power requirements of an installation assuming the power of each MIC is fixed. Thus a non-bypassed MIC failure will result in only one of the cascaded systems failing. This leads us to the conclusion that the smaller the cascaded system is, the more reliable the entire PV installation is. Thus, fault tolerance requires that the number of MICs be minimised.

2.2.7 Final System Size Selection

To make the final selection of the ideal cascaded system size for 110Vrms and 230Vrms AC grids, all of the factors should be consolidated and weighed against each other. These factors are the MOSFET conduction efficiency, DC-link film capacitor viability, multilevel switching frequency reduction, partial shading resilience, DC-link voltage gain requirements and the total installation fault tolerance. To weigh the effects of these factors against each other in this study, a 1-10 scoring system was developed for each factor that is influenced by the number of MICs in the system for both the 230Vrms and 110Vrms grids. This scoring system was developed as follows:

1. MOSFET conduction efficiency – Based on Fig. 2-5, a resistance ratio of 1.0 represents a score of 0, whilst a resistance ratio of 0.1 represents a score of 10.

2. DC-Link film capacitor viability – Based on Fig. 2-6, a cost above $300USD represents a score of 0 and a cost below $20USD represents a score of 10.

3. Switching frequency reduction – Non-multilevel operation (1-MIC) represents a score of 0 and 4-MIC multilevel operation represents a score of 10. 4-MIC operation is the minimum cascaded system size to at achieve at least a ten-fold switching frequency reduction from multilevel operations. This scoring is somewhat based on Fig. 2-7, but mostly on intuition. The transition to a cascaded system should make the most of multilevel switching and a system that is 3 MICs or less just doesn't offer a significant enough switching frequency reduction.

4. Partial shading resistance – For a DC-link magnitude of 1.1p.u. (see Fig. 4-11), a maximum shading of 100% represents a score of 10 and a maximum shading of 0% represents a score of 0. This criterion assumes that only a single MIC is being shaded in any given system. Thus, the 10% line represents a 10-MIC system and the 25% line represents a 4-MIC system, etc.

5. DC-link voltage gain requirements – Based on Table 2-1, a gain of 1.0 represents a score of 10, whilst a gain of 4.0 represents a score of 0.

6. Fault tolerance – A general rule is applied here that incrementally decreases the score as the number of MICs increases. A score of 10 is given for a single MIC system and a score of 0 is given for an 11 MIC system.

It was also concluded that the MOSFET efficiency due to the resistance ratio and film capacitor viability were of less importance compared with the switching frequency, partial shading resilience, boost converter gain requirements and the fault tolerance. As a result, the weighting for the first two factors is half that of the final four. This weighting and subsequent final system size selection is visualised by the final scores seen in Table 2-2 (for the 230Vrms AC system) and Table 2-3 (for the 110Vrms AC system).

Table 2-2. Weighted comparison of the six different selection factors for finding the optimal number of cascaded MICs for connection to a 230Vrms grid.

230Vrms Grid – System Size Viability								
No. MICs	**DC-Link Voltages**	**MOSFET Efficiency**	**Film Caps.**	**Switch. Freq.**	**Partial Shading**	**Boost Gain**	**Fault Tol.**	**Final Score**
Relative Weight:		1x	1x	2x	2x	2x	2x	-
1	400V	0	10	0	10	0	10	50
2	200V	5	5	2	5	0	9	42
3	133V	10	4	7	6	4	8	64
4	100V	8	1	10	7	6	7	69
5	80V	5	0	10	8	8	6	69
6	67V	5	0	10	8	9	5	69
7	57V	5	0	10	9	8	4	67
8	50V	5	0	10	9	9	3	67
9	44V	5	0	10	10	8	2	65
10	40V	5	0	10	10	9	1	65
11	36V	5	0	10	10	7	0	59
12	33V	5	0	10	10	7	0	59
13	31V	5	0	10	10	8	0	61
14	29V	5	0	10	10	8	0	61
15	27V	4	0	10	10	8	0	60
16	25V	4	0	10	10	10	0	64

It can be concluded by looking at the right-most column of Table 2-2 that the optimal size for a cascaded system connected to a 230Vrms grid is between 4 and 10 MICs. The switching frequency, partial shading resilience and voltage gain requirements all favour any system that is at least 4 MICs large. Conversely, fault tolerance favours the smallest system possible. The MOSFET efficiency and film capacitor viability favour very specific system sizes, but due to the lower weightings of these factors they do not have much influence. Ultimately, this results in a range of optimal system sizes that require at least 4 MICs (smaller systems lack the actual cascaded benefits of cascaded systems), but cannot exceed 10 MICs (primarily due to the falling fault tolerance).

Table 2-3. Weighted comparison of the six different selection factors for finding the optimal number of cascaded MICs for connection to a 110Vrms grid.

110Vrms Grid – System Size Viability								
No. MICs	**DC-Link Voltage**	**MOSFET Efficiency**	**Film Caps.**	**Switch. Freq.**	**Partial Shading**	**Boost Gain**	**Fault Tol.**	**Final Score**
Relative Weight:		1x	1x	2x	2x	2x	2x	-
1	200V	5	5	0	10	0	10	50
2	100V	8	1	2	5	6	9	53
3	67V	5	0	7	6	9	8	65
4	50V	5	0	10	7	9	7	71
5	40V	5	0	10	8	9	6	71
6	33V	5	0	10	8	7	5	65
7	29V	5	0	10	9	8	4	67
8	25V	4	0	10	9	9	3	66
9	22V	3	0	10	10	0	2	47
10	20V	2	0	10	10	0	1	44
11	18V	1	0	10	10	0	0	41
12	17V	0	0	10	10	0	0	40
13	15V	0	0	10	10	0	0	40
14	14V	0	0	10	10	0	0	40
15	13V	0	0	10	10	0	0	40
16	13V	0	0	10	10	0	0	40

Similar to Table 2-2, Table 2-3 shows that the optimal size of a cascaded system connected to a 110Vrms grid is between 3 and 8 MICs. Compared with the 230Vrms grid (with an optimal range of 4-10 MICs), the 110Vrms grid has a range with both a lower minimum and maximum cascaded system size. Primarily, this is due to both the voltage gain requirements cutting off to a score of 0 above 8 MICs (the region where boost/buck converters are required in Table 2-1) and the MOSFET efficiency sweet spot aligning with the DC-link voltage of the 3-MIC sized system.

Ultimately, the optimal size of a cascaded system should be as small as possible, which allows ease of manufacture and a greater flexibility in PV system installation. For the purposes of this research, a smaller system is selected to offer an ease of production and a low cost. Thus, the smallest possible cascaded system that fits the viability criteria for both the 110Vrms and 230Vrms grid (i.e. scored at least 65) would be a system with 4 MICs. Note that the 4-MIC cascaded system also scored the highest overall (tied) for both

grid voltages. Unless mentioned otherwise, the 4-MIC system size will be utilised for future assumptions, simulations and as the primary prototype implementation in this thesis.

2.3 Filter Analysis

2.3.1 Grid-Tied Inverter Filters

All grid-tied inverters require a low-pass output filter in order to control the generated current harmonics. Effectively, the output filter adds a slewing effect to the grid current, reducing the di/dt and allowing for controllability. Seen in Fig. 2-8, grid-tied centralised inverters or other inverters with a single output stage (i.e. micro inverters) typically utilise a 1st order (L), 2nd order (LC), or 3rd order (LCL) output filter. The higher the filter order, the sharper the frequency response roll-off, which allows the fundamental grid current frequency and switching frequency to be closer (i.e. a lower switching frequency).

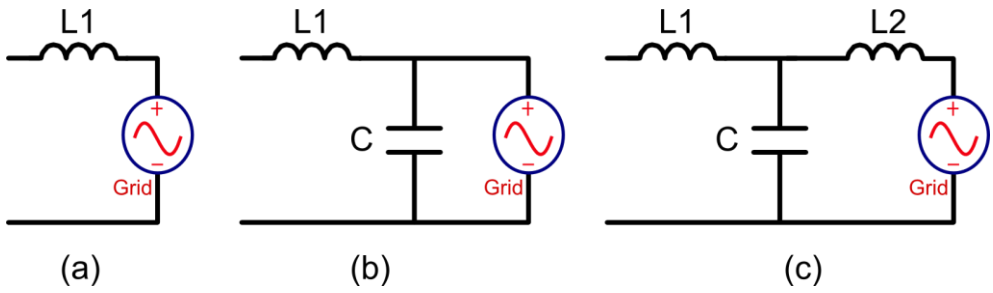

Fig. 2-8. First order (a), second order (b) and third order (c) low pass filters for grid-tied inverters.

For the 1st order filter, efficacy can be explained in terms of the voltage across the inductor. The greater the difference in voltage between the inverter and grid (i.e. as a result of the transistor switching), the greater the di/dt of the current. As the inductance increases the di/dt of the current is proportionately decreased. Any inductance in the grid is beneficial to the filter as it adds in series. Similarly, any grid resistance will add in series and have a minor effect on operation (i.e. current takes longer to rise but is faster to fall). Ultimately, high frequency harmonics are blocked but the fundamental grid current is allowed to flow through the filter.

A 2nd order filter uses the blocking effect of the 1st order filter's inductor, but then shunts the remaining high frequency harmonic current through a capacitor. However, this shunt relies on there being a non-zero grid impedance. If there is no grid impedance then

effectively it is as if the capacitor does not exist. This is because any instantaneous harmonic current through the capacitor would raise the capacitor voltage, which then would stop any further harmonic current. Although good for voltage regulation, it is therefore not typical for current controlled grid-tied inverters to utilise 2nd order low pass filters [28].

3rd order filters solve the dependence on the grid impedance problem through the utilisation of another filtering inductor. So long as the impedance of the second inductor is significantly large by comparison to any expected grid impedance, the shunting effect of the capacitor for harmonic current will always be effective. However, 3rd order filters are more difficult to design compared with 1st and 2nd order filters, especially when considering a grid-tied connection, control and stability [28]. Finally, although 4th order and higher low-pass filters are possible, the number of capacitors and inductors begins to permit multiple circuit configurations that cannot be covered by a general figure.

2.3.2 Analysis of Decentralised Grid-Tied Cascaded Filters

In a central inverter, the filter is in a single location (as seen in Fig. 2-8). Conversely, a decentralised cascaded system demands that the filter be spread out across the MICs (see Fig. 2-9). Effectively, the filter in each MIC is smaller, but when added together the cumulative harmonic filtering effect is comparable to that of an equivalently rated central inverter. However, for 2nd order and above filters, this is not the case. As the generated current from different H-bridges (Fig. 2-9) must now flow through one-another, the capacitance 'C' acts as a harmonic bypass to 'L1', significantly affecting the frequency response of the system compared with a centralised equivalent.

Referring to the decentralised 3rd order cascaded system of Fig. 2-9, we can see that from the point of view of a single H-bridge (e.g. H-bridge "D"), the other H-bridge filters (along with the grid impedance) form a total apparent series filtering impedance against any harmonics generated. Effectively, a single H-bridge first sees its own filter, followed by the filters of the other H-bridges and then the impedance of the grid. However, the impedance of other H-bridges from the outside looking in is complex and requires simplification via a Thevenin equivalent Impedance (Zth), which is given in equation (2-2). Zth is an equivalent impedance that represents the filter of an MIC as seen by another MIC. Thus, model wise, a series connected MIC can be represented by Zth.

$$Z_{th} = Z_{L2} + \frac{Z_C \cdot Z_{L1}}{Z_C + Z_{L1}} \qquad (2\text{-}2)$$

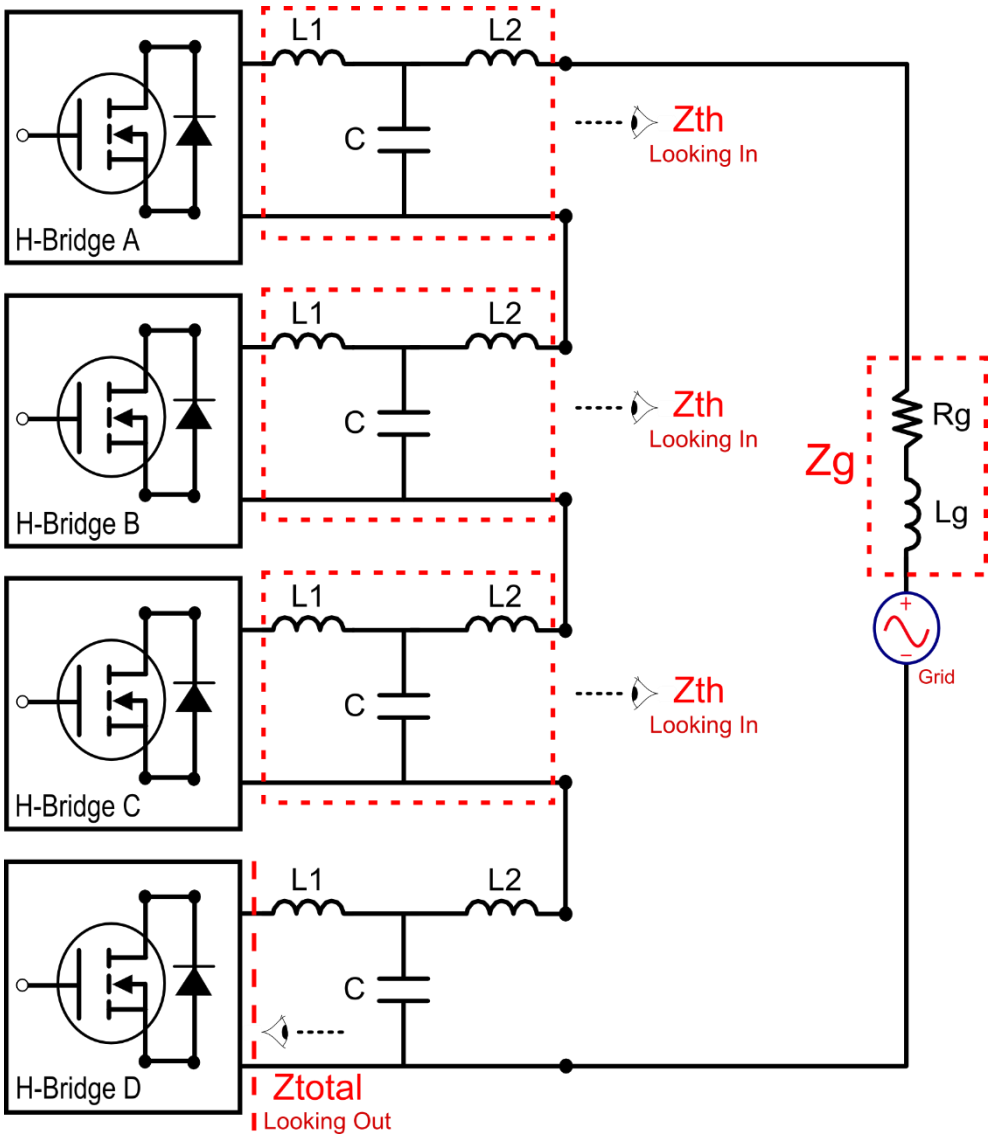

Fig. 2-9. A decentralised 3rd order cascaded 4-MIC system. The impedance looking into one filter from the output of another can be described by the Zth. The grid impedance is described by Zg.

Looking at Fig. 2-10 we can see that from the point of view of a single H-bridge, the grid and other H-bridges can be represented by the series connected impedances Zth and Zg. Thus, the total impedance seen by a single H-bridge as a function of the number of MICs 'n' and the system impedances 'Z' can be calculated by equation (2-3):

$$Z_{Total} = Z_{L1} + \frac{Z_C \cdot [Z_{L2} + (n-1) \cdot Z_{th} + Z_g]}{Z_C + [Z_{L2} + (n-1) \cdot Z_{th} + Z_g]} \qquad (2\text{-}3)$$

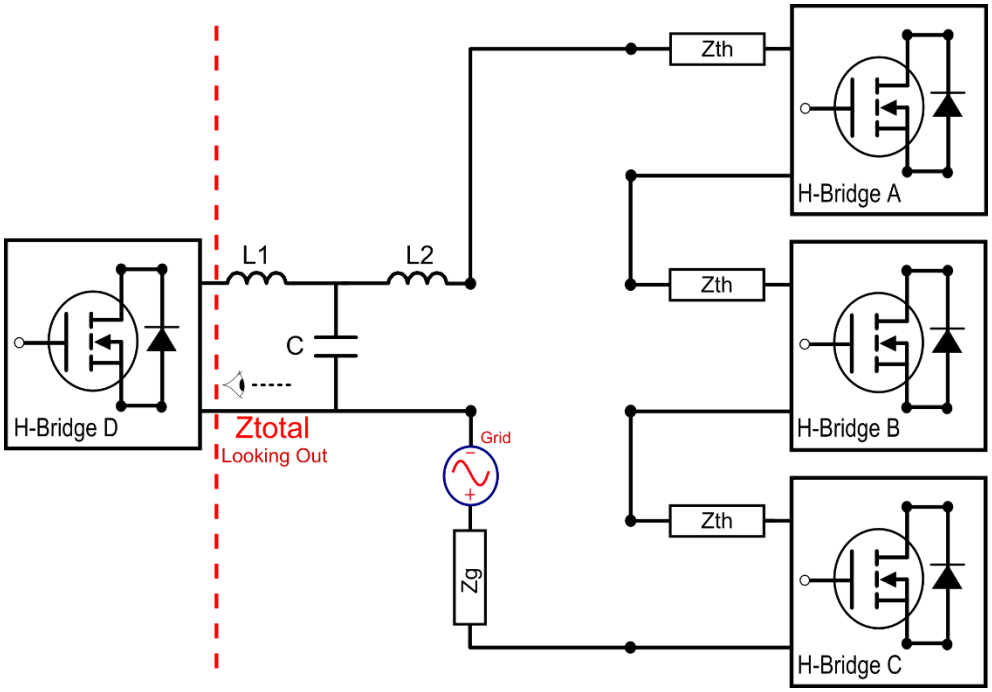

Fig. 2-10. A decentralised 3rd order cascaded 4-MIC system from the point of view of the H-bridge "D". Other H-bridges and the grid are now seen as the series impedances described by Fig. 2-9.

The current generated by an H-bridge for a given voltage produced by that H-bridge is given by equation (2-4):

$$I_{generated} = \frac{V_{generated}}{Z_{total}} \qquad (2\text{-}4)$$

Thus, the current supplied to the grid by an H-bridge for a given H-bridge voltage is given by a current divider between that H-bridge's capacitor and the rest of the entire system (excluding the impedance of L1):

$$I_{grid} = I_{generated} \cdot \frac{Z_C}{Z_C + [Z_{L2} + (n-1) \cdot Z_{th} + Z_g]} \qquad (2\text{-}5)$$

To demonstrate how the decentralised cascaded filter differs from that of a centralised filter, values for L1, C and L2 were selected. According to [29], the resonant frequency of the filter must be at least 10 times that of the grid frequency (to eliminate 50Hz reactive power) and at most, half of the switching frequency. However, to minimise the filter size, a higher resonant frequency is desirable. Thus, a filter resonant frequency of 2.5kHz was selected, allowing for a minimum switching frequency of 5kHz. L1, C and L2 can be found from equation (2-6):

$$F_{resonant} = \sqrt{\frac{L_1 + L_2}{L_1 \cdot C \cdot L_2}} \cdot \frac{1}{2\pi} \qquad (2\text{-}6)$$

For the purposes of this exercise, the centralised filter was configured as follows. C was set to 22µF and L1 and L2 were found to be both 368µH to achieve a resonant frequency of 2.5kHz. However, for the decentralised cascaded cases, these values were divided amongst each of the H-bridge filters. For example, if the number of MICs is 4, then C, L1 and L2 are set to a quarter of the centralised filter case. In this way, the total sum of the filter capacitance and also inductance remains the same for any 'n' sized system. In other words, the total filter energy storage remains the same across a cascaded system of any size. The grid resistance and inductance was maintained at 1Ω and 30µH respectively.

Here equation (2-5) is plotted as a function of the harmonic voltage frequency and the resultant generated harmonic current can be obtained as in Fig. 2-11. Note that for the n=1 case (i.e. a centralised filter) the resonant frequency is 2.5kHz. However, for a cascaded system with 2 MICs (n=2), the resonant frequency doubles to 5kHz, which then increases to 10kHz for the 4 MIC case (n=4). As the true harmonic reduction occurs beyond the resonant frequency and it is recommended that the switching frequency be at least twice that of the resonant frequency (for stability) [29], the minimum switching frequency is effectively pushed up as the number of cascaded MICs is increased.

However, it is possible to operate below the resonant frequency. Looking at the 1st order filter frequency response of Fig. 2-11 (i.e. when the capacitors are removed), it can be seen that that during and before the resonance point that the 1st order frequency response offers greater harmonic current reduction compared with all system sizes. Thus, operating below

the resonance point renders the filtering capacitors worthless and reduces the filter to a 1st order system. As decentralised cascaded multilevel switching techniques have the potential to significantly reduce the switching frequency (see Fig. 2-7) and require the modular filter to be spread over multiple MICs (increasing the resonance frequency), it is almost certain that the final operating switching frequency will be to the left of any 3rd order resonance point. Thus, a 1st order filter offers superior harmonic reduction and stability for decentralised cascaded multilevel MICs.

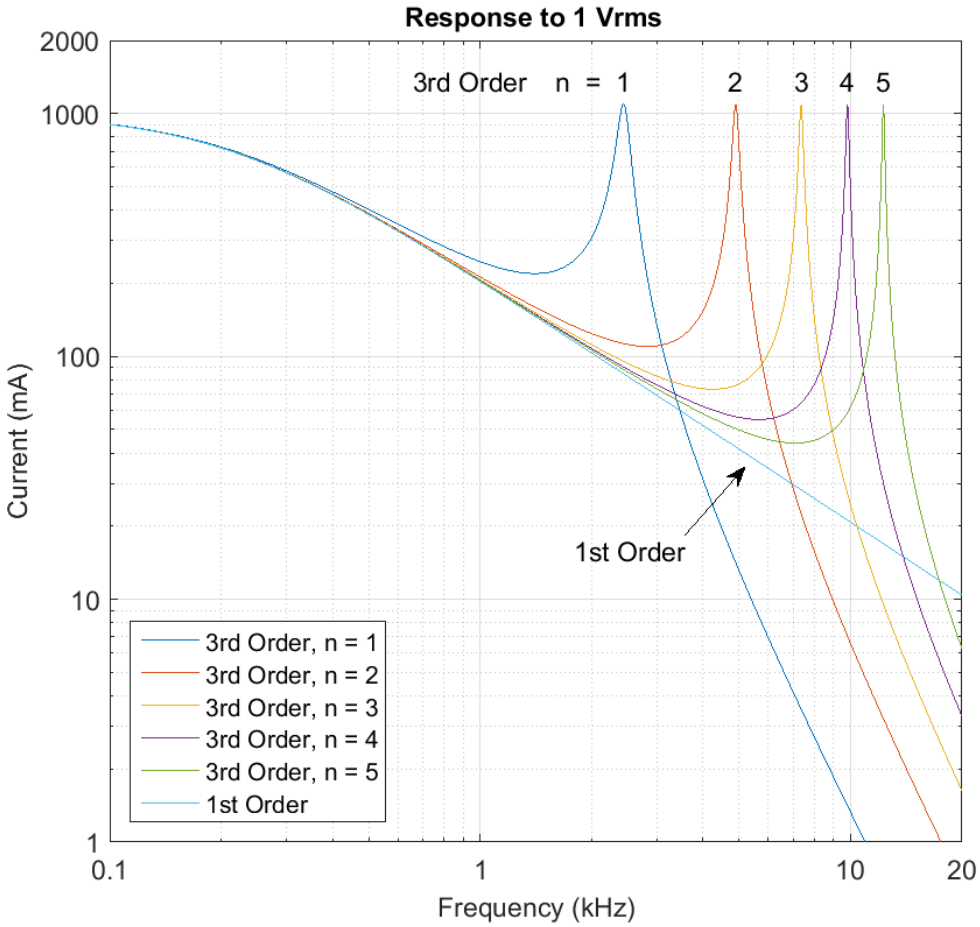

Fig. 2-11. The harmonic grid current generated by an H-bridge supplying 1Vrms to the system described by equation (2-5) for 'n' sized decentralised cascaded filters.

The utilisation of 1st order inductive filters for cascaded systems in the thesis allowed for simplicity in control and the ability to implement the cumulative filter of the entire system as a single inductor. This allowed for easy prototyping of the filter in a single unit that can be quickly modified, but at the same time is functionally identical to distributed

inductors throughout a decentralised filter. In addition, this increased the accuracy and simplified the computer modelling of control as used in chapters 3 and 4.

2.4 MIC Prototype Design

Implementation of a prototype MIC system first requires the design and construction of individual MICs, each as a standalone inverter. Each MIC is composed of four primary circuitry stages that are critical to any power electronics converter. This includes the power electronics stage (H-bridge power transistors, diodes, etc.), the gate driving stage (dead time control, opto-couplers, etc.), the measurement stage (voltages and currents) and the control stage (the µcontroller). For the purposes of simplification of design in this research, the µcontroller section was implemented separately from the H-bridge power module section.

2.4.1 H-Bridge Power Module Circuit Design

Although it was possible to purchase premade H-bridges from manufacturers, it was decided that a custom H-bridge module would be designed and manufactured instead. This approach was selected as it allowed for individual transistor control, specific voltage/current measurements, complete control over power isolation and the implementation of overvoltage protection. In addition this approach also allowed for a complete through-hole component design, which was much easier to physically manipulate the H-bridge module during repairs/modifications if needed. Hence, the custom H-bridge module approach allowed greater flexibility during the prototyping of the cascaded system. A list of the requirements for the H-bridge module is given in Table 2-4.

Table 2-4. The required functional capabilities of the H-bridge power module.

H-Bridge Capabilities	Specific Features
Isolated Measurements	Grid Voltage & Current Measurement PV Voltage & Current Measurement
Isolated Control Inputs	Transistors 1, 2, 3 & 4 On/Off Safety Enable/Shutdown
Isolated Power (DC/DC)	For Grid Voltage Measurement Circuits For all Other Measurements and Gate Circuitry
Protection: Signal Level	Dead Time Shoot Through Protection
Protection: Power Level	Over Voltage Power Dissipation (Solid State) Over Voltage Disconnect (Relay) PV Reverse Shading Protection (Diode)
Energy Storage	Expandable DC-Link Capacitance

The requirements of Table 2-4 were taken and implemented into a general functional circuit diagram that can be seen in Fig. 2-12, demonstrating how the H-bridge power module functions and its input/outputs.

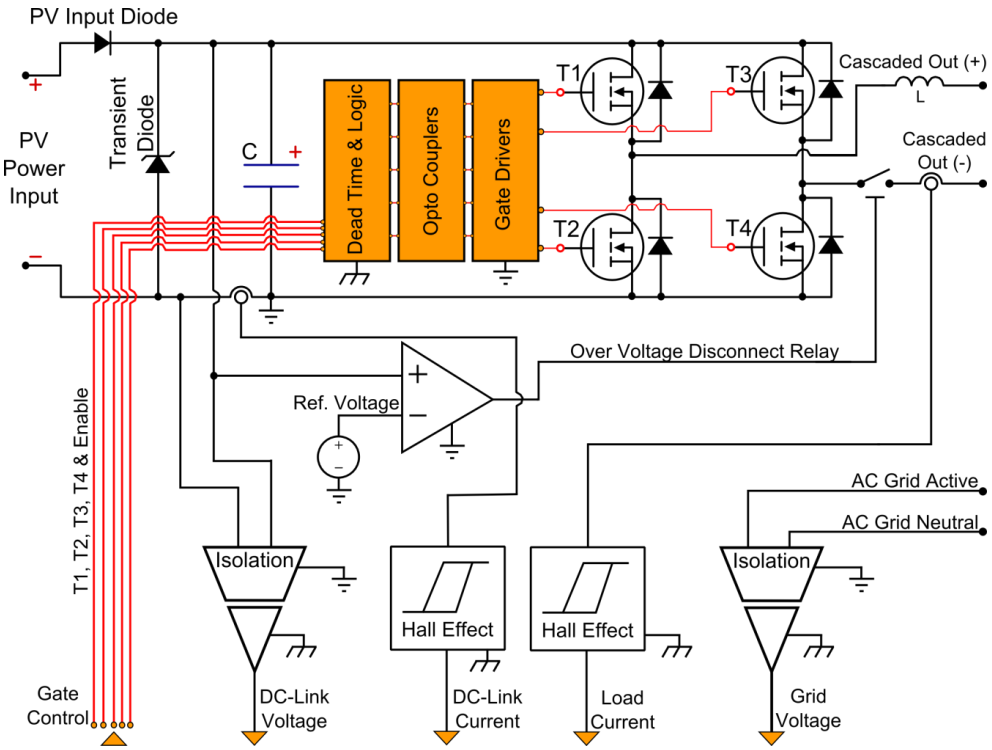

Fig. 2-12. A complete breakdown of the primary functionality of the H-bridge power module prototype. See appendix 6.2.1 for further details.

Fig. 2-12 shows that power is fed from the PV panel (modelled by a power supply in the lab) through the PV diode (DSEI60-02A 200V/69A), which then charges the (expandable) 63V/3300µF DC-link electrolytic capacitors. If the DC-link voltage exceeds safe limits, then a transient diode (5KP43A 45V) dissipates power briefly. If over voltage conditions continue, a power relay (RTD34012F 230V/16A) disconnects the grid from the entire H-bridge module. The H-bridge itself contains 4 MOSFET switching devices (IRFP3006 60V/200A) in a standard configuration with internal integrated freewheeling diodes.

Gating signals to the H-bridge module are first introduced through a dead time (1.5µs) and logic block, which introduces asymmetrical switching delays and protects against invalid MOSFET operating states (preventing shoot through). Gating signals then pass through optocouplers (HCPL2631), providing electrical isolation for MOSFET control.

Finally, the gate drivers (IRS2110) take the gate signals and drive the MOSFETs. These gate drivers are powered from 15V by an isolated DC/DC power converter (JAH0224D15), which also powers the optocouplers. The gate drivers are of the bootstrap variety and contain a maximum duty cycle limitation (about 98%).

The H-bridge output current (or grid current) and the PV input current are both measured by high bandwidth (200kHz) Hall effect sensors (LTS 6-NP), whilst the DC-link voltage is measured through an isolation amplifier (ISO122PE4), with a moderately high bandwidth of 50kHz. Finally, the grid voltage is also measured by an identical isolation amplifier (ISO122PE4, 50kHz), which is powered by an isolated DC/DC converter (IL2424S) from the rest of the gate drive and voltage/current measurement circuitry.

2.4.2 H-Bridge Power Module PCB Layout

In order to ensure the H-bridge power module had a rugged reliability and resilience, very wide traces and large tolerances were used. To further this goal, all components used through-hole packages, meaning simplicity with further manual variation was still possible. Strong bypass capacitors and snubber circuits were utilised where possible. Ultimately, the final H-bridge power module design was a basic, yet powerful and rugged generic H-bridge block which could be inserted in a final cascaded and/or parallel system.

Fig. 2-13 shows a small version of both the layout traces and a computer generated 3D rendition of the H-bridge power module PCB. Fig. 2-14 then visualises how the functionality of Fig. 2-12 and Table 2-4 is distributed around the final PCB.

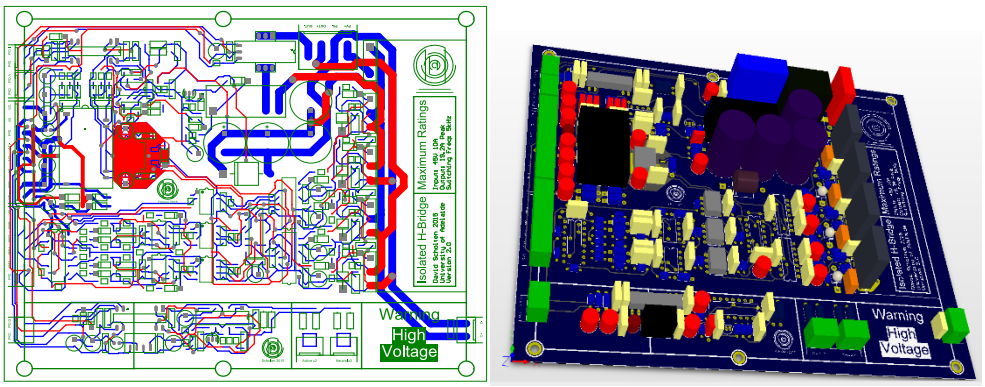

Fig. 2-13. The H-bridge power module PCB layout in the Altium Summer 09 environment.

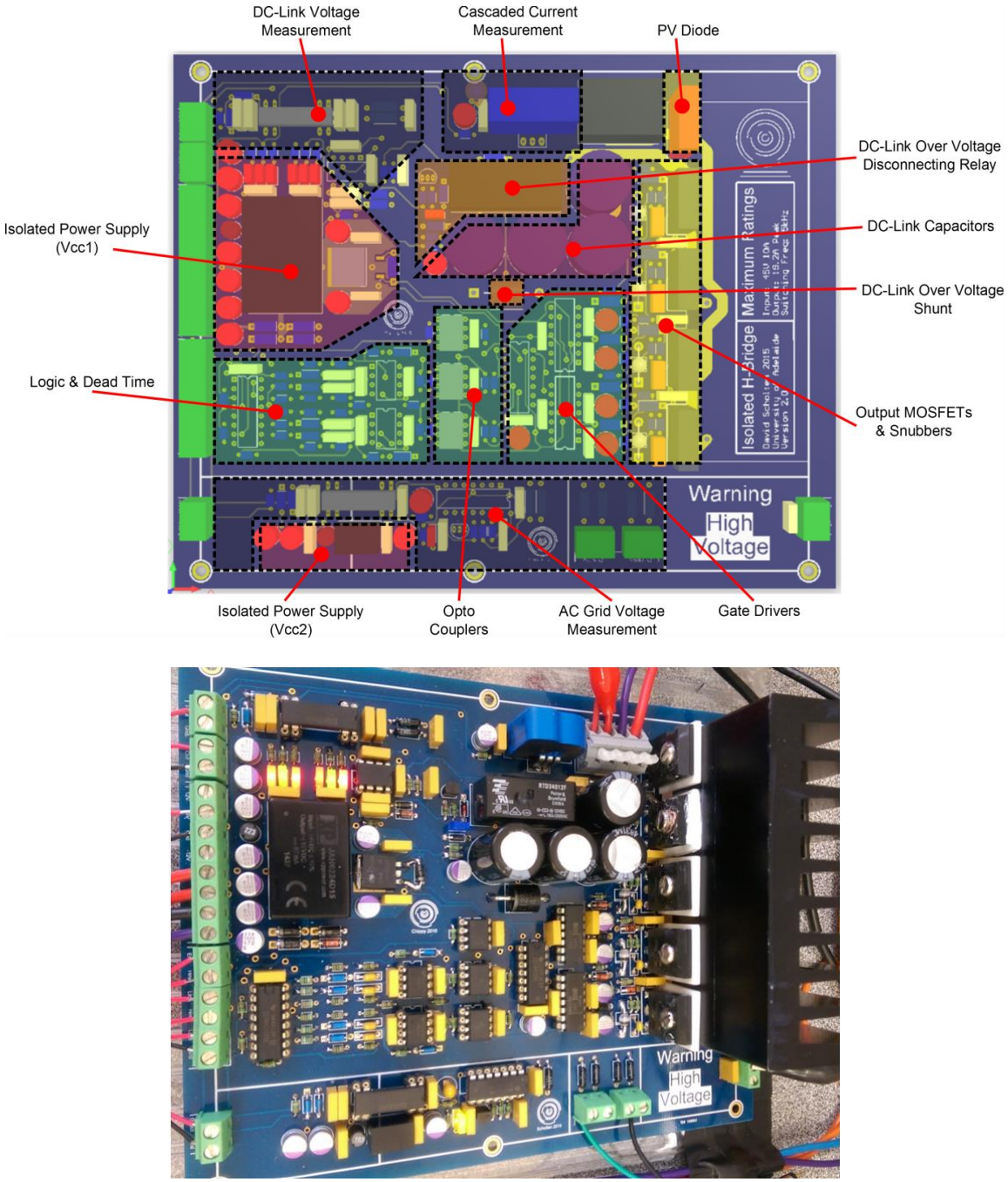

Fig. 2-14. The H-bridge power module PCB functional overlay (top) and the populated PCB (bottom). Note that the PV current measurement was implemented separately as a late addition.

As a common practice, digital control signals were kept well away from analogue measurement circuits and star grounding was used to minimise interference between the two circuits. The switching time of the MOSFETs were maximised in order to reduce di/dt noise across the entire board. Relevant components were kept as close to each other as

possible and bypass capacitors were used liberally, without constraint. All electrically safe connectors were placed at the left side of the PCB for ease of connection and control purposes. The heat sink is also positioned on the right side of the PCB with the possibility of multiple H-bridge modules being stacked and sharing a common cooling fan.

2.4.3 µController Interface, Communications and Software

Although the H-bridge power module contained the power electronics, gate driving capability and measurement capability of the MIC (as stated earlier), it did not contain the control stage (i.e. a µcontroller). Separating this stage allowed for the use of off-the-shelf µcontroller development boards, permitting simple interfacing with µcontrollers that are sold in small footprint surface mount packaging. To permit maximum flexibility during research, a µcontroller development board was chosen that was both powerful and well supported. The Arduino Due was used which contains a 84MHz 32-bit SAM3X8E µcontroller. Since the Arduino Due utilises 3.3V logic, an interfacing circuit was built (see Fig. 2-15) to match the 5V logic levels of the H-bridge module.

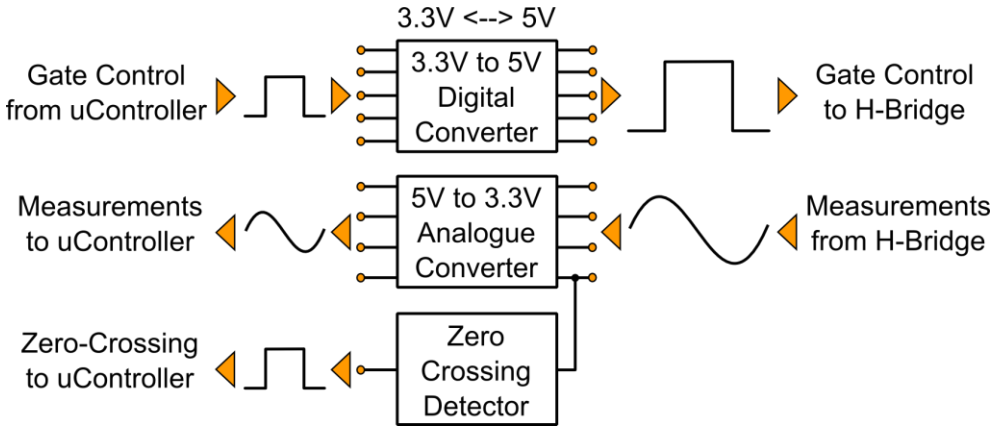

Fig. 2-15. A breakdown of the functionality of the 3.3V to 5V converter utilised to interface the 3.3V SAM3X8E µcontroller with the 5V H-bridge power module. (See Fig. 6-17 for the complete circuit diagram).

As shown in Fig. 2-15, we can see the converter board needed to convert both digital signals from 3.3V to 5V and analogue signals from 5V levels to 3.3V levels. As the incoming signals had already been conditioned by the H-bridge module to suit a 5V µcontroller (especially the analogue signals), adapting them to a 3.3V equivalent was conceptually very simple. To further simplify the operations of the Arduino Due (SAM3X8E), the zero-crossing detection of the grid voltage was performed by separate

electronics also included in the 3.3V to 5V circuit. However, the analogue portion of the constructed conversion circuit proved difficult to calibrate. Since the central zero point of the analogue signals constantly drifted with time, high precision multi-turn potentiometers are used to achieve stability. The final implementation of one of these converters is illustrated in Fig. 2-16.

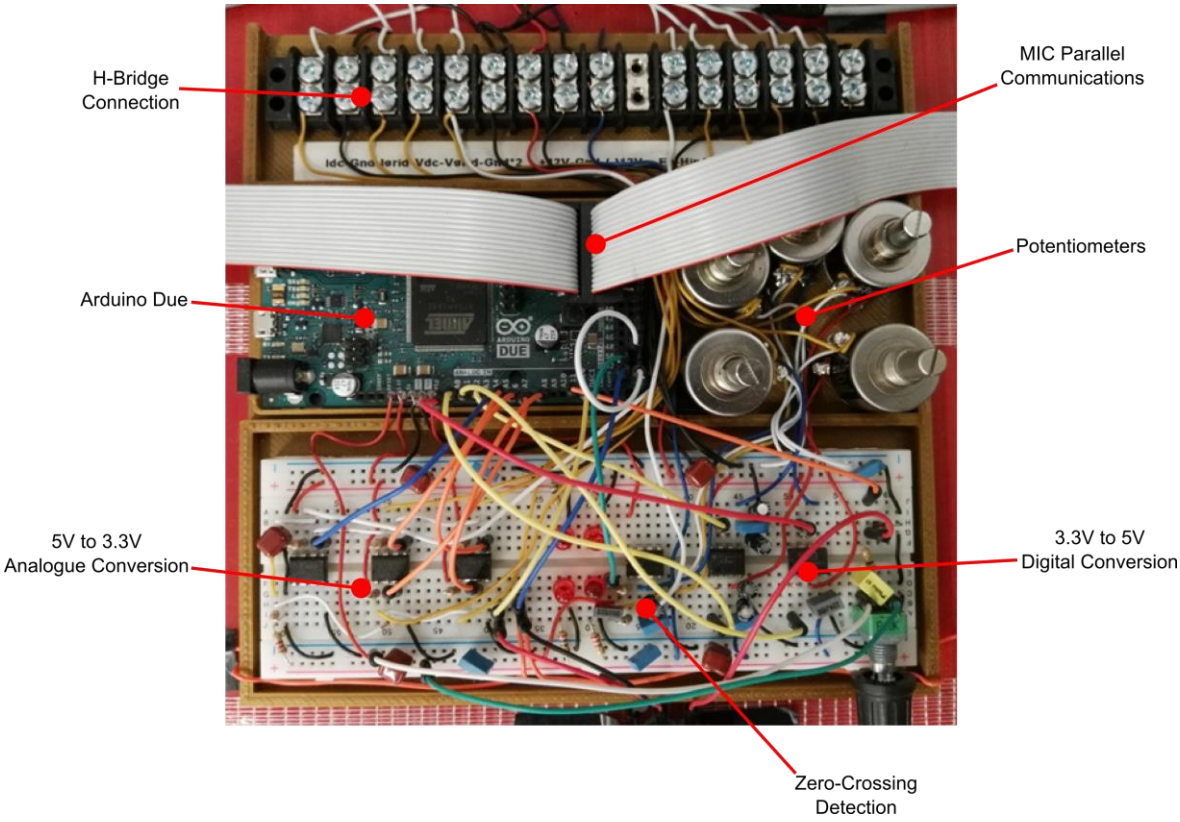

Fig. 2-16. An image of the final implementation of the 3.3V to 5V converters of Fig. 2-15.

Software for the SAM3X8E µcontroller was written in C using the Arduino interactive development environment (IDE). Low level control of the H-bridge power module was primarily implemented through interrupt driven code. At regular intervals an interrupt would trigger according to a timer and all relevant system measurements would be sampled. From this, the gates of the H-bridge power module would be controlled according to the measured grid current (i.e. current control) and the harmonic limits set. Slower functions such as serial communications, measurements of some variables (i.e. DC-link voltage) and MPPT were operated based on flags set by timers. Essentially, current control was prioritised and everything else occurred in the µcontroller's spare processing time. In

efforts to maximise the sample rate of the SAM3X8E µcontroller, floating point calculations were reduced, some overclocking was performed and logical shortcuts were applied to make sacrifices for speed where possible.

The communications link between the MICs was implemented using a custom 16 pin parallel communications link rather than wireless or EOP protocols. This allowed for greater flexibility during the development of the µcontroller code and complete control of communications timing and troubleshooting processes. The logic of the custom 16 pin parallel communications protocol can be seen in Table 2-5.

Table 2-5. Logic breakdown table of the 16 pin custom parallel communications protocol.

Pin No.	Function
1	MASTER CLK
2	SLAVE RSP
3-4	ADDRESS
5-16	12-BIT DATA

Although the decentralised cascaded system is decentralised in concept, it is practical (from a research perspective) for one MIC to carry out some additional master control functions. Thus, the communications protocol assumes that there is one master and three slaves. First, the master writes an address to pins 2 and 3. The appropriate slave then responds with pin 2. The master then uses the part of the data bus (pin 5) to indicate if it wishes to send or receive. The slave then responds with pin 2 again. For the case of sending, the master places data on the line (pins 5-16) and the slave responds with pin 2 once it has read the data. For receiving, the slave places data on the line (pins 5-16) before then signalling that the data is ready to be read by responding with pin 2. Each stage in the communications procedure is synchronised by the master's clock (pin 1).

Multilevel switching requires the exchange of timing information between MICs to facilitate the construction of a staircase waveform that satisfies the conditions of MPPT. Each MIC can measure the grid voltage magnitude (through the grid voltage tap) and assumptions can be made that each MIC has approximately the same DC-link voltage. This alone would allow multilevel operation without communications, but MPPT demands that the balance of power between the MICs be variable. Thus, it is necessary to have the inter-

MIC communications of power targets (for MPPT) and corresponding timing information to reconstruct a new multilevel waveform that rebalances the power across the system according to the targets. Effectively, decentralised cascaded multilevel operations in a PV system requires a form of communications link between MICs.

2.4.4 Prototype System Implementation

Implementation of the prototype system involved establishing a virtual grid that could be used with the cascaded MICs (i.e. creating the grid seen in Fig. 2-1). This was accomplished through the use of multiple 30V/300VA transformers that were finely controlled (in voltage) using a variac on the primary side.

Fig. 2-17 shows the basic connection layout of the prototype system. Note that we can see that AC power (230Vrms grid) is connected to the power supplies, which then feed the cascaded MICs. This power then continues through the inductive filter and into the transformers (i.e. the virtual grid) followed by the variac that connects back to the 230Vrms AC grid. However, there is also a resistive load bank attached to the transformers that represents a parallel load on the virtual grid. The cascaded MICs are controlled by the PC directly (serial link to the master MIC) and indirectly (through the Simulink DSPACE module). Power analysers and measurement devices are also accommodated in the system. Fig. 2-18 shows the implemented "cascaded MICs" portion of the system from Fig. 2-17.

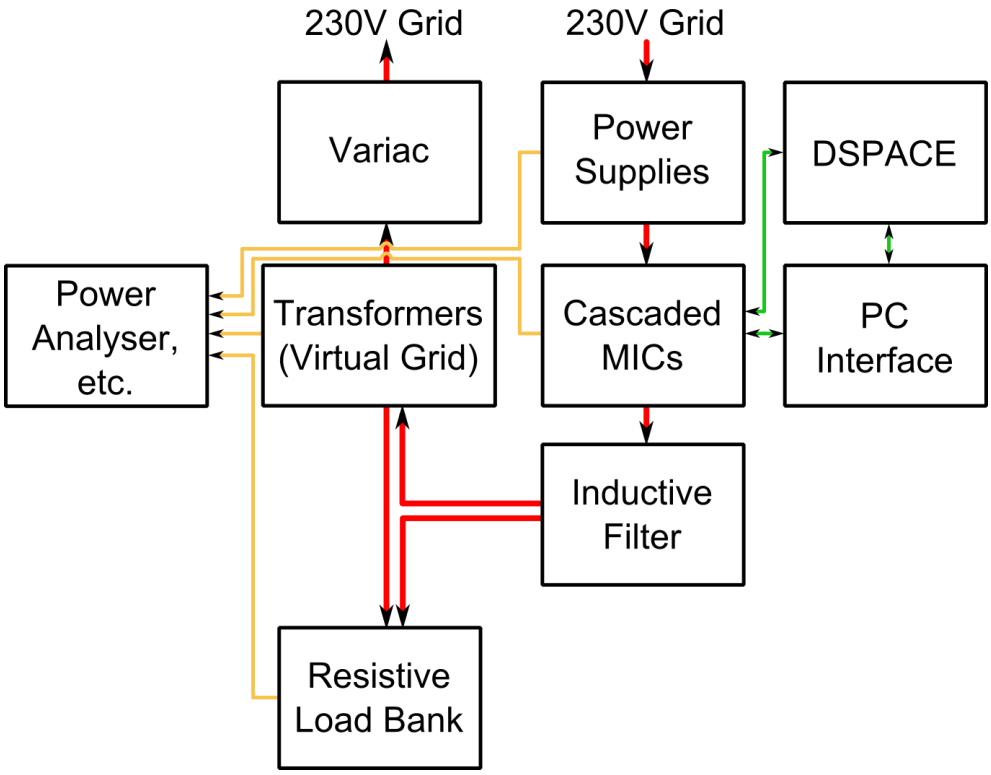

Fig. 2-17. Overview of the final prototype system as implemented in the lab. Red lines indicate the flow of power, green lines are for control and yellow lines are for lab measurements.

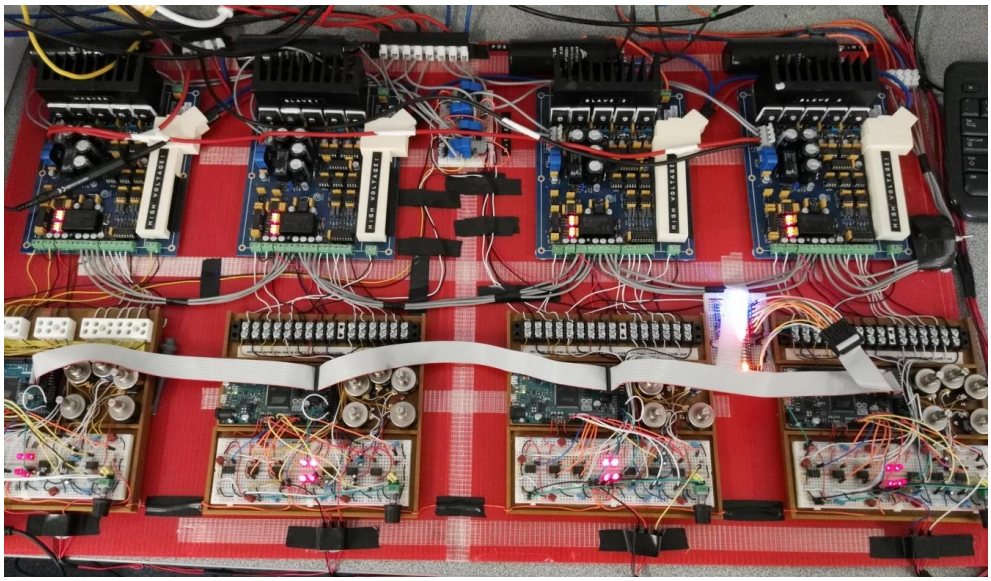

Fig. 2-18. The 4-MIC system seen in the "cascaded MICs" block of Fig. 2-17. Top: The four MIC power stages. Bottom: Serially linked master/slave controllers.

It should be noted here that using variacs and transformers increases the source impedance (i.e. grid impedance). Typically this was found to be about 1Ω looking in to the secondary of the transformers. To offset this, the resistive load bank can be set to dissipate an amount of power that is equal to the power being generated by the cascaded MICs. This creates a situation where the net power through the variac and transformers is near zero, negating the effects of the grid impedance. However, for a varying MIC power this is difficult and was not always utilised.

2.5 Summary of Results

In this chapter the practical decentralised cascaded multilevel system was analysed and the ideal number of cascaded MICs was found. This was done through consideration of the MOSFET voltage-resistance ratios, film capacitor viability at different voltages, multilevel switching frequencies, partial shading resistance, DC-link voltage gain requirements and the increasing likelihood of faults with larger systems. This analysis was performed using both market data and analytical calculations. After determining the system size, the decentralised modular nature of the cascaded filter was then analysed.

By developing equations to describe the grid current harmonics produced by a cascaded MIC, the frequency responses of the filters were plotted and compared to show the effect of filter decentralisation as the system size increased. From this the ideal filter order was found.

Finally, knowing both the system size and filter type, the MICs themselves were designed based on the unique safety requirements of a decentralised system that relied on accurate series voltage balancing for successful operation. Implementing this resulted in the production of the final prototype decentralised cascaded multilevel system for utilisation in this research. The key findings of this chapter are summarised below:

- Decentralised cascaded systems only require one additional conductor to be added to the cable lug in comparison with micro-inverter systems. However, multilevel operation requires Ethernet Over Power (EOP), wireless or other forms of MIC to MIC communications to generate a staircase waveform that can accommodate the MPPT differences between MICs.

- The ideal system sizes for the decentralised cascaded multilevel system was found to be between 3 and 8 for a 110Vrms grid and between 4 and 10 for a 230Vrms grid. In both cases the 4-MIC system size scored highly and was chosen as it can be used at both grid voltage levels.
- The basic 1st order filter was compared with the 3rd order filter for modular distribution across cascade-connected MICs. It was found that as the inductance/capacitance of a standard filter was spread across an increasing number of MICs, the unusable resonance point (and thus the ineffectiveness of the filter) proportionally increased in frequency. It was concluded that the low switching frequency of multilevel control would result in an operating region resulting in the same harmonic current reduction for both 3rd and 1st order filters. Thus, 1st order filters were selected for simplicity.
- The final MIC prototype system contained powerful overvoltage safety features and a custom communications protocol that allowed complete control over all system wide timing. The connected virtual grid was generated by multiple 300VA transformers with a variac on the primary side for fine tuning.

In conclusion, as will be analysed in the following chapters, the decentralised cascaded multilevel level system is a practical solution that can be used in small scale PV rooftop environments. Any such system will require MIC-to-MIC communications, 4-8 cascaded MICs, a 1st order inductive filter and over-voltage protection capability.

3 Comparative Analysis of Parallel and Decentralised 2-Cascaded MICs

Compared with PV micro inverters, multilevel cascaded MIC systems have the added advantages of multilevel waveform switching and higher conversion efficiencies due to the absence of high gain voltage boost requirements and reduced filter requirements. However, decentralised control with restrictive low bandwidth communications is preferred over traditional centralised operation. This chapter aims to provide a detailed comparison analysis of PV MIC systems operating in both parallel (analogous to micro inverters) and cascade (decentralised, 2-MIC & multilevel) configuration with equivalent hardware. The latter system (cascaded) can be seen in Fig. 3-1.

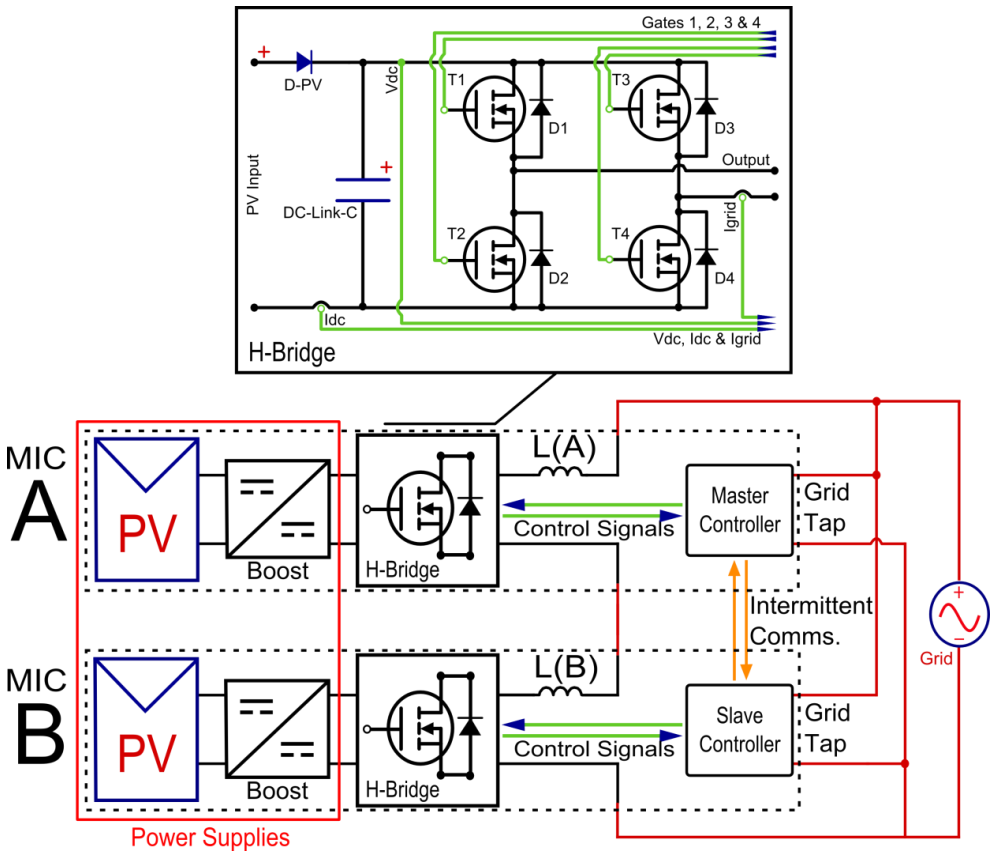

Fig. 3-1. The 2-MIC multilevel decentralised cascaded system with built in local switching control (a detailed diagram of the H-bridge can be seen in Fig. 2-12).

Using simulation models and the hardware developed in section 2.4, the harmonic current, switching frequency, efficiency and losses of the differently configured, identical MICs are compared. An analysis of the MIC filter design confirms that a 50% per-MIC filter reduction when moving from the parallel to the 2-MIC cascaded system maximises the efficiency and halves the per-MIC switching frequency. Inherent zero-crossing mismatch issues and power sharing limitations are also analysed for the 2-cascaded configuration. It was found that with only a 4˚ relative phase error in zero-crossing detection, the 2-cascaded system could no longer meet grid requirements. In addition, the power ratio between the two MICs in cascade could almost exceed 2:1 before substantially increasing the harmonic current.

3.1 Introduction

3.1.1 Background

As explained in sections 1.5 and 1.6, there are many potential system topologies for small scale PV systems, but it is the cascaded system that has the ability to perform multilevel switching and per-panel MPPT without the need for high-gain boost converters. Effectively, this combination of characteristics allows for the maximum energy yield from a PV system over its lifetime. However, a cascaded inverter requires decentralisation to reduce the physical complexity of the system to allow for simple and low cost installation in small scale applications. Both a communications link between MICs and a parallel measurement tap from each MIC to the grid are required for multilevel switching. The research in [23-26] approached the cascaded decentralised MIC problem by forfeiting the ability to utilise multilevel voltage interleaving between series connected MICs, opting for a sinusoidal output from each MIC instead. Such simplification allows operation without the need for MIC-MIC communications, achieving series modular operation. A multilevel approach is reported in [27], where there are direct connections to the grid and low bandwidth data links existed between the MICs. This approach allowed for advanced timing between MICs to perform multilevel voltage interleaving, which is a key benefit of the standard cascaded inverter.

This chapter considers the topology as shown in Fig. 3-1, where communication links are used to allow for series voltage interleaving (see section 1.7). Note that in this

topology, even when restricting communications between cascaded MICs to the bare minimum, it is possible to carry out multilevel operations with only a grid connection and a simple wireless link (or power line communications (PLC) through the grid measurement connection). As each MIC is also directly connected to the grid, critical zero crossing information for timing is available to all MICs, which is utilised in control synchronisation for multilevel voltage interleaving. A working decentralised cascaded PV MIC system is simply several MICs connected in series, but without a central controller. In order to make concessions for a varying PV voltage (I-V characteristics), there needs to be an assumption of a low-gain boost converter. For example, a boost converter in the MIC module is used in [26], but only for up to a maximum voltage gain of 2. This is to avoid the necessary over rating of the MICs with unregulated DC-links and is a compromise between over rating costs/losses and boost converter costs/losses.

This chapter aims to benchmark the performance of decentralised multilevel cascaded MICs against a base reference analogous micro inverter system (parallel) operating with an identical hardware and load configuration. The filter selection, harmonic current, switching frequency, power losses and zero-crossing synchronisation error and MPPT restrictions are all compared and analysed. Any intrinsic operating limitations of such decentralised cascaded systems need further exploration and analysis if they are to ever see widespread practical use in low power applications.

3.1.2 Comparison Assumptions & Parameters

To make a valid comparison between a parallel and a cascaded MIC system (containing two MICs in series), two test systems have been conceptualised. The first is as seen in Fig. 3-1, which is considered as the cascaded arrangement. The second is the parallel arrangement, which is simply one of the MICs operating independently. Both configurations expose the MICs' identical voltages, currents and power conditions, which provides a comparison of MICs at equal ratings. Thus, it is the grid voltage that changes when moving from the parallel MIC system to the 2-cascaded MIC system configuration. This was done in order to normalize the comparison. It should be noted that only a single MIC is present in the parallel configuration (instead of two MICs in parallel), as the effects of accidental switching interleaving were intentionally avoided. Furthermore, MPPT was not implemented in either configuration. A summary of the parallel and cascaded MIC

system parameters are given in Table 3-1.

For the simulation aspect of this comparison, a MATLAB Simulink based simulation was developed. The hardware prototype uses the H-bridge power stages explained previously in section 2.4. Both the simulation and prototype were configured according to Table 3-1 for this comparison. The filtering inductance is chosen (see section 3.2.1) to maximise the efficiency of the parallel and 2-cascaded MIC configurations.

Table 3-1. Comparison of system variables for the Parallel and 2-cascaded system.

Variable	**Parallel**	**2-Cascaded**
MIC PV Voltage	42Vdc	42Vdc
MIC Power Out	200W	200W
MIC Voltage Out	38V peak	38V peak
MIC Current Out	10.52A peak	10.52A peak
MIC MPPT	No	No
MIC DC-Link C	18.3mF	18.3mF
Per-MIC Filter "L"	**495uH (137uJ/W)**	**248uH (68.5uJ/W)**
Grid Power	**200W**	**400W**
Grid Voltage	**38V peak**	**76V peak**
Grid Current	10.52A peak	10.52A peak
Rated Specs.	50Hz, <5% THD, PF = 1	50Hz, <5% THD, PF = 1
Per-MIC Current Sample Freq.	160kS/s	160kS/s

3.1.3 Comparison Hardware

MIC prototype hardware with the specifications of Table 3-1 was developed for the parallel/cascaded comparison. Each MIC consists of a power supply (42V/428W capable), H-bridge (Fig. 2-12) and a SAM3X8E microcontroller with voltage/current sensors and gating control. For the purposes of comparison in this paper, no physical boost converter is used. Instead, the power supplies were used to represent the outputs of PV modules with boost converters (constant voltage at 42V). A large 18.3mF capacitor was used to represent a "near-perfect" DC-link for each MIC, completely decoupling the 100Hz power ripple. Cascaded communications between MICs for the comparison was achieved using a two wire I2C serial link between the MICs that transceived once a second and updated variables relating to current reference commands and voltage transition timing. Note that the 16 pin parallel communications link was not used here (utilised in section 4). The finer timing of

these instructions were executed based on the calibrated grid zero-crossing measurement tap of each MIC. The parallel 38Vpeak grid was created using a single 30V-300VA transformer, whilst the 2-cascaded 76Vpeak grid was created using two of these transformers in series. The voltage was finely adjusted on the primary side with a 230Vrms auto-transformer. The effective series inductance of this grid configuration was found to be minimal compared with that of the designed grid filtering inductance. Hysteresis control was used to rapidly control the current with a 160kS/s sampling frequency per-MIC. The AS/NZS 4777.2 standards [9] were used as a guideline to harmonic performance. Specifically, the harmonic current of the first 50 harmonics (<2.5kHz) was kept below 5% of the rated current. The prototype system can be seen in Fig. 3-2.

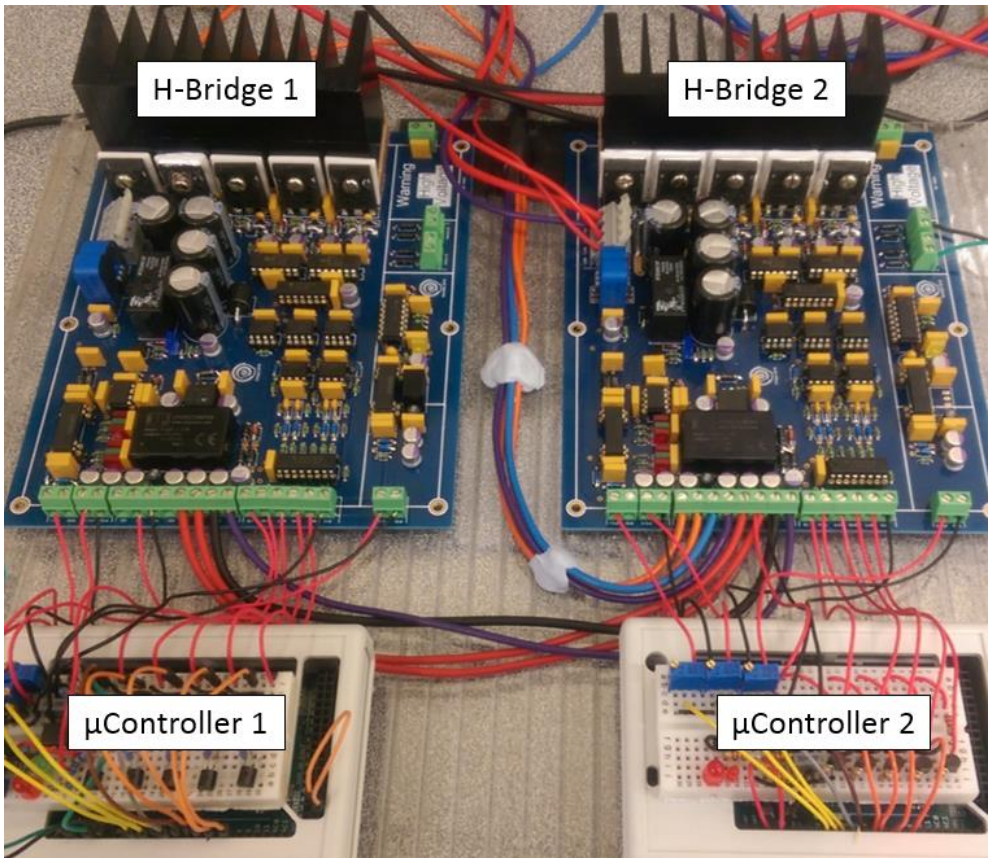

Fig. 3-2. The prototype hardware implementation of the comparison MICs. For this comparison old versions of the 3.3V to 5V µcontroller boards were used.

3.1.4 Comparison Software

Hysteresis control was chosen for the parallel and cascaded systems so that the ripple current could be directly specified. This therefore sets the switching frequency as a

dependent variable of the total harmonic distortion (THD), which is useful for comparison purposes and grid-tied operation. The current reference of the inverter, along with upper and lower bands, are generated and compared with the measured current through the load (see Fig. 3-3). As a result of this control, the switching frequency is inversely proportional to the distance between the hysteresis bands. Note that the hysteresis band-width represents the maximum peak-to-peak ripple of the harmonic current, which in turn controls the THD, which is the ratio of the ripple current root-mean-squared (RMS) magnitude to the fundamental current RMS magnitude (IEEE specification). For a harmonic waveform which has a triangular shape with a certain RMS and peak value [30], the THD at the rated power can be given by:

$$THD_{Rated} = \frac{I_{Harmonic_{RMS}}}{I_{Rated_{RMS}}} = \frac{I_{Harmonic_{Peak}}}{\sqrt{3} * I_{Rated_{RMS}}} \qquad (3\text{-}1)$$

In order to adapt hysteresis current control to work with a cascaded system, a modified version of the sorted pulse width modulation was used [31]. As illustrated in Fig 1-12, at any one time, only one cascaded MIC may be operating under hysteresis current control, whilst all other MICs are either on or off. To control and synchronise the timing of these different operating modes across the system, the locally detected grid zero crossing of each MIC was utilised in conjunction with a low bandwidth data link between MICs.

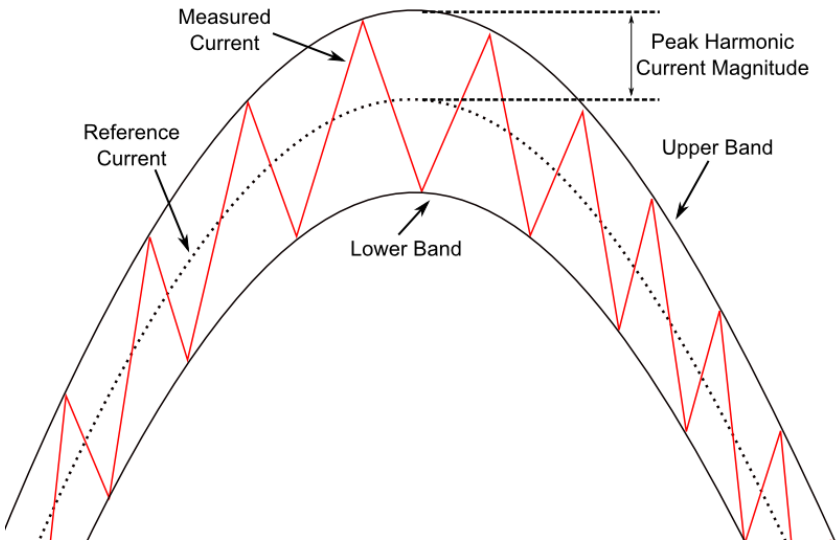

Fig. 3-3. Hysteresis band based current control for a traditional grid-synchronised inverter.

The approximate proportional relationship between the switching frequency and other operating variables of a hysteresis current controlled MIC can be given by:

$$f_{sw} \propto \frac{V_{DC-Link} * V_{Grid}}{I_{GridRated} * THD_{Rated} * L_{MIC} * n^2} \qquad (3\text{-}2)$$

Where f_{sw} is the average switching frequency of a single MIC, $V_{DC-Link}$ is the average H-bridge DC-link voltage, I_{Grid} is the output current to the grid, $V_{Grid}$is the grid voltage, L_{MIC} is the filtering inductance per-MIC and n is the number of MICs in the cascaded system. Accurate analytical calculations of the exact switching frequency for a given hysteresis system are possible [32].

For standalone, voltage controlled inverters, it is typical that the switching frequency is held constant whilst the harmonic current changes in response to a given load condition. However, as this chapter's comparison is between grid-tied, current controlled inverters, where multilevel versus non-multilevel operation is a main point of comparison, it is more suitable to hold the harmonic current constant (i.e. hysteresis control) rather that hold the switching frequency constant. This allows for a simpler presentation of how the switching frequency difference between the two systems is attributable to the average size of the voltage step applied by each system to the output grid filter (in proportion to the grid voltage magnitude), which therefore influences the average di/dt and thus the switching frequency itself. Thus, we can more immediately see the switching frequency benefits of multilevel operation.

3.2 Comparison of Parallel/Cascaded Filter Design

3.2.1 Filter Inductor Selection

The grid filtering inductances (L(1) and L(2) in Fig. 3-1) are an important design parameter. Their values are a tradeoff between the filter copper losses and the MIC switching frequency. Increasing the grid filtering inductance reduces the grid current di/dt and increases the Ohmic resistance in the filter, which in turn reduces the switching frequency (i.e. reduces switching losses) and increases the conduction losses respectively. A MATLAB Simulink simulation with configurable MIC blocks (see appendix 6.1) was used to obtain the operating switching frequencies for loss and efficiency calculations. To

obtain the "rated" efficiencies of the MICs across the entire output power range of both system configurations, the California Energy Commission (CEC) standard was used, which places significant weighting on the 50% and 75% input power efficiency operating points, as shown in Fig. 3-4. In this comparison research, the output power (%) was used to calculate the metric in place of the input power (for reasons of prototype simplicity).

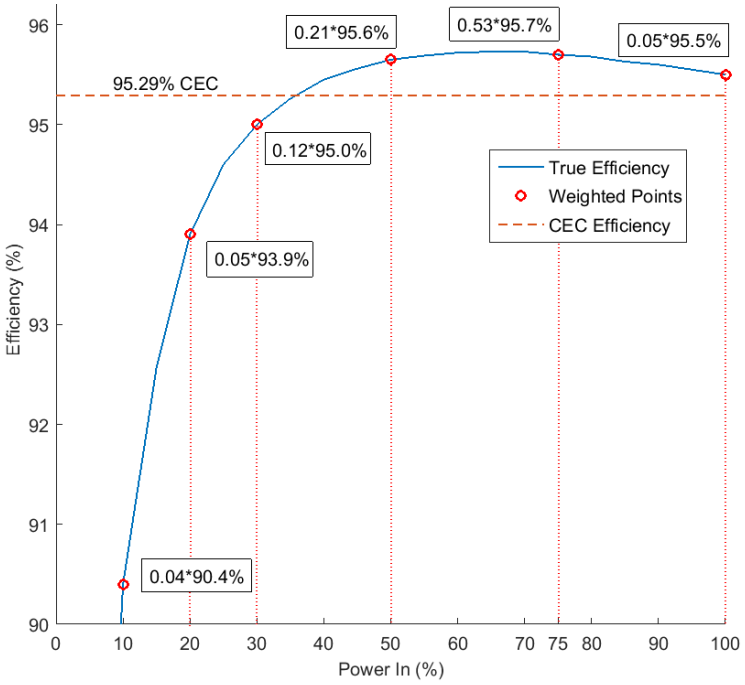

Fig. 3-4. An example case of the California Energy Commission (CEC) weighted efficiency calculation. This metric weighs the efficiencies at different input power levels.

A number of inductor values were simulated for both the parallel and 2-cascaded systems until two values of inductors (330µH and 165µH) were found that maximised the CEC efficiency respectively (see Fig. 3-5). The superior efficiency of the 2-cascaded system compared with the parallel system is due to the inherent switching frequency advantage of the multilevel interleaved topology, which is explained in section 1.6. The multilevel switching frequency reduction in the 2-cascaded case allows for a smaller grid filter to be utilised, which in turn reduces the conduction losses. The balance between the switching losses and conduction losses results in clear efficiency peaks for both systems.

However, due to hardware sampling limitations (160kS/s), 495µH was chosen for the parallel system (instead of 330uH) and 248µH was chosen (per-MIC) for the 2-cascaded

system (instead of 165uH), which are both seen in Table 3-1. The chosen parallel MIC inductor (495µH) is rated for 10.52A, with a stored energy of 27.4mJ. As the MICs are rated for 200W output, this is a grid filter storage-to-output power ratio of 137.0µJ/W. Similarly, the 2-cascaded MICs each have a chosen filter inductance of 248µH (13.7mJ) with the same ratings, placing their same ratio at 68.5µJ/W. Note that the rated filter energy per watt is a useful metric as it is independent of the inverter power.

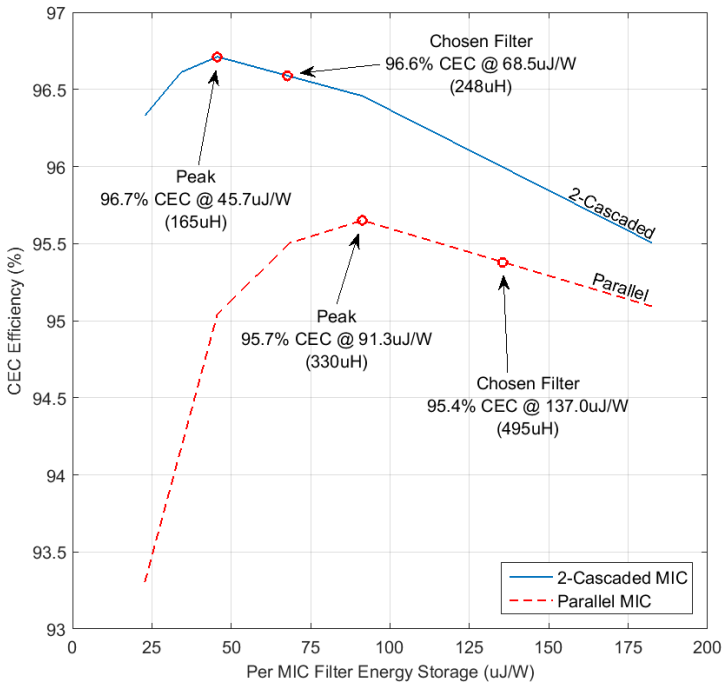

Fig. 3-5. The simulated CEC efficiency of the parallel and 2-cascaded MICs as a function of the per-MIC output filtering energy storage.

3.2.2 Switching Frequency and Filter Conduction Losses

To help understand what process is driving the decrease in filtering inductance per-MIC when moving from the parallel system to the 2-cascaded system, Fig. 3-6 shows how the switching frequency varies with the energy storage of the inductive filter per-MIC. Starting with Point A highlighted in Fig. 3-6, if the per-MIC filter energy storage is kept the same between the parallel and 2-cascaded systems then the switching frequency per-MIC is reduced by 71% (Point B). Similarly, if the switching frequency is maintained, then a 74% per-MIC filter energy storage reduction can be achieved (Point C). An operating point was chosen between the two (Point D) that gave a 42% switching frequency reduction and a 50% per-MIC filter reduction in the simulation when moving from the parallel to the 2-

cascaded configuration (i.e. approximately 50% switching and conduction loss reduction).

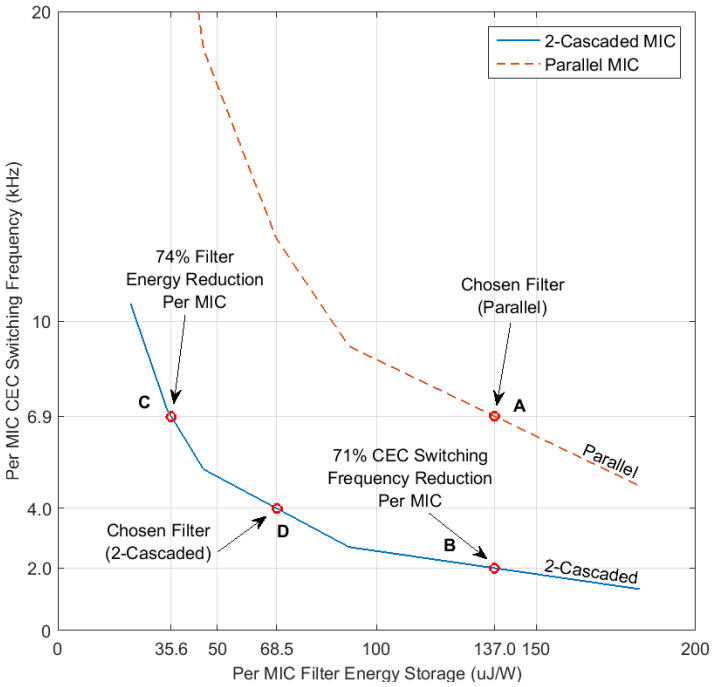

Fig. 3-6. The simulated CEC switching frequency of the parallel and 2-cascaded MICs as a function of the per-MIC output filtering energy storage.

To better understand the effect of the filter selection on the MIC losses, Fig. 3-7 is given to show how the switching and filter losses behave as the filter energy is varied. As expected, when these two varying losses are equal (in either configuration), the total losses are minimised. Although the filter corresponding to the minimum losses was not selected for either system, the filter-conduction to switching loss ratio (2:1) was maintained between them (i.e. the filter value was halved). Comparing the points A, B, C and D from Fig. 3-7 with the same points from Fig. 3-6 allows the designer to understand the implications of filter selection when moving from the parallel to the 2-cascaded system.

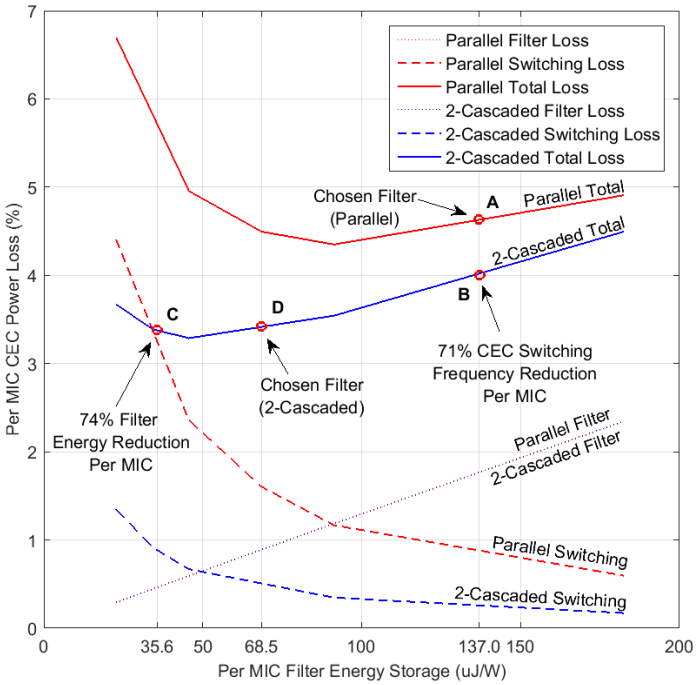

Fig. 3-7. The simulated CEC (partial) loss breakdown of the parallel and 2-cascaded MICs as a function of the per-MIC output filtering energy storage. Not all losses are shown (i.e. PV diode).

Given an efficiency-optimised parallel system, a designer moving to a 2-cascaded configuration should aim to select a cascaded filter that halves both the filter losses and the switching losses per-MIC. Maintaining the optimal filter-conduction to switching loss ratio (1:1) ensures the 2-cascaded system will maintain its maximum efficiency operating point.

3.3 Comparison of Parallel and Decentralised 2-Cascaded Operation

3.3.1 Transient Comparison

Fig. 3-8 and Fig. 3-9 show the transient results of operation from both the parallel and 2-cascaded system respectively. In both cases ideal simulation results are displayed alongside the measured equivalents from the prototype. Although hysteresis control is (in theory) useful for holding the harmonic content (THD) of the current waveform constant (Fig. 3-8b), practical implementation is imperfect (Fig. 3-8e) due to the finite sampling frequency of the implemented micro controller (resulting in 4.3% THD vs. 4.8% THD). However, it is evident that decentralisation has increased this sim/prac difference for the cascaded case of Fig. 3-9b/g (4.4% THD vs. 5.2% THD). Ideally, if the harmonic currents are held constant then the only variable that should change between the parallel and 2-

cascaded systems is the switching frequency as a function of the filter-energy-per-unit-output-power (µJ/W). As the harmonic content is fixed, both Fig. 3-8c/e and Fig. 3-9c/h make it very apparent the regions of low and high di/dt (it is possible to see the variations in the switching frequency). Both the harmonic current and the switching frequency are discussed in the following sections.

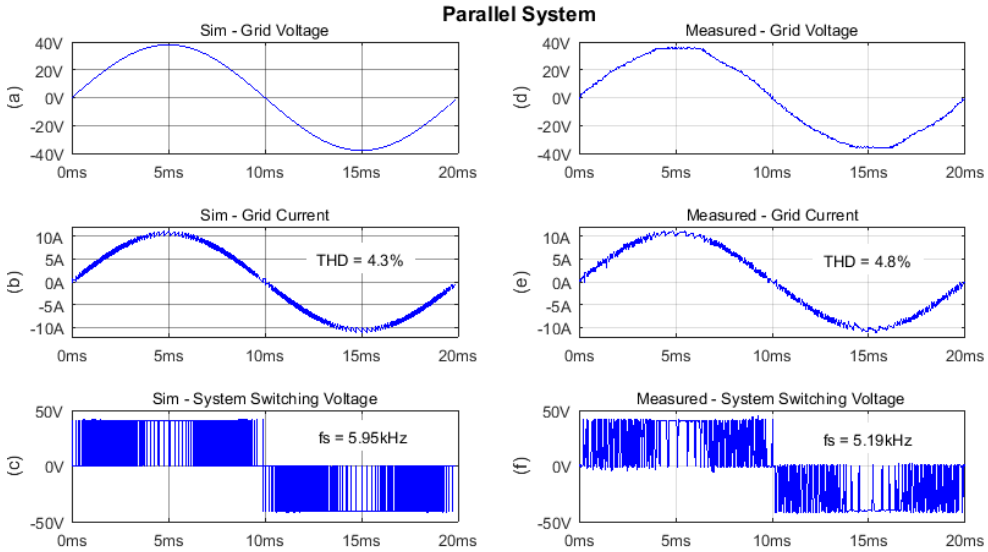

Fig. 3-8. The transient comparison (simulation and measured) for the parallel MIC system, with the variable values specified in Table 3-1.

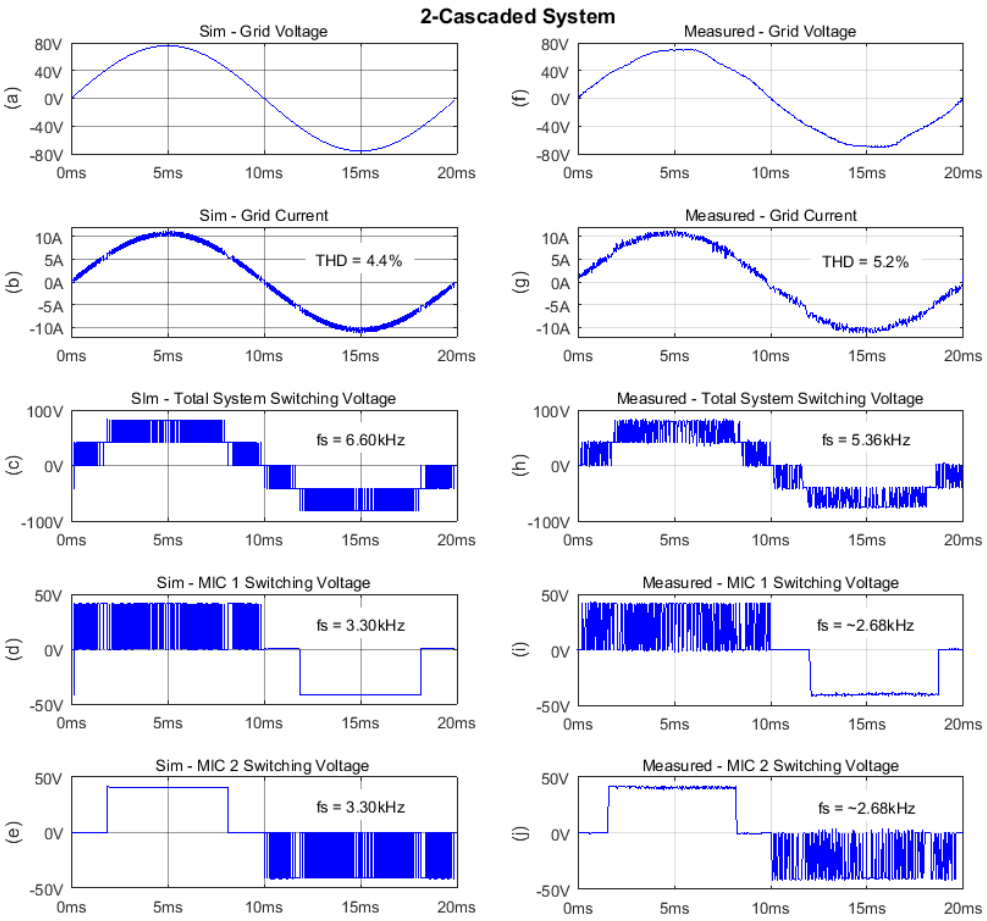

Fig. 3-9. The transient comparison (simulation and measured) for the decentralised 2-cascaded MIC system (Fig. 3-1), with the variable values specified in Table 3-1.

3.3.2 Harmonic Current Comparison

Referring to Fig. 3-10, it can be seen that the harmonic content of the two measured systems are higher than their simulated values, which is due to the 160kS/s sampling limitation allowing the current to briefly leave the hysteresis bands. However, the measured 2-cascaded system shows some fluctuations in its harmonic content, which is 10.8% larger than the parallel system at the rated output power, but is only 3.3% higher on average across the entire output range. This implies that the prototype system has a slight interleaving (zero crossing detection) timing error or current sensor mismatch, which ultimately is the result of having decentralisation in the system. This effect of the decentralisation introduces harmonic current that tends to increase with the magnitude of the fundamental current. This can be observed by comparing the grid currents of Fig. 3-9g (measured, 2-cascaded) and Fig. 3-9b (simulated, 2-cascaded). It can be seen that as the

system transitions the control of the current between the MICs, the current tends to increase/decrease in magnitude quickly (small current bumps). It can be noted here that a centralised multilevel inverter would not have transition timing issues or current magnitude measurement mismatch issues.

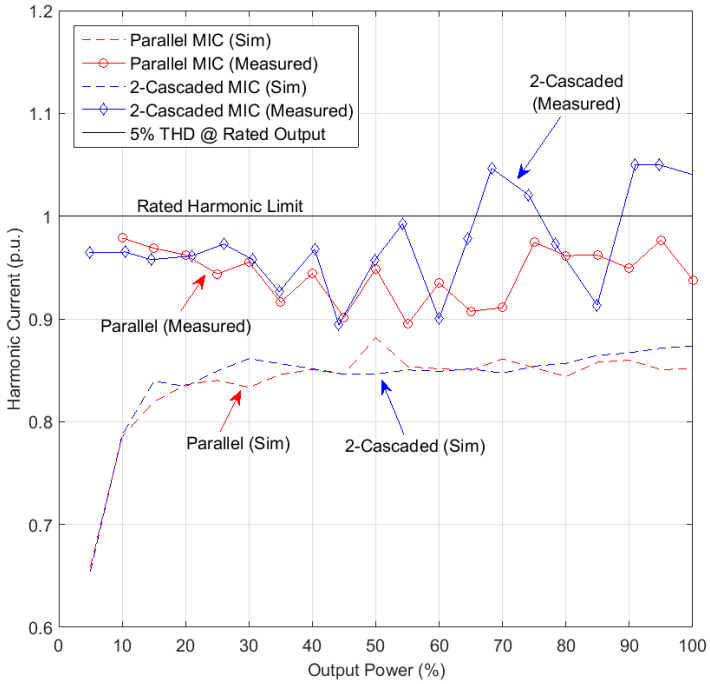

Fig. 3-10. The harmonic currents of the parallel and decentralised 2-cascaded systems (relative to the rated harmonic current limit) as a function of the output power. 1p.u. = 0.372Arms.

As the additional harmonic content in the decentralised 2-cascaded prototype system comes from the practical differences between the grid voltage/current sensors of the two MICs, manual tuning of the circuitry was required. This was done in order to minimise both the MIC current measurement mismatch and reduce the MIC relative zero-crossing phase error to generally less than 0.3°. If these actions are not considered then distorted currents occur during MIC voltage transition points, increasing the THD. This tuning, however, could not completely eliminate the effect of the additional harmonic current of the 2-cascaded system brought about by decentralisation, which is what is seen in Fig. 3-10. However, it can be summarized that generally the decentralised 2-cascaded total harmonics still stay below 5% of the rated fundamental current (i.e. 5% THD at max power, specified by AS/NZS 4777.2 [9]). It should be emphasised here that harmonics

beyond the first 50 have also been included for the sake of this research.

3.3.3 Switching Frequency

The CEC weighted switching frequency ratio between the 2-cascaded and parallel systems (see Fig. 3-11) was observed to be 0.504 in measurement and 0.563 in simulation (i.e. about 50%). The lower ratio in measurement is primarily caused by the slight differences in the inductance of the prototype's artificially created grid when operating across the two configurations. As discussed in section 1.6, the move to a multilevel waveform brings about switching frequency reductions that increase with the square of the number of voltage levels that are possible. For the parallel system only a single voltage can be generated (albeit positive or negative). The 2-cascaded system can produce twice as many voltage levels, which should result in a quarter of the switching frequency. However, as seen in Table 3-1, the filter energy per-watt of the MICs has been reduced by 50% in the 2-cascaded case compared with the parallel case. This filter energy was selected to increase the overall 2-cascaded efficiency as discussed in section 3.2. As a result, the 2-cascaded system has a switching frequency that is half of the parallel case instead of a quarter.

In Fig. 3-11, the measured switching frequency of both the parallel and the decentralised 2-cascaded system are found to be lower than the simulated values, which is related to the higher harmonic currents in the measured systems caused by the finite sampling frequency. As the sampling frequency is limited, the current exceeds the hysteresis bands briefly (producing a higher THD), increasing the average time intervals between switching and thus decreasing the switching frequency. Moreover, any source inductance in the grid reduces the di/dt of the current and assists in lowering the switching frequency further compared with the simulation. Both of these effects are described by equation (3-2).

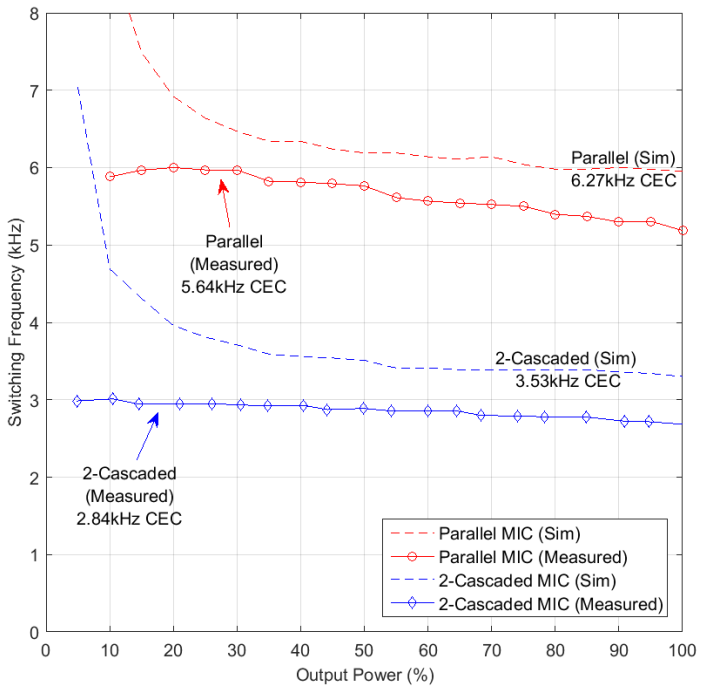

Fig. 3-11. The per-MIC switching frequencies of the parallel and decentralised 2-cascaded systems as a function of the output power.

In the parallel system, there is a region centred on the peak of the voltage and current waveforms where the instantaneous difference between the DC-link voltage and the grid voltage (i.e. the filter voltage) becomes so small that the current di/dt becomes near zero (see the low di/dt ripple in Fig. 3-8e at the 5ms and 15ms mark). This effect is made more pronounced by the peak resistive voltage drop of the filter. In these regions the inverter's instantaneous switching frequency was reduced by 75% from the average switching frequency (Fig. 3-8f at 5ms and 15ms) in the measured system. Note that since the sinusoidal waveforms spend 29% of their period above 90% of their peak value, this switching frequency reduction has a significant effect on the average switching frequency. This is typical in a non-multilevel (parallel) system and is usually a design parameter (voltage headroom versus minimisation of switching frequency). In the 2-cascaded system (keeping the same DC-link voltages and grid ratios) the average filter voltage in the sinusoidal peak regions is doubled, which results in a comparatively larger switching frequency in these regions of operation (Fig. 3-9(g/h) at 5ms and 15ms) compared with the parallel case. This phenomenon is a symptom of comparing the parallel/2-cascaded MICs with two different grid voltages instead of two different DC-link voltages. Regardless,

there are now also additional transition regions between levels in the 2-cascaded system, which have near zero di/dt (Fig. 3-9i at 2ms and 8ms and Fig. 3-9j at 12ms and 18ms), serving to partially mitigate the switching frequency increase from the filter voltage doubling at the peaks. The net result, still, is a slightly higher total system switching frequency in the 2-cascaded case (Fig. 3-9h vs. Fig. 3-8f), but this is then divided between the two MICs. This results in an MIC switching frequency that is slightly higher than half that of the parallel connected MIC.

Ultimately, the 2-cascaded switching frequency does not deviate significantly from what is expected after the effects of the grid inductance, sampling frequency and low di/dt regions have been taken into account. Thus, when using the above proposed control approach, decentralisation plays no direct role in changing the switching frequency of the 2-cascaded system from that expected of a centralised equivalent. However, as the THD of the 2-cascaded system was affected by decentralisation, it stands to reason that if improved control techniques were used to correct the additional harmonic content then the switching frequency would be increased. An example of this is high frequency switching overlap around the multilevel transition regions to ensure smooth level transitions between the MICs, increasing the switching frequency. See Fig. 3-14 in section 3.4.1 which shows an exaggerated situation where this would be necessary.

3.3.4 Efficiency and Losses

Fig. 3-12 shows that the simulated and measured efficiency of the 2-cascaded system outperforms that of the parallel system. The absolute measured CEC weighted efficiency difference between the 2-cascaded system and the parallel system was 1.1%, whilst the simulated difference was 1.2% (the latter does not take into account wiring, PCB and magnetic filter losses). Similar to the hypothetical case of modifying the switching frequency at the end of section 3.3.3, decentralisation can only indirectly affect the 2-cascaded efficiency through other interacting factors (i.e. manipulating the switching frequency to correct for decentralised harmonics and hence increasing the switching losses). Regardless, the improved decentralised 2-cascaded efficiency seen in Fig. 3-12 demonstrates the fundamental benefit that multilevel operation can bring to a system's operation.

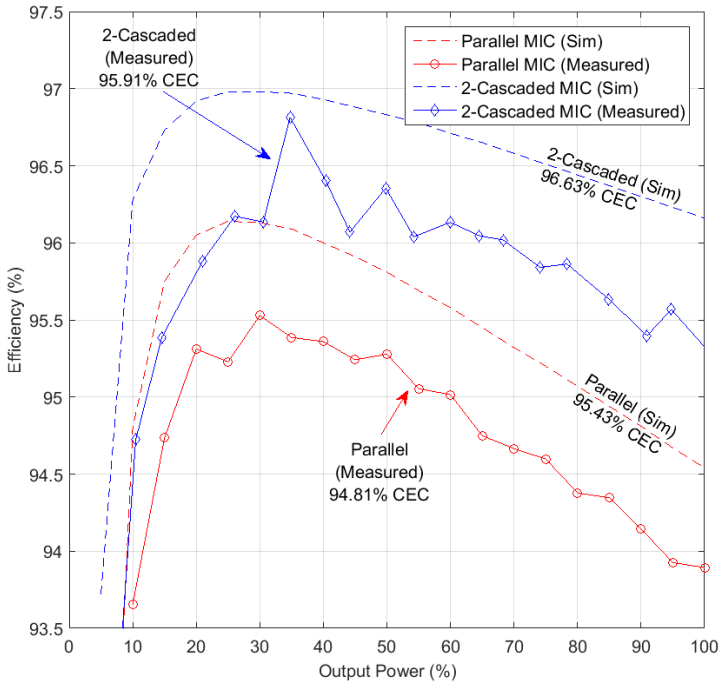

Fig. 3-12. The efficiencies of the parallel and decentralised 2-cascaded systems as a function of the output power.

Fig. 3-13a and Fig. 3-13b shows the calculated per-MIC loss breakdown for the parallel and 2-cascaded systems at the 100% and 30% output power levels respectively, which are performed using the measured switching frequencies. As the move from the parallel to the decentralised 2-cascaded system brings a measured 49.6% CEC switching frequency reduction (Fig. 3-11), it is expected that switching losses will halve. Similarly, as the filter has been reduced by 50% from 137.0µJ/W (495µH) to 68.5µJ/W (248µH), the filter losses will also halve. All other conduction losses remain unchanged in the system. Fig. 3-13 visualises these reductions, confirming that both the filter losses (i and iii) and the switching losses (ii and iv) halve for both the 100% and 30% power output levels. Thus, the filter-conduction to switching loss ratio is maintained in the transition to the 2-cascaded system. Note that there are also the PV diode losses, which are significant, but this can be realistically improved upon by considering a synchronous (MOSFET) diode.

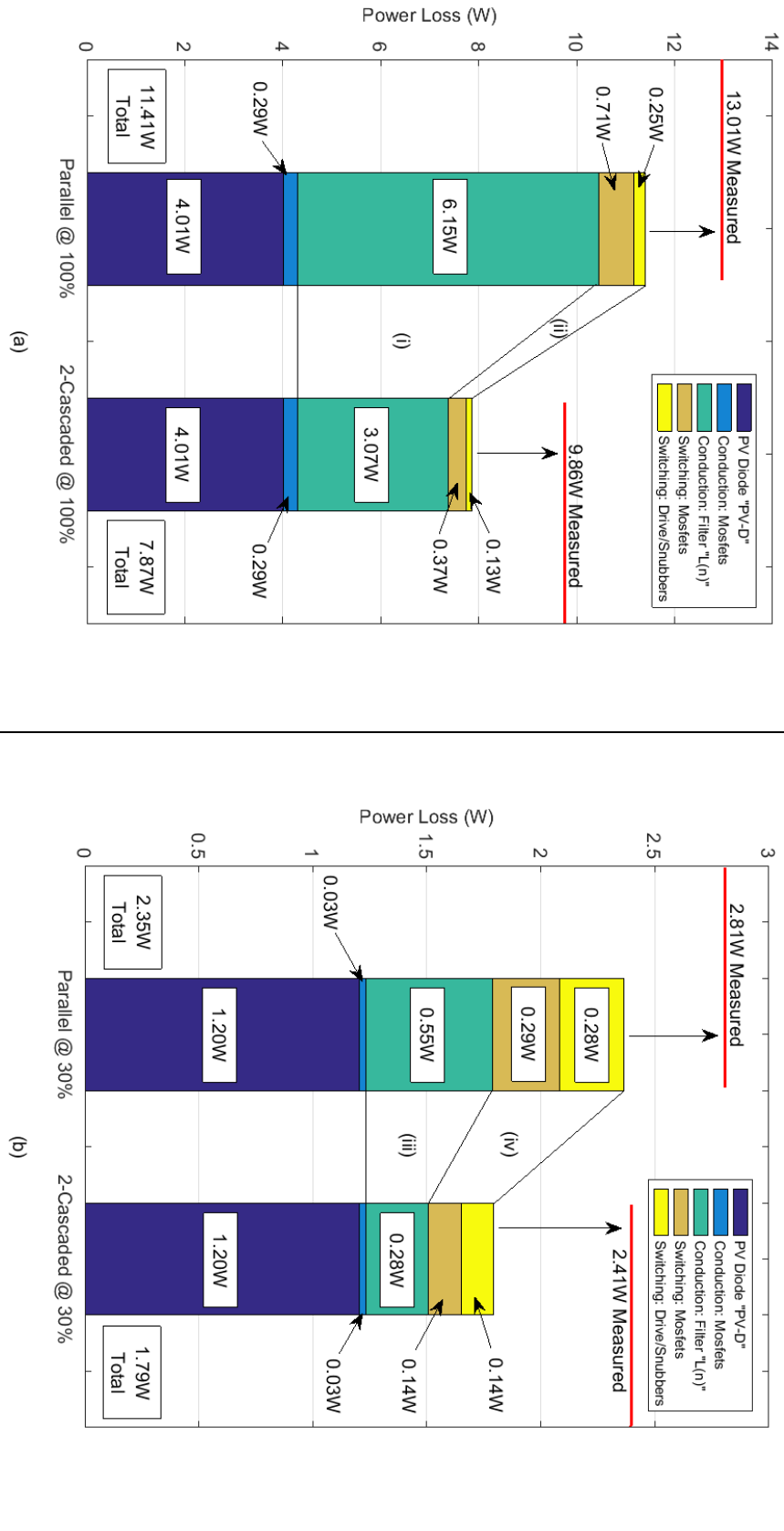

Fig. 3-13. Calculated per-MIC loss breakdown of the parallel and decentralised 2-cascaded MICs. The MICs are operating at (a) 200W (100%) output power and (b) 60W (30%) output power. Total measured loss results are also shown for each case (red lines).

The measured total losses of the systems are also shown in Fig. 3-13 (solid red lines). The difference between the calculated and measured total losses increased by 24.4% (Fig. 3-13a) and 34.8% (Fig. 3-13b) in the parallel to 2-cascaded transition, revealing larger unforeseen losses in the cascaded configuration. These differences are likely due to both the additional cascaded wiring between the MICs (significant at 100% power due to higher currents) and the ignored magnetic losses in the filter (proportionally more significant at 30% power due to the lower conduction losses). In total, the move from the parallel to the 2-cascaded system decreased the measured losses per-MIC by 24.2% at 100% power (Fig. 3-13a), by 14.2% at a 30% power (Fig. 3-13b) and by 22.1% for the CEC weighted output power (based on the Fig. 3-12 losses) for the hardware that was utilised.

3.4 Intrinsic Decentralised and Cascaded Multilevel Limitations

3.4.1 Zero Crossing Error

As the cascaded system relies on accurate timing for voltage interleaving, synchronisation between the modules needs to be established through either low latency PLC or independent measurements of the grid zero-crossing by each MIC. Whatever the method, if one MIC's grid zero-crossing detection is significantly delayed relative to the other's detection then the current can no longer be accurately controlled. In Fig. 3-14 (a-c), the timing of one decentralised 2-cascaded MIC no longer matches up with the other and this causes the current to operate in an uncontrolled manner for brief periods of time. An example of this delay issue is when one MIC stops operating and expects the other MIC to take over, but it does not (i.e. Fig. 3-14d at 18-20ms). Effectively, any operating region commands sent to one MIC are phase shifted relative to the other MIC. If such zero-crossing errors were present in the cascaded system, the only way to remove it would be to intentionally overlap the modulation regions of each MIC – Resulting in an increase to the switching frequency.

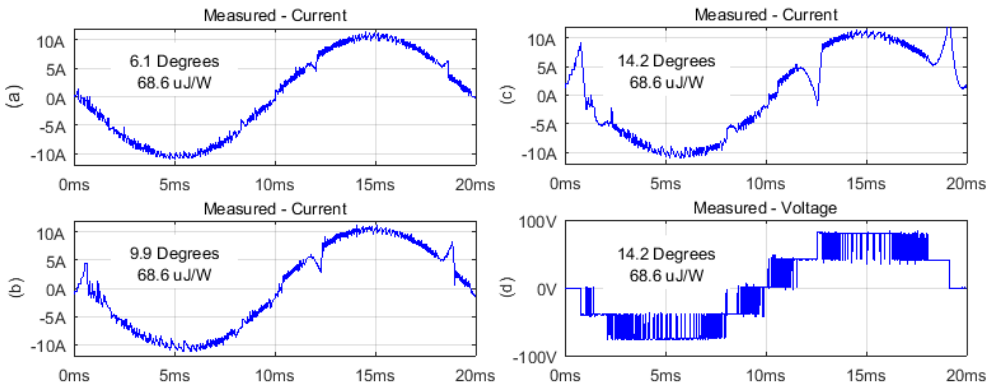

Fig. 3-14. The measured transient zero crossing error behaviour in the 2-cascaded system showing an increasing current error (a-c) and the final resultant system voltage (d). All plots use the 2-cascaded filter value selected in Fig. 3-5 (248uH per-MIC). Normal behaviour can be seen in Fig. 3-9.

The error introduced by a relative zero crossing error between MICs for the system seen in this study is primarily composed of both a sinusoidal half-cycle phase shift (i.e. Fig. 3-14c at 0-10ms) and three triangular transient spikes (i.e. Fig. 3-14c at 0ms, 12ms and 18ms). The half-cycle phase-shift RMS current (I_{Offset}) can be modelled approximately as half of the RMS of the difference between two full-wave phase-shifted currents, which is given by:

$$\begin{cases} I_{Offset} = \frac{1}{2}\sqrt{\frac{I_P}{\pi}\int_0^{\pi}[\sin(x) - \sin(x-\phi)]^2 dx} \\ I_{Offset} = \frac{1}{2} I_P \sqrt{1-\cos(\phi)} \end{cases} \quad (3\text{-}3)$$

Where ϕ is the relative zero-crossing error and I_P is the rated grid peak current. The three transient spikes can be approximated as a triangle wave with a reduced duty cycle. The peak current value of the triangle wave can be found from the average inductor voltage magnitude during these events and knowledge of the duration that they occur for (the zero-crossing error). The inductor voltages during these events can be approximately given by:

$$\begin{cases} V_{L(1)} = \dfrac{V_{gm}}{2}\sin(\phi) \\ V_{L(2)} = \dfrac{V_{gm}}{2}[\sin(\theta+\phi) - \sin(\theta)] \\ V_{L(3)} = \dfrac{V_{gm}}{2}[\sin(\theta) - \sin(\theta-\phi)] \end{cases} \quad (3\text{-}4)$$

Where V_{gm} is the peak grid voltage and θ is the transition angle between MIC voltage levels defined by:

$$\theta = \arcsin\left(\frac{V_{DC-Link}}{V_{gm}}\right) \quad (3\text{-}5)$$

Where $V_{DC-Link}$ is the DC-link voltage of a single MIC. Knowing the inductor voltage equation and the inductor voltages of (3-4), the change in current (i.e. the triangle peak) can be found from:

$$\begin{cases} |V_L| = L\dfrac{|di|}{dt} \\ |di|_{average} = \dfrac{1}{3} * \dfrac{\phi\left(|V_{L(1)}| + |V_{L(2)}| + |V_{L(3)}|\right)}{2\pi * f * L} \\ \quad = \dfrac{\phi * V_{gm}}{12\pi * f * L} * \sin(\phi) * [2\cos(\theta) + 1] \end{cases} \quad (3\text{-}6)$$

Where f is the grid frequency and $|di|_{average}$ is the average triangle wave peak current. Using the equation for variable duty cycle triangular rms current [30] and (3-6), the transient spike harmonic current (I_{Spikes}) can be found as:

$$I_{Spikes} = I_P\sqrt{\frac{k}{3}} = |di|_{average} * \sqrt{\frac{1}{3} * \frac{3\phi}{2\pi}} \quad (3\text{-}7)$$

Where k is the duty cycle. Thus, combining the offset (3-3) and the spikes (3-7) harmonic current together, the total introduced harmonic current for a given zero-crossing error is approximately:

$$I_{Harmonics-ZeroCrossing} = \sqrt{{I_{Offset}}^2 + {I_{Spikes}}^2} \quad (3\text{-}8)$$

Following equation (3-8), Fig. 3-15 shows how the decentralised 2-cascaded system

acts when the zero-crossing detection of one of the MICs is delayed by a varying amount. To obtain the measured data, delay elements (RC filters) were used in one of the MIC's zero-crossing detection circuits. The resultant zero-crossing (square wave pulse) difference was then measured between the two MICs with a differential probe. No effective pre-existing zero-crossing error was found due to previous THD tuning (i.e. it was below 0.3°). The known baseline quantity of switching harmonics (based on the normal 2-cascaded THD) was subtracted from the total harmonics to find the measured zero-crossing error harmonics. This subtraction is possible as the switching harmonics are at a much high frequency compared with the zero-crossing error harmonics.

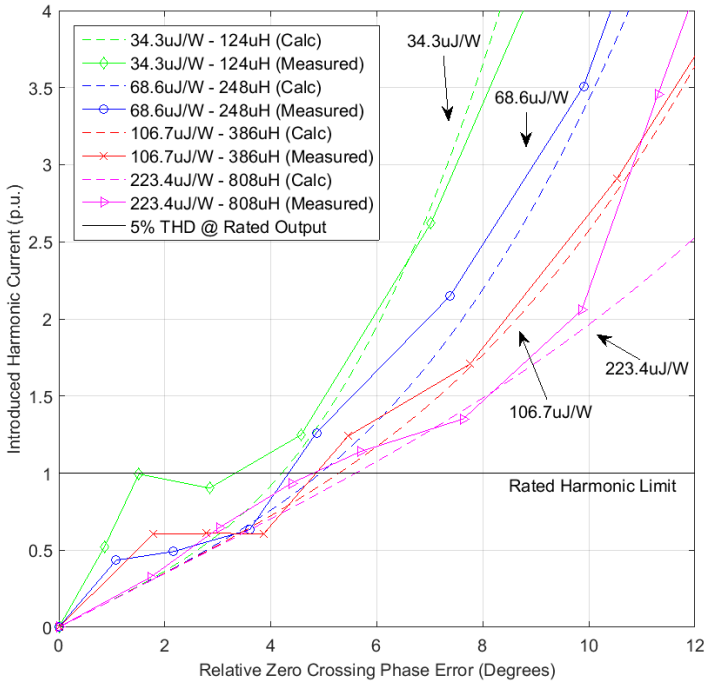

Fig. 3-15. The introduced harmonic current in the decentralised 2-cascaded system as a function of the relative zero-crossing errors between the two MICs operating at the rated current. Filter values are all stated on a per-MIC basis. 1p.u. = 0.372Arms. Calculations are based on (3-8).

Note that the harmonic current limit in Fig. 3-15 is the point at which the introduced zero-crossing harmonics are equivalent in magnitude to the general AS/NZS 4777.2 5% limit [9] (i.e. equivalent to the maximum allowable hysteresis switching harmonics). At this point even an infinite switching frequency would not allow the 2-cascaded system to operate below a 5% THD.

Although Fig. 3-15 shows that the 2-cascaded system seems to be quite sensitive to zero-crossing error, the filtering inductor only has a moderate effect on reducing this sensitivity. Using the rated harmonic limit as a boundary (i.e. 1p.u.), a 550% increase in inductance (34.4µJ/W to 223.4µJ/W) only results in approximately a 50% higher tolerance to zero-crossing error (calculated and measured). This is because only the spikes (3-7) harmonic component is dependent on the di/dt of the filtering inductor whilst the phase offset (3-3) harmonic component is completely independent (though still significant). It can be generally concluded from this harmonic limit that the relative zero-crossing error needs to stay below 4° to ensure the decentralised system meets the THD requirements.

It should be noted that these spike harmonics can be avoided by having shared control zones (share-zones) around the transition points where both MICs are trying to control the current simultaneously. However, this results in a much higher switching frequency during these transition points due to the system temporarily forfeiting multilevel control and acting more like a single level inverter. Though share-zones are feasible with only two MICs in cascade, higher order multilevel cascaded systems with many transition points (between the multiple levels) would begin to suffer more severely from this overhead. A more realistic approach would be to ensure the accuracy of the zero-crossing detectors to decrease the relative error.

If minimal zero-crossing timing differences between MICs cannot be achieved, then low latency PLC communications will need to implemented to send timing pulses between MICs from a master MIC. However, a commitment to PLC forfeits the opportunity to solely rely on standard, higher latency, protocol based wireless for intersystem communications. As the ability to work with a higher latency communications system is always desirable, it is therefore beneficial to focus effort on reducing the relative zero-crossing error between the decentralised cascaded MICs.

3.4.2 Minimum Power Sharing Ratio

MPPT and the resultant balance of power between MICs in a multilevel 2-cascaded system is different from that of a parallel system. In the parallel system, each MIC adjusts its power output by changing its own current reference. However, in the 2-cascaded system, the current is common between the two MICs. If both MICs are shaded equally, the shared current is simply reduced in both modules by the master. However, if there is

unequal shading (i.e. unbalanced power), then it is the slices of the generated multilevel voltage waveform that are reorganized and "resliced" by the master to accommodate this new power ratio between the MICs. An example of power distributions in multilevel waveforms can be seen in [31].

However, there exist regions of operation in the multilevel waveform voltage where all modules on the system must be active in order to exceed the grid voltage and inject power into the grid with low harmonics. For the 2-cascaded system, Fig. 3-16a shows the minimum voltage on-time that the shaded MIC needs to produce. Conversely, Fig. 3-16b shows the maximum voltage that the other module can produce. This is the voltage power sharing limit.

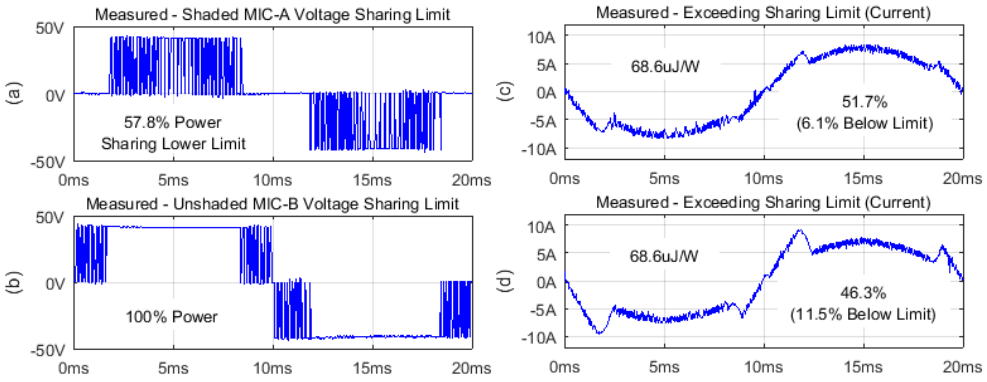

Fig. 3-16. The measured transient behaviour of the 2-cascaded system at (a and b) and beyond (c and d) the limit of voltage sharing. 248uH per-MIC (68.6µJ/W).

If this voltage sharing limit is too restrictive, then the current can be altered between the different regions of operation (to further increase the sharing ratio), greatly increasing the harmonic current. This can be seen in Fig. 3-16c and Fig. 3-16d, which both show the shape of the current waveform where MIC-A (shaded) has a reduced current reference while MIC-B (non-shaded) has an increased current reference to compensate for the effect of MIC-A (MIC-B stays at a constant power). Ultimately, MIC-B maintains its power output whilst the power of MIC-A is successfully reduced, increasing the power sharing ratio through the use of non-sinusoidal current. Fig. 3-17 shows how quickly additional harmonics (i.e. not counting the hysteresis switching harmonics) are introduced from this strategy as the limit of voltage sharing is exceeded. Effectively, the limit of voltage sharing cannot be exceeded by more than a few percent before exceeding the general 5% AS/NZS

4777.2 [9] limit. Fig. 3-17 (points "C" and "D") shows the harmonic operating points of Fig. 3-16 (c and d) respectively.

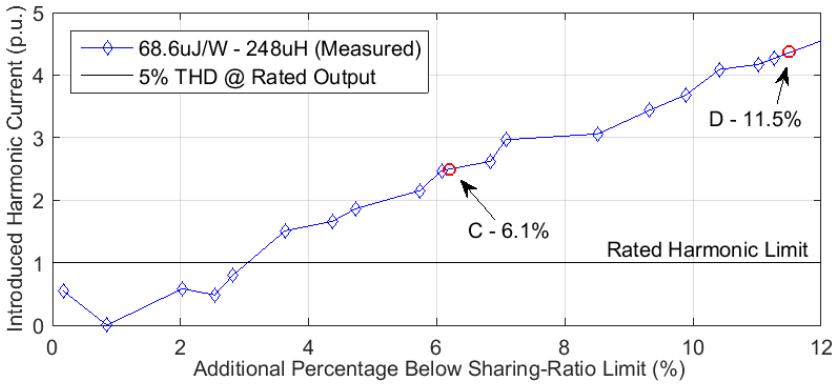

Fig. 3-17. The measured introduced harmonic current of the 2-cascaded system as a function of the "additional percentage" below the voltage power sharing limit (i.e. below 57.8% from Fig. 3-16a). 248uH per-MIC. 1p.u. = 0.372Arms. C/D are the operating points of Fig. 3-16c/d.

To find the limit of voltage sharing for a 2-cascaded system, the power of the shaded module (MIC-A) operating in hysteresis mode between the transition points needs be determined by:

$$\begin{cases} P_{MIC-A} = \left[\frac{1}{\pi}\int_{\theta}^{\pi-\theta} I_{gm}\left(V_{gm}\sin x - V_{DC-Link}\right)\, dx\right] \\ P_{MIC-A} = \left[\frac{V_{gm}I_{gm}}{4\pi} * (2\pi - 4\theta + 2\sin 2\theta)\right] \\ \qquad -\left[\frac{2V_{DC-Link}I_{gm}}{\pi} * (\cos\theta)\right] \end{cases} \qquad (3\text{-}9)$$

Where V_{gm} and I_{gm} are the peak grid voltage and current respectively, θ is the transition angle defined by (3-5) and $V_{DC-Link}$ is the DC-link voltage of the unshaded MIC. The power of the unshaded module (MIC-B) is given by

$$P_{MIC-B} = \left(\frac{I_{gm}V_{gm}}{2}\right) - P_{MIC-A} \qquad (3\text{-}10)$$

Thus, the minimum ratio of power of the shaded module (MIC-A) to the unshaded module (MIC-B) becomes:

$$P_{min_{MIC-A}\%} = \left(\frac{P_{MIC-A}}{P_{MIC-B}}\right) * 100\% \qquad (3\text{-}11)$$

This minimum ratio between MIC-A and MIC-B represents the limitation imposed by the voltage sharing limit, which is both a function of the grid voltage and the DC-link voltage.

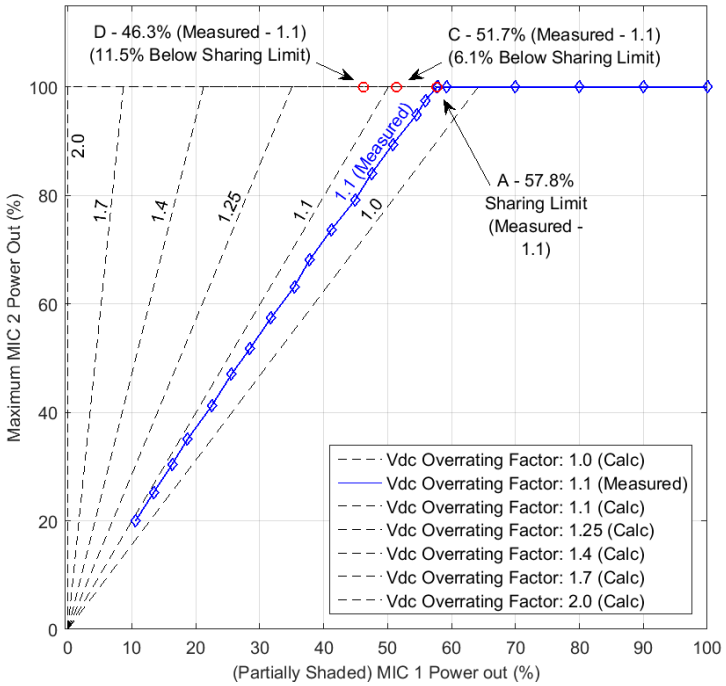

Fig. 3-18. Effect of a shaded MIC on the unshaded MIC for multiple "system-total-DC-link" to "grid-voltage-peak" ratios for the 2-cascaded system. A/C/D refers to Fig. 3-16a/c/d.

Fig. 3-18 shows graphically the power limitations that must be enforced upon the unshaded MIC if the minimum sharing ratio is not met. By defining the overrating factor of the DC-link as the ratio between the system-total-DC-link (i.e. the DC-link of MIC-A and MIC-B added together) and the grid-voltage-peak, a ratio of 1:1 (factor of 1.0) would result in a calculated minimum sharing ratio of 64% to prevent the power of the unshaded MIC being scaled back. Conversely, an overrating ratio of 2:1 or a factor of 2.0 (i.e. a single MIC in the 2-cascade system can meet the grid-voltage-peak with just its own DC-link voltage) has no minimum power sharing ratio as each MIC can operate independently with the other in a bypass mode. The chosen measured 2-cascaded system of Table 3-1 operates with a 1.1 overrating factor (Fig. 3-18, point "A"), but due to the filtering inductor and PV diode, it effectively has a factor of 1.05 and the transition angle was calculated by

the hardware as such. Fig. 3-18 (points "C" and "D") show the harmonic-rich operating points of Fig. 3-16 (points "C" and "D"), which force the unshaded MIC to operate below the minimum power sharing ratio through the use of non-sinusoidal currents.

Although this power sharing ratio limit exists, if energy is transferred from the unshaded MIC to the shaded MIC by switching the H-bridge voltages of the two MICs to oppose each other in the series connection, then the shaded MIC effectively has less shading and more power. Thus, the DC-link of one MIC charges the other in a process commonly known as inphase DC-link balancing [33]. However, this adds complexity and is affected by the type of communications protocol utilised between MICs in the decentralised system (high latency, low bandwidth or intermittent, etc.).

3.5 Summary of Findings

In this chapter a detailed analysis was made of MICs operating both in a parallel and in a decentralised 2-cascaded configuration, revealing the subtle differences between the expected and measured results due to decentralisation. This analysis was performed using both simulated and measured results from 200W MICs. After performing an overview of both hysteresis control and the hardware utilised, parameters were given for the parallel/cascaded comparison. Simulated filter design for both systems was compared and discussed in the context of efficiency, switching frequency and losses. With the filters selected, the transient operations, harmonic current, switching frequency, efficiency and losses were then analysed and compared between the parallel and 2-cascaded configurations in the context of decentralisation (simulated and measured). Finally, both the relative decentralised zero-crossing error and the power sharing ratio limits (and beyond) were explored for the 2-cascaded system using both analytical equations and measured results from the MIC prototypes. The key findings are listed below:

- Transitioning from the parallel to the decentralised 2-cascaded system allowed for a 50% reduction in both the conduction losses and the switching losses when the filter was designed to maximise efficiency (ideal loss balance). For the case of the prototype system utilised, the overall measured CEC efficiency of the system increased from 94.8% to 95.9%.

- Decentralisation of the 2-cascaded system increased the full-load THD from the expected 4.8% (measured parallel) to 5.2% (measured 2-cascaded). The additional harmonic content was found to come from minor voltage and current sensor mismatches between the MICs. This ultimately affected the expression of the current reference and the synchronisation of the zero-crossing detections between the cascaded MICs respectively.
- The decentralised 2-cascaded MICs have a high sensitivity to the relative zero-crossing error between them. Analysis and prototype measurements found that a zero-crossing difference between the two MICs of just 4° introduced harmonics that were equivalent to the limits of the grid standard utilised (5% THD). It was also found that increasing the MIC filters by 550% only served to increase this zero-crossing error ceiling by about 50%.
- It was found that for the 2-cascaded system, the measured minimum power that a shaded MIC can produce without affecting the other unshaded MIC is 57.8%. Reducing the shaded MIC's power below this introduces large harmonic currents due to the non-sinusoidal current references utilised to maintain the unshaded MIC's power at 100%. It was measured that an additional 3% below the minimum power allowed for the shaded MIC (i.e. 57.8% down to 54.8%) was sufficient to introduce enough harmonic current to exceed the limits of the grid standard.

Ultimately, the decentralised 2-cascaded multilevel system can offer performance improvements and hence, necessitates further analysis. Just as with centralised cascaded multilevel converters, decentralised converters function almost identically in terms of their efficiency gains due to their switching and conduction loss reductions. Similarly, minimum power ratios between MICs still exist regardless of whether or not the system is centralised or decentralised. However, decentralisation affects the harmonic current and is sensitive to the zero-crossing error between the MICs. Regardless, so long as there is accurate MIC synchronisation, decentralised multilevel cascaded systems can be preferred in small scale PV applications.

4 Implementation and Analysis of the 4-MIC System MPPT

By increasing the size of the decentralised system to 4 MICs (Fig. 4-1), it is now possible to implement a more realistic prototype that is representative of real world conditions. An MPPT algorithm can then be implemented that demonstrates the true decentralised nature of the system. However, the power sharing issues of section 3.4.2 still exist between MICs and there are limits to the MPPT speed that result in design tradeoffs. Operation of the decentralised system is split into local (single MIC) and global (system wide master) modes of operation. The coordination between the two modes is significantly affected by the communications polling frequency between the MICs.

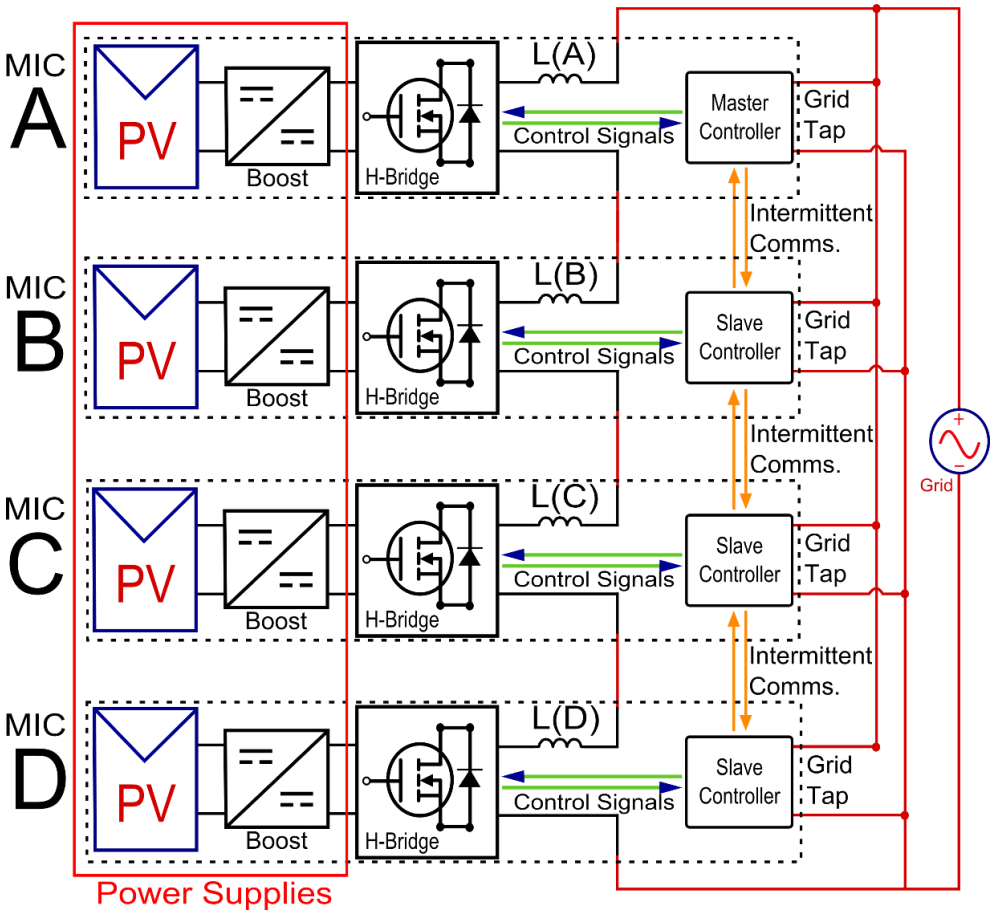

Fig. 4-1. The proposed 4-MIC multilevel decentralised cascaded system. A controller is built into each MIC for local switching control.

4.1 Hybrid Global and Local Waveform Fundamentals

The proposed decentralised system of Fig. 4-1 has two possible modes of operation. The choice of which is highly reliant on the frequency of the communications polling rate between the MICs. If the master has a fast polling rate to the slaves (>100Hz), then the master controller can simply read the system status and quickly perform MPPT for each MIC by rearranging the multilevel waveform pulses [27]. As of 2016 there is one such commercial system to achieve this on a residential scale [34]. If there are no communications within the system at all then each MIC will need to control the grid current simultaneously and independently [23-26], making multilevel interleaving with MPPT impossible. However, for the intermediate case, if the polling rate is at a low frequency (i.e. under 25Hz) then the master cannot correctly control the slave MPPT via multilevel interleaving. This results in poor MPPT and significant DC-link oscillations, causing significant issues in the system's capability to control the grid current.

The MICs of the decentralised system of Fig. 4-1 have both direct connections to the grid (for zero crossing timing and grid voltage measurement) and communication links to the other MICs (for multilevel operations). However, the communications link between the MICs could be considered intermittent and generally unreliable (such as wireless). This can result in multilevel-based system calculations that are spaced multiple seconds apart, completely compromising the MPPT control of the decentralised system and destabilising the DC-link voltages of the MICs. To account for this, a control approach needs to consider both the intermittent, master-controlled multilevel operations aspect (global control) in conjunction with simplified shared current forms of operation (local control) – Thus requiring a hybrid approach.

In order to perform multilevel interleaving in a cascaded system and still maintain the MPPT capability without a high speed central controller, a hybrid approach to operation is considered. To change the power distribution of MICs, a typical high speed multilevel system would quickly adjust the operating on time (and therefore RMS voltage) of each MIC during one waveform cycle. Conversely, a micro inverter has no cascaded connection and each module is therefore solely in control of its own current reference (similar to any single level central inverter). The proposed cascaded hybrid algorithm splits operation between these two methodologies into both multilevel interleaved control (global) regions and shared control (local) regions (Fig. 4-2), comparable to the sorted and unsorted

(respectively) pulse width modulation (PWM) control techniques explored in [31]. This allows for a limited (but fast) local MPPT and unrestricted multilevel (but slower) global MPPT.

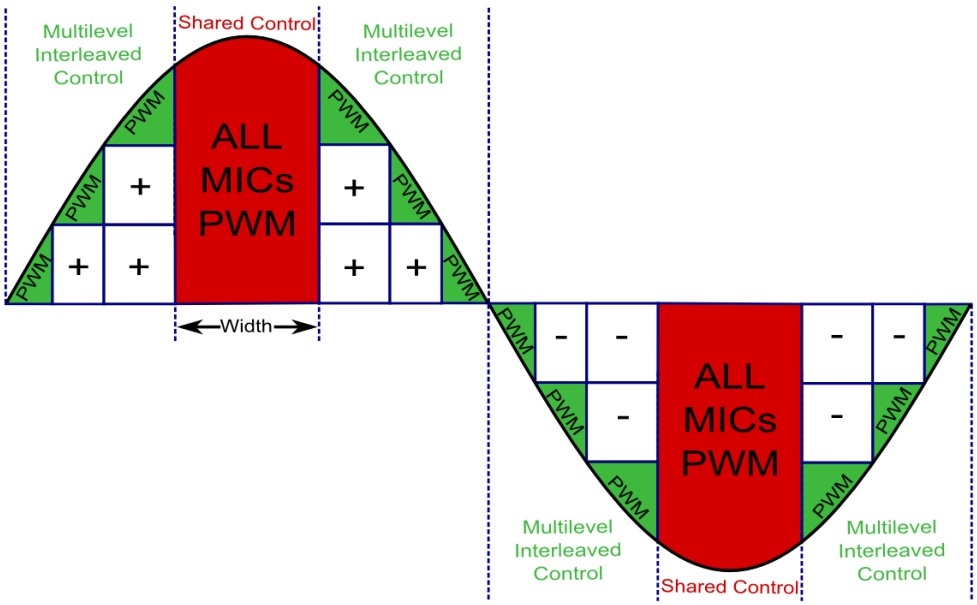

Fig. 4-2. Operating regions and blocks of the 4 MIC cascaded system across one cycle.

Fig. 4-2 visualises the different regions of the multilevel waveform in the decentralised hybrid system. The multilevel interleaved control regions operate in coordination, with one MIC modulating its voltage to control the current and the other MICs either in the on state or in the bypass state. If the current reference in this region is modified by the modulating MIC then the power produced by the other MICs are affected as well. Only a redistribution of the multilevel voltage blocks can independently change the operational power distribution of the MICs in this control region. However, the shared control regions operate with no centralised coordinated timing and allow for MICs to modulate their voltage freely, with independently derived current references attempting to control the same current. It is in this region that fast MPPT can occur as the MICs all aim to simultaneously control the cascaded grid current in response to local power targets. Fig. 4-3a and Fig. 4-3b show the simulated voltage and current waveforms produced by the proposed system respectively. Note that the inductor voltage (and thus, the switching frequency) of the system during these shared control regions is up to four times that of the multilevel interleaved control regions.

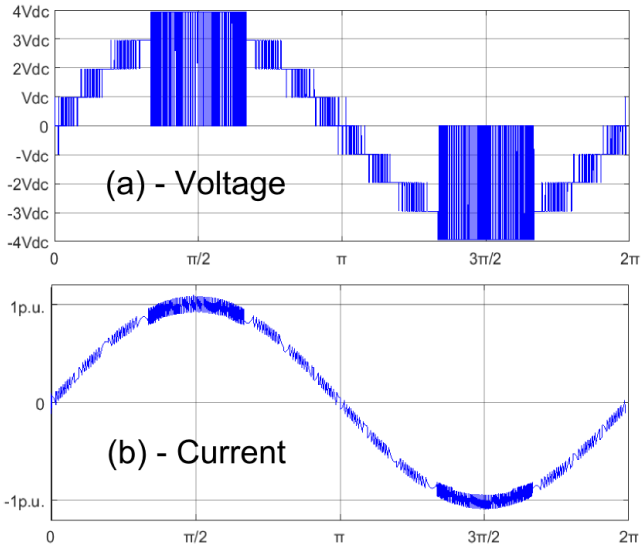

Fig. 4-3. The simulated voltage (a) and current (b) of the 4 MIC cascaded system across one cycle (see Fig. 4-2).

The transition point angles between the (identical) MIC DC-link voltage steps of Fig. 4-2 is controlled by the ratio of the sum of all of the DC-link voltages (SumVdc) to the grid peak voltage (Vg). This ratio determines at what angles the grid voltage will equal the DC-link voltage (or multiples of it) and thus the appropriate transition points. This SumVdc to Vg ratio can be thought of as the over-rating ratio for the DC-link voltage. The width of the shared control region, which does not affect the MIC voltage step transition points (unless it is expanded to encompass them), can arbitrarily be set to be larger or smaller than the natural 4th MIC voltage step of Fig. 4-3a (4Vdc). This width represents a balance between the two underlying types of control in the hybrid system: coordinated multilevel (global) and uncoordinated shared (local).

4.2 MPPT Principle of Operation

Fundamentally, the proposed MPPT algorithm works by having each MIC manage its own power within the MPPT shared control region (Fig. 4-2) until a set of instructions is received from the master to coordinate a new global multilevel interleaving configuration across the MICs. This new global interleaving configuration takes into account the change in power (since the last global communications update) caused by the local MPPT of each MIC. Thus, the sum of all the local power changes guides the global redistribution of power within the entire system at each communications update. After the global update,

the individual MICs are then free again to quickly (>50Hz) modify their current reference in the shared zones once more (local MPPT) while they await new global instructions. Examples of the blocks of power that are allocated to MICs during the global update process can be seen in the example power distribution of Fig. 4-4. In this figure, each MIC has a total power of 200W except for MIC A, which is set to 140W. Thus, looking at Fig. 4-4a, it can be seen that MIC A infrequently appears in the total distributions of the blocks compared with the other MICs. Taking note of the power associated with each block (ranging from 2W to 58W for the 740W waveform), the total sum of MIC A's blocks perfectly add up to 140W, which is the goal of the global MPPT. Looking at Fig. 4-4(c-f), the voltage waveform produced by MIC A (Fig. 4-4c) is (on average) lower than the voltages of the other MICs, indicative of the unequal power distribution across the entire system.

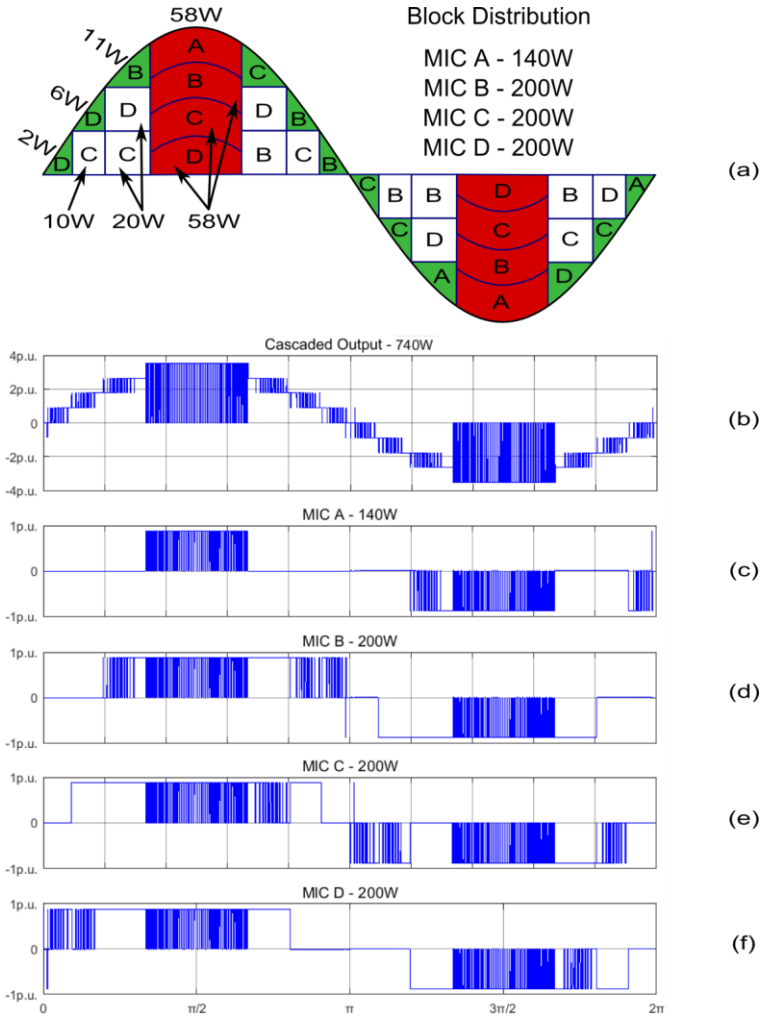

Fig. 4-4. An example simulated block distribution for the 4-MIC cascaded system of Table 4-1, but with a reduced current output (6.72Arms) to give a total system power of 740W. (a) shows the where MICs A-D are allocated and the power magnitudes associated with each block, (b) shows the simulated total system voltage and (c-d) shows the individual MIC voltage waveforms.

4.2.1 Global Control

When a global update request arrives from the master, the slave MICs each report their operating power (the PV MPP) and their DC-link voltages. The master then uses the knowledge of the MIC PV MPPs and the self-measured total grid power to proportionally calculate the new total system and individual MIC power allocation. First, the master calculates the new current reference for the entire system based on the measured grid power (i.e. based on the distorted current waveform). Then, the master accounts for the efficiency of the MICs by scaling the total PV input powers down according to the total PV input to grid output ratio. Now that the grid output power for each MIC is known for

the selected current reference, the multilevel waveform can be constructed. Initially, the master calculates the switching angles for the block allocation based on the grid voltage measurement and the reported DC-link voltages of each MIC. For the system analysed by this thesis, the DC-links are assumed to be equal, which greatly simplifies the multilevel waveform construction process. Based on the calculated angles, the master calculates the power associated with each block of the waveform. These blocks (e.g. Fig. 4-4a), which also include the four blocks in each shared control region, then need to be allocated to individual MICs. As the DC-link voltages are the same amongst the MICs, the power blocks will each contain the same amount of power regardless of the MIC that is assigned to producing it. A converse example would be if the DC-link voltage of MIC B was twice that of MIC A, then MIC B would always produce twice the power in a power block that was calculated based on MIC A's DC-link voltage. This would also affect the switching transition angles between MICs (due to the different DC-link voltages) as blocks are allocated to MICs. Thus, any sorting algorithm would have to consider significantly more variables if the MIC DC-links had significantly different voltages.

4.2.2 The Allocation of Power

The allocation of power blocks to MICs presents what is known as the Knapsack Problem [35], which is the difficulty in allocating a group of fixed value items into multiple containers of fixed capacities as efficiently as possible. In the case of the decentralised system, blocks of power need to be allocated to MICs. If too much or too little power is allocated to an MIC, then the power will not be matched to the MPP of that MIC's PV panel. Thus, the moment the system starts operating with the over/under allocated power block values, it is as if the MPP of the PV panels have immediately shifted. Local control of the shared control region will immediately have to correct for this until the next global update cycle. To solve the Knapsack Problem, a greedy approximation algorithm [36] was utilized. A greedy algorithm does not look ahead and makes the best choice based on the current situation. It can produce poor results in certain applications, but by using a custom MIC round-robin variation it was found to be very effective in the 4-MIC decentralised system.

The greedy-round-robin algorithm starts with the first MIC and finds the largest power block that can be allocated and then allocates it (i.e. "greedy"). This is repeated for the

other three MICs sequentially until each MIC has a single power block allocated. This continual rotation is the round-robin aspect of the algorithm. After this, the four MICs then have another next-largest power block allocated so that they now have two power blocks each. This process is repeated until one of the MICs has its power requirements satisfied, after which it is removed from the pool and the round-robin search continues for the remaining three MICs. If an allocated power block results in an invalid multilevel waveform configuration (i.e. an MIC needs to be on twice at the same time) then that result is discarded and the next best fitting block is found. This continues until all power blocks are allocated. An example of this can be seen in Fig. 4-5. By rotating between the MICs during allocation (round-robin), the average power block size in each MIC is kept relatively similar, spreading the final allocation error evenly. Allocation error can be eliminated by splitting up the power blocks into smaller portions of energy (i.e. smaller blocks), but at the cost of a higher switching frequency and greater sorting complexity. This was not necessary for the actual 4 module system, as the reported allocation error in the final prototype was generally less than 1-2%. Additionally, as implemented, this allocation process does not take into account effects on the PV power ripple that may result from specific block arrangements (though a weighting process can be added to balance block sorting with this requirement).

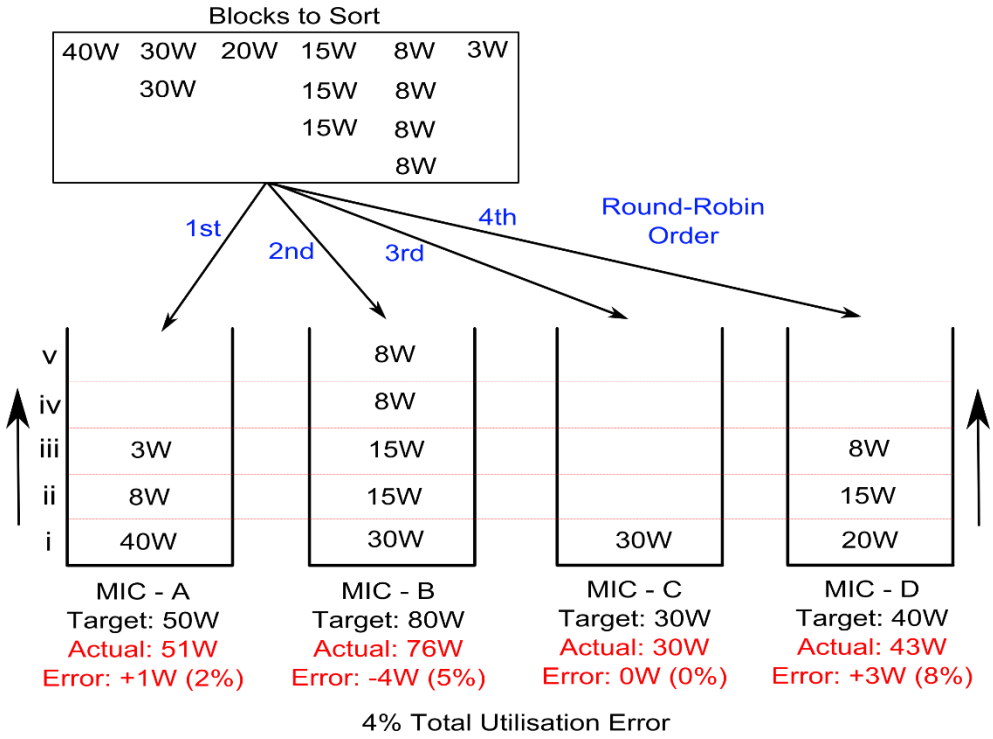

Fig. 4-5. An example of how the round-robin greedy algorithm sorts power blocks and allocates them to individual MICs for an imaginary case. During each sweep of the MICs (A-D) a power block is allocated. This is repeated (i-v) until power targets are met.

4.2.3 Local Control

After a global update and the round robin greedy sorting algorithm is finished, all the MICs are free to once again MPPT (according to Fig 1-6) and modify their local current reference in the shared control regions. In these shared regions, all four MICs are needed to match the grid voltage and therefore it is the MIC with the lowest current reference that is truly in control of the actual grid current. However, when this lowest-power MIC reduces the current below the current reference of the other MICs, those other MICs will increase their voltage to resist this change and then compensate their own sudden voltage (and thus power) increase by reducing their own current references. Thus, the grid current can be quickly reduced. Conversely, if an MIC tries to increase the current beyond the current reference of the other MICs, then those other MICs will reduce their voltage contribution in an attempt to maintain their own current references. These other MICs will then compensate their own sudden voltage (and thus power) decrease by increasing their own current references. Thus, the grid current is quickly increased.

Effectively, this shared control region becomes a voltage-current balancing act as the MICs push and tug at each other until either power targets are reached, or the voltage requirements of one of the MICs exceeds its own DC link voltage (due to another MIC trying to reduce the current so significantly). When the latter occurs, MPPT begins to fail as the lowest power MIC takes complete control of the grid current. If all four MICs increase/decrease their current references together (uniform irradiance change) then the local MPPT current change is only limited by hardware current limits (i.e. magnetic saturation). However, this reference manipulation distorts the current waveform and ultimately, local MPPT is limited by the current harmonics generated. As these harmonics can only be cleared by another global update (the redistribution of the power blocks and a new current reference), this effectively creates an MPPT speed limit on the system that is set by the global update rate itself. Thus, the MPPT speed is primarily controlled by the rate at which the system can redistribute power blocks and reset/match all the current references of the MICs. The entire MPPT process can be seen in Fig. 4-6 and a measured example is seen later in Fig. 4-8, the latter showing how the decentralised system transitions from 800W to 740W during global/local operation.

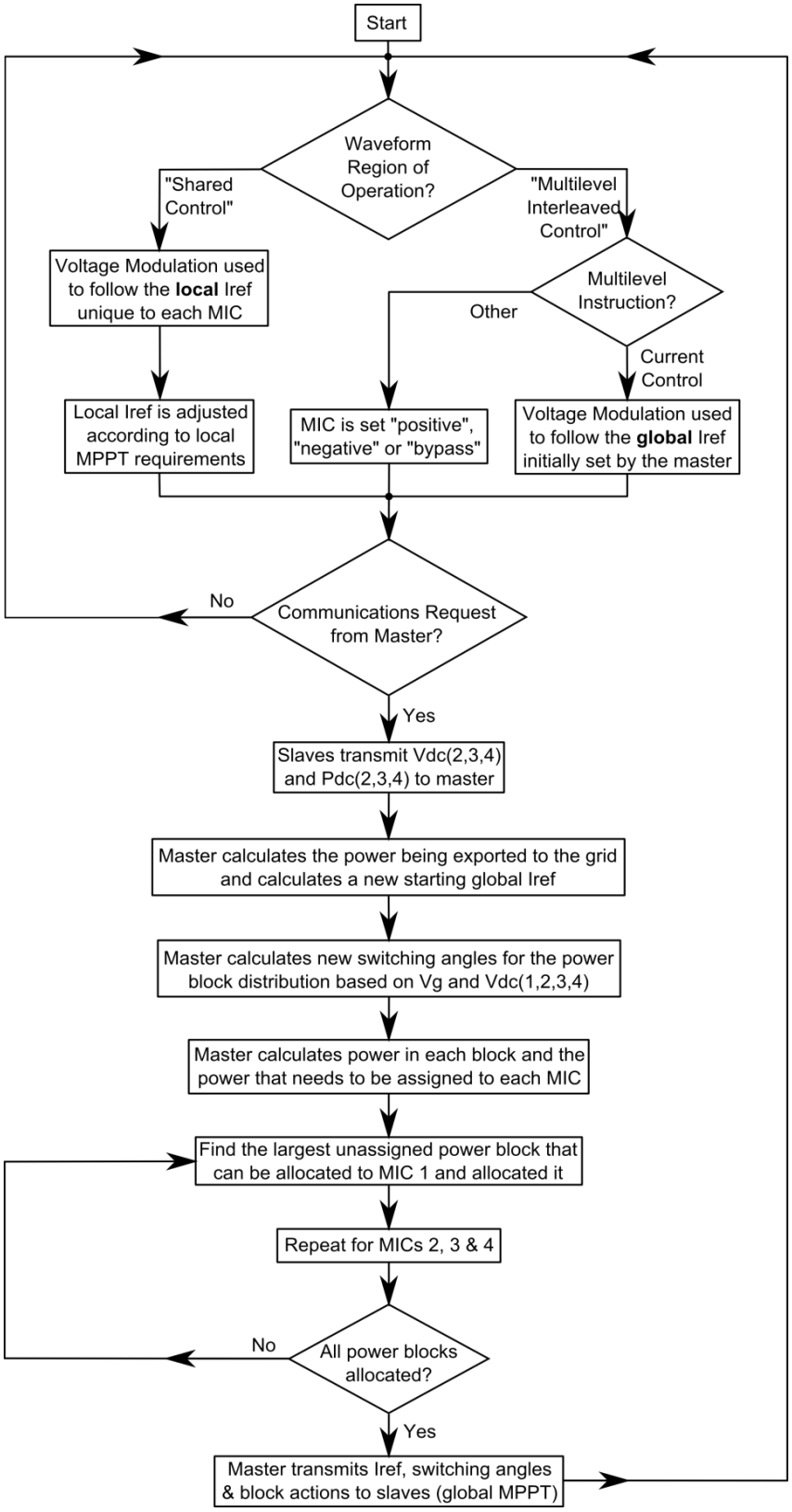

Fig. 4-6. The control diagram of the internal operations of the decentralised multilevel cascaded system performing MPPT.

4.3 Prototype System Implementation

A 4-MIC prototype system (see Fig. 2-18) with the specifications of Table 4-1 was developed to test the decentralised algorithm. Each MIC consists of a power supply (44.3V/225W capable), H-bridge (Fig. 2-12) and a SAM3X8E microcontroller. The power supplies were used to simulate the outputs of PV modules with boost converters. To emulate MPPT with power supplies, DSPACE was used to issue 0-200W power commands to the individual MICs. These power commands were then interpreted internally using only more/less power based logic (to emulate the P&O MPPT algorithm of Fig 1-6). A large 18.3mF capacitor was used to simulate an ideal DC-link for each MIC. Communications between MICs was achieved using a custom 16 pin parallel communications protocol, with a variable delay between global transmissions (global updates). The 110Vrms grid was simulated by four 30V-300VA transformer secondary windings connected in series. An 110V grid was chosen to reduce the number of MICs from 8 to 4. The voltage was finely adjusted on the primary side with a 230Vrms auto-transformer. The effective series inductance of this grid configuration was found to be minimal compared with that of the designed grid filtering inductance. To rapidly control the current, bang-bang control was used with a 100kS/s sampling frequency per-MIC. The move to bang-bang control (zero hysteresis band – fixed sampling frequency) from the hysteresis control of chapter 3 was made to allow for the lower inductance values (forces a higher switching frequency) that would be utilised for the 4-MIC system. Ideally, the sampling frequency would be increased, but this was not possible with the available hardware (it instead decreased due to increased software complexity). The AS/NZS 4777.2 standards [9] were used as a guideline to harmonic performance. Specifically, the harmonic current of the first 50 harmonics (<2.5kHz) was kept below 5% of the rated current. The shared control region width was set to match the natural 4th step of the multilevel waveform (63° for an over-rating ratio of 1.14p.u.). The MPPT global update rate was arbitrarily set to 0.5Hz, but reliable 5Hz operation was possible. Update rates slower than this were also possible (i.e. <0.5Hz).

Table 4-1. Specifications for the proposed 4-cascaded MIC system seen in Fig. 4-1 and Fig. 2-18.

Prototype Specification	**Operating Value**
Number of MICs	4
MIC Rated Input Voltage	44.3Vdc
MIC Rated Input Current	4.52Adc
MIC Rated Input Power	200W
MIC DC-Link Capacitance	18.3mF @ 50V
Rated Grid Voltage	110Vrms
Rated Grid Current	7.27Arms
Rated Grid Power Total	800W
Grid Frequency & PF	50Hz & PF = 1
Harmonic Current Target	<5% of Rated Grid Current (To the 50th Harmonic)
Per-MIC Grid Filtering Inductance	165uH (50uJ/W)
Per-MIC Current Sample Freq.	100kS/s
Over-Rating Ratio (SumVdc/Vg)	1.14p.u.
Hybrid Central Region Width	63°
Hybrid Global Update Rate	0.5Hz

To simplify development of the decentralised system, the two different regions of operation from Fig. 4-2 (multilevel and shared) were initially operated separately for benchmarking purposes. Experimental results for complete multilevel operation can be seen in Fig. 4-7a (i.e. no central shared region) while complete shared region operation can be seen in Fig. 4-7b (i.e. a central shared region of 180° or 100%). The multilevel-only mode did not use MPPT and had its block allocation manually configured. Although the multilevel-only mode was the top performer (in terms of switching frequency and THD), 100Hz global updating would be required for MPPT. Conversely, the shared-only mode (the worst performer) requires no global updating for MPPT. Finally, Fig. 4-7c shows the proposed hybrid decentralised mode of operation discussed in this chapter. The hybrid mode (being a combination of the multilevel and shared region modes of operation) requires only low frequency or infrequent global updating for MPPT, but still operates with a partially reduced switching frequency and THD. Thus, the hybrid system offers an intermediate compromise between the two modes of operation, allowing for many of the multilevel benefits without the need for consistent high speed communications to redistribute blocks at 100Hz.

However, by comparing the system switching frequency of the multilevel-only system (7.97kHz) and the shared-only system (26.76kHz) from Fig. 4-7(a/b) it can be calculated that this is a ratio of 1:3.4, which differs from the theoretical ratio of 1:4. This difference is due to the non-synchronisation of the PWM switching between MICs whilst they are in the shared-only mode. Although it is true the inductor voltage may be four times larger during shared region operation compared with multilevel operation, this is not always the case. As each MIC is sampling the grid current separately, there will be moments when one or more of the MICs are not in the same state as the other MICs. It is only when all four MICs simultaneously perform the same action (switch on or bypass) that the inductor voltage reaches its peak (and thus the di/dt). Thus, the switching frequency is reduced compared to what is expected. This effect can be seen in the system voltage of Fig. 4-7b, where it is very obvious that not all four MICs are switching together a significant portion of the time (i.e. around the 90° and 270° mark).

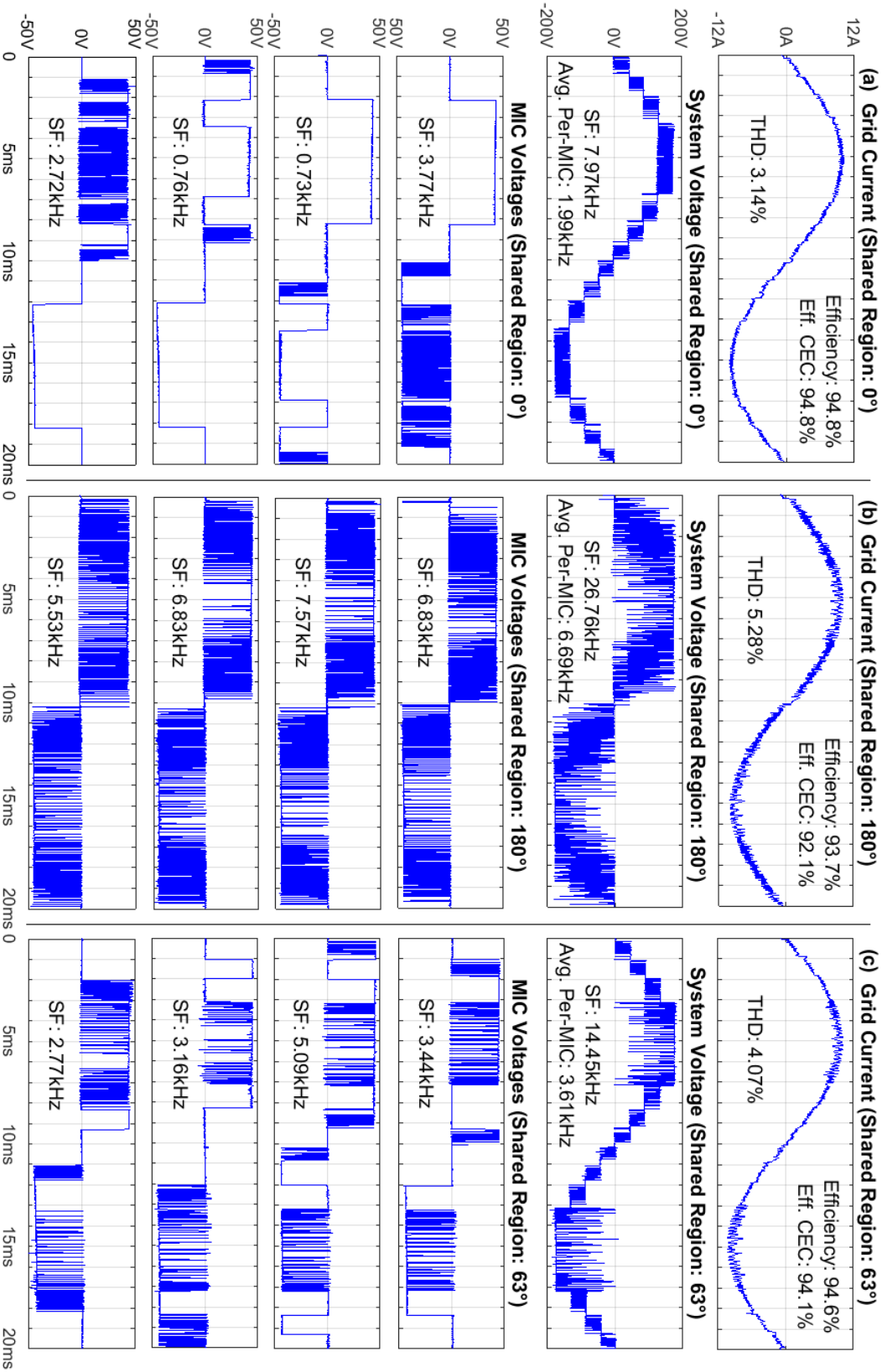

Fig. 4-7. The prototype (Table 4-1) decentralised system operating in multilevel-only mode (a), shared-only mode (b) and the proposed hybrid mode (c). These three modes correspond to central shared region widths of 0° (a), 180° (b) and 63° (c).

The process of global/local MPPT in the proposed hybrid system, as explained in section 4.2, can be seen in Fig. 4-8 as a practical example. At first the system is operating with the power block distribution of Fig. 4-8a and the grid current of Fig. 4-8b. Soon after, the local MPPT power target of one of the MICs (MIC-A) tries to change from 200W to 140W, quickly altering the grid current in the central shared control regions in Fig. 4-8d. This is a net power change of 60W in the 800W system (0.075W p.u.), which is spread unevenly between the MICs (local control) by allowing them to manipulate their voltage contributions within the central regions themselves (Fig. 4-8c). This allows the system to maintain a constant 200W in the unchanged MICs and have only MIC-A change in power (by 60W). However, this non-sinusoidal current change momentarily increases the current harmonics. At the next global MPPT update, the power blocks are redistributed away from MIC-A (Fig. 4-8e), which allows the voltage distribution within the central region to be rebalanced. Thus, with a balanced power distribution, the current reference has reset to a sinusoidal waveform that injects 60W less power than before (Fig. 4-8f), restoring the harmonics back to acceptable levels (<5% of the rated current).

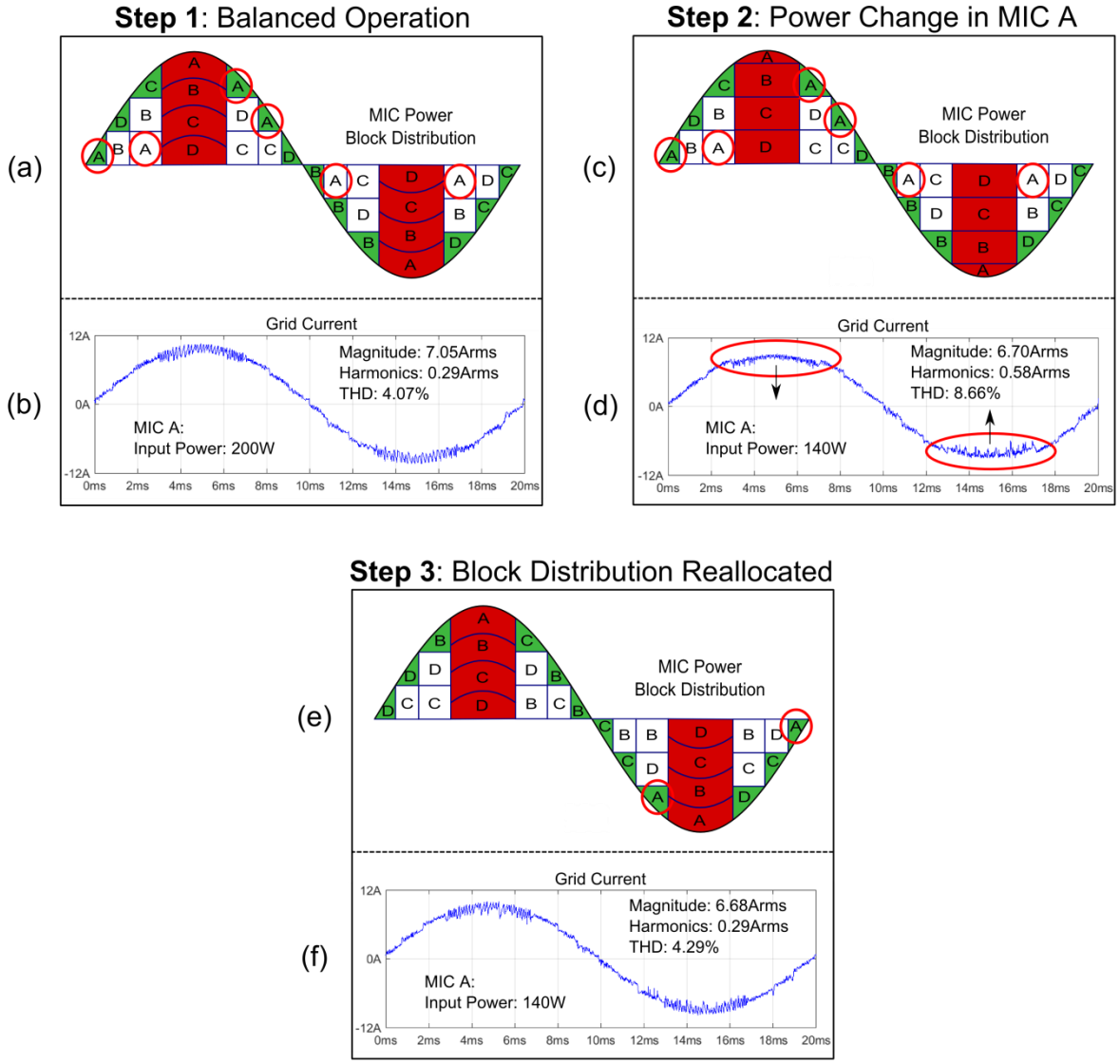

Fig. 4-8. A step-by-step walkthrough of the global and local MPPT as the power of MIC A is reduced from 200W to 140W in the prototype system (Table 4-1 specifications).

Thus it is possible to conclude from the prototype implementation that on a fundamental level, the system can perform decentralised hybrid global/local MPPT. However, there are limits to the effectiveness of the proposed system that require further analysis.

4.4 Fundamental Limits of Partial Shading

In a grid-tied cascaded system, whether multilevel or not, there is a fundamental limit to the distribution of power between the MICs due to partial shading and mismatch. In order for the system to inject sinusoidal current into the grid, it is necessary to generate a voltage waveform whose peak exceeds that of the peak of the grid voltage. With a boost converter in each MIC there is no problem generating the voltage to do this, but the problem occurs

when the shared grid current is too high for an MIC with a lower power capability. In this case the grid current is set, which means that only a reduction in the voltage can reduce the power contribution of that MIC. If there are more MICs than are needed to reach the grid voltage, then this lower power capability MIC can even reduce its voltage to zero. However, if the number of MICs is matched to the magnitude of the grid voltage (i.e. in most reasonable systems) then all of the MICs are needed to generate at least some voltage waveform for the system to function correctly. When the instantaneous grid voltage magnitude exceeds the voltage that occurs at the critical angle of equation (4-1), all of the cascaded MICs are required to work together to correctly inject current into the grid (i.e. only the total sum of the DC-link voltages can exceed the grid peak voltage). This is the same issue that was explored in a more limited fashion in section 3.4.2 for the 2-cascaded system.

However, as mentioned in section 3.4.2, there is a way to defeat this minimum proportional power requirement for a shaded MIC. If energy is transferred from an unshaded MIC to a severely shaded MIC by switching the H-bridge voltages of those two MICs to oppose each other in the series connection (during periods when the grid voltage is low), then that severely shaded MIC effectively has more power capability during the peak grid voltage. Thus, the DC-link of one MIC charges another in a process commonly known as inphase DC-link balancing [33]. This process can be used to both transfer power between MICs and regulate DC-link voltages. Detrimentally, inter-MIC voltage regulation is not suited to the slow global update rate of the proposed decentralised system, but inter-MIC power transference is plausible at the cost of significant added software complexity. However, this technique is not explored in this thesis as the proposed greedy-round-robin block sorting algorithm of 4.2.2 would be overwhelmed by the possibilities of both negative power block allocation and the additional invalid states introduced by the concept. Additionally, the system would require an awareness of the power sharing limit to at least some degree to be able to account for it. As implemented in the prototype, this fundamental power sharing limit is therefore important to be aware of and merits further generalised analysis.

4.4.1 Analysis of the Partial Shading Limits

The minimum on time for a single shaded MIC in a system is the duration of the minimum critical region (unrelated to the central shared control region width). For the 4-MIC prototype system the critical region is the portion of the waveform where the grid voltage exceeds the sum of the DC-link voltages of 3 MICs as seen in Fig. 4-9.

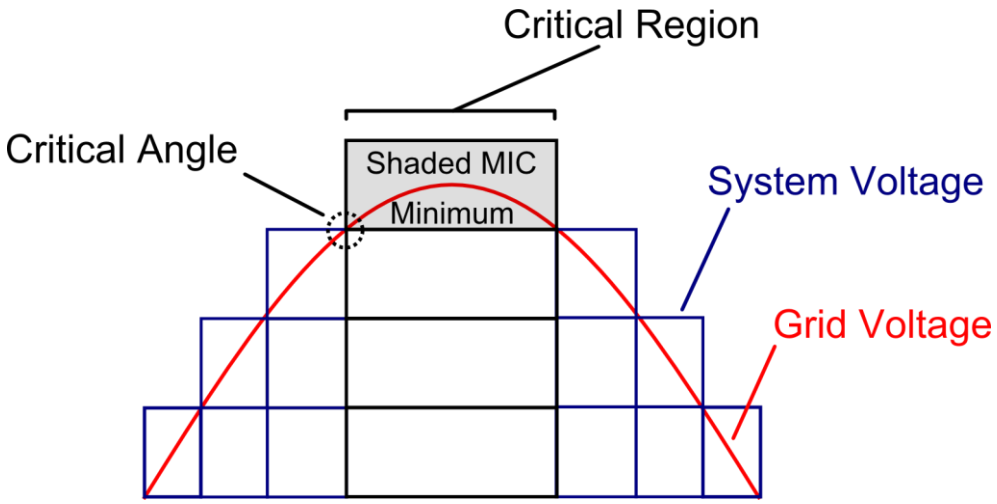

Fig. 4-9. For a single shaded MIC, the critical region can be defined as the region in which the shaded MIC must continuously produce at least some voltage in order for the entire cascaded system to exceed the instantaneous grid voltage.

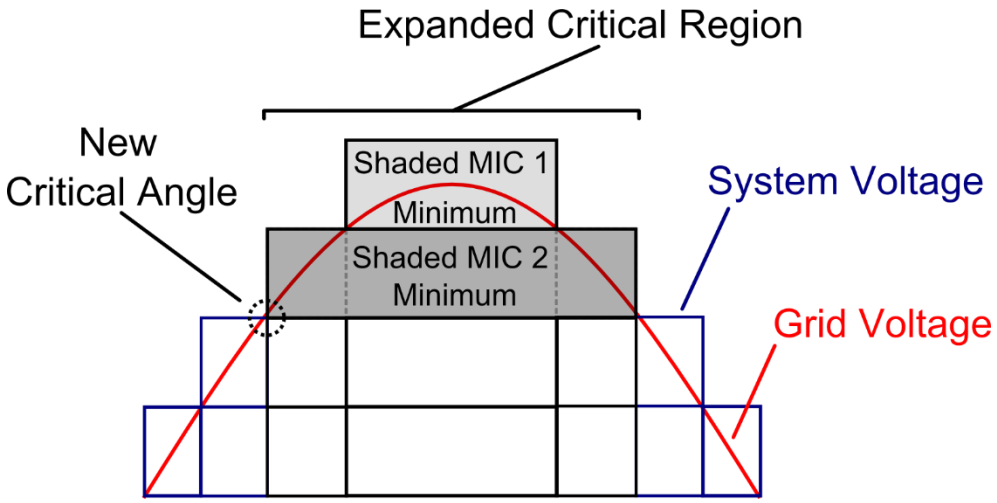

Fig. 4-10. As more MICs are shaded the minimum critical region is expanded. In addition to the requirements of the original critical region of Fig. 4-9, the second MIC must produce a necessary voltage throughout the entire expanded critical region in order for the entire cascaded system to exceed the instantaneous grid voltage.

If two MICs are experiencing heavy shade then we need to consider a larger minimum critical region. The first MIC needs to operate within the original critical region of Fig. 4-9, as all 4 of the MICs must produce a voltage to control the current here. Thus, it is logical that a second heavily shaded MIC still needs to produce a voltage in this region. However, the second heavily shaded MIC needs to also produce a voltage on both sides of the original critical region as seen in Fig. 4-10 (expanded critical region). Since we assume the first shaded MIC can only just manage to produce enough voltage to fill the original critical region, it cannot assist in producing voltage in the new expanded critical region area on each side. Thus, analogous to the original single shaded MIC limit, the problem is repeated, but this time it is all 3 remaining MICs that must operate simultaneously here to control the current. Thus, (in the 4-MIC prototype) the expanded critical region is the portion of the waveform where the voltage of the grid exceeds the sum of the DC-link voltages of 2 MICs.

The starting angle of the critical region is found from:

$$\theta = \text{asin}\left[\frac{(n-s)V_{dc}}{V_m}\right] \qquad (4\text{-}1)$$

Where 'n' is the number of MICs in a system, 's' is the number of shaded MICs in the system, 'V_{dc}' is the DC-link voltage of a single MIC and 'V_m' is the peak grid voltage. As the number of shaded MICs grow, so too does the size of the expanded critical region, defining the total minimum voltage/power that needs to be produced by these shaded MICs. The expanded critical region covers all of the recursively occurring critical regions that occur as more and more MICs are shaded. The per-unit power of the MICs within the expanded critical region is defined by:

$$P_{TotalCritical} = \frac{1}{\pi}\int_{\theta}^{\pi-\theta}[2\sin^2(x)]dx \qquad (4\text{-}2)$$

To calculate the minimum power that must be contributed by a shaded group of MICs within the expanded critical region, the per-unit power of the lower part of the region is first calculated (i.e. non-shaded MIC power contribution in the expanded critical region):

$$P_{UnshadedCritical} = \frac{1}{\pi}\int_{\theta}^{\pi-\theta}\left[\frac{2V_{dc}}{V_m}(n-s)\sin(x)\right]dx \qquad (4\text{-}3)$$

This is then subtracted from the total critical region to find the minimum power required of the group of shaded MICs:

$$P_{ShadedCritical} = P_{TotalCritical} - P_{UnshadedCritical} \qquad (4\text{-}4)$$

Now that the minimum power required for a group of shaded MICs is known, the power calculation needs to be scaled down for per-unit calculation purposes as the total system power has changed due to the shading, affecting the per-unit base:

$$P_{scalingFactor} = \frac{1}{n}\cdot\frac{(n-s)}{(1-P_{ShadedCritical})} \qquad (4\text{-}5)$$

Thus, the average minimum power required per-MIC in a group of shaded MICs can be found from:

$$P_{MICmin(p.u.)} = P_{scalingFactor}\cdot\frac{P_{ShadedCritical}}{s}\cdot n \qquad (4\text{-}6)$$

Fig. 4-11 shows the calculated maximum shading that is allowed per-MIC in a group of shaded MICs without compromising the PV utilisation of the unshaded MICs (forced derating). Critically, this is plotted as a function of the DC-link magnitude, where 1 p.u. implies that the sum of all the MIC DC-link voltages is equal to the grid peak voltage. This is the DC-link over-rating ratio. If the ratio were 2 p.u. then the sum of the MIC DC-links would be twice the grid peak voltage. Each of the plot lines represents a cascaded system of any number of MICs, but with a set proportion of those MICs shaded to the maximum amount relative to the unshaded MICs. For example, if there are 4 MICs in the system and 2 are shaded, then the proportion shaded is 50%. This is identical to a 16 MIC system with 8 MICs shaded. Thus, the p=50% curve can be used to find the maximum shading that is allowed, per-shaded-MIC, in a system where 50% of the MICs are shaded. This maximum shading is given as a percentage reduction compared to the power of the non-shaded MICs. It can be seen that as the over-rating ratio goes up, the maximum shading percentage that can occur for a shaded MIC eventually reaches 100%. This occurs regardless of the system shading proportion. When the maximum shading reaches 100%, the DC-link magnitudes

are such that even in the critical region, not all MICs are required to exceed the peak grid voltage and thus one (or more) MIC(s) are rendered redundant (and can be 100% shaded). As the number of MICs in the system increases, the size of the critical region shrinks (for a given number of shaded MICs), reducing the minimum power requirement in the region (by ultimately decreasing the system shaded proportion). Fig. 4-11 is useful for quickly gauging how the DC-link magnitude selection (or grid voltage fluctuations) can alter the non-uniform shading performance of differently sized systems. For the 4-MIC prototype system, a shading proportion of 25%, 50% & 75% represents 1, 2 and 3 MICs shaded respectively.

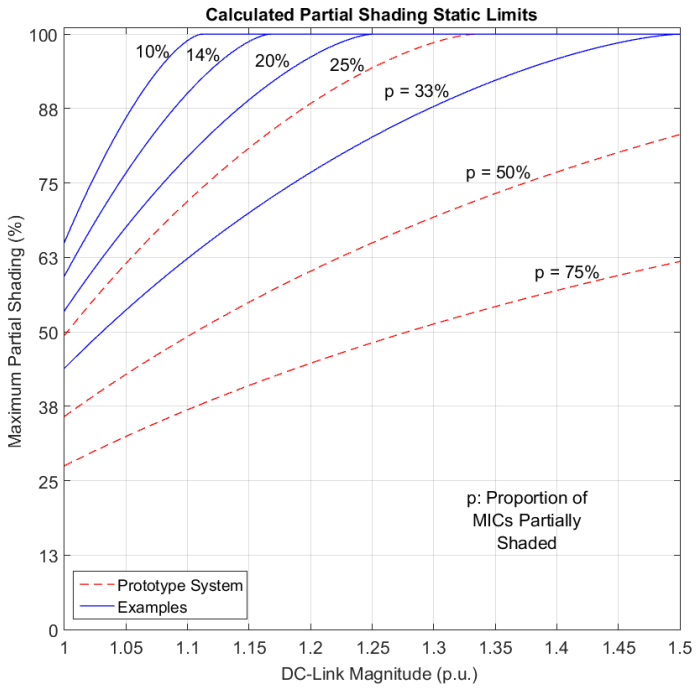

Fig. 4-11. The calculated maximum partial shading allowed per-MIC in a group of shaded MICs. The group size of the shaded MICs is given as a proportion of the total number of system MICs.

To visualise the fundamental limits of power sharing in multilevel systems, Fig. 4-12 shows measured results from the prototype system when it is following power commands over a five minute period with an over-rating ratio of 1.14 (i.e. a DC-link magnitude of 1.14 p.u.). Seen in Fig. 4-12a and Fig. 4-12b are the individual MIC power commands and measured responses respectively, which is then followed by the total commanded and measured power overlay in Fig. 4-12c. Finally seen is the power utilisation (Fig. 4-12d),

which represents the instantaneous percentage ratio of the total measured power to the total commanded power.

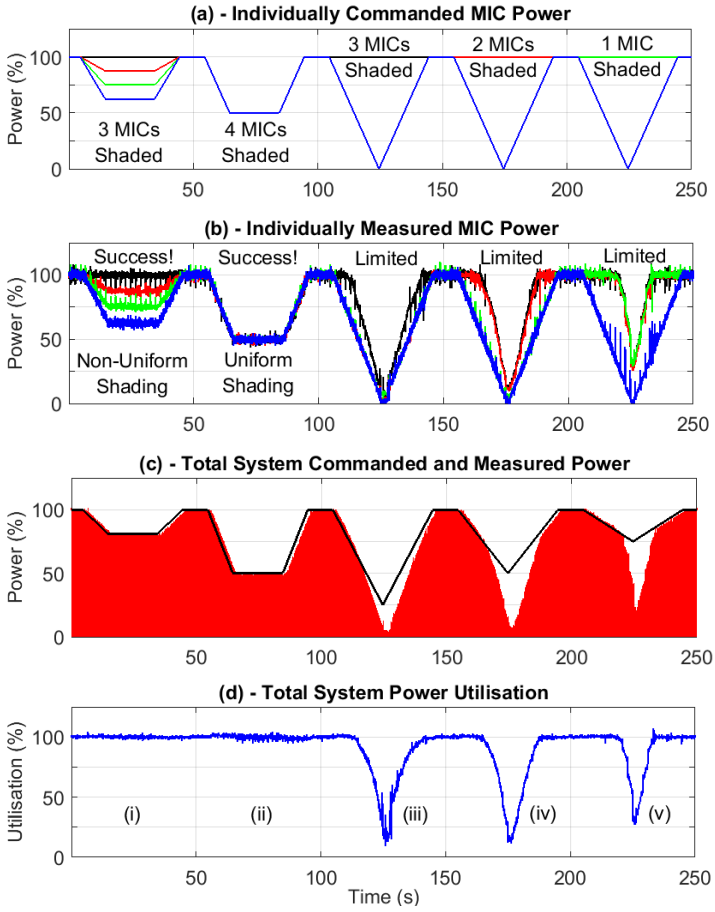

Fig. 4-12. The commanded MIC power levels (a) and their measured responses (b), followed by the total commanded/measured power (c) and the resultant total utilisation of commanded power (d).

The time interval of (i) in Fig. 4-12 shows a moderate power difference between the MICs (non-uniform partial shading) and (ii) shows identical, but reduced power across the MICs (uniform shading). In both cases the power utilisation remains at 100%. However in (iii), (iv) and (v), the power targets of three, two and one MICs are dropped to 0% (i.e. they approach 100% shading) respectively. In these cases the power of the non-shaded MICs are affected and the power utilisation of the entire system quickly drops as the power commands are no longer being met due to the fundamental cascaded partial shading limit. As per Fig. 4-11, when a higher proportion of the MICs are shaded, the allowable percentage shading per-MIC is lower due to the larger expanded critical region. Thus, in Fig. 4-12, the single unshaded MIC in (iii) is quickly affected by the three shaded MICs

(shaded proportion = 75%) compared with the case of (iv), where instead now two MICs are unshaded (shading proportion = 50%), increasing the average utilisation during the period. Finally, in the case of (v), where three MICs are unshaded (shading proportion = 25%), there is a much reduced negative effect on the power utilisation than either the (iii) or (iv) situations.

It can be seen from Fig. 4-12(i) that moderate amounts of partial shading were easily tolerable even on the relatively small 4-MIC prototype system. There were concerns that the lowest shading proportion possible for a 4-MIC system (p=25% - 1 MIC shaded) was too high, but Fig. 4-12(v) shows that even at p=25% there is a large power difference between the MICs before utilisation drops. As the DC-link over-rating ratio utilised is realistic (1.14 p.u.), this suggests that the partial shading limit is not worthy of too much concern for at least any system equal to or larger than 4 MICs. This is especially true when we consider that the purpose of per-panel MPPT is primarily for correcting PV mismatch and not typically for the exaggerated cases of extreme partial shading caused by trees, building protrusions, etc.

A direct comparison between the measured and calculated partial shading limits is given in Fig. 4-13. To measure the maximum shading of groups of shaded MICs, the shading (power commands from Simulink-DSPACE) was increased until the unshaded MICs began to struggle to meet power targets by about 2.5%. For this comparison the measured curves were shifted to the left to compensate for practical factors that reduced the effective DC-link voltage (and thus the over-rating ratio) of the prototype. Voltage drops such as on-state switch resistance, filter resistance, wiring resistance and DC-link ripple were considered in this adjustment. Looking at Fig. 4-13, for the cases of one and two shaded MICs, the calculations are mostly accurate until the over-rating ratio exceeds 1.2. Beyond this DC-link over-rating ratio the algorithm (as implemented) started to struggle as the 4th MIC voltage step became increasingly narrow. Similarly, when three MICs are shaded the measured data is significantly different due to a fundamental flaw in the power block round-robin greedy sorting algorithm shown in Fig. 4-5, which sorts power block allocations by a rotating nearest fit. This is useful for reducing block allocation error, but it does not take into account extreme power sharing ratios between MICs (i.e. a specific block that should have been allocated to a shaded MIC may have

previously been allocated to another MIC). When the number of shaded MICs is higher, misallocation in extreme ratios is more likely due to the requirement of a more specific arrangement of power blocks and results in larger average allocation errors. A modified algorithm can correct for this, but it will first need to be able to analytically identify when the system is approaching a sharing limit (and not just detect when it is at the limit).

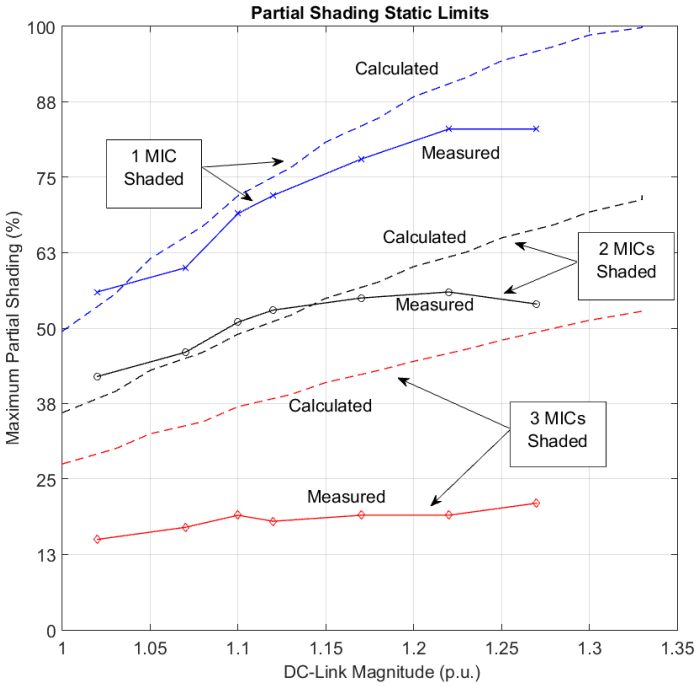

Fig. 4-13. The calculated & measured maximum partial shading allowed per-MIC in a group of shaded MICs for the 4-MIC prototype system of Fig. 4-1/Table 3-1.

4.5 Fundamental Limits of the Decentralised MPPT Speed

In addition to the fundamental limits of the partial shading distribution amongst MICs, the proposed decentralised system also has a limit to how fast MPPT can occur. In typical MPPT for standard inverters, MPPT is limited by the controller's power slew rate, which is intentionally restricted to maintain stability (i.e. lower control loop gains). For the proposed decentralised system, there are additional restrictions that can greatly reduce the MPPT speed if not considered. The MPPT speed of the proposed decentralised system is controlled by the following four factors:

1. The MPPT speed of the local controller of each MIC (stability).

This is a speed restriction placed on the control system of each local MIC as they attempt to increase/decrease their current within the shared control region, as explained in 4.2.3. The local MIC MPPT speed ultimately controls how fast the system can respond to a change in power in any one PV panels. Too fast and the system power output oscillates (resulting in poorer utilisation under stead-state conditions), but too slow and rapid MPPT tracking is impossible (resulting in poorer utilisation during transient conditions). Note that this control is applied to the shared control region and not the entire waveform.

2. The harmonic restrictions of the grid standards.

As the local controllers of each MIC start to increase/decrease their current reference within the shared control region (Fig. 4-2 and Fig. 4-14), that portion of the waveform begins to extend beyond a sinusoidal shape (creating harmonics). This can be seen in Fig. 4-8d, where the shared control region current is reduced, increasing the harmonic content. If the change in current in this region is only moderate, then the grid harmonic standards will not be breached before a global update occurs and resets the sinusoidal shape of the waveform through readjusting the multilevel block allocation (Fig. 4-8e and Fig. 4-8f). Thus, if the grid harmonic standards are strict then they will be reached/exceeded as the current references reach a certain point, forcing the local controller of each MIC to restrict MPPT until a global update is received.

3. The width of the shared control region (Fig. 4-2 and Fig. 4-14).

To decrease the current harmonics produced by the local MPPT process in each MIC, the width of the shared control region can be widened. Widening the shared control region allows for a greater amount of energy in each cycle to be available for local MPPT, which results in a shallower, but wider protrusion from the sinusoidal shape of the waveform. This results in a reduction of the harmonic content of the waveform, which can be seen as the sharing region width is increased in Fig. 4-15 (by moving up the y-axis). However, this comes at the expense of reducing the size of the multilevel region in the waveform, increasing the switching frequency. It is important to note that the width of the shared control region can be of arbitrary size and does not need to align with the natural steps of a multilevel converter.

4. The global update rate of the entire system.

As the local MPPT of each MIC increases/decreases the current reference (and therefore the power) within the shared control region, the harmonics will grow until the grid limit is reached, forcing a temporary stop to MPPT. To avoid this, the global update rate of the system can be increased to allow the current reference to be reset by block allocations (Fig. 4-8e and Fig. 4-8f) more frequently. The increased update rate ensures that the change in power during the time that passes between those global updates will be smaller, as less time will now exist between each update. For a given set of weather conditions (i.e. the speed of change of solar irradiance), width of the shared control region and harmonic limits, a certain global update rate will be required to avoid compromising the MPPT. The effects of an insufficient global update rate can be seen in Fig. 4-14, where the harmonics are clearly too high by any standard.

Practically speaking, the MPPT speed limit of the local controller (factor 1) can be made to be so fast as to have no effect on the system and it is in fact the harmonic restrictions of the grid standards (factor 2) that set a hard limit on the global MPPT speed. This hard limit is in turn affected by a tradeoff between the shared control width (factor 3) and the global update rate (factor 4), with factor 3 affecting the system switching frequency. This tradeoff is explored further in the following section.

4.5.1 Analysis of the Local MPPT Speed Limit and Tradeoff Implications

To visualise the distorted waveforms created by the local MPPT of each MIC, the Fourier series was chosen to mathematically analyse the system current. The Fourier series is especially useful here for harmonic calculations as the Australian grid standards [9] are only concerned with the first 50 harmonics. Thus, a 50 harmonic Fourier series is used to find the time domain sum, $F_n(x)$, of the harmonic currents generated when the local shared region current differs from the global current (the starting sinusoidal reference):

$$F_n(x) = \sum_{n=2}^{50} \left[\left(\frac{1}{\pi} \int_0^{2\pi} f(\phi) \sin(n\phi)\, d\phi \right) \sin(nx) \right] \qquad (4\text{-}7)$$

Where ‘f(ϕ)’ is the distorted current waveform of (Fig. 4-2 & Fig. 4-14), described by:

$$\begin{cases} f_1(\phi) = I_G \sin(\phi) \\ f_2(\phi) = I_L \sin(\phi) \end{cases} \qquad (4\text{-}8)$$

Where $f_1(\phi)$ is the function describing the global region current (I_G = conceptual sinusoidal peak) and $f_2(\phi)$ is the function describing the locally controlled, shared region current (I_L = sinusoidal peak). The balance between the two is based on the width of the shared region. The system waveform can be seen in Fig. 4-14, which shows an extreme example to visualise the Fourier series integral regions of equation (4-8).

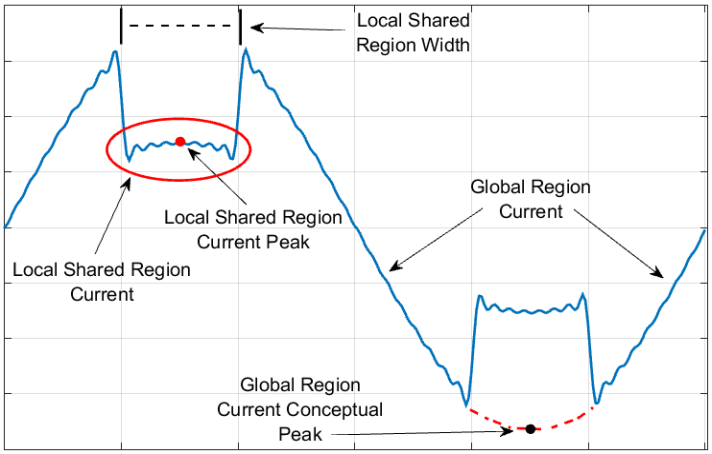

Fig. 4-14. A 50-harmonic (plus fundamental) Fourier series approximation of the system waveform undergoing a large change in power due to an insufficient global update rate (increasing the THD).

The harmonic RMS current of the system waveform Fourier series is therefore:

$$I_{HarmonicsRMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} F_n(x)^2 dx} \qquad (4\text{-}9)$$

The total change in power that occurs due to local MPPT within the shared control region can be found from:

$$P_{change} = \frac{1}{\pi}\int_{\frac{\pi}{2}-\frac{width}{2}}^{\frac{\pi}{2}+\frac{width}{2}} V_m(I_L - I_G)\sin(\phi)^2 d\phi \qquad (4\text{-}10)$$

Where V_m is the peak grid voltage. From (4-10) it is possible to find I_L as a function of the shared region 'width' (radians) and the power change (due to local MPPT) between global updates. Thus knowing I_G, taking I_L from equation (4-10) allows (4-8), (4-7) and then (4-9) to be solved respectively. The MPPT peak RMS harmonic current (4-9) is therefore a function of both the shared control width and the change in power between global updates,

which is illustrated (including the fundamental current) in Fig. 4-15. This figure, using the derived Fourier series equations, shows the system waveform operating in various situations as an array of possibilities. The x-axis, or change in power, represents a varying difference in the change in power between global updates. That is, the total change in power that the local MPPT controllers accumulate within the shared region before the global algorithm has a chance to reset the current reference and remove the harmonics. Ultimately, Fig. 4-15 demonstrates how the system waveform (with a base power of 0.75W p.u.) is changed as the power is decreased/increased by 0.25W p.u. to 0.5W/1W p.u. respectively, with multiple different shared control regions widths.

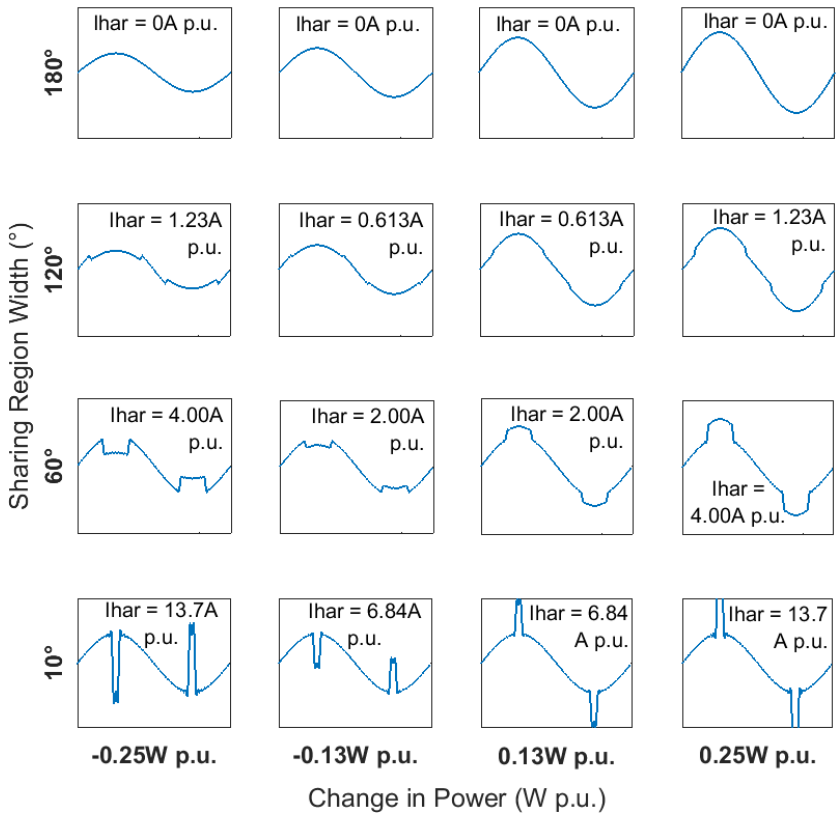

Fig. 4-15. The calculated peak harmonic current waveforms generated by local MPPT as a function of the shared region width and the power change between global updates. Where 1W p.u. is the total system power and 1A p.u. is the allowed harmonic current (5% of rated current). See Fig. 4-18 for similar measured MPPT waveforms from the prototype system.

For a given filter-energy-storage-per-watt and bang-bang control with a constant sampling rate, the hybrid control (Fig. 4-7c) average switching frequency per-MIC $SF_{HybridMIC}$ can be equated as a function of three variables:

$$SF_{HybridMIC} = \frac{SF_{UncoordinatedMIC}}{\pi}\left[\frac{width(n-1)+\pi}{n}\right] \qquad (4\text{-}11)$$

Where $SF_{UncoordinatedMIC}$ is the shared-only (sharing region of 180° as seen in Fig. 4-7b) average switching frequency per-MIC, 'width' is the shared region width in radians and 'n' is the number of MICs in the system. This equation shows that the shared region width has a heavy influence on the hybrid control switching frequency per-MIC. Effectively, equation (4-11) describes the balance between the shared control region and the multilevel region seen Fig. 4-2. In the shared control region, the switching frequency per-MIC is set based on how the entire 'n' sized system would act if there were no multilevel switching. However, in the multilevel region, more MICs in the system (higher 'n') results in the periods of PWM being spread between a larger amount of MICs (smaller time allocations), reducing the switching frequency per-MIC. Additionally, when the number of steps in a multilevel waveform 'n' increases the instantaneous voltage across the filter is reduced, decreasing the di/dt and thus, the necessary switching frequency. However, in 1st order bang-bang control the switching frequency is not actively adjusted to maintain a constant THD and thus, the THD is free to vary with the di/dt. Thus, it is instead the baseline THD that is reduced by the lower filter voltage within the multilevel region and not the switching frequency. This effect is also reinforced by the fact that in Fig. 4-7b, not all of the MICs are switching simultaneously, which serves to reduce the shared region switching frequency. As the hybrid switching frequency is calculated as a proportion of the uncoordinated switching frequency (Hz p.u.), this serves to further increase the p.u. switching frequency. Thus the overall effect for a decentralised 4-MIC system is that changing the shared region width from 180° to 0° results in a reduced baseline THD and a switching frequency that is a quarter of what it was and not a sixteenth. Thus, equation (4-11) reflects this by not squaring the 'n' term.

Practically, equation (4-11) can be used to quickly calculate the switching frequency per-MIC as the shared control region is varied, which is visualised in Fig. 4-16. We can see that as the sharing region width approaches the maximum (180°), the switching frequency per-MIC approaches the switching frequency that would occur if there was no multilevel interleaving (1Hz p.u.). As the number of MICs in the system is increased the switching frequency reduction per-MIC becomes more significant due to increased number

of steps in the multilevel waveform. By increasing the sharing region width, the portion of the system waveform that actually participates in multilevel interleaving is reduced until eventually there is no period of multilevel operation. Thus, the change in the switching frequency per-MIC for the full range of sharing regions widths is more pronounced for systems with larger numbers of MICs (as they are more able to benefit from the substantially reduced switching frequency per-MIC during multilevel operation). Also seen in Fig. 4-16a is the operating point of the prototype system (shared region of 63°) and the measured switching frequency per-MIC as a p.u. value (0.54Hz p.u.), which can be obtained from the ratio of the switching frequencies from Fig. 4-7c (3.61kHz) and Fig. 4-7b (6.69kHz). This measured switching frequency ratio differs from the calculated per-MIC switching frequency (0.51Hz p.u.) by only 0.03Hz p.u.

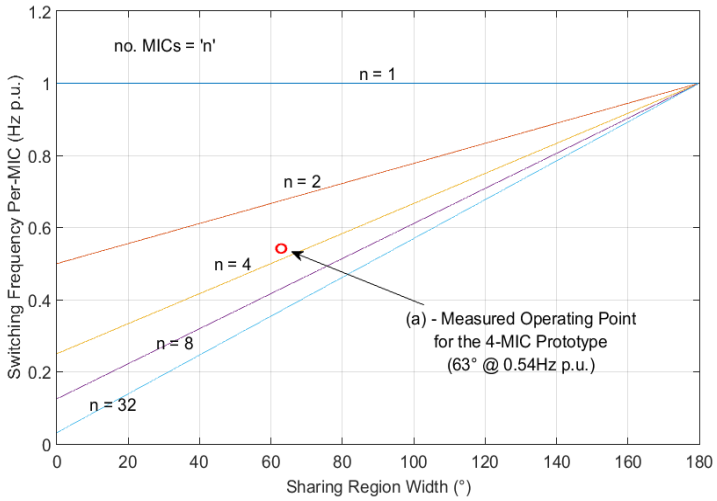

Fig. 4-16. Calculated effect of the shared region width on the switching frequency per-MIC, where 'n' is the number of MICs in the system. 1Hz p.u. is equivalent to the switching frequency of an 'n' sized system operating without any multilevel interleaving (i.e. shared region width = 180°).

It has been identified that the MPPT speed of the decentralised system is effectively based on the tradeoff between the global update rate, the harmonic grid restrictions, the sharing region width and the switching frequency. Therefore, it is possible to definitively visualise the problem. By taking the array of waveforms from Fig. 4-15 and instead representing each waveform as purely a magnitude representing its harmonics, the contour plot of Fig. 4-17a can be plotted using the Fourier analysis discussed previously. As discussed with Fig. 4-15, Fig. 4-17a shows that as the positive/negative change in power between global updates increases, the peak harmonic current will quickly rise unless the

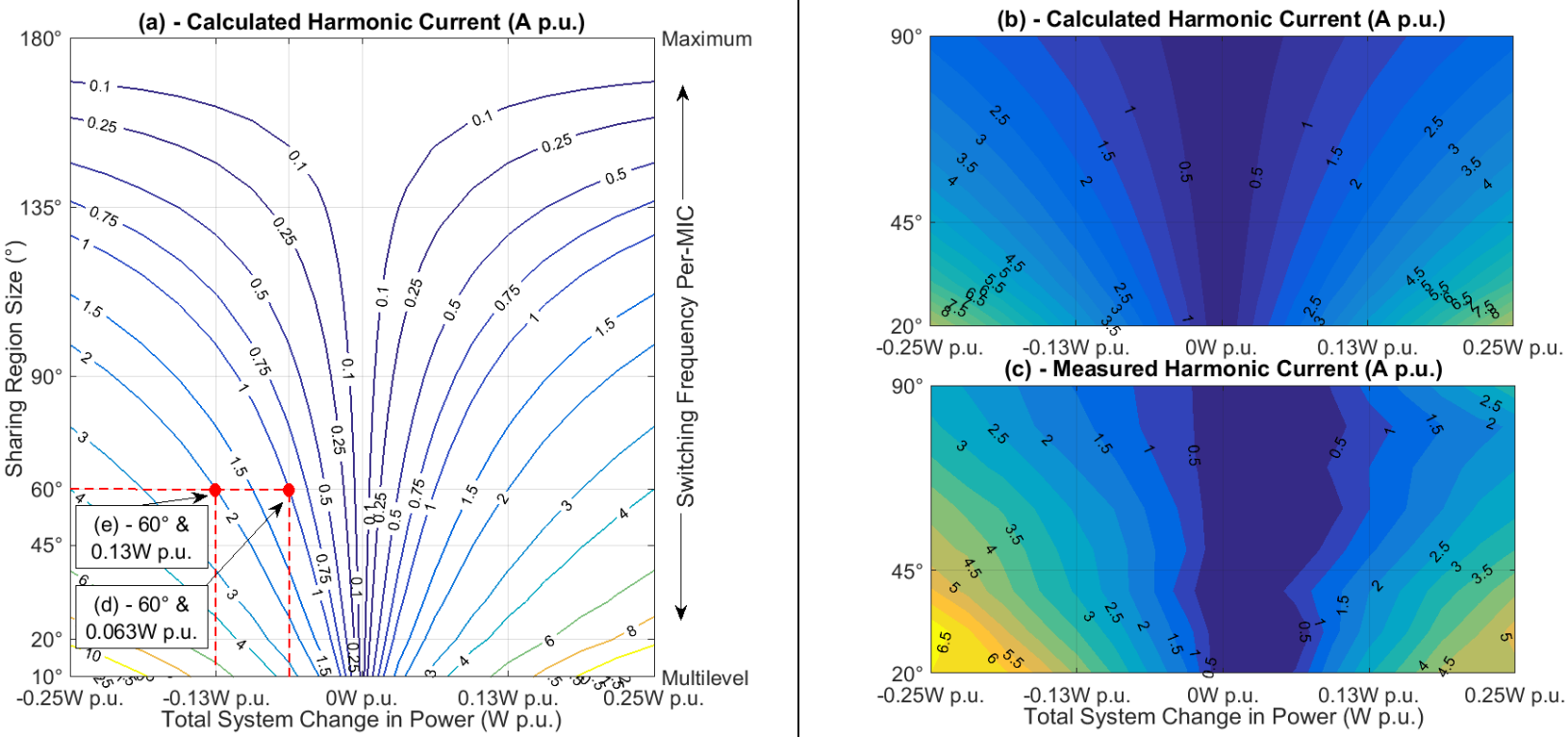

Fig. 4-17. The peak harmonic current (to the 50th harmonic) generated by local MPPT as a function of the shared region width and the power change between global updates. Plots (a) and (b) are calculated and (c) is measured over a restricted range. 1W p.u. is the total system power and 1A p.u. is the allowed harmonic current (5% of rated current). Specifications according to Table 3-1.

shared control width is increased to compensate. However increasing the width also increases the switching frequency towards that of completely non-multilevel control.

Regardless of the number of MICs that are undergoing local MPPT within the shared control region (i.e. uniform or non-uniform partial shading), the current waveforms are identical for a given total system p.u. power change and sharing region width. To generalize Fig. 4-17a, a current of 1A p.u. represents the maximum harmonic current allowed in the system for the Australian grid standards [9] (5% of rated current). However, these harmonic currents only account for the additional harmonics introduced by the MPPT process and do not take into account the baseline harmonic current in the static system when MPPT is not in use. Fig. 4-17a also reveals that unless the shared region width is sufficiently large enough, the maximum possible change in power between updates is limited by harmonics that are well in excess of 1A p.u. Note that these harmonic currents represent the peak or worst-case harmonics just before a global update. When averaged over a global update cycle, the harmonics are approximately half of these peak values.

Fig. 4-17b and Fig. 4-17c compare the predicted and measured results. To simplify this comparison, the measured data was corrected for changing grid voltages during testing. Additionally, by subtracting the non-MPPT baseline harmonic current from each point, only the MPPT harmonics remain for comparison. In general, the measured harmonic currents are similar between the two graphs, but the extremes of the measured harmonics (at large power changes and small central widths) are smaller in the measured case. This is due to the prototype's di/dt which is limited by the inductive filter. The limited range of the shared region width explored in Fig. 4-17b and Fig. 4-17c (20°-90°) compared with Fig. 4-17a (10°-180°) is due to MIC control software limitations. The right shift in Fig. 4-17c is due to the global MPPT algorithm allocating too much power during block allocation. As a result, the local MPPT algorithm corrects for this in the central region and reduces the output power. Thus, a small positive change in local MPPT power at this point is actually restoring the waveform to a low harmonic state. This power over-allocation error is not seen by the system itself and is caused by systematic power measurement error. The result of such an error would therefore be higher harmonics when reducing power.

Conversely, increasing the power with this problem would result in comparatively lower harmonics compared with the calculated case.

Just as the calculated harmonics of Fig. 4-17a are visualised in Fig. 4-15 as an array of calculated waveforms, some of the measured harmonics of Fig. 4-17c are visualised in Fig. 4-18 as an array of measured waveforms. Due to software limitations, some waveforms are not included. Firstly, the current harmonics are less significant for positive changes in power (due to the systematic power measurement error as discussed in the previous paragraph). Secondly, it is possible to see the finite slew rate of the current. This is especially apparent in the bottom left waveform (30°,-0.25W p.u.), where the central shared region current has an obvious non-infinite slope as it transitions between the two regions of operation (global/local). In the calculated waveforms of Fig. 4-15, this slope exists due to the limited number of harmonics (first 50) that are included in the Fourier series analysis. However, the measured slope seen is due to the inductive filter of the system, limiting the di/dt. If the sharing region were very narrow (or the filter inductance very large) then it would be difficult for the sharing region to function correctly as the transition time between the two regions would be relatively large.

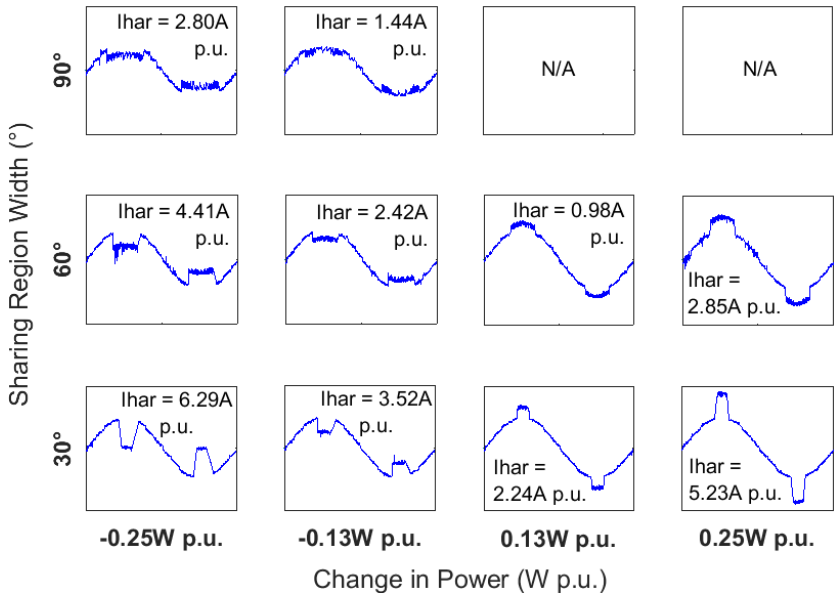

Fig. 4-18. The measured peak harmonic current waveforms generated by local MPPT as a function of the shared region width and the power change between global updates. Where 1W p.u. is the total system power and 1A p.u. is the allowed harmonic current (5% of rated current).

Fig. 4-17a is best understood in the context of practical inverter design. In [37], it was found that over a period of one second, the fastest that a cloud could reduce solar luminosity was a reduction of 22.9% (or 0.229W p.u.). From a desired switching frequency and equation (4-11) we may select 60° as the central shared region width. Following this, it is desirable for the peak MPPT harmonics never to exceed the Australia grid standards [9] at any point. Thus, 1A p.u. contour line can be chosen. The point (d) in Fig. 4-17a shows the maximum change of power that is possible at this point between each global update is only 0.063W p.u. Thus, the required global update rate (to be able to track this rate of change of input power) is the desired change in power per second (0.229W p.u.) divided by the possible change in power per global update (0.063W p.u.), which results in 3.6Hz for this example.

For comparison, using the measured results of Fig. 4-17c, the global update rate required for the same conditions is 5.3Hz, but after compensating for the power measurement offset (i.e. taking an average of positive/negative MPPT), the global update rate requirement is found to be 2.6Hz. This is the worst case example and in practice (depending on the harmonic standards utilised) occasional spikes may be tolerable, or instead poorer PV power utilisation under these transient conditions may be preferable instead. Either way, a more pragmatic design would allow for a much lower global update rate.

As one such pragmatic example, we can again look at Fig. 4-17a and choose the same shared region width of 60°. Let us consider a system that can go from full power to zero in 10 seconds (i.e. a more feasible 0.1W p.u. per second) and let us choose the harmonic contour line of 2A p.u., as these contours represent only the peak MPPT harmonics. If the 0.1W p.u. per second MPPT solar transient occurs continuously, the harmonics will ramp up to their peak and then reset to near zero, resulting in an average harmonic content of half of the peak. Thus, a 2A p.u. peak harmonic current can still be considered within the grid specification on average (depending on the interpretation). Therefore, at point (e) in Fig. 4-17a, it can be seen that 0.13W p.u. is possible per global update cycle, which (for a 0.1W p.u. per second desired MPPT rate) requires a global update rate of only 0.77Hz (or 0.7Hz for the power-offset-corrected prototype system). However, lower update rates are possible if we form the premise that solar transients are rare and that the harmonics

produced (which will exceed the grid standards) occur infrequently. Thus, the THD over a long period of time will be well below the grid standard, which, depending on how the THD is defined, may be partially or completely acceptable.

4.6 Summary of Findings

In this chapter a simplified decentralised algorithm for multilevel cascaded MICs was analysed and then verified with a prototype system. The hybrid multilevel/shared region waveform concept was described, along with the concepts of the global/local MPPT operation and the resultant greedy round robin power sorting algorithm that controls the entire process. Additionally, the MPPT partial shading limits of cascaded systems were analysed, along with the dynamic tradeoff between the MPPT speed and the global update rate. An 800W, 4-MIC prototype system was used to verify these concepts and analysis. The key findings are summarised below:

- The round robin greedy MPPT algorithm to successfully allocated power between the four MICs in the decentralised system with allocation error generally below 2%. The computation power required to do so is minimal. However, the algorithm is not suited to more complex tasks that require taking other variables or future situations into account. Specifically, it is difficult to allocate power blocks whilst arranging them to reduce the 100Hz PV power ripple or to transfer power between MICs (i.e. negative power blocks). As the variable complexity grows, so too does the number of invalid states, increasing the need for foresight and the likelihood of significant allocation errors.
- There is a calculable limit to the power distribution limits between the MICs themselves, which is controlled by the proportion of MICs that are shaded and the total-DC-link-to-grid-voltage over-rating ratio. It was found that when high proportions of MICs were shaded in the prototype system (and very specific MIC power block configurations were required) the greedy round robin sorting algorithm struggled to allocate power near the calculated theoretical limits of what should be possible. It was found that (for an over-rating ratio of 1.14p.u.) a single MIC in the prototype system could be shaded by up to 74% (compared with a 78% theoretical limit) before the power utilisation of the other MIC's were affected.

- The proposed decentralised system has a finite MPPT speed limit that is controlled by the harmonic limit, the switching frequency, the shared region width and the global update rate of the system. For the worst case scenario (continuous maximum solar transients – 0.229W p.u. per second), it was found that the global update frequency needed to be at least 2.6Hz. For a more relaxed general purpose scenario (continuous 0.1W p.u. per second solar transients), update rates of 0.7Hz were found to be plausible. Both cases allowed for a 50% switching frequency reduction compared with non-multilevel operation (vs. a 75% switching frequency reduction for high speed centralised multilevel operation). Depending on the definition of the THD in the grid standards utilised (specifically the averaging period), much lower update rates are feasible.

In conclusion, the proposed decentralised cascaded system allows for both module-level MPPT (without high-gain boost converters) and a partial implementation of coordinated multilevel switching without the need for a centralised controller. However, this does come with the requirement of an infrequent/intermittent global communications link (<1Hz) between MICs, which can easily be achieved through a wireless link.

5 Conclusions

5.1 General Summary

As demonstrated, the decentralised cascaded multilevel level system can offer a high efficiency solution for small scale grid-connected PV applications as an alternative to conventional parallel connected micro-inverters. Such a system will require MIC to MIC communications, will have between 4 to 8 cascaded MICs, contain a 1st order inductive filter and should have over-voltage protection capability.

Multilevel switching in such systems can offer significant switching frequency reduction capability, which justifies the additional timing complexity through a measureable increase in conversion efficiency. The final 4-MIC proposed decentralised cascaded system allows for both PV-module-level MPPT (without using high-gain boost converters) and a partial implementation of coordinated multilevel switching without the need for a centralised controller. These factors increase the total PV energy utilisation. Although, decentralised multilevel switching does come with the requirement of an infrequent/intermittent global communications link (<1Hz) between MICs, this can easily be achieved through means such as a wireless connection.

Chapter 2 dealt with the analysis of the practical decentralised cascaded multilevel system and determined the ideal number of cascaded MICs for grid voltages of 110Vrms and 230Vrms. This was done through consideration of existing MOSFET voltage-resistance ratios, film capacitor viability at different voltages, multilevel switching frequencies, partial shading resistance, DC-link voltage gain requirements and the increasing likelihood of faults with larger systems. This analysis was performed using both market data and analytical calculations.

After determining the system size, the decentralised modular nature of the cascaded grid filter was analysed. By developing equations to describe the grid current harmonics produced by a cascaded MIC, the frequency response of the grid filters were plotted and compared to show the effect of filter decentralisation as the system size increased. From this, a first order filter was identified as the best solution for the decentralised system. Finally, knowing both the system size and filter type, the MICs themselves were designed

based on the unique safety requirements of a decentralised system that relied on accurate series voltage balancing for successful operation.

Chapter 3 covered a detailed analysis made between MICs operating both in a parallel and decentralised 2-cascaded configuration, revealing the subtle differences between the expected and measured results due to decentralisation. This analysis was performed using both simulated and measured results from 200W MICs. After performing an overview of both hysteresis control and the hardware utilised, parameters were given for the parallel/cascaded comparison. Simulated filter designs for both systems were compared and discussed in the context of efficiency, switching frequency and losses. After the filters were selected, then the transient operations, harmonic current, switching frequency, efficiency and losses were analysed and compared between the parallel and 2-cascaded configurations in the context of decentralisation (simulated and measured). Finally, both the relative decentralised zero-crossing error and the power sharing ratio limits (and beyond) were explored for the 2-cascaded system using both analytical equations and measured results from the MIC prototypes.

Chapter 4 discussed the analysis and experimental verification of a simplified decentralised algorithm for multilevel cascaded MICs. The hybrid multilevel/shared region waveform concept was described, along with the concepts of the global/local MPPT operation and the greedy round robin power sorting algorithm that controls the entire process. Additionally, the MPPT partial shading limits of cascaded systems were analysed, along with the dynamic tradeoff between the MPPT speed and the global update rate. An 800W, 4-MIC prototype system was used to verify these concepts and analysis.

5.2 Summary of Key Findings

- The ideal system size for the decentralised cascaded multilevel system was found to be between 3 and 8 for a 110Vrms grid and between 4 and 10 for a 230Vrms grid. Therefore, the 4 MIC system size was chosen as it can function as an effective test platform for both voltage levels.

- The basic 1st order filter was compared with the 3rd order filter for modular distribution across cascade-connected MICs. It was found that as the inductance/capacitance of a 3rd order filter was spread across an increasing number of MICs, the unusable resonance point (and thus the ineffectiveness of the filter)

proportionally increased in frequency. It was concluded that the low switching frequency of multilevel control would result in an operating region resulting in the same harmonic current reduction for both 3rd and 1st order filters. Thus, 1st order filters should be selected for simplicity.

- Transitioning from the parallel to the decentralised 2-cascaded system increased the measured CEC efficiency from 94.8% to 95.9%, but also increased the full-load THD from 4.8% to 5.2%. The additional harmonic content was found to be due to minor voltage and current sensor mismatches between the MICs, which affected the current reference and the synchronisation of the zero-crossing detections between the cascaded MICs.
- The decentralised 2-cascaded MICs have a high sensitivity to the relative zero-crossing error between them. Analysis and experimental measurements showed that a zero-crossing difference between the two MICs of just 4° introduced harmonics that were equivalent to the limits of the grid standard utilised (5% THD). It was also found that increasing the MIC grid filter inductance by 550% only served to increase this zero-crossing error ceiling by about 50%.
- There is a calculable limit to the power distribution limits between the MICs themselves, which is controlled by the proportion of MICs that are shaded and the total-DC-link-to-grid-voltage over-rating ratio. It was found that when high proportions of MICs were shaded in the final 4-MIC MPPT prototype system (and very specific MIC power block configurations were required) the greedy round robin sorting algorithm struggled to allocate power near the calculated theoretical limits of what should be possible. It was found that (for an over-rating ratio of 1.14p.u.) a single MIC in the 4-MIC prototype system could be shaded by up to 74% (compared with a 78% theoretical limit) before the power utilisation of the other MIC's were affected.
- The final proposed decentralised system has a finite MPPT speed limit that is controlled by the allowable harmonic limit, the switching frequency, the shared region width and the global update rate of the system. For the worst case scenario (continuous maximum solar transients – 0.229W p.u. per second), it was found that the global update frequency needed to be at least 2.6Hz. For a more relaxed general

purpose scenario (continuous 0.1W p.u. per second solar transients), update rates of 0.7Hz were found to be plausible. Both cases allowed for a 50% switching frequency reduction compared with non-multilevel operation (vs. a 75% switching frequency reduction for high speed centralised multilevel operation). Depending on the definition of the THD in the grid standards utilised (specifically the averaging period), much lower update rates are feasible.

Future research in decentralised cascaded multilevel systems could focus on the balance between the MPPT speed and the harmonic limits given by the relevant standards. Firstly, a real world PV test of the harmonics produced by the system over a period of 1 to 3 months needs to be performed, primarily focussing on the number of harmonic excursions beyond the permitted grid limits. This would allow for a more realistic understanding of how far/fast the decentralised MPPT algorithm can be pushed. Following this, the MPPT algorithm would then be modified to dynamically adjust its power tracking performance (the central shared region width) in exchange for a more regulated harmonic content. Ultimately, the MPPT algorithm will need to sacrifice some PV energy during brief periods of rapid solar irradiance variation for automatic harmonic regulation to be possible.

6 Appendix

6.1 System Simulation

Final simulations of the cascaded multilevel grid-tied inverter were made using MATLAB (Simulink). The graphical mathematics based environment of MATLAB Simulink allowed for a greater degree of flexibility in comparison with the circuit simulator Multisim, which required models to be described by electrical components. This allowed for the simple execution of code and scripts, which provided programmability.

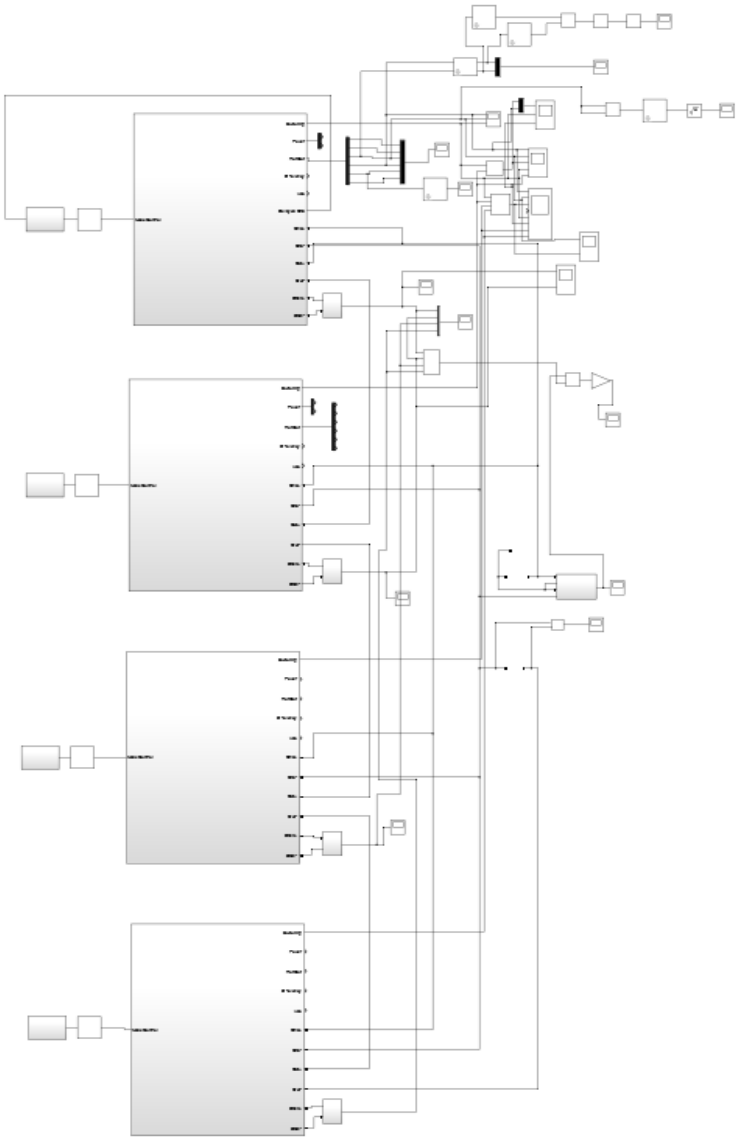

Fig. 6-1. The complete cascaded H-bridge MIC system in the Simulink environment. Each primary block represents one of the 4 MICs.

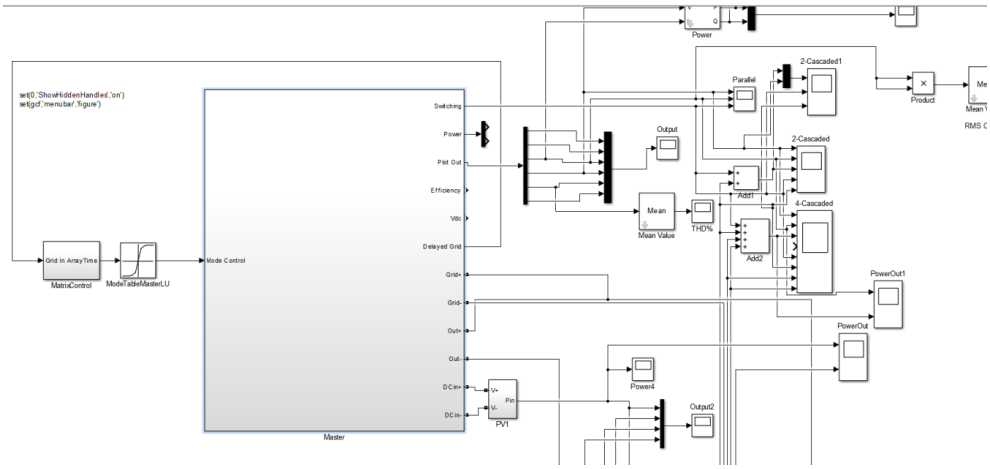

Fig. 6-2. A close up of one of the 4 Simulink MIC simulation blocks.

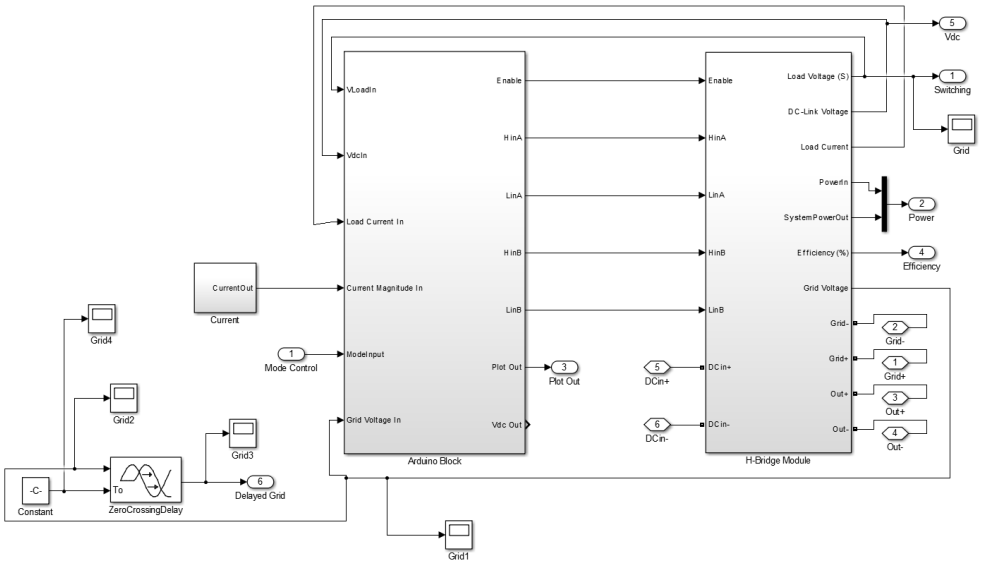

Fig. 6-3. Inside one of the Simulink MIC Simulation blocks. The two blocks seen are the "Arduino Block" (left - Representing the µController operations) and the "H-Bridge Module" block (right – Representing the power stage of the MIC).

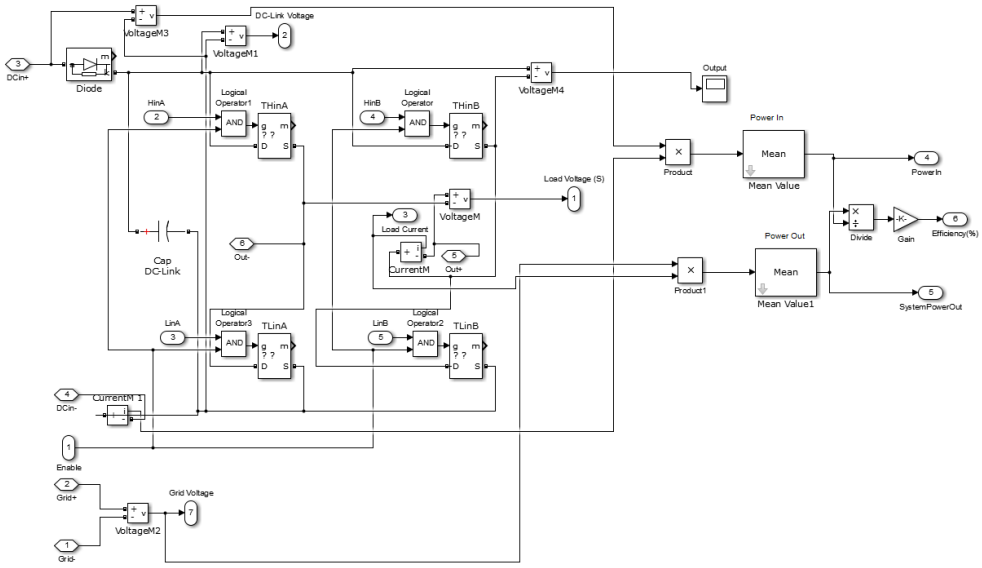

Fig. 6-4. A view of the contents of the "H-Bridge Module" block.

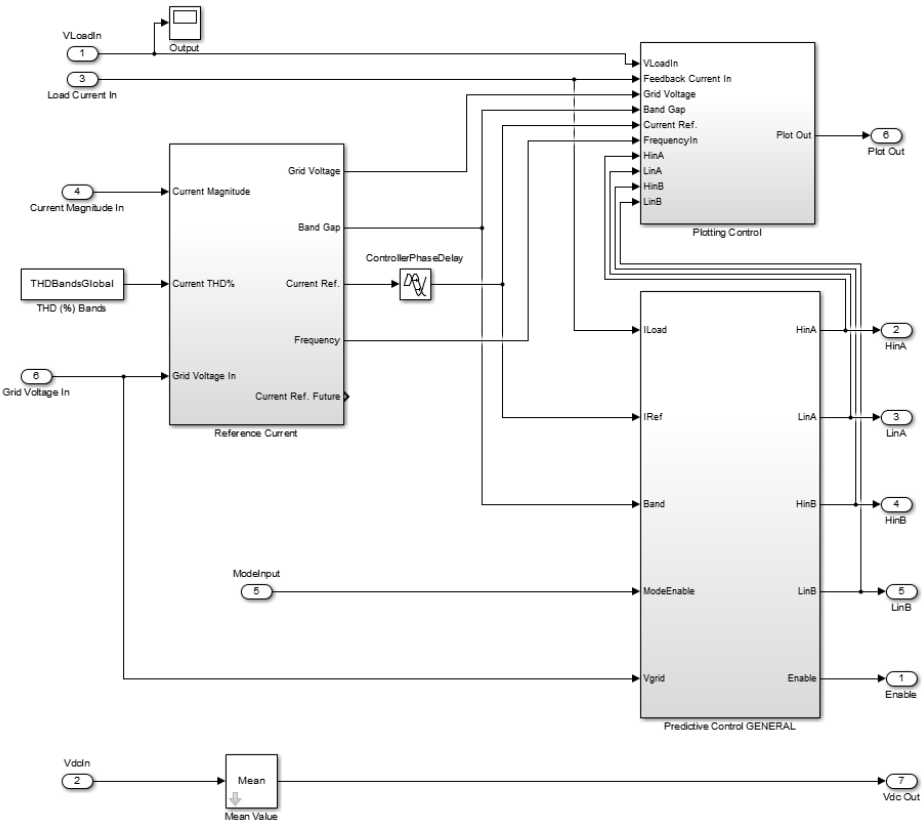

Fig. 6-5. A view of the contents of the "Arduino" block. Seen are the blocks responsible for the reference current generation (top left), plotting generation (top right) and the overall control of the MIC (bottom right).

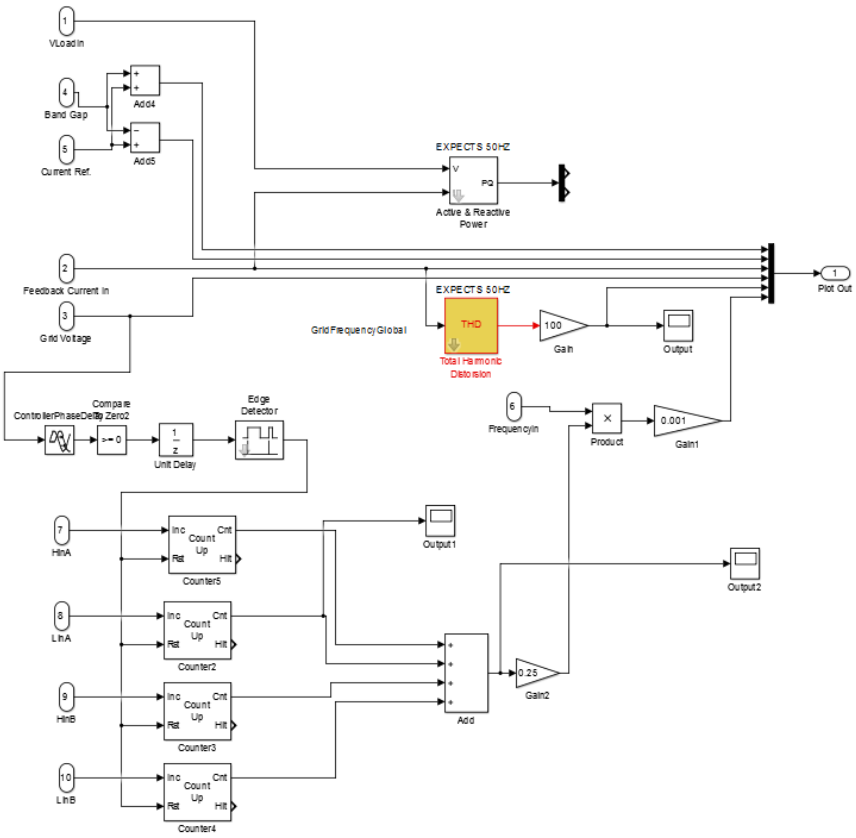

Fig. 6-6. A view inside the block responsible for the generation of the plotted waveforms (i.e. current voltage, total harmonic distortion, etc.).

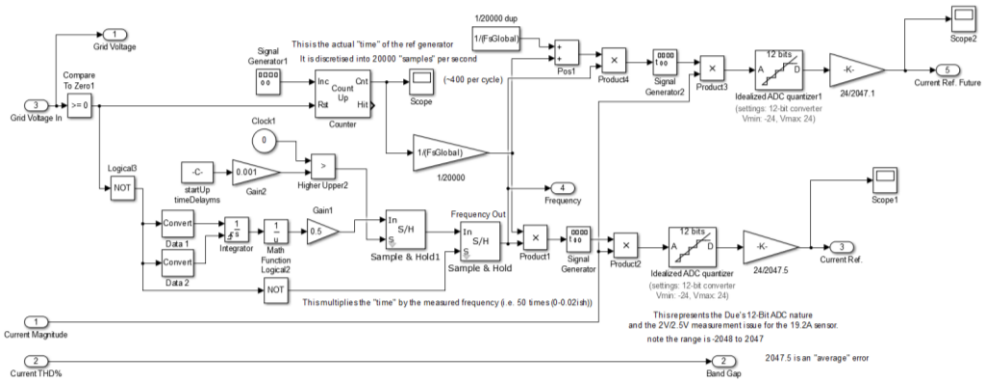

Fig. 6-7. A view inside the block responsible for the reference current generation. This block generates a grid synchronised sinusoidal waveform that is equivalent to the desired current waveform.

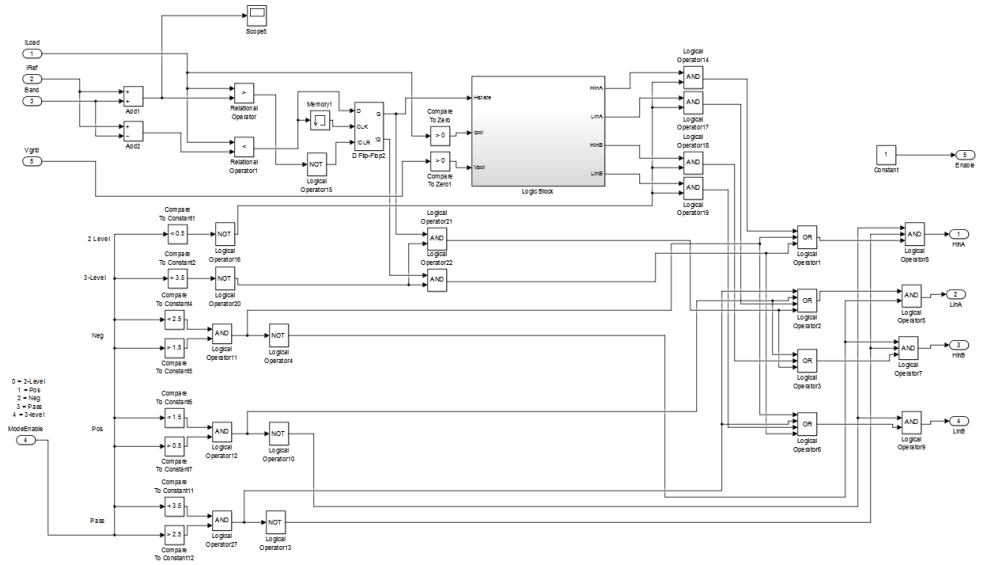

Fig. 6-8. A view inside the block responsible for the general control of the MIC. This block is responsible for hysteresis control, multilevel mode select and generally selecting which transistor to turn on/off in the "H-Bridge Module" according to current reference and power requirements. This block also contains another block called the "Logic Block", responsible for final transistor selection.

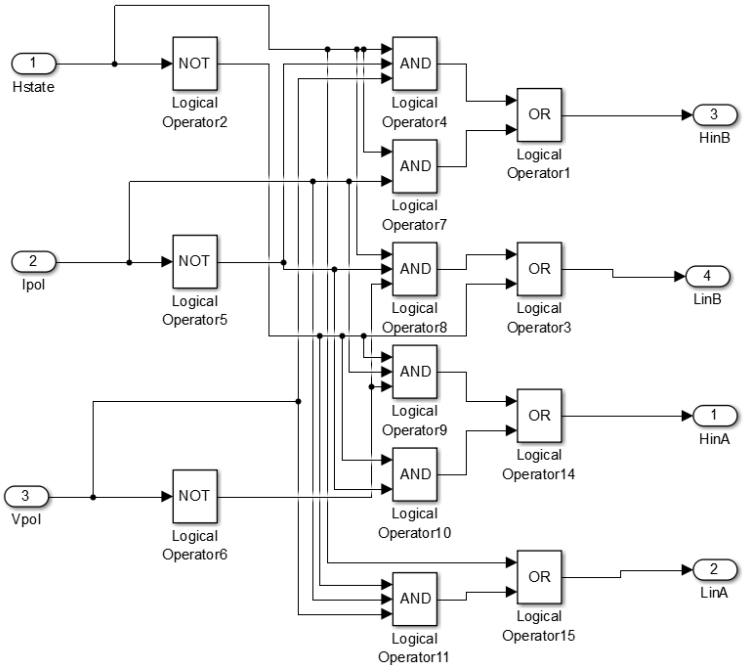

Fig. 6-9. The inside view of the "Logic Block", which takes information regarding an increase/decrease requirement for the current and then used digital logic to find the combinations of transistors required to achieve the desired change in current.

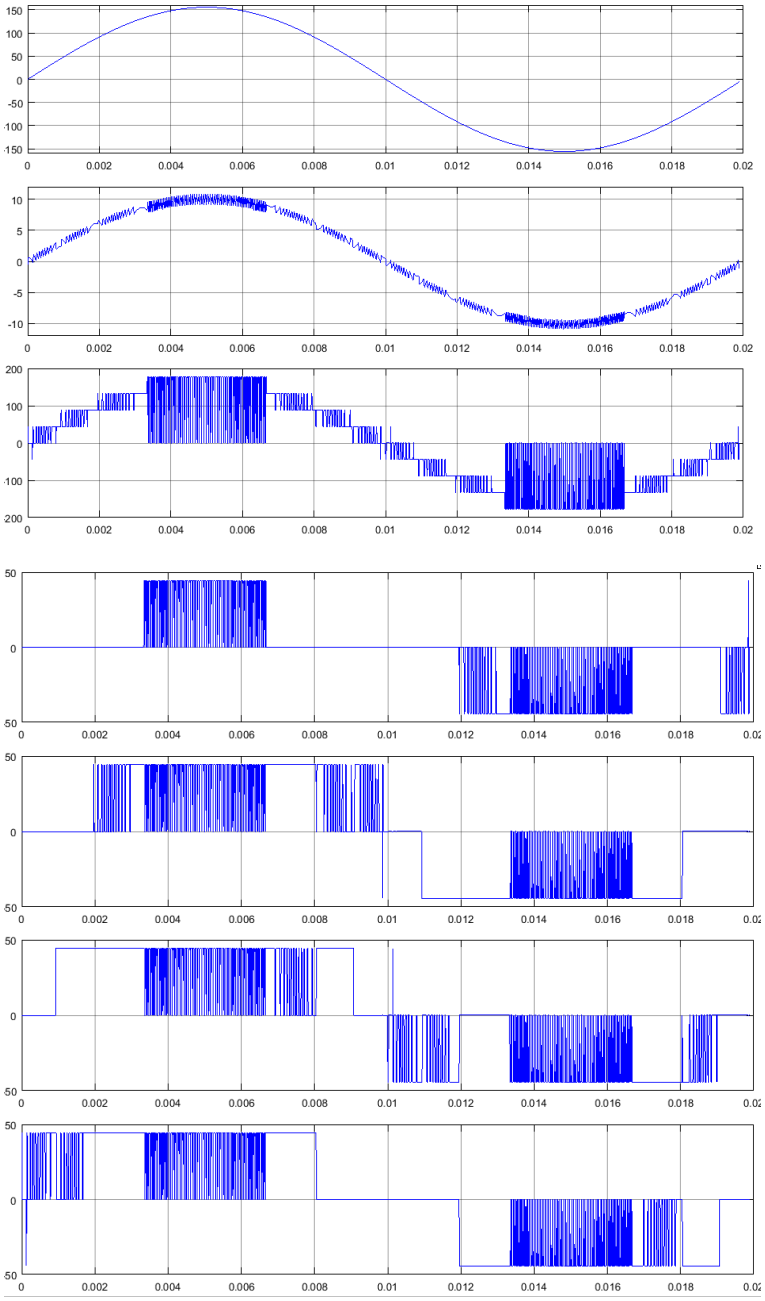

Fig. 6-10. An example of the simulation in operation. From top to bottom: The grid voltage, grid current, system total voltage and the output voltage of MICs 1-4.

The Simulink simulation allows for MATLAB scripts to be implemented before the Simulink portion of the simulation is initialised. This allows for instant reconfigurations of the simulation according to pre-programmed settings. Below is the MATLAB script to setup the Simulink simulation to the most common configuration utilised.

```
%Setup file for the simulation.
clear all
clc

%TEST VARIABLES
MagnitudeReduction = 0;%The proportion of the currentRefMagnitude to be removed.
TimeReduction = 0;%The time at which this occurs.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
MasterZeroCrossingPhaseDelay = 0; %This is proper zero crossing delay! USE THIS!!!! (MASTER
ONLY) PHASE IN DEGREES!
ControllerPhaseDelayMaster = 0; %Not used here, see 2-level.
ControllerPhaseDelaySlave1 = 0; %Not used here, see 2-level.
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%SETUP VARIABLES
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
NoModules = 4;
InOutPowerPercent = 100;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
PowerPVMax = 420;
VoltagePVMax = 45;
CurrentPVGlobal = (PowerPVMax*0.01*InOutPowerPercent)/VoltagePVMax;
VoltagePVGlobal = VoltagePVMax;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
GridFrequencyGlobal = 50;
GridPeakGlobal = 155.56%13.5*sqrt(2)*8;
RGlobal = 0.074*2;
LGlobal = 0.000330*2;
DCLinkCGlobal = 18.28e-3;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
FsGlobal = 200000;
MasterR = 0.0025;
Slave1R = 0.0025;
Slave2R = 0.0025;
Slave3R = 0.0025;
SnubberC = 10*10^(-9);
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
powerOutMax = 200*NoModules;
currentRefMagnitude = (((InOutPowerPercent*0.01)*powerOutMax)/(GridPeakGlobal))*2.0;
currentRefMagnitudeMaster = currentRefMagnitude;
currentRefMagnitudeSlave1 = currentRefMagnitude;
currentRefMagnitudeSlave2 = currentRefMagnitude;
currentRefMagnitudeSlave3 = currentRefMagnitude;
THDBandsGlobal = (powerOutMax/GridPeakGlobal)*2.0*0.05;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
ArrayLength = round(FsGlobal/50);
ModeTableMaster = zeros(1,ArrayLength);
ModeTableSlave1 = zeros(1,ArrayLength);
ModeTableSlave2 = zeros(1,ArrayLength);
ModeTableSlave3 = zeros(1,ArrayLength);
PointTable = zeros(1,16);

n = 1;
while (n <= ArrayLength)
ModeTableMaster(1,n) = 3;
ModeTableSlave1(1,n) = 3;
ModeTableSlave2(1,n) = 3;
ModeTableSlave3(1,n) = 3;
n = n + 1 ;
end
```

```
% Guess = asin(VoltagePVGlobal/GridPeakGlobal);
% Vr = currentRefMagnitude*RGlobal*sin(Guess);
% Vl = LGlobal*currentRefMagnitude*2*pi*GridFrequencyGlobal*cos(Guess);
% SwitchPoint = asin((VoltagePVGlobal-Vr-Vl)/(GridPeakGlobal));
% PointTable(1) = round((SwitchPoint*ArrayLength)/(2*pi));
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
PointTable(1) = round((asin(VoltagePVGlobal/GridPeakGlobal))*((ArrayLength/2)/pi));
PointTable(2) = round((asin(2*VoltagePVGlobal/GridPeakGlobal))*((ArrayLength/2)/pi));
PointTable(3) = round((asin(3*VoltagePVGlobal/GridPeakGlobal))*((ArrayLength/2)/pi));
PointTable(4) = ArrayLength/4;
PointTable(5) = ArrayLength/2-PointTable(3)+5;%CORRECTION APPLIED
PointTable(6) = ArrayLength/2-PointTable(2)+4;%CORRECTION APPLIED
PointTable(7) = ArrayLength/2-PointTable(1)+3;%CORRECTION APPLIED
PointTable(8) = ArrayLength/2;
PointTable(9) = PointTable(1) + ArrayLength/2;
PointTable(10) = PointTable(2) + ArrayLength/2;
PointTable(11) = PointTable(3) + ArrayLength/2;
PointTable(12) = PointTable(4) + ArrayLength/2;
PointTable(13) = PointTable(5) + ArrayLength/2;
PointTable(14) = PointTable(6) + ArrayLength/2;
PointTable(15) = PointTable(7) + ArrayLength/2;
PointTable(16) = ArrayLength;
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

n = 1;
while (n < PointTable(1))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 3;
    ModeTableSlave2(1,n) = 3;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(2))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 3;
    ModeTableSlave2(1,n) = 1;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(3))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 1;
    ModeTableSlave3(1,n) = 1;
n = n + 1 ;
end
while (n < PointTable(4))
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(5))
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(6))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 1;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 1;
n = n + 1 ;
end
while (n < PointTable(7))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 1;
    ModeTableSlave3(1,n) = 3;
```

```
n = n + 1 ;
end
while (n < PointTable(8))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 3;
    ModeTableSlave3(1,n) = 3;
n = n + 1 ;
end
while (n < PointTable(9))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 3;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 3;
n = n + 1 ;
end
while (n < PointTable(10))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 2;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 3;
n = n + 1 ;
end
while (n < PointTable(11))
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 2;
    ModeTableSlave2(1,n) = 3;
    ModeTableSlave3(1,n) = 2;
n = n + 1 ;
end
while (n < PointTable(12))
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(13))    %%%%
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 4;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(14))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 2;
    ModeTableSlave2(1,n) = 2;
    ModeTableSlave3(1,n) = 4;
n = n + 1 ;
end
while (n < PointTable(15))
    ModeTableMaster(1,n) = 3;
    ModeTableSlave1(1,n) = 3;
    ModeTableSlave2(1,n) = 4;
    ModeTableSlave3(1,n) = 2;
n = n + 1 ;
end
while (n < PointTable(16))
    ModeTableMaster(1,n) = 4;
    ModeTableSlave1(1,n) = 3;
    ModeTableSlave2(1,n) = 3;
    ModeTableSlave3(1,n) = 3;
n = n + 1 ;
end

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
display(PointTable)
display('Ready to make curvey lines!')
```

6.2 Circuit Schematics

6.2.1 MIC Schematic

The following are some circuit schematic captures from Altium Summer 09 of the MIC power stage (H-bridge). These schematics are difficult to capture and as such, non-essential elements such as snubber circuits and many bypass capacitors could not be fitted in the selected pictures. In order, we see the actual H-bridge, the gate driving circuitry, the dead time control, the DC-link over voltage protection and an example of one of the voltage measurement circuits (grid voltage). In addition to these circuits, there are many other basic circuits not shown that make use of complete integrated packages for power supplies (i.e. linear 5V regulators, isolated proportional switching regulators and complete isolated dual supply modules that perform all the difficult tasks of power conversion). Though incomplete, these images give a feel to the process behind the MIC design. Regardless of the quality, Fig. 6-16 does show the entire circuit in its entirety. It should be noted that some component values have since changed (i.e. the gate driving resistors, etc.)

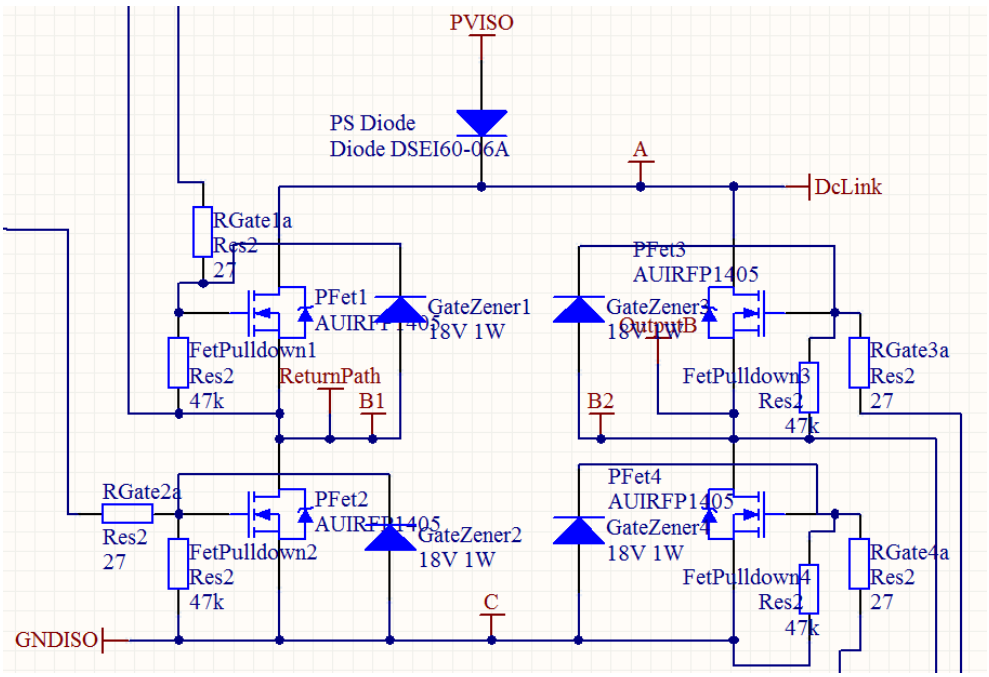

Fig. 6-11. The final output stage of the H-bridge module. Zeners are used to help protect the MOSFET gates from over voltage conditions. DC-link capacitors and MOSFET snubbers not shown.

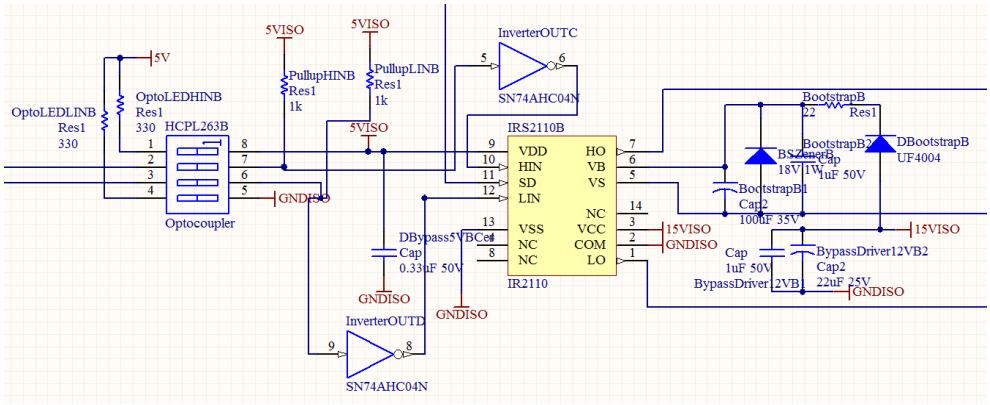

Fig. 6-12. A close up of one of the MOSFET gate driving circuits (a half bridge driver). The IR2110 drivers are not isolated and so opto-couplers must be used.

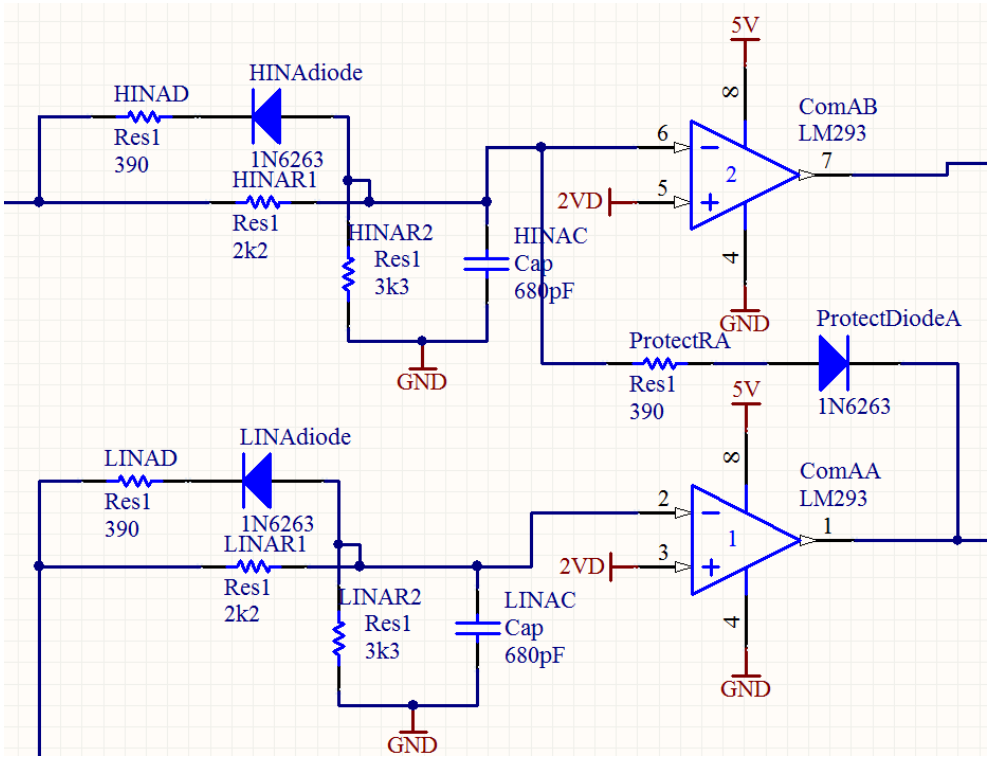

Fig. 6-13. A close up of one of the pairs of dead time logic blocks. The capacitor takes longer to charge during the transition to the on state than to the off state. The diode on the right serves to prevent both comparators (open collector) from being low at the same time.

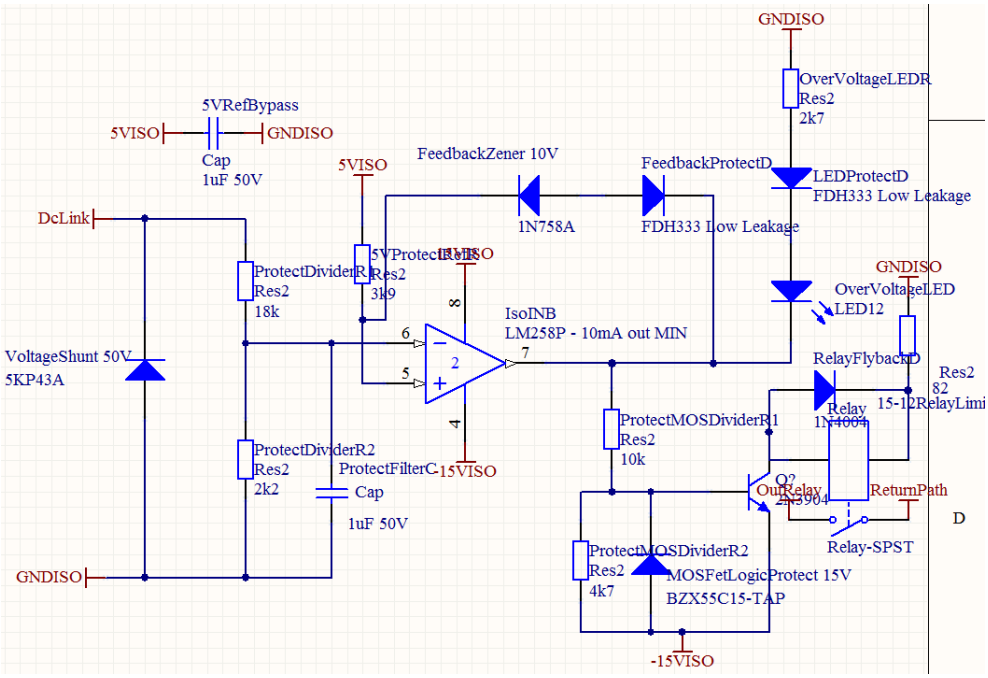

Fig. 6-14. A close up of the DC-link over voltage protection relay control circuit. If the specified voltage (R divider) is exceeded for more than the specified time (RC filter), then the op-amp output will latch high and keep the output relay off until logic power is removed from the circuit.

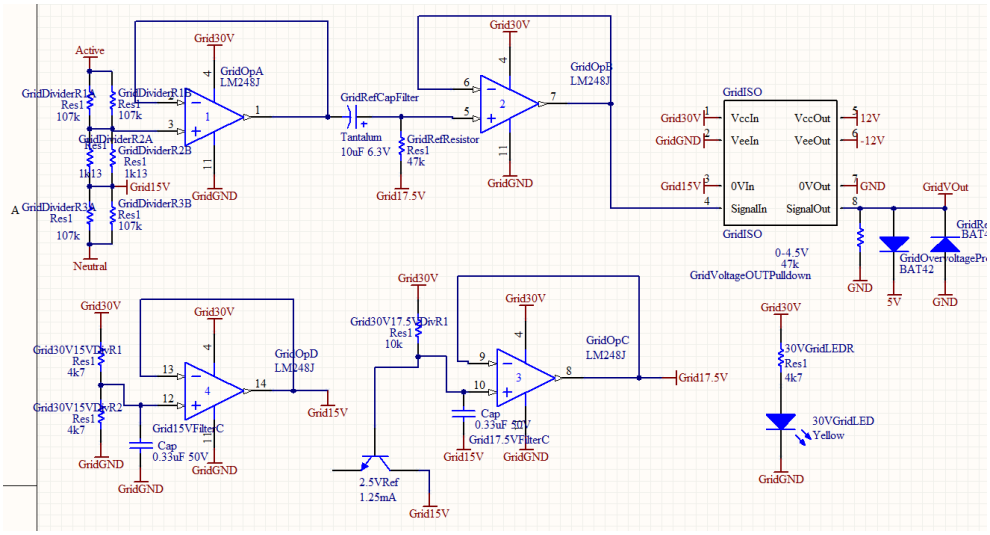

Fig. 6-15. A close up of the grid voltage measurement circuit. This circuit uses a single quad package op-amp to process the signal and prepare it for the isolation amplifier. Critically, a precision voltage reference is used to set the new bias point for the signal to 2.5V.

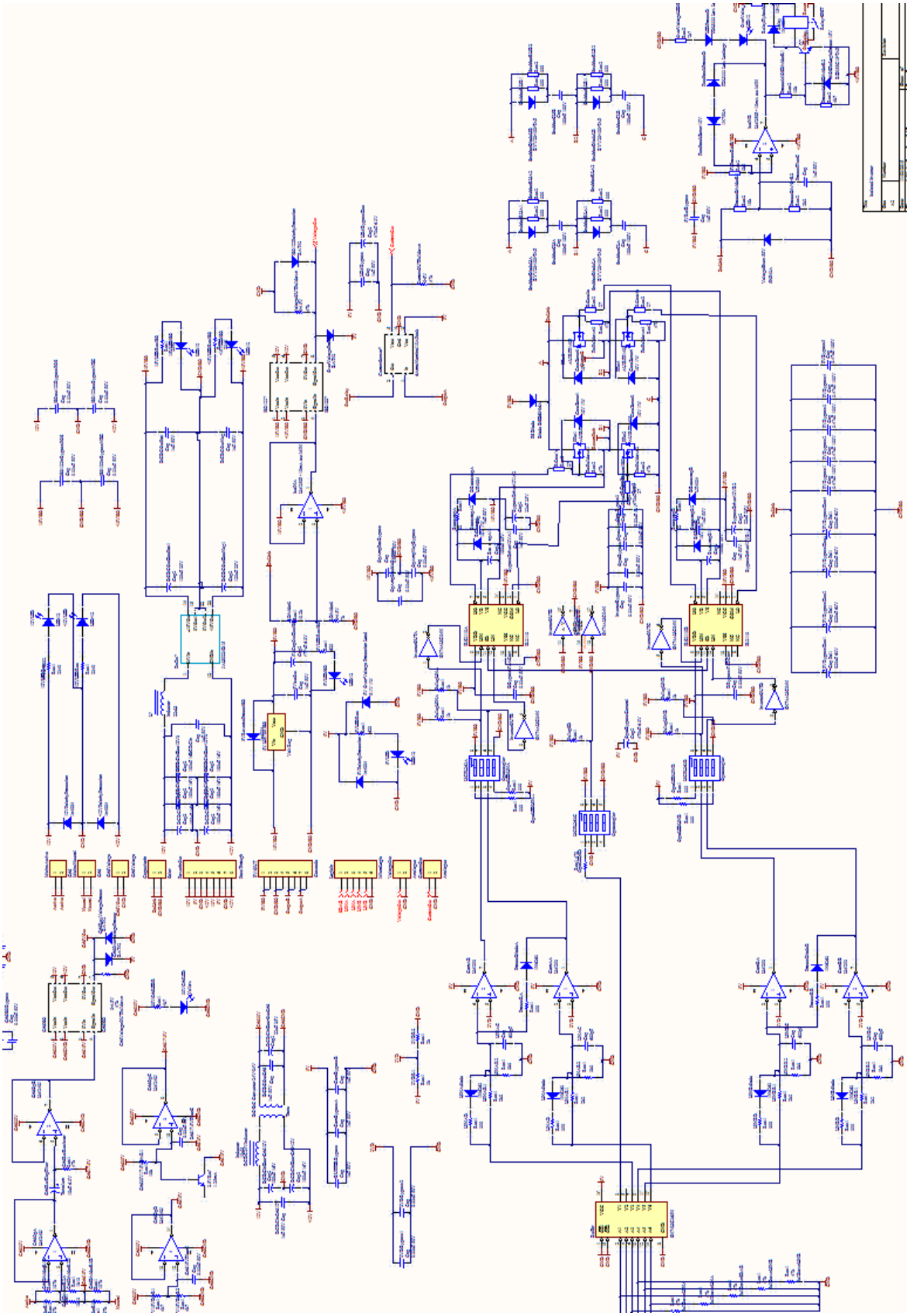

Fig. 6-16. The entire MIC H-bridge circuit schematic as seen in Altium Summer 09.

6.2.2 3.3V – 5V Converter

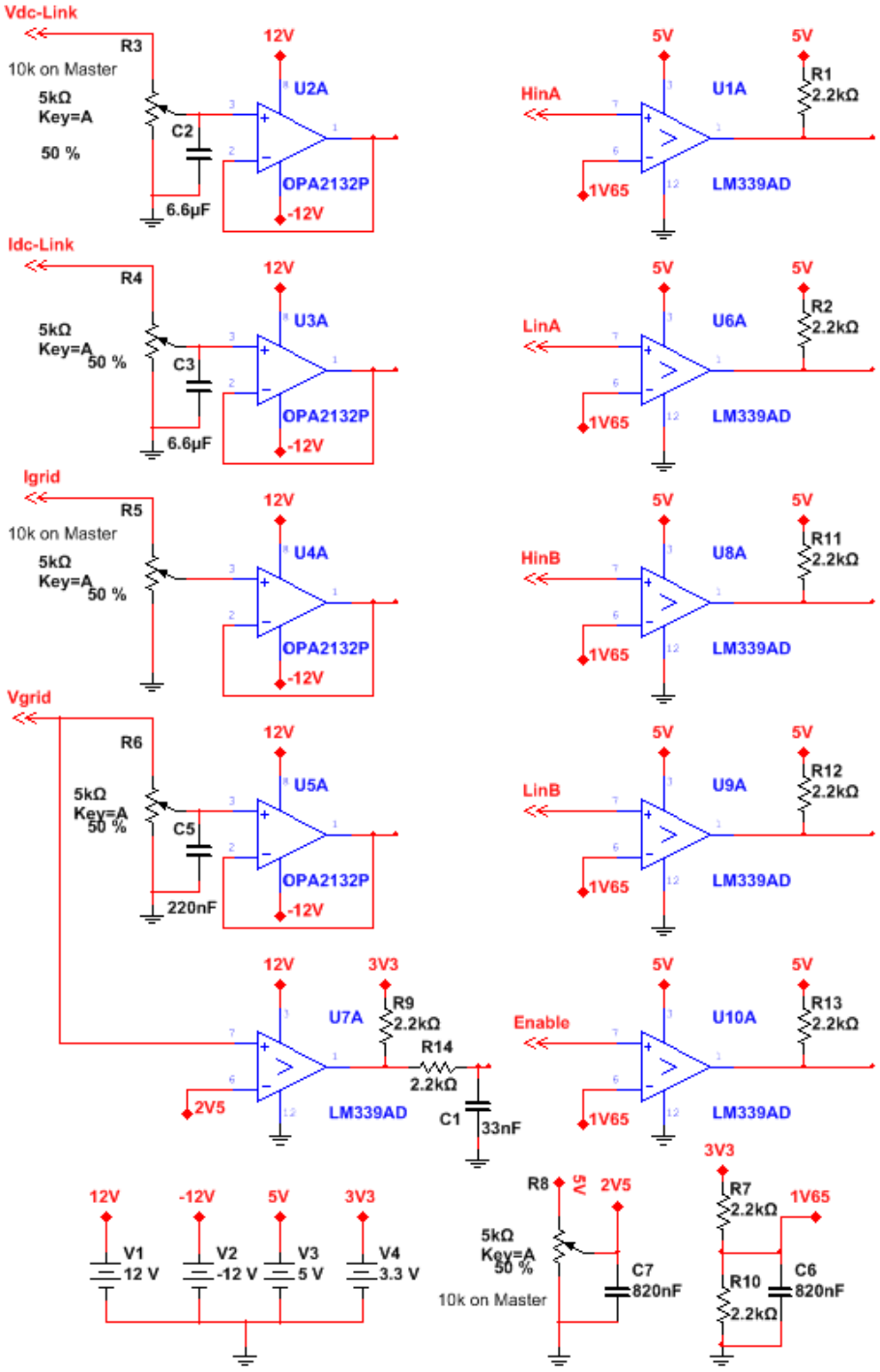

Fig. 6-17. The circuit schematic for the final 3.3V to 5V converter module to interface the MIC H-bridge PCB with the SAM3X8E µController board. In addition to zero-crossing detection, this circuit allows for digital signals to transition from 3.3V to 5V (µC to H-bridge) and for analogue signals to transition from 5V to 3.3V (H-bridge to µC).

6.3 Circuit PCB Layout

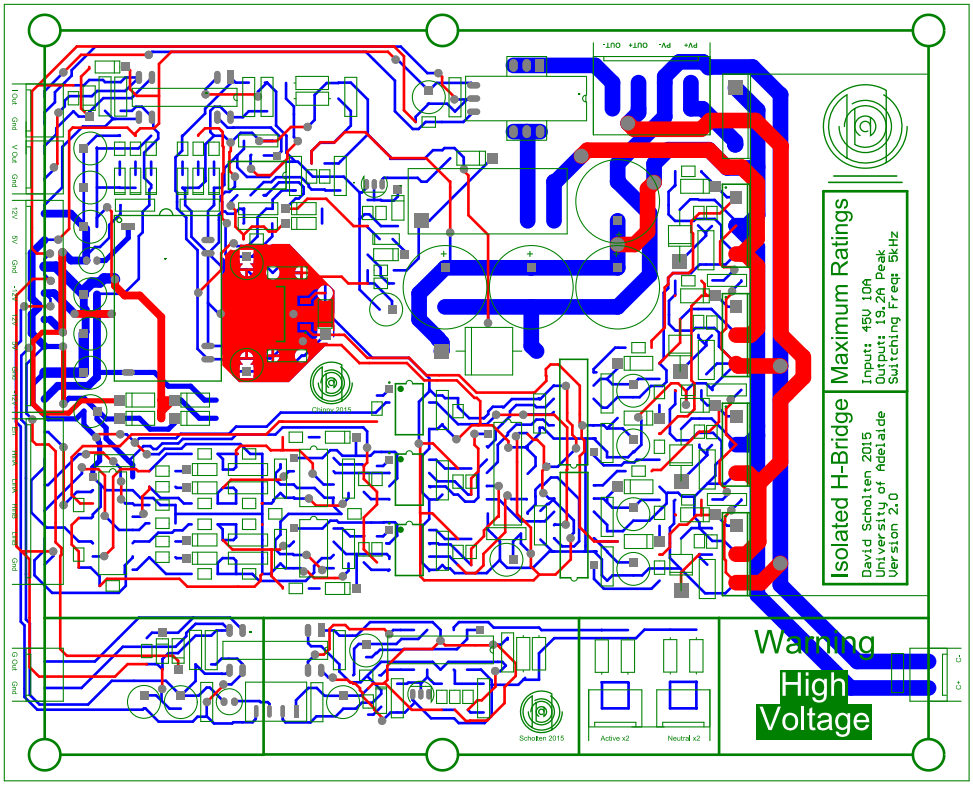

Fig. 6-18. Final MIC H-bridge PCB layout from Altium Summer 09.

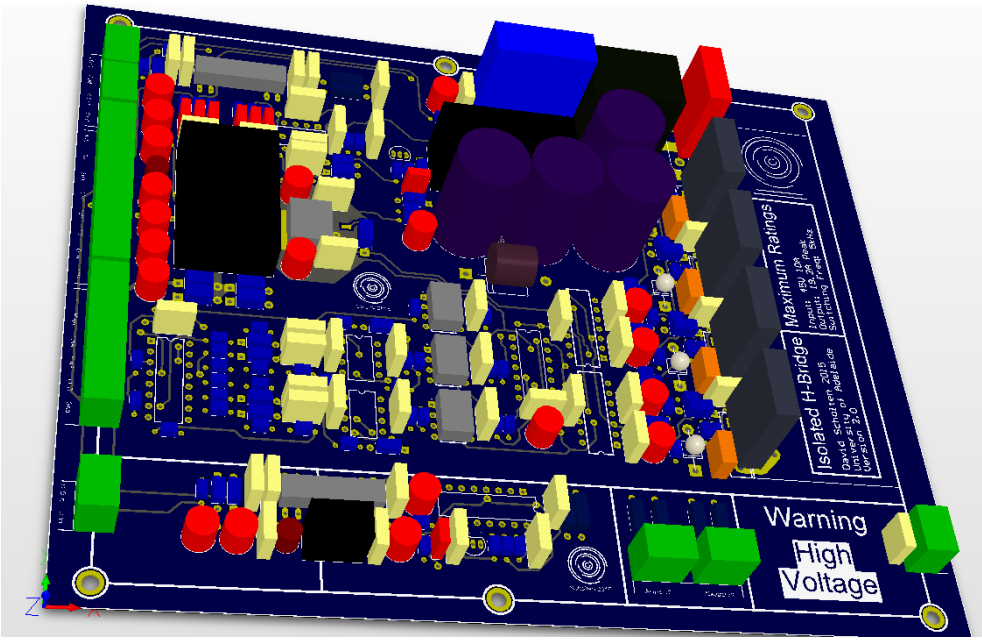

Fig. 6-19. 3D render of the final MIC H-bridge PCB layout.

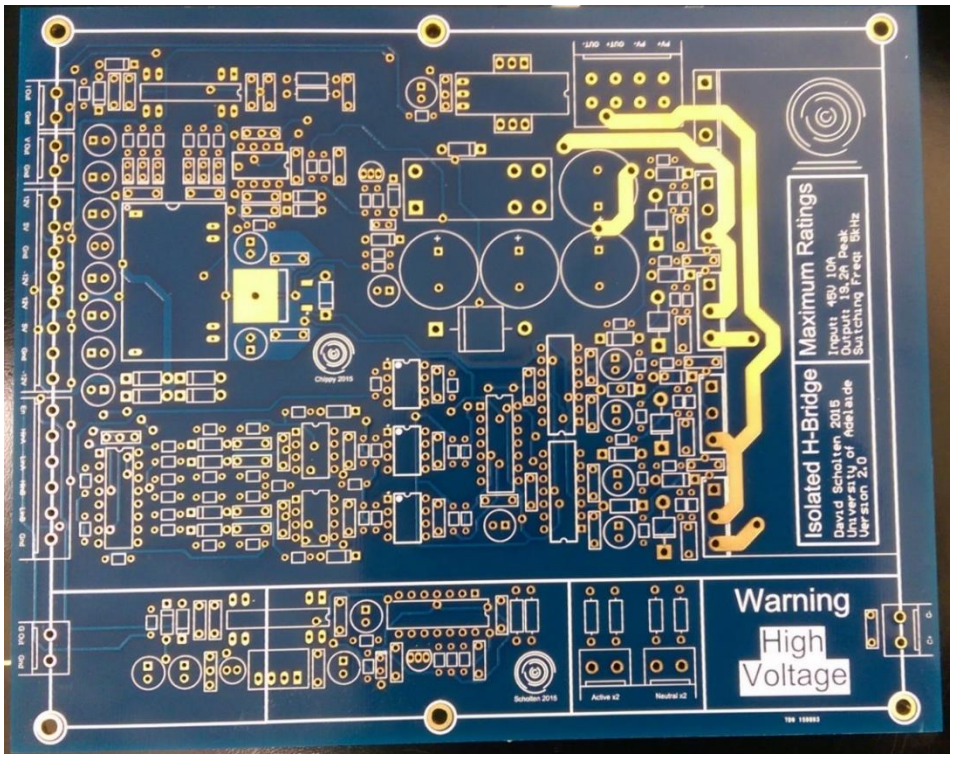

Fig. 6-20. MIC H-bridge PCB manufactured by Seeed Studio (top side).

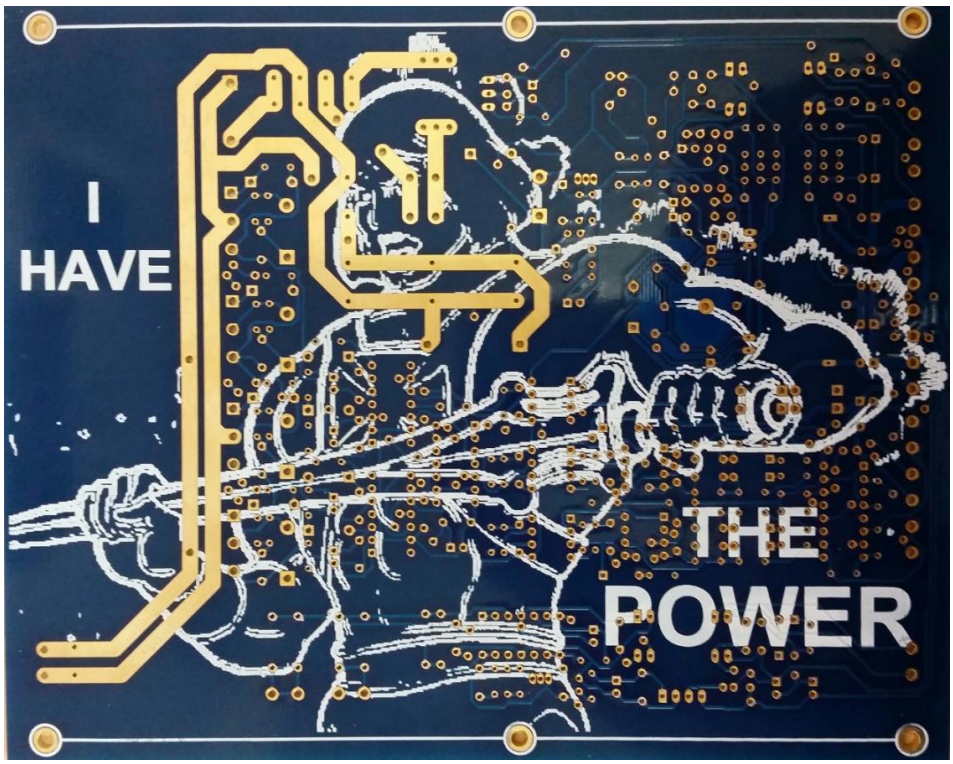

Fig. 6-21. MIC H-bridge PCB manufactured by Seeed Studio (bottom side).

Fig. 6-22. Two completed MIC H-bridge PCBs undergoing testing.

Table 6-1. The initial specifications of the H-bridge power module. Some values (such as the switching time and DC-link/snubber capacitance) have varied with the different phases of research.

Specification	Designed/Rated Value	Measured Value
Max. Input Voltage (V_{in})	42V	44V
Max. Input Current (I_{in})	9.6A	15A
Max. Output Current Peak (i_{out})	19.2A Peak	19.2A Peak
Max. Switching Frequency (f_{sw})	5kHz	9.5kHz
DC-Link PV Diode Voltage Drop ($V_{D_{PV}}$)	0.8V	0.773V
DC-Link Capacitance	3.3mF	2.624mF
Capacitor Breakdown Voltage	63V	N/A
DC-Link Over Voltage Protection Threshold (Transient Diode)	45V	50V
DC-Link Over Voltage Protection Threshold (Delayed Relay Disconnect)	45V	46.6V
MOSFET Gate Supply	15V	14.5V
MOSFET Gate Resistor	27Ω	27 Ω
MOSFET Gate Charge	300nC	N/A
MOSFET Snubber Capacitor ($C_{snubber}$)	100nF	90nF
MOSFET Breakdown Voltage	60V	N/A
MOSFET Parallel Balancing Resistance	10kΩ	9kΩ
MOSFET On-State Resistance ($R_{DS_{on}}$)	2.5mΩ	2.61mΩ
MOSFET Body Diode Voltage ($V_{BD_{MOS}}$)	0.8V	0.7V
MOSFET Body Diode Reverse Charge ($Q_{D_{MOS}}$)	70nC	N/A
MOSFET Switching Time ($T_{rise/fall}$)	540ns	500ns
MOSFET True Dead Time (T_{dead})	1060ns	10ns
MOSFET Total Transition Time (T_{trans})	$2 * T_{rise/fall} + T_{dead} = 2140ns$	1010ns
MOSFET Duty Cycle Max (D_{max}) *This is the maximum duty cycle that can occur before the negative pulse in the switching waveform is eliminated due to dead & switching time constraints.	$1 - (2 * T_{trans} * f_{sw}) = 0.9786$	0.995

During general operation of the H-bridge power module it was found that all the safety circuits worked as intended (overvoltage, reverse voltage, invalid logic states, relay disconnect, etc.) and all sensor measurements (bar one faulty component) functioned without troubleshooting. During assembly, the safety circuitry actual protected the module from damage several times due to user error. It should be noted that in general, the final H-bridge module was successful in what it sought to achieve.

Table 6-2. Some sample losses calculations and corresponding lab measurements for the H-bridge power module undergoing some basic testing with an inductive load.

Power Losses @ Max. Spec. PV DC IN: 42V, 9.6A, 403.2W AC OUT: 19.2A peak @ 5kHz	Calculated Losses	Measured Losses
PV Diode Loss	$V_{D_{PV}} * I_{in} = \mathbf{7.68W}$	**7.42W**
Switching Loss	$2 * T_{rise/fall} * f_{sw} * \left[\frac{i_{out}}{\sqrt{2}}\right] * V_{in} * \frac{1}{2} * 4 = \mathbf{6.15W}$ *Where 1/2 is derived from the integrated energy under the ideal *inductive* switching waveform. $\int_0^{T_{rise/fall}} p(t)\,dt = \frac{1}{2} * T_{rise/fall}$	N/A
On-State Conduction Loss	$R_{DS_{on}} * \left[\frac{i_{out}}{\sqrt{2}}\right]^2 * D_{max} * 2 = \mathbf{0.90W}$	**0.96W**
Snubber Loss $C_{snubber} = 100nF$	$\frac{1}{2} * C_{snubber} * (V_{in})^2 * f_{sw} * 4 = \mathbf{1.76W}$	**1.584W**
MOSFET Body Diode Conduction Loss	$T_{dead} * f_{sw} * \left[\frac{i_{out}}{\sqrt{2}}\right] * V_{BD_{MOS}} * 4 = \mathbf{0.23W}$	**0.095W**
MOSFET Shoot-Through Losses	No Loss: **0W**	**2.15W**
MOSFET Body Diode Reverse Recovery Loss $Q_{D_{MOS}} = 70nC$	$f_{sw} * Q_{D_{MOS}} * V_{in} * 4 = \mathbf{0.06W}$	N/A
Logic Losses (Gate Drivers, DC/DC Converters, etc.)	Approximately **5W**	**3.42W**

Table 6-2 shows that, the switching and losses (>6W) were comparable with the PV diode losses (>7W). These significant losses were due to the on-board input diode (an unnecessary feature) and the long switching/dead times, which were chosen to reduce di/dt noise and eliminate shoot through respectively. However, upon measurement, it was found that little dead time actually existed and partial shoot through was occurring. The dead time delay was (technically) working correctly, but the asymmetry of the MOSFET's gate turn off/on point (>4V) compared with the final gate voltage (15V) meant that the MOSFETs reacted much more quickly to the "on" command than the "off" command

(asymmetrical latency or "reverse" dead time). This effectively resulted in a cancelling of the dead time in the final hardware. Fortunately, only minimal overlap occurred, which resulted in partial shoot through of 2.15W (@5kHz). The other major effect of the minimal dead time in the final measured hardware was an approximate 50% (0.23W → 0.095W) decrease in the body diode conduction losses (vs. calculated), which was due to the faster switching interval overall.

Reverse recovery losses (60mW estimate) and on-state conduction losses (0.96W) were as expected, as were the snubber losses (1.58W). The snubber losses were as large as they were in order to reduce any spikes on the DC-link that may have inadvertently triggered the over voltage protection circuit. Even larger though were the logic losses (3.42W), which were actually lower than the calculated expected (5W). It should be noted here that logic/gate power was derived from power supplies separate from that of the input power to the H-bridge and that any logic/gate power was considered a loss.

Although significant, all of these losses are considered par for the course as the main goal for the H-bridge module was capability, safety, serviceability and a rugged resilience to faults (i.e. an experimental platform).

Table 6-3. Full bill of materials list for the final MIC H-bridge PCB population.

Qty.	Part No	Order Code
13	N/A	3041440 (Terminal Headers 5.08mm Pin Spacing)
1	JAH0224D15	1859094 (24V to +-15V Isolated DC-DC Converter)
2	ISO122PE4	1178433 (Isolation Amplifier)
3	HCPL2631	1495381 (Dual Optocoupler)
1	0256-0404	1311526 (High Current PV and AC Output Terminal Block 4 Pos)
12	MFR3 330R FC	1565304 (Opto Coupler LED & Snubber Resistor 330 Ohm 400mW)
13	MFR3 47K FC	1565317 (47k Pull Down Resistor)
4	IRFP3006PBF	2456721 (0.0025 Ohm, 60V, TO-247 MOSFET, 200-300nC)
2	IRS2110PBF	1271795 (MOSFET Driver)
1	11R223C	2062673 (22uH Inductor)
2	UF4004	1467502 (Ultra Fast Bootstrap Diode)
6	1N4004	1467510 (1A General Diode)
1	LTS 6-NP	2146860 (Current Transducer)
1	L7805ABD2T-TR	1366571 (LM7805 Surface Mount)
4	BAT42	9801430 (Schottky Diode 200mA 0.4Vf 30V)
2	FDH333	9843760 (Low Leakage Diode (3nA @ 25C) 0.8-0.9Vf)
5	L-113IDT	2314275 (Red LED)
1	DSEI60-02A	1427261 (Power Diode 200V 69A Vf=0.88 @ 20A TO-247)
2	L-113GDT	2314276 (Green LED)
2	MFR3 680R FC	1565326 (LED Green Resistor 5V 680 Ohms)
5	MFR3 2K7 FC	1565302 (LED Red Resistor 12V/15V 2k7 Ohms)
1	RC55Y 18K2 0.1%	9500642 (18.2KOhm 0.1% Resistor Measurement)
1	RC55Y 2K 0.1%	9501479 (2KOhm 0.1% Resistor Measurement)
5	MFR3 1K FC	1565287 (1k Ohm Opto-Coupler Pullup Resistor)
1	MC33078PG	9664980 (16MHz, 7V/us Op-Amp min 10V swing, min 15mA @ 10V)
4	6SEPC470ME	2354637 (5V Bypass Electrolytic 470uF 0.02 Ohm D6.3mm H7mm 6.3V)
8	16SEPF180M	2354647 (12V Bypass Electrolytic 180uF 0.022Ohm D6.3mm H6mm 16V)
4	20SEPF120M	2354650 (15V Bypass Electrolytic 120uF 0.022Ohm D6.3mm H6mm 20V)
2	MFR3 22R FC	1565296 (22Ohm Bootstrap Resistor 0.4W)
2	25SEPF56M	2354657 (Bootstrap Electrolytic (25V, 56uF 0.022Ohm D6.3mm H6mm 25V)
6	1N4746A,113	1826119 (Zener MOSFET Gate & Bootstrap Protection 18V 1W)
2	LM293P	2292956 (Dead Time Comparator LM293)
8	MFR3 2K2 FC	1565301 (Dead Time Divider Resistor 2k2 Ohm 400mW)
5	MFR3 3K3 FC	1565313 (Dead Time Divider Resistor 3k3 Ohm 400mW)
1	MFR3 470R FC	1565316 (OPTO ENABLE Diode resistor 470 Ohm 400mW)
6	MFR3 390R FC	1565309 (Dead Time Capacitor Discharge 390 Ohm 400mW)
4	MFR3 27R FC	1565300 (MOSFET Gate Resistor 27 Ohm 400mW)

4	K681J15C0GF5TH5	3327450 (Dead Time Capacitor 680pF 50V)
1	1C20C0G102J050B	1793652 (Protect Ref Filter 1nF 50V)
6	1N6263	9801251 (Dead Time Discharge RF UF Schottky Diode 0.41Vf 15mAf 60V)
1	CD74AC04E	1102987 (INVERTER Gate 24mA Per Channel)
1	CD74HCT365E	1739589 (Input Buffer Non-Inverting Gate 25mA Per Channel)
4	BYV28-100-TAP	1612307 (Snubber Diode 30ns Recovery 3.5Aavg Ap rep is 25A)
4	C322C104K1R5TA	1457685 (Snubber Cap X7R 0.1uF 100V 0.318mm Thickness)
4	EEUFR1J821	2079312 (63V PV Bypass Electrolytic 820uF 0.024 Ohm D16mm H25mm)
2	MC0805N152J500A5.08MM	1694206 (1.5nF Cap Analogue Sensor Filter 50V)
1	MFR3 18K FC	1565285 (Protect Divider Resistor 18k Ohm 400mW)
1	MFR3 3K9 FC	1565314 (Protect 5V Ref Resistor 3k9 Ohm 400mW)
2	MFR3 10K FC	1565271 (MOSFET Gate Divider 10k Ohm 400mW)
4	MFR3 4K7 FC	1565318 (MOSFET Gate Divider 4k7 Ohm 400mW)
1	2N7000	9845178 (Voltage Protect MOSFET Switch 200mA 60Vds)
1	1N758A	1861492 (10V Zener Overvoltage Reverse Feedback)
1	BZX55C15-TAP	1779207 (15V Zener Logic 2N7000 GS Protect)
1	5KP43A	1677439 (Over Voltage Protection SHUNT)
1	MFR3 100R FC	1565270 (Relay Current Limiter 100 Ohm 400mW)
1	RTD34012F	1136821 (Voltage Protect RELAY 12V 360 Ohm Coil 6ms Release)
1	LM385LP-2-5	1509501 (2.5V Voltage Reference 20uA - 20mA)
1	IL2424S	2084325 (24V to 24V Isolated Regulated DC/DC Converter)
1	35SEPF22M	2354662 (24V Bypass Electrolytic 22uF 0.035Ohm D6.3mm H6mm 35V)
1	L-113YDT	2314278 (Yellow LED)
1	11R103C	2062671 (10uH Inductor 0.95A)
1	MC33079PG	9665030 (16MHz, Quad 7V/us Op-Amp)
1	T350B106K006AT	1878947 (Tantalum Capacitor Filter 10uF 0.5uA Leakage 6.3V)
2	RC55Y 1K13 0.1%	9500774 (0.1% 1k13 Ohm Resistor Grid Measurement)
4	RC55Y 107K 0.1%	9499911 (0.1% 107k Ohm Resistor Grid Measurement)
5	MR061C474KTA	1740531 (PV Bypass Cap 0.47uF X7R 100V 2.28mm Thickness)
16	CK06BX105K	287064 (Bypass Cap 1uF X7R 50V 2.28mm Thickness)
21	MR065C334KTA	570930 (Bypass Cap 0.33uF X7R 50V 2.28mm Thickness)
1	1N4733A	1861447 (Zener 1W 5.1V 5V Over Voltage Protection)
1	1N4734A	1861448 (Zener 1W 5.6V 5V Over Voltage Protection)
13	N/A	IC Headers
1	SK 92/50 SA	4621566 (40mm by 50mm by 100mm 1.9C/W Heat Sink)
5	4180G	1577101 (TO-247 Thermal Insulation Pad)
5	N/A	Isolating Screw Casing TO-247 & Screws
6	N/A	Nylon Separators & Screws
4	N/A	Rubber Feet

6.4 Prototype System Hardware

6.4.1 2-MIC Prototype System

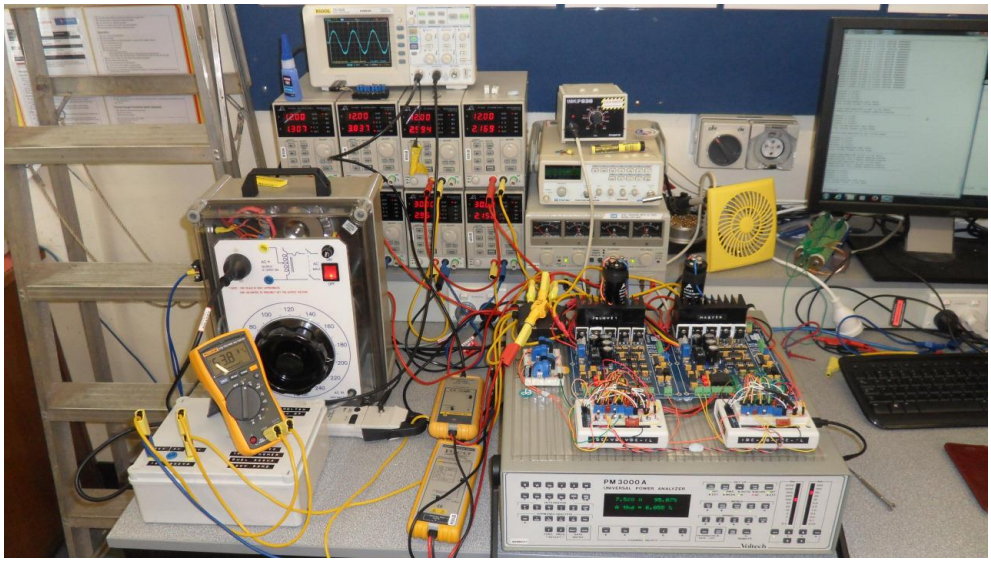

Fig. 6-23. An image of the 2-MIC cascaded system undergoing parallel/cascaded comparison investigation, operating with a grid interface (i.e. grid-tied mode).

6.4.2 4-MIC Prototype System

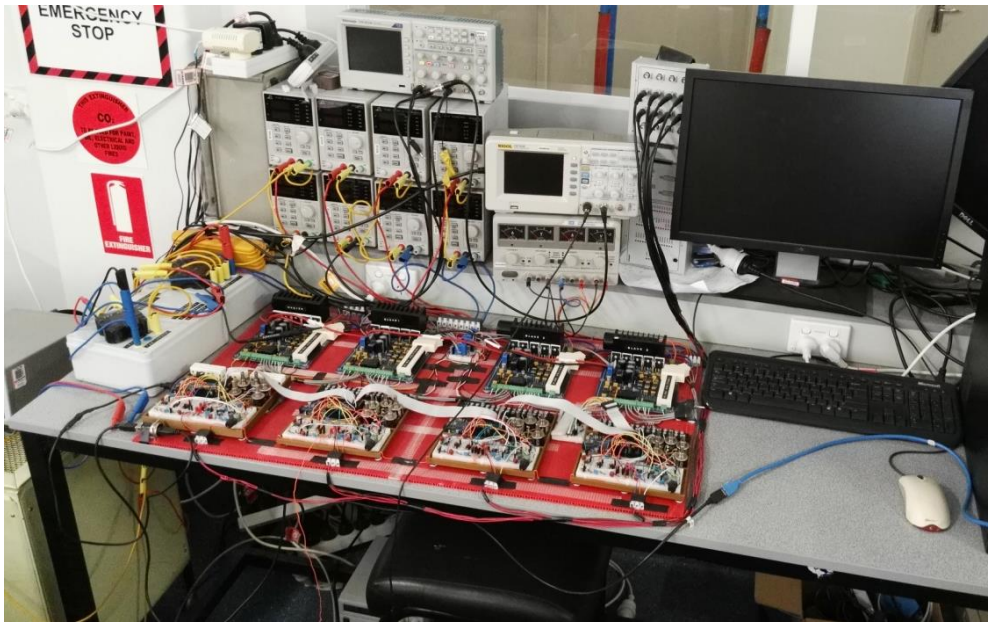

Fig. 6-24. A complete view of the experimental setup testing the 4-MIC decentralised MPPT algorithm. On the far left can be seen a resistive load bank (yellow box on the floor) and just to the left of the PC monitor can be seen the vertical Simulink DSPACE DAC/ADC box.

6.5 MIC µController Software

The software written for the SAM3X8E microcontroller was written using the Arduino IDE in the C programming language. Unfortunately, the code is excessively long and if presented in its entirety would consume 60+ pages in size 8 font. To essentially summarise the software, only the "main" section of the code is presented, which details the higher level coding used to control the decentralised MIC system. With the exception of the variable and function declarations, below can be seen the main code.

```
/*
H-Bridge Module Driver
By David Scholten 2016
The University of Adelaide
Please use with the Arduino IDE V1.6.8 and the Arduino Due Board V1.6.7.
*/

void setup()
 {
   //Startup procedure functions
   overClock();//Must be first.
   startUp(); //Must be second.
   voltageSourceMode();//Special testing mode, setup in the function.
   setupADC();
   setupDAC();
   currentRefGenerator(); //Generates the sinetable with the current ref magnitude incorporated. (Only on
a flag!)
   parallelSetup();//Must be before serial (sets commsFlag) and before interruptSetup/timerSetup
(interrupts are poisonous).
   serialSetup(); //The last things before the interrupts start.
   interruptSetup(); //Place just before the more frequent timer interrupts and after serial setup.
   timerSetup(); //Keep the interrupts from starting until last.
 }

 void TC7_Handler()
   {
    //g_APinDescription[testPin2].pPort -> PIO_SODR = g_APinDescription[testPin2].ulPin; //Sets the pin
(arduino pin numbering) HIGH
    //g_APinDescription[testPin2].pPort -> PIO_CODR = g_APinDescription[testPin2].ulPin; //Sets the pin
(arduino pin numbering) LOW
    //http://2manyprojects.net/timer-interrupts //Due timer help!
    //"Refresh" the interrupt and allow it to activate again (or something).
    TC_GetStatus(TC2, 1);
    //Update the timer variables:
    if (timeCounter >= (timerCounterLimit-1))//20,000
     {
       //Per-second activities (flags, notifications, leds, etc).

////////////////////////////////////////////////////////////////////////////////////////////////////////
/////
```

```
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
////////////////////////
      //Switching Frequency Measurement (very accurate).
      frequencyQuickCheckResult = frequencyQuickCheckCounter/2;
      frequencyQuickCheckCounter = 0;

      //Measures the grid frequency (approximately).
      gridFrequency = gridFrequencyTotal/noGridIntNegSamples;
      gridFrequencyTotal = 0;
      noGridIntNegSamples = 0;

      if(commsFlag == 1)//Master
       {
         if (minimumPowerFailFlag==1){digitalWriteDirect(masterBuzzer, HIGH);}
         else{digitalWriteDirect(masterBuzzer, LOW);}
         serialFlag = 1;//Allow the serial function to run once per second.
       }

      if (ledFlag == 0){ledFlag = 1; digitalWriteDirect(led, HIGH);}
      else{ledFlag = 0; digitalWriteDirect(led, LOW);}

      timeCounter = -1;


////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
////////////////////////

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
/////
     }
    timeCounter++;
    //serialResetCounter++;//Watchdog timer for the serial rest check.

    //Sycnhronised main loop operation though grid crossing interrupts //THIS IS NO LONGER USED TO
CONTROL MPPT - NOW DONE EVERY 20ms DIRECTLY IN THE NEG CROSSING!
    if (counterMPPT >= (timerCounterLimit/16-1))//~Every 60ms
      {
       //Operate the slow calculations once per second in the main loop.
       globalTimerMPPTFlag = 1;
       counterMPPT = -1L;
      }
    counterMPPT++;

    //Sycnhronised main loop operation though grid crossing interrupts
    if (slowCalcCounter >= (timerCounterLimit/10-1))//~Every 100ms second. ////Counter for the slow
calculations flag (should not exceed 1 second to avoid overflows). TOO SHORT AND THE FUNCTION WILL
NEED TO BE SYNCHRONISED WITH THE CROSSINGS.
      {
       //Operate the slow calculations in the main loop via a grid crossing interrupt.
       globalSlowCalcFlag = 1;
       slowCalcCounter = -1L;
      }
    slowCalcCounter++;
```

```
    //Sycnhronised main loop operation though grid crossing interrupts
    if (commsFlag == 1)//Master Only
     {
       if (globalCounter >= (globalCounterLimit))//This sets the flags for updating the global system through
comms each interval set by gloablCounterLimit.//Changed in the serial menus.
         {
          //Tells the global communications to update at the next zero crossings.
          globalSendReceiveFlag = 1;
          globalCounter = -1;
         }
       globalCounter++;
     }

    //Everything here is 20,000 times per second, tasks must not be too long either.

////////////////////////////////////////////////////////////////////////////////////////////////////////////
/////

////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////////////////////////

    currentRefTime++;
    if (currentRefTime >= (sineTableSize)){currentRefTime = 0;}//Loops around if it exceeds sineTableSize.

    //Checks if a sample (recorded to a variable total sum) should/can be taken this interrupt and does so if
possible (low di/dt). The goAhead is 0 if this occurs.
    //goAhead = 1;//Ensure the goAhead status default is "1"/True.
    //checkTakeSample();
    //Not needed for journal paper 2015

    //Ensure the current is on track.
    checkAndCompare();

    //If no ADC samples are being taken (checkTakeSample()), "goAhead" = 1 and therefore go ahead with
the typical current check and gate update, etc.
    if (currentRefTime & 0b00000001 == 1)//Main hysteresis code (standard operation).
     { //^^^ Checks if the nuber is odd or even.
       measurementADC(4);//Cycle the ADC samples.
     }

    universalTimer = universalTimer + 1LL;//The universal clock of the system (a replacement for millis(),
etc.)

    //g_APinDescription[testPin2].pPort -> PIO_CODR = g_APinDescription[testPin2].ulPin; //Sets the pin
(arduino pin numbering) LOW
   }

  void loop()
   {
    //START OF MAIN LOOP - Continuous - Everything here can take any amount of time, but will be
interrupted (no slow input/outputs).
```

```
////////////////////////////////////////////////////////////////////////////////////////////////////////////////
////////////////////////

//0s  //Run the serial monitor/control function continuously.
    //serialInterface();//Only run for troubleshooting - You do not want this running continuously!
Suspected to crash the serial link with high dv/dt.
    //serialResetCounter = 0L;//Debugging

//0s  //Run the "encoding is dangerous" end check over and over for all modules.
    //checkSetDecoding(0);//Check to see if 40ms has elapsed since the the dangerous region began. If so,
decode and end the daaaaanger zone~ (runs on all modules).
    //This has specific functions to differentiate the MASTER AND SLAVE.

//20ms//Runs approximately every 60ms (set in the interrupt).
    if (crossingTimerMPPTFlag == 1)//EVERY 60MS
     {
      localMPPT();//Power tracks the target power set by matlab. //Sycnhronised main loop operation
though grid crossing interrupts
       crossingTimerMPPTFlag = 0;
     }

//0.1s//Run only once per 100 milli seconds (time set in the interrupt).
    if (crossingSlowCalcFlag == 1)//NOT once per second!
     {
      slowCalculations();//Calculate system values for everything. //Sycnhronised main loop operation
though grid crossing interrupts
       crossingSlowCalcFlag = 0;
     }

//?s  //Decode the information from the communcations directly after TWO POSITIVE CROSSINGS SINCE
THE INITIAL RECEIVE COMMUNICATIONS
    if (communicationsDecodingFlag == 1)//On the second positive zero crossing!
     {
      if (commsFlag == 1)//Master
       {
        delayedDecodingMaster();//Decoding for the master.
        //decodingWarningFlag = 0;//Safe to use masterEnableTable.
       }
      else//Slave
       {
        //This warning tells the inverter to use 4's until the warning is removed (i.e. it's encoding/writing
the masterEnableTable still).
         delayedDecodingSlave();//Decoding for the slave.
        //decodingWarningFlag = 0;//Safe to use masterEnableTable.
       }
      communicationsDecodingFlag = 0;
     }

    //START OF SLAVE OPERATIONS

////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////
```

```
//0s
////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////
    if (commsFlag > 1)//If a slave, then run this check continuously.
     {
         //Slave is sending to the master.
         if (parallelOperationsSlaveSend() == HIGH)
          {
            //checkSetDecoding(1);//Start the 40ms timer for the slave of dangerous decoding.
          }
         //Slave is receiving from the master.
         if (parallelOperationsSlaveReceive() == HIGH)//If data is received from the master:
          {
            //This warning tells the inverter to use 4's until the warning is removed (i.e. it's encoding/writing
the masterEnableTable still).
             communicationsCompleteFlag = 1;//Signal to the crossing interrupt that the communications has
been completed.
          }
     }

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////
    //END OF SLAVE OPERATIONS

    //START OF MASTER OPERATIONS

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////

////////////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////

//1s  //The serial function runs once per second on the master only.
    if ((commsFlag == 1) && (serialFlag == 1))
     {
      serialInterface();//Also run the serial communications at this point, synchronised with calculations.
      serialFlag = 0;
     }

    //If it is the master and communications are enabled. This controls communications with the system.
Also, the flag from the zero crossing interrupt must have been set.
//2s  //Ultimately, runs at a frequency set by "globalCounterLimit" --> set in the serial interface.
    if ((commsFlag == 1) && (commsEnableFlag == 1) && (crossingSendReceiveFlag  == 1))//Sycnhronised
main loop operation though grid crossing interrupts
     {
       digitalWriteDirect(masterBuzzer, HIGH);//Beeps for a little bit each transmission!
       //crossingSendReceiveFlag = 0;//TEMP
       //Receive stuff from slaves.
       if (communicationsReceivedFlag == 0)//Hasn't yet received data.
        {
         if (parallelOperationsMasterReceive() == HIGH)//Main receiving function (receives from slaves).
```

```
          {
            //checkSetDecoding(1);//Start the 40ms timer for the master of dangerous decoding.
            if(localMPPTFlag == 1)//MPPT Time!
              {
                //IN THIS ORDER ONLY
                globalCalculateNewPowerRequirements();//Calculate the new current reference and set it, and
also calculates the desired power of each module.
                globalSetSwitchingPoints();//Calculates and sets the switchings points ready for transmission.
                globalCalculateNewBlockPowers();//Calculate the power that will be in the blocks of the next
cycle to be allocated to inverter modules.
                globalSetBlocksToModules();//Sorts and assigns the power blocks to the modules based on the
power requirements and future current ref.
              }
            else//Not MPPT time :(
              {
                globalSetSwitchingPoints();//Calculates and sets the switchings points ready for transmission.
                globalSetBlocksStupid();//Sets the operations of all modules in their blocks for for transmission
without any further calculations.
              }

              communicationsReceivedFlag = 1;//Signal that the receiving stage of communications has been
completed.
            }
        }
       else if (timeToSendFlag == 1)
        {
          //Send stuff to the slaves.
          if (parallelOperationsMasterSend() == HIGH)
            {
              //Reset the zero crossing send/receive flag. This only occurs if all of the receving/sending has
been successful!
            crossingSendReceiveFlag = 0;//Says that all communications have finished.
            communicationsReceivedFlag = 0;//Resets the "has communicated" flag.
            timeToSendFlag = 0;//Has sent, it's no longer TIME TO SEND :D

            communicationsCompleteFlag = 1;//Signal to the crossing interrupt that the communications has
been completed.
            }
         }
       digitalWriteDirect(masterBuzzer, LOW);//Beeper off after the small ~60ms interval during receiving,
calculating and transmitting.
     }

////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////

////////////////////////////////////////////////////////////////////////////////////////////////////////////
//////
   //END OF MASTER OPERATIONS

////////////////////////////////////////////////////////////////////////////////////////////////////////////
////////////////////////
   //END OF MAIN LOOP
  }
```

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