

"MICROCOMPUTER CONTROL OF A BLAST FURNACE STOVE MODEL"

PETER BUDIMIR, B.Sc., B.E.(Hon)

BEING A THESIS SUBMITTED

AS PARTIAL FULFILMENT FOR THE

DEGREE OF MASTER OF ENGINEERING SCIENCE

IN THE

DEPARTMENT OF ELECTRICAL ENGINEERING

THE UNIVERSITY OF ADELAIDE

APRIL 1983

This thesis embodies the results of supervised project work making up 2/3 of the work for the degree.

DECLARATION

This thesis contains no material which has been accepted for the award of any other degree or diploma in any University, and to the best of my knowledge it contains no material previously published or written by another person, except where due reference is made in the text of the thesis.

P. BUDIMIR

ACKNOWLEDGEMENT

Many have been an encouragement and help in the work relating to this thesis. In particular I am grateful to my project supervisors, Dr. D.A. Pucknell and Dr. C.P. Jeffreson for assistance of both technical and non-technical nature.

Thanks go to Telecom Australia for the leave granted to enable me to complete the thesis writing.

There are also a number of other individuals who were of particular help or encouragement; Dr. C.W. Nettle, Mr. N.M. Martin, and Mr. R.W. Korbel who produced the DAC/ADC board and developed stage 2 of the SDK-86 software.

Finally, but most importantly, I would thank my wife, Alison, for invaluable support throughout the project.

SUMMARY

Because of the large fuel requirements of blast furnace stoves, methods of increasing their operating efficiency are of real practical concern.

This has motivated research into the feasibility of implementing a microprocessor system to control these stoves so as to achieve maximum thermal efficiency. The first phase of this study is the subject matter of this thesis. It involves the initial development of a system to be used for verifying/developing control strategies on an experimental stove model in the Department of Chemical Engineering, University of Adelaide.

The thesis describes,

- (1) basic stove structure,
- (2) operation and control requirements,
- (3) system specifications,
- (4) followed by a description of the microcomputer control system: consisting of an 'upper level' PDP-11/03 microcomputer (DEC) and a 'lower level' SDK-86 microcomputer kit (INTEL).

Hardware design, construction and testing has been completed. A pre-written 'package' has been chosen for the 'upper level' software and 'lower level' software has been developed in two stages. The first stage only involved a single feedback loop for initial hardware tests whereas stage two incorporates the multi-loop system as specified.

1.	NTRODUCTION	- 1
2.	LAST FURNACE STOVE OPERATION	3
i-	.1 INTRODUCTION	3
	.2 BLAST FURNACE STOVES	3
	2.2.1 Introduction	3
	2.2.2 Stove Description	4
	2.2.3 Stove Operation	= 4
	2.2.4 Stove Configuration	6
	.3 EXPERIMENTAL STOVE MODEL	9
	2.3.1 Introduction	9
	2.3.2 Description	11
	2.4 MATHEMATICAL DESCRIPTION	13
	2.4.1 Introduction	13
	2.4.2 Analysis	14
	2.4.3 By-Pass Main Operation	17
	2.4.4 Thermal Efficiency	19
	2.4.5 Conclusion	20
3.	BLAST FURNACE STOVE CONTROL	21
	3.1 INTRODUCTION	21
	3.2 CONTROL REQUIREMENTS	21
	3.2.1 Introduction	21
	3.2.2 Switching Period	22
	3.2.3 Hot Blow Flowrate and Inlet Gas Temperature	22
	3.2.4 Zero Changeover Time	24
	3.2.5 Non-Zero Changeover Time	25
	3.3 CONCLUSION	27

4. 3	SYST	EM REQUIREMENTS
1	4.1	INTRODUCTION
1	4.2	REQUIREMENTS
		4.2.1 Overall Objectives
		4.2.2 Computational Requirements (Original Concepts)
		4.2.3 Computational Requirements (Later Developments)
	4.3	PROCESS DESIGN
		4.3.1 Introduction
		4.3.2 Thermal Design
		4.3.3 Flow Control
	4.4	OPERATOR/MACHINE INTERFACE
		4.4.1 General Requirements
		4.4.2 Processor to Processor Interface
		4.4.3 "Analogue" Transfers
	6	4.4.4 Digital Transfers
		4.4.5 Priorities and Interrupt Considerations
	4.5	SUMMARY
5.	PRO	CESSOR SYSTEM
	5.1	INTRODUCTION
	5.2	HARDWARE SYSTEM STRUCTURE
		5.2.1 Introduction
		5.2.2 PDP-11/03 Microcomputer
		5.2.3 SDK-86 Microcomputer
		5.2.4 Inter-Processor Interface
		5.2.5 Up Transfer
		5.2.6 Down Transfer
		5.2.7 A/D and D/A Convertors

-	
5.3 SOFTWARE	49
5.3.1 Introduction	49
5.3.2 PDP-11/03 Software (DDACS)	49
5.3.3 SDK-86 Software	51
5.4 OPERATION - STAGE 1	52
5.4.1 Introduction	52
5.4.2 Auto/Manual Transfer	53
5.5 OPERATION - STAGE 2	55
5.5.1 Introduction	55
5.5.2 Operation	57
5.6 SYSTEM PERFORMANCE	59
C. CONGLUGION	60
6. CONCLUSION	00
REFERENCES	62
ADDRESS A MADDIADE DEGGDIDETON	
APPENDIX A - HARDWARE DESCRIPTION	
A.1 INTRODUCTION	
A.2 INTER-PROCESSOR INTERFACE BOARD	
A.2.1 BOARD LAYOUT	
A.2.2 EDGE CONNECTIONS	
A.2.3 ADDRESS DECODING AND BUS INTERFACE	
A.2.4 UP TRANSFER (CSR AND DBR HARDWARE)	
A.2.5 DOWN TRANSFER HARDWARE	
A.2.6 SDK-86 ADDRESSING	
A.2.7 PDP-11/03 ADDRESSING AND INTERRUPTS	
A.2.8 IPI REGISTER DESCRIPTIONS (CSR AND DBR)	
A.3 DAC/ADC BOARD	
A.3.1 BOARD LAYOUT	

- A.3.2 EDGE CONNECTIONS
- A.3.3 ADC SECTION HARDWARE
- A.3.4 DAC AND DECODE SECTION HARDWARE
- A.3.5 ADDRESSING
- A.3.6 A/D CONVERSION
- A.3.7 D/A CONVERSION
- A.3.8 ADC RANGE SELECTION
- A.3.9 DAC RANGE SELECTION
- A.3.10 ADC SAMPLING MODE
- A.4 DATA SHEETS (AD363 and DAC80)
- APPENDIX B SOFTWARE DESCRIPTION
- B.1 DDACS DESCRIPTION
- B.2 SDK-86 SOFTWARE LISTING STAGE 1
- B.3 KEYBOARD PARSER STAGE 1
- B.4 SDK-86 SOFTWARE DESCRIPTION STAGE 2
- B.5 SDK-86 SOFTWARE LISTING STAGE 2