



AN IMAGE PROCESSING TERMINAL

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## SUMMARY

An electronics design for an image processing terminal is presented which uses a raster scanned, electronic storage tube for storing a single television frame from any television source such as a television camera, television receiver or video recorder. The storage tube is scanned at normal TV scan rates with the video output signal displayed on any conventional television monitor.

The stored image may be digitized into a matrix of 64, 128, 256 or 512 rows by 64, 128, 256 or 512 columns, each independently selected resulting in a combination of 16 matrices. During digitization, each row is scanned by the electron beam which remains stationary over each column for two microseconds while the video signal is digitized into 1 in 256 levels by an 8-bit analogue-to-digital converter. Each row is digitized and held temporarily in a random access memory before being transferred to a minicomputer. This procedure is repeated until the image has been digitized and moved to the computer for processing.

After digitally processing the image, the data may be returned to the storage tube for viewing at normal television scan rates. In this mode, each digitized row is moved from the computer into the random access memory from where it is converted to an analogue signal and written on the storage tube. Where less than 512 rows are written on the tube, the system executes a write-repeat, writing the same information stored in random access memory over consecutive rows. The write-repeat is set to

1, 2, 4 or 8 when 512, 256, 128 or 64 rows of data are returned for storage.

The objective was to develop a prototype image processing terminal capable of being supported by a small general purpose computer which would also make the system portable. Included is a functional description of the system together with details on its operation and performance.

DECLARATION

This thesis contains no material which has been accepted for the award of any other degree or diploma in any University and to the best of the author's knowledge and belief, contains no material previously published or written by another person, except where due reference is made in the text of the thesis.

T.W. Mahoney. <sup>U</sup>

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## 1. INTRODUCTION

The attributes of the human eye are probably taken for granted. For example, the eye presents high resolution, colour, binocular viewing and functions over a wide range of ambient light levels from near starlight to bright sunlight. By comparison, no colour TV system has yet achieved a similar performance.

It became apparent when studying the Naval applications of low light level television (LLTV) systems that the eye-brain combination can be regarded as a powerful image processor which is difficult to emulate, even with today's technology. With low light level devices, the very nature of the image is determined by the statistical arrival and detection of photons. As the light level decreases, the number of photons arriving per unit time becomes insufficient to form a high resolution image and their statistical fluctuations are such that the image itself can be regarded as noise. The image may be almost obscured by a very high level of background noise from a variety of sources such as electron noise, head amplifier noise and image intensifier scintillations. If the output from the LLTV camera is recorded on a video tape recorder and replayed, there is a significant degradation in picture quality when examining the image in the stop frame mode, when compared with the replayed image. This effect is clearly demonstrated in photographs 1 and 2. In both cases, the shutter speed of the camera used to photograph the TV display was set to 0.25 second. Photograph 1 shows the result of photographing the TV display from a replay of a stationary scene at approximately starlight. Photograph 2 shows the result of

photographing the TV display at the same section of video tape but with the video recorder in the stop frame mode.

The reason for this degradation is that the stimuli produced by light impinging on the retina within the eye are averaged over approximately 0.2 second. This time constant is often referred to as the eye integration time. Hence the eye can be regarded as a filter which averages the image over 0.2 second, reacting in effect to a summation of the signal amplitudes which are coherent from TV frame to TV frame and the summation of noise powers which are incoherent from TV frame to TV frame. In essence, the eye is a parallel processor which simultaneously operates on all points within an image. By contrast, a digital computer can be regarded as a serial processor which digitizes the image over a number of points and sequentially processes the data from each point.

Aside from this important feature, the eye can effectively perform image stabilization by tracking a slowly moving target. Also, it is not necessary to see all of the target at any one time. The eye may see aspects of a target which are highlighted for short periods by sea glint or breaks in heavy cloud covering a moonlit sky. These aspects are pieced together by the brain to form a composite mental picture of the image. Further, the eye-brain combination may correlate a visual image with a mental picture derived from other sources. For example, sonar or audible emissions from a target may be of assistance in visually identifying it.

At the time this project was conceived, work was being

undertaken to employ a silicon dioxide storage tube (see reference 1, 2 and Appendix I) to extend the process of eye integration by storing the video signal from the LLLTV camera over a longer period of time. While this proved encouraging in the laboratory with a stationary target, the technique was limited in the field because of image movement. Photographs 3 and 4 show the effectiveness of this technique by storing an image for 0.2 and 1 second from the same section of video tape used for the previous photographs. The uneven light distribution is caused by the electrostatically focused image intensifiers forming part of the LLLTV camera and the bright arc is the result of accidentally exposing the LLLTV camera tube to a bright light.

The rate at which the image moved was usually known, for example, it was the rate of roll of the platform on which the LLLTV camera was mounted. One paper (reference 3) indicated that the image blur could be partially corrected by digital processing techniques. This prompted the idea of marrying the storage tube with a digital computer. Because of the type of application envisaged for this device, a small portable computer was a basic requirement.

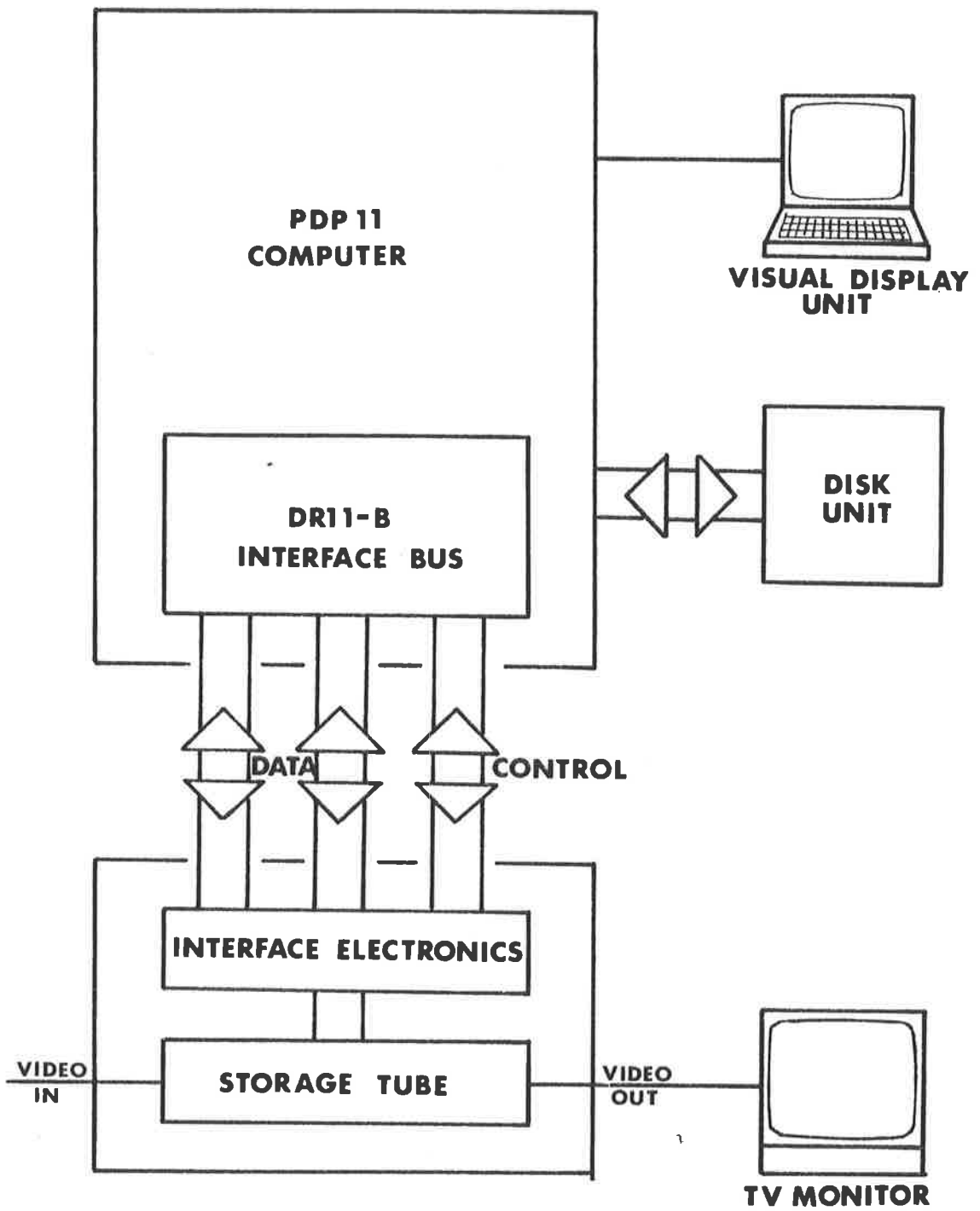


## 2. COMPUTER SELECTION

A large amount of data is generated by digitizing just one image. For example, digitizing an image into 1 in 256 levels over a matrix of 512 x 512 points results in 1/4 million 8-bit bytes of data. This volume of data could be held only in the central memory of either a special purpose computer or an extremely large computer. The former was not available and the latter, an IBM 370, was neither portable nor did it allow for easy access to a hardware interface.

The final choice of a computer was restricted to what was available, in this case, a PDP-11/45 minicomputer with a DR11-B direct memory access interface bus. Not all of the generated data could be accommodated in central memory, hence the additional requirement for a fast access, mass storage device. This requirement was satisfied by an RM02 disk unit. The next question was, how best to store this data on disk? Data is generally stored on disk units in logical blocks. One digitized row was considered a suitable choice for a logical block of data. The final configuration for the Image Processing Terminal is shown in figure 1.

Although the PDP-11/45 is one of the most powerful computers within the PDP-11 family, it should be noted that the Image Processing Terminal has been designed to interface with the smallest PDP-11 computer capable of supporting a DR11-B interface bus and a disk unit.



**FIGURE 1 SCHEMATIC IMAGE PROCESSING TERMINAL**

### 3. IMAGE PROCESSING

A system which provides a means of digitizing an image and displaying the processed image is a useful tool for investigating a much broader field of image processing than just correcting for image blur. For example, one important area of signal processing is the Fourier Transform, a topic well known to electrical engineers. Greater emphasis has been placed on the Fourier Transform with the development of fast processing techniques such as the Fast Fourier Transform, see references 4 and 5. Its advantage lies in the fact that the signal is converted from the time domain to the frequency domain where it becomes a simple task to implement various filtering techniques. The filtered waveform is then converted back to the time domain by the inverse Fourier Transform.

The Fast Fourier Transform (FFT) is performed on a two dimensional image by implementing the FFT firstly on rows and then on columns. If for example, a matrix of  $2^N$  rows by  $2^M$  columns was stored in row accessible order on disk, performing the FFT on rows would involve  $2^N$  disk read/write operations to retrieve each row, perform the FFT, and return the processed rows to disk. The difficulty now lies in performing the FFT on columns. All rows must be accessed to recover one column of data. This involves  $2^{(N+M)}$  disk read/write operations to perform the FFT on every column. A matrix of 1024 x 1024 points would require in excess of  $10^6$  disk read/write operations. Based on a disk read or write time of 40 milliseconds, over 23 hours of disk transfers would be necessary to process the image. This time would be doubled when applying the inverse FFT.

The number of disk transfers was reduced significantly by applying a technique developed in reference 6, 'A Fast Computer Method for Matrix Transposing'. This method transfers row pairs from disk to central memory, exchanges certain elements and returns the row pairs to disk. It requires  $N$  passes through a matrix of  $2^N \times 2^N$  points, transposing the matrix in  $N \times 2^N$  disk read/write operations. This represents a ten-fold reduction in disk transfers when applied to the previous example. Even further gains can be achieved if more than one row pair can be held in central memory.

In principle, row pairs are retrieved in a binary sequence and elements are exchanged in a binary pattern. For example, during the first pass through the matrix, adjacent row pairs are retrieved and elements are exchanged. In pass two, alternate rows are transferred to memory and pairs of elements are exchanged. Rows, four apart are retrieved in the third pass and blocks of four elements are exchanged. In general, row pairs  $2^{(P-1)}$  apart are accessed in pass  $P$  and blocks of  $2^{(P-1)}$  elements are exchanged. It can be seen that if the matrix is transposed after performing the FFT on all rows, the FFT can be performed on each transposed column. In practice, the FFT could be performed on the transposed columns during the last pass through the transpose algorithm.

Another technique was developed by the author to modify the transpose algorithm enabling it to be performed in bit-reversed order. Simple and efficient bit-reversal FFT algorithms could then be performed on the data, see reference 7. Reference 7 gives a background into the FFT algorithms, the transpose

algorithm from disk and the bit-reversed transpose algorithm. The report represents the theoretical background for the row digitization approach and has such a significant bearing on the hardware for this project that a microfiche is included inside the rear cover.

The bit-reversed transpose is similar to the normal transpose in that row pairs are retrieved in the same order, the difference being that elements are exchanged in the reverse order. That is, the pattern of element exchange during the last pass through the matrix in the normal transpose is performed during the first pass of the bit-reversed transpose. In general, pairs of rows  $2^{(P-1)}$  apart are accessed in pass P and blocks of  $2^{(N-P)}$  elements are exchanged.

#### 4. IMAGE PROCESSING TERMINAL

The Image Processing Terminal incorporates a silicon dioxide storage tube (see Appendix I) which functions as a single frame video store. It is electronically coupled to a PDP-11 minicomputer via a DR11-B direct memory access (DMA) interface bus, as shown in figure 1.

##### 4.1 Image storage

A video signal from any conventional TV source such as a TV camera, TV receiver or video recorder can be stored on the storage tube. Video storage may be initiated either manually or by the computer. In the manual mode, the number of frames over which storage occurs is set by front panel thumbwheel switches. Normally these switches are set to 2 TV frames or one TV field, a field being 625 scan lines. When integration techniques are employed, the switches may be set in the range 1 to 99 TV frames. In the computer initiated mode, the number of storage frames (1 to 99) is transmitted by the computer. If a zero is transmitted, the thumbwheel switch setting is accepted.

##### 4.2 Digitization

The stored image may be digitized into a matrix of 64, 128, 256 or 512 rows by 64, 128, 256 or 512 columns, each independently selected giving a combination of 16 matrices. Upon a command from the computer, a code defining the selected matrix combination is loaded into a register and the storage tube executes a 1 millisecond retrace to the top left-hand

corner of the stored image. It then automatically proceeds to digitize the first row, remaining stationary over each column for 2 microseconds while the video output signal is converted to its 8-bit digital equivalent by an analogue-to-digital (A/D) converter, see figure 2. The digitized row is stored temporarily in a 512 x 8-bit random access memory (RAM) awaiting transfer to the minicomputer. A status flag, DSTAT B, remains cleared while digitization is in progress. After digitizing the selected number of columns, the electron beam executes a retrace and the status flag is set indicating that row digitization is complete. Digital data held in this memory is then transferred to the PDP-11 computer via the DR11-B interface bus. The memory appears as a 512 x 8-bit memory to the analogue-to-digital converter and as a 256 x 16-bit memory to the DR11-B interface bus, thereby reducing the number of word transfers per row to half the number of columns.

After transferring the data from RAM to the computer's central memory, the row number is then read and appended to the data. The Image Processing Terminal then automatically digitizes and stores the next row. While digitization is in progress, the computer is free to transfer the previously digitized row from its central memory to disk. This process continues until all rows have been digitized.

#### 4.3 Writing-digital

After digitizing the image and executing some form of signal processing, be it spectral filtering by FFT techniques

or signal normalization by removing a background component, the processed image may be transferred back to the storage tube for viewing at normal TV scan rates.

This mode is similar to digitization in reverse, in that each digitized row is transferred back to the RAM before being written on the storage tube, see figure 2. It is assumed in this mode that rows are not necessarily in a numerical order, hence the row number must be transmitted to the storage tube. Effectively, the vertical scan may be positioned on any row. A second device status flag, DSTAT A, has been assigned to memory availability (RAM AVAILABLE). If DSTAT A is HIGH, the digitized row may be transferred from the PDP-11 computer to the random access memory. Immediately the number of words have been transmitted the device status flag is cleared and the Image Processing Terminal writes the stored data on the storage tube.

Unlike the digitization process, the horizontal scan executes a linear slow-scan as the data is simultaneously being clocked from memory, converted to an analogue signal by a digital-to-analogue (D/A) converter and written on the storage tube. This has the effect of filling in areas of the picture as opposed to discrete points if a staircase function was used. Also, depending on the specified number of rows, the tube executes a write-repeat, writing the same data over multiple rows. For example, if 128 rows had been specified, the Image Processing Terminal writes the same data over four consecutive rows. This has been the primary reason for using a temporary store. Alternatively, the computer would need to



transmit the same row of data four times with a data transfer rate that coincided with the linear slow-scan.

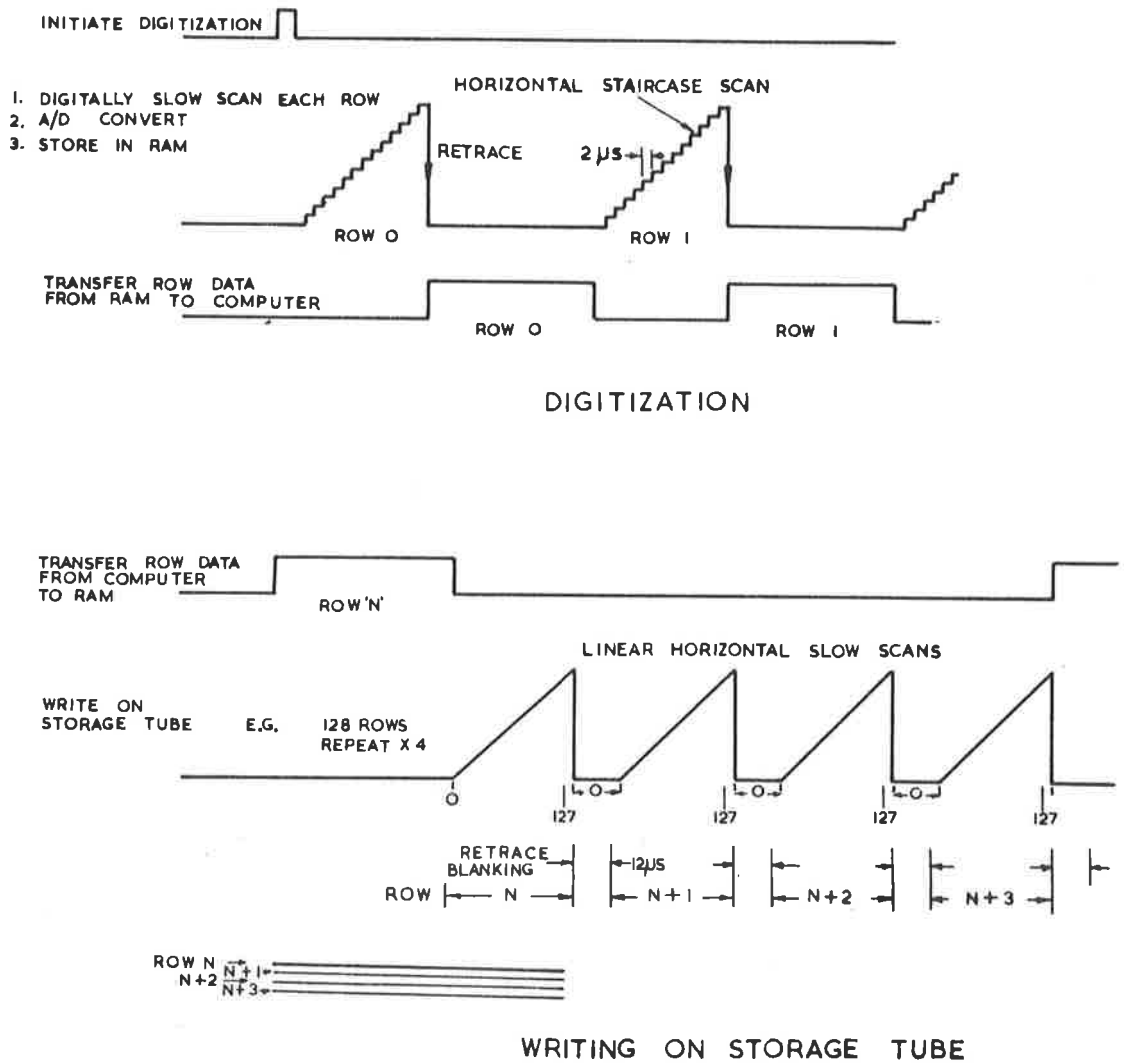


FIGURE 2. IMAGE PROCESSING TERMINAL - MODES OF OPERATION

## 5. PDP-11 COMPUTER

The PDP-11 is a 16-bit minicomputer having an architecture similar to a number of microprocessors with a data/control bus (called a UNIBUS<sup>®</sup>) which is common to the central processor, memory and all peripheral devices, see figure 3. A complete description of this computer would occupy several volumes, however it is considered important to present a brief overview of the PDP-11 computer to assist in understanding the hardware interface bus, the Image Processing Terminal and its associated software. A detailed description is given in the appropriate PDP-11 Processor Handbook, reference 8.

### 5.1 Memory configuration

The PDP-11 family of computers has an instruction set which manipulates either 8-bit bytes or 16-bit words. For this reason, the PDP-11 memory is configured as a series of 8-bit storage locations, see figure 4. Words are always referenced to even numbered memory locations and each word is divided into a high byte and a low byte. The PDP-11 word length is 16-bits and can address a maximum of 32K words (65K bytes) of memory. In all PDP-11 computers, the topmost 4K words of the address space are reserved for peripheral and general registers with the net result that the programmer has 28K words of memory for program development.

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<sup>®</sup> UNIBUS is a trademark of the Digital Equipment Corporation.

## 5.2 Central processor address capability

The central processor (CPU) is broadly classified into a number of sub-units such as the arithmetic logic unit, instruction decoder and address buffer. Although the PDP-11 is a 16-bit machine, the CPU (and Unibus) have an 18-bit address capability by including two additional extended bus address bits. These two additional bits are utilized by the memory management option to expand the maximum memory capacity to 128K words or 256K bytes.

## 5.3 Memory management

Larger computers within the PDP-11 family, such as the PDP-11/45 used for this project, may be fitted with a memory management unit which allows the PDP-11 memory capacity to be expanded to 128K words. Again, the topmost 4K words of the address space, addresses 760000 to 777777 octal, are reserved for the peripheral and general registers, see figure 4. This address space is referred to as the I/O page and is common to all user programs.

The memory management unit is optimized for the multi-user environment by assigning segments (pages) of memory to each user and allowing a number of user programs to reside in memory at any one time. It also prevents each user from making unauthorized access to memory and arbitrates on use of the I/O registers. In essence, the 16-bit program references are now virtual addresses which are mapped into 18-bit physical addresses by the memory management unit.

#### 5.4 Master-slave relationship

Transfer of data between devices connected to the Unibus is by a master-slave relationship with only one device in control at any one time. The controlling device may not necessarily be the CPU. For example, in this application a Direct Memory Access interface bus (DR11-B) becomes the controlling device when data is being transferred either to or from the PDP-11's central memory.

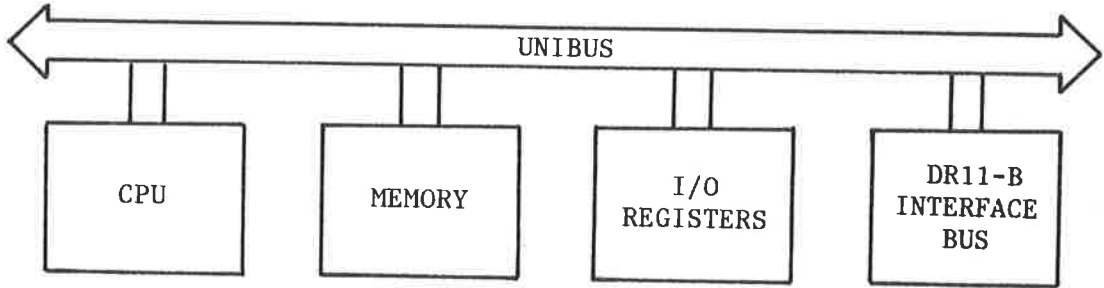


FIGURE 3. PDP-11 ARCHITECTURE

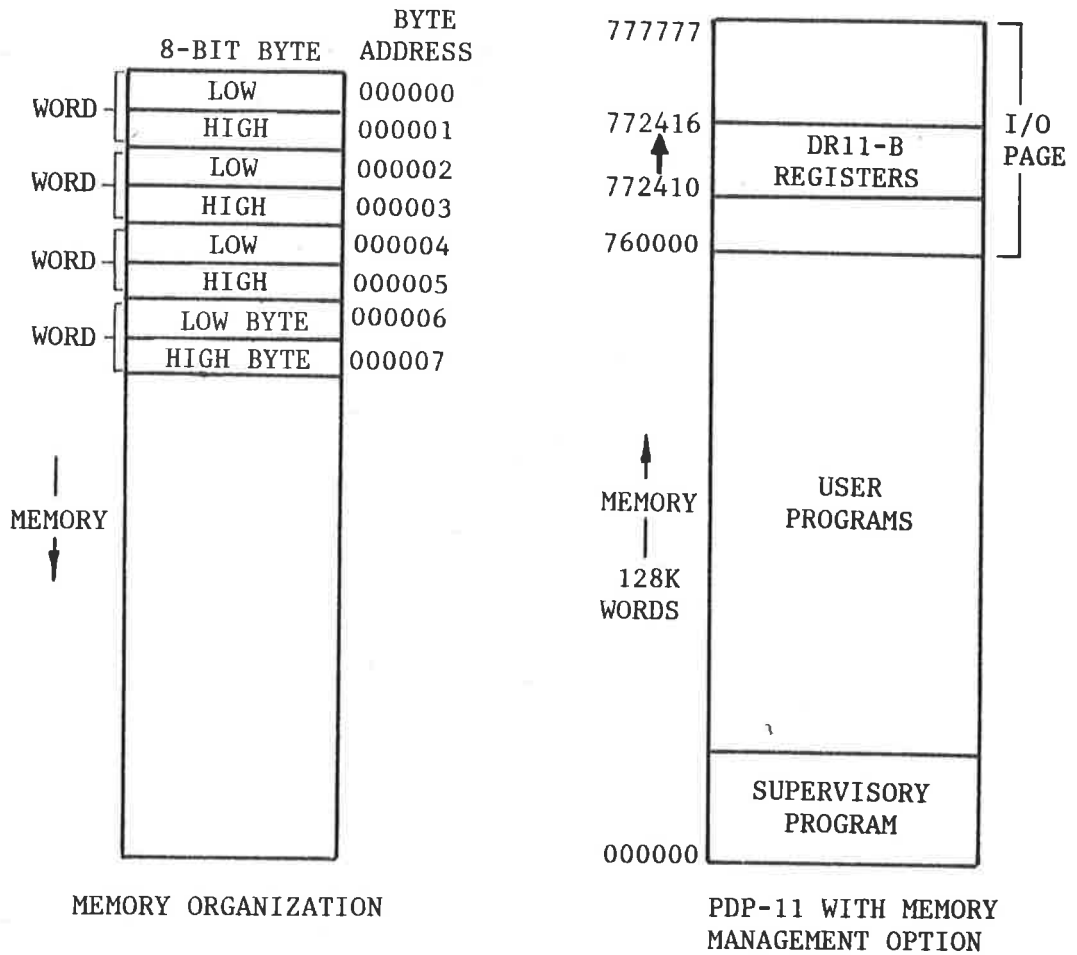


FIGURE 4. PDP-11 MEMORY ORGANIZATION

## 6. THE INTERFACE BUS

The DR11-B is a Direct Memory Access (DMA) interface bus marketed by the Digital Equipment Corporation for interfacing external equipment with their range of PDP-11 computers. A schematic diagram of the DR11-B is shown in figure 5. No attempt has been made to show all internal connections between the input-output signals and the four peripheral interface registers.

Basically, the DR11-B operates directly with the PDP-11's central memory by gaining control of the Unibus and performing block data transfers between central memory and the user device. Operation is controlled by four registers; command and status, bus address, word count and data buffer. Each register has a specific memory address on the Unibus and can be loaded or read under program control. In any data transfer, the 2's complement of the number of words to be transferred is loaded into the word count register, and the bus address register is loaded with the starting address in central memory where the block transfer will commence. Finally, loading the command and status register transmits output signals to the user device which responds with input signals initiating data transfers through the data buffer register. The registers are described in the following sections. A detailed description is given in the DR11-B Manual and Engineering Drawings, references 9 & 10.

### 6.1 Bus address register

The bus address register (DRBA) is a 15-bit register ( $A_{01}-A_{15}$ ) which is loaded with the starting address in a 32K word central memory block where data transfers will begin.

The least significant bit  $A_{00}$  is supplied by the user device and is required for byte addressing. An absolute memory address is specified by loading the extended bus address bits,  $XBA_{16}$  and  $XBA_{17}$ , into the command and status register, see section 6.4.3. The DRBA is normally incremented after each data transfer and may be inhibited by the BA INC ENB user input signal. For this application, sequential word addressing has been specified by grounding  $A_{00}$ , and by connecting BA INC ENB to 5 volt, see figure II-2.

## 6.2 Data buffer register

The data buffer register (DRDB) operates in two modes, a write only mode in which data is transferred to the user device or a read only mode in which data is transferred from the user device to central memory. The data buffer register is split into a buffered 16-bit output port ( $DAT_{00}$ - $DAT_{15}$ OUT) and a 16-bit input port ( $DAT_{00}$ - $DAT_{15}$ IN) with data direction controlled by two additional user input signals designated C0 and C1, see figure II-3.

## 6.3 Word count register

The word count register (DRWC) is a 16-bit register which is loaded under program control with the 2's complement of the number word transfers to be implemented. With the word count increment enable (WC INC ENB) tied HIGH, the word count register increments after each word transfer and automatically inhibits further data transfers when overflow occurs, i.e., all 1's to all 0's.



## 6.4 Command and status register

Commands are transmitted to the user device by loading the command and status register (DRST). In response, the user device makes requests for data transfers through the DRST. Certain functions within the DRST are not available to the user but required for internal operation of the DR11-B interface bus. Each functional bit of the DRST, see figure 5, is described in the following sections.

### 6.4.1 Go

The GO bit is not directly available to the user, however when loaded with a logical 1 under program control, it causes a 200nS GO pulse to be transmitted to the user device indicating that a command has been issued.

### 6.4.2 Function bits

Three bits, FNCT 1, 2 and 3 are loaded under program control and made available to the user device. In this application, they are decoded in a 3 to 8 line decoder and provide the Image Processing Terminal with eight separate modes of operation. These modes are described in section 7.1 .

### 6.4.3 Extended bus address

As already indicated the PDP-11 word is capable of addressing up to 32K words of memory, whereas the PDP-11/45 with memory management may address up to 128K words of memory. Two bits in the command and status register, XBA16

and XBA17 extend the bus addressing capability of the bus address register to 18 bits allowing it to reference up to 256K-bytes of memory. These two bits are loaded under program control.

#### 6.4.4 Interrupt enable, ready and cycle

An interrupt can occur only if the INTERRUPT ENABLE bit (IE) is set. This bit has no significance for this application as no attempt has been made for the Image Processing Terminal to exercise a system interrupt. READY is a read only bit indicating that the DR11-B may accept another command, and the CYCLE bit is required for internal operation of the DR11-B.

#### 6.4.5 Device status

Three read only bits DSTAT A, B and C are provided for monitoring operations within the user device. Each bit may be masked and tested for specific events. In this application, DSTAT A is HIGH when an intermediate memory within the Image Processing Terminal is available for loading with a digitally processed row of data. DSTAT A is LOW as the data is being clocked from this memory, converted to an analogue signal and written on the storage tube. DSTAT B is LOW when image digitization is in progress and HIGH when the digitized row is available for transmission to the PDP-11 computer. A HIGH on DSTAT C indicates that either a WRITE(TV) or an ERASE operation is in progress.

#### 6.4.6 Maintenance bit

When a special maintenance module is inserted into a socket within the DR11-B, diagnostic programs may be run by setting the maintenance bit (MAINT). This bit is not normally available to the user. In the Image Processing Terminal design, the INITIALIZE bit was used as a system reset. Even though INITIALIZE is a DR11-B output signal, it cannot be pulsed with a RESET instruction in a multi-user environment without disastrous consequences for other users. For this reason, the DR11-B was modified by jumpering the MAINT bit on the wiring backplane to the user input-output socket allowing it to perform the same function as INITIALIZE.

#### 6.4.7 Attention

If the interrupt enable (IE) is clear, a HIGH on the attention line (ATTN) causes an error condition which inhibits further bus cycles. An interrupt occurs if the interrupt enable is set.

### 6.5 Additional input-output signals

In addition to those functions already described, the DR11-B requires the following user input-output signals for its operation.

#### 6.5.1 Cycle request

A positive pulse of 100nS minimum duration on either CYCLE REQUEST A or B requests bus usage and initiates data

transfers. The CYCLE REQUEST is issued by the user device and hence data transfers are controlled at a user defined rate.

#### 6.5.2 Single cycle

If SINGLE CYCLE is held HIGH, bus control is released after each data transfer allowing other devices to gain access to the Unibus. If SINGLE CYCLE is held LOW, the DR11-B does not release control of the Unibus until the number of words specified in the word count register has been transferred either to or from central memory. The latter mode is used when transferring digitized rows either to or from the Image Processing Terminal.

#### 6.5.3 End cycle

A pulse of approximately 100ns duration, END CYCLE, is transmitted to the user device upon completion of each data transfer.

#### 6.5.4 Busy

BUSY indicates the status of the DR11-B and is not used in this application.

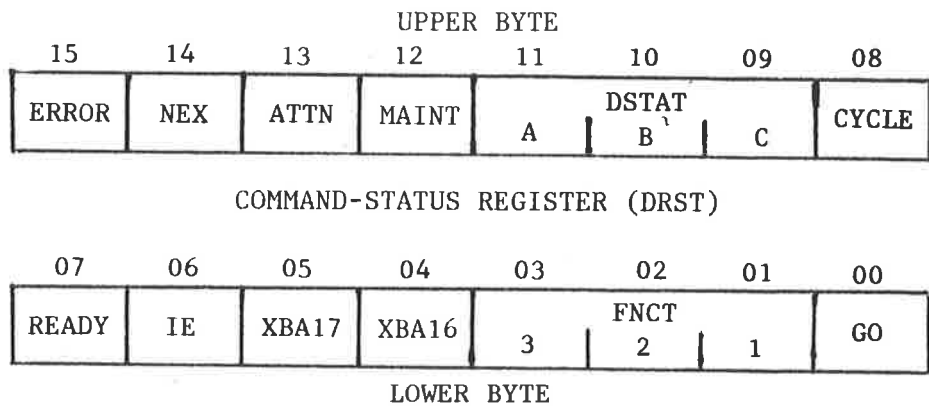
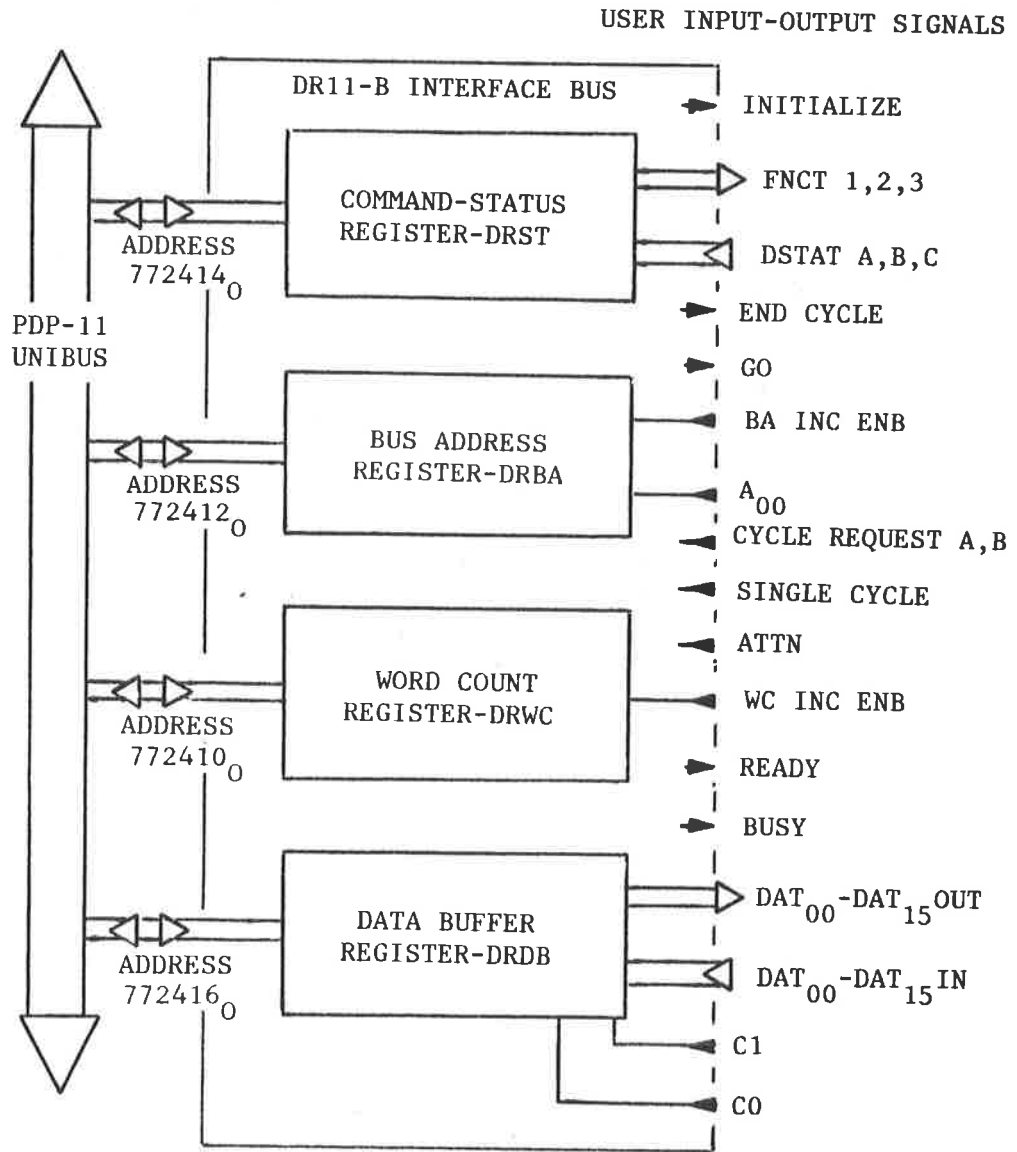


FIGURE 5. BLOCK DIAGRAM - DR11-B INTERFACE BUS

## 7. FUNCTIONAL DESCRIPTION - IMAGE PROCESSING TERMINAL

The Image Processing Terminal has been constructed on a number of printed circuit cards and assembled into the prototype form shown in photograph 5. All printed circuit artwork, loading of printed circuit cards with components and interwiring were performed by the author. An overall block diagram is shown in figure II-1 and a detailed description is given in the following sections.

### 7.1 Function decoder

Eight separate functions are assigned to the Image Processing Terminal by decoding the three DR11-B function bits, FNCT 1, 2 and 3, in a 3 to 8 line decoder (IC56), refer to figure II-3. Each of these functions is described in the following sections.

#### 7.1.1 Read row number - function zero

The present row number may be read into the PDP-11 computer by firstly loading the function bits with a zero. This causes the READ ROW NUMBER output to go LOW if the complemented MEMORY OUTPUT CONTROL is also LOW. The MEMORY OUTPUT CONTROL is LOW when data is being read from the dual port memory to the D/A converter and written on the storage tube, see figure II-8. Gating of these two functions eliminates conflict between enabling the output of the dual port memory and loading the contents of the row counter onto the data bus. A LOW on the READ ROW NUMBER output enables the DR11-B data direction control, C1, and enables

3-state buffers (IC34,35), figure II-5, which transfer the contents of the row counter (IC26-28) onto the DR11-B data-in bus.

#### 7.1.2 Write row number - function one

The electron beam can be positioned on any row within the storage tube by loading the row number into the row counter. Loading the function bits in the DR11-B command and status register with a one, causes the WRITE ROW NUMBER output to go LOW, enabling the load inputs to the row counters (IC26-28), figure II-5. The row number is then transmitted to the DR11-B data bus and synchronously clocked into the row counter by the END CYCLE pulse, see section 7.3.4 .

#### 7.1.3 Read from memory - function two

Each row is digitized and stored temporarily in the dual port memory. The digital data is then transferred in burst mode to the PDP-11 computer by implementing function two. Loading a binary two into the function bits causes the READ FROM RAM output to go LOW only when the complemented MEMORY ADDRESS CONTROL is also LOW. The complemented MEMORY ADDRESS CONTROL (figure II-6) is HIGH whenever a row is being digitized. It is also HIGH as each row is being read from the dual port memory, converted to an analogue voltage and written on the storage tube. Hence, gating the output from the 3 to 8 line decoder with this function prevents the READ FROM RAM output from interrupting either row digitization or writing on the

storage tube. A LOW on the READ FROM RAM output sets SINGLE CYCLE, HIGH, thereby requesting burst mode transfer of data from the dual port memory to the PDP-11 computer. It also enables the word transfer counter, see section 7.4, and gates END CYCLE pulses to the DR11-B, CYCLE REQUEST B input. The first data transfer is always initiated by coupling the GO pulse directly to the CYCLE REQUEST A input. Subsequent data transfers are initiated by gating the END CYCLE pulse to the CYCLE REQUEST B input.

#### 7.1.4 Write into memory - function three

After an image has been processed by the computer, it is returned to the storage tube and viewed at normal TV scan rates. Each processed row of data is transferred from the PDP-11 computer into the dual port memory. Upon completion of the number of word transfers, the data is automatically read from memory, converted into an analogue signal by the D/A converter and written on the storage tube. Where less than 512 rows have been specified, the system executes a write-repeat, writing the contents of the dual port memory over multiple rows. The write-repeat is set to 1, 2, 4 or 8 when 512, 256, 128 or 64 rows of data are returned for storage. This process continues until all rows have been returned to the storage tube.

Loading the function bits with binary three causes the WRITE INTO RAM output to go LOW. Again, the complemented MEMORY ADDRESS CONTROL must be LOW. A LOW on the WRITE INTO RAM output sets SINGLE CYCLE, LOW,



requesting the transfer of data in burst mode. It also enables the word transfer counter and directs END CYCLE pulses to the CYCLE REQUEST B input.

#### 7.1.5 Initiate digitization - function four

Loading binary four into the DR11-B function bits causes the INITIATE DIGITIZATION output to go LOW. A detailed description of this function is given in section 7.2 .

#### 7.1.6 Initiate write-digital - function five

Loading binary five into the DR11-B function bits causes the INITIATE WRITE/STORE output to go LOW. A detailed description of this function is given in section 7.2 .

#### 7.1.7 Initiate write(TV) - function six

The process of storing a conventional TV image on the storage tube may be initiated either manually or by the computer. When initiated manually, the number of TV frames over which image storage will occur is set by two front panel thumbwheel switches. These switches may be set in the range 01 to 99, however, for most applications they are set to 02, corresponding to two TV frames or one TV field of 625 interlaced scan lines.

In the computer initiated mode, the number of TV frames is transmitted by the computer. If a zero is transmitted, the thumbwheel switch setting is assumed.

Detailed descriptions of initiating a write and erasing the storage tube are presented in section 7.8 .

#### 7.1.8 Initiate erase - function seven

Initiating an erasure of the storage tube is similar to initiating a write(TV). It may be triggered manually or by the computer. The difference is that the number of TV frames is in multiples of 10 giving a range of 10 to 990 TV frames or 0.2 to 20 seconds of erasure.

## 7.2 Column counter

The column counter has two modes of operation, a digitize mode when digitizing the stored image, and a write mode when data stored in an intermediate memory is written on the storage tube. In the digitize mode, the binary outputs from a counter are coupled to a digital-to-analogue converter which generates a staircase waveform causing the electron beam to step column by column across the stored image at  $2\mu\text{S}$  intervals. As the electron beam remains stationary over each column, the video output signal is converted to its 8-bit digital equivalent by an analogue-to-digital converter. This data value is stored in a random access memory at the address specified by the binary counter.

In the write mode, the horizontal staircase generator is disabled and the horizontal slow-scan circuits are enabled, see section 7.7. Unlike the digitization process, the horizontal deflection executes a linear slow-scan as data is being clocked from memory, converted to an analogue signal and written on the storage tube. Where less than 512 rows of data are returned for storage, the system executes a write-repeat, writing the same data stored in memory over multiple rows. The net result is that the image is always written over 512 rows. A detailed description of the column counter is given in the following sections, refer to figure II-4.

### 7.2.1 Digitize mode

Digitization is initiated by loading the function bits in the DR11-B command and status register with the

binary equivalent of four. This causes the INITIATE DIGITIZATION input to go LOW enabling a gate (IC58a,b) which directs the END CYCLE pulse to the retrace monostable multivibrator (IC59) and to the mode flip-flop (IC60a). Waveform diagrams are shown in figure 6. Data on the DR11-B data bus setting the row and column matrix combination is simultaneously loaded into the row/column register by the END CYCLE pulse, see section 7.5 . The END CYCLE pulse sets the mode flip-flop which remains set until clocked by the END OF DIGITIZATION pulse which is generated after digitizing the last row. Also, the END CYCLE pulse triggers the retrace monostable multivibrator (IC59) which generates a one millisecond pulse to allow the frame scan to retrace to the top left-hand corner of the stored image. At the end of this delay, the digitize clock (IC48) is enabled. IC48 is a four-input NAND Schmitt trigger. In operation, when any one input is LOW, the output is HIGH and capacitor C11 is charged to the output voltage through resistor R11. When all of the inputs go HIGH, the output goes LOW discharging C11 through diode D9 towards the lower trigger threshold. When the lower threshold is reached, the output switches HIGH charging C11 through R11 towards the upper threshold level. Oscillations are sustained as the capacitor alternately charges and then discharges between the upper and lower threshold levels. Resistor R11 is adjusted for a clock frequency of 500KHz.

The first two clock pulses are prevented from triggering the start conversion monostable multivibrator

(IC45) by the action of IC46a,b and IC47. This allows 4 $\mu$ S for the storage tube blanking to be released. Subsequent clock pulses trigger the start conversion monostable multivibrator, generating 75nS pulses which initiate analogue-to-digital conversion (IC87). The electron beam remains stationary over each column while the video output signal is converted to its 8-bit digital equivalent. Immediately each start conversion pulse is issued to the A/D converter a busy output goes HIGH, remaining HIGH for approximately 800nS until A/D conversion is complete. The negative transition of the busy signal triggers the write pulse monostable multivibrator (IC50) which generates a 100nS pulse. Resistor R12 and capacitor C17 provide a delay allowing the data from the A/D converter to be valid before storing the data in the dual port memory. The write pulse loads the data output from the A/D converter into the dual port memory at the address specified by the 10-bit binary counter (IC5-7). The trailing edge of the write pulse is also delayed before incrementing the 10-bit binary counter.

Stepping across the stored image is controlled by coupling the output from the binary counter through a shift network (IC15-19) to a digital-to-analogue converter (IC22). The binary output may be coupled either directly to the D/A converter or shifted 1, 2 or 3 places right depending on whether 512, 256, 128 or 64 columns respectively have been selected. Shifting is controlled by two bits, COLUMN SELECT 0 and 1 stored in the row/column

register. Hence, the D/A converter generates a staircase voltage waveform with either 64, 128, 256 or 512 steps of  $2\mu\text{S}$  duration and a step amplitude of  $5/64$ ,  $5/128$ ,  $5/256$  or  $5/512$  volt respectively. Incrementing the binary counter by the trailing edge of the write pulse allows approximately  $1\mu\text{S}$  for the horizontal scan to step and settle prior to digitizing the next column.

After digitizing the selected number of columns in the first row, the output from IC19b goes HIGH, clocking the RAM LOADED output from IC60b HIGH. The complemented RAM LOADED output then inhibits the digitize clock (IC48). The RAM LOADED output releases the reset from the word transfer counter, see section 7.4, and also provides the device status to the DR11-B via the DSTAT B status bit. The change in state from LOW to HIGH on the DSTAT B input signifies to the PDP-11 computer that the row is digitized and stored in the dual port memory. After the digitized row has been transferred to the PDP-11 computer the complemented END OF WORD TRANSFER output from the word transfer counter momentarily goes LOW, clearing IC60b and enabling the digitize clock to digitize the next row.

#### 7.2.2 Write-digital mode

Loading the DR11-B function bits with the binary equivalent of five causes the INITIATE WRITE/STORE input to go LOW enabling a gate (IC58c,d) which directs the END CYCLE pulse to a second retrace monostable multivibrator (IC67) and to the write-digital flip-flop (IC68a).

Waveform diagrams are shown in figure 7. The END CYCLE pulse which is generated by loading the matrix combination into the row/column register simultaneously triggers the retrace mono and sets the write-digital flip-flop (IC68a). The write clock cannot be enabled until one millisecond after the END CYCLE pulse is transmitted, again to allow the electron beam within the storage tube to retrace to the top left-hand corner of the stored image.

In this mode, the binary counters (IC5-7) are held reset until the digitized row has been transferred from the PDP-11 computer to the dual port memory. Immediately the number of words have been transferred, the END OF WORD TRANSFER input momentarily goes HIGH clocking a second flip-flop (IC68b) which enables the write clock. The write clock circuit is identical to that of the digitize clock and set to a frequency of 500KHz. Again, the first two clock pulses are prevented from clocking the binary counters (IC5-7) by the action of IC46c,d and IC52. Data stored in the dual port memory is addressed by the outputs from the binary counters and applied to a D/A converter (IC73), see figure II-8. Unlike the digitization mode, the horizontal staircase generator is disabled and the horizontal linear slow-scan circuits are enabled, see section 7.7. As the horizontal scan sweeps across the storage tube, the analogue signal generated by the D/A converter is written on the storage target. After storing one row of data, the output of multiplexer IC19b goes HIGH triggering the line retrace monostable multivibrator (IC54)

and clocking the write-repeat binary counter (IC8). The 12 $\mu$ S line retrace pulse resets the write clock and blanks the storage tube as the electron beam executes a horizontal retrace. At the same time, the vertical scan steps to the next row and the write process is repeated by writing the same data on the storage tube.

The write-repeat counter outputs are coupled to a multiplexer (IC9) which is controlled by the ROW SELECT 0 and 1 inputs. The output of this multiplexer clears flip-flop IC68b which inhibits the write clock, resets the write-repeat counter and blanks the storage tube. Simultaneously the RAM AVAILABLE output (DSTAT A) goes HIGH indicating that the dual port memory is available for loading with the next row of data. For example, if 512 rows are specified by the ROW SELECT 0 and 1 inputs, the least significant bit of the write-repeat counter is coupled to the multiplexer output, thereby inhibiting additional write-repeats after storing each row. If 64 rows are specified, the fourth output from the write-repeat counter is multiplexed to the output. This output goes HIGH after the eighth write-repeat inhibiting further write-repeats. Hence, the write-repeat is set to 1, 2, 4 or 8 depending on whether 512, 256, 128 or 64 rows of data are returned for storage.



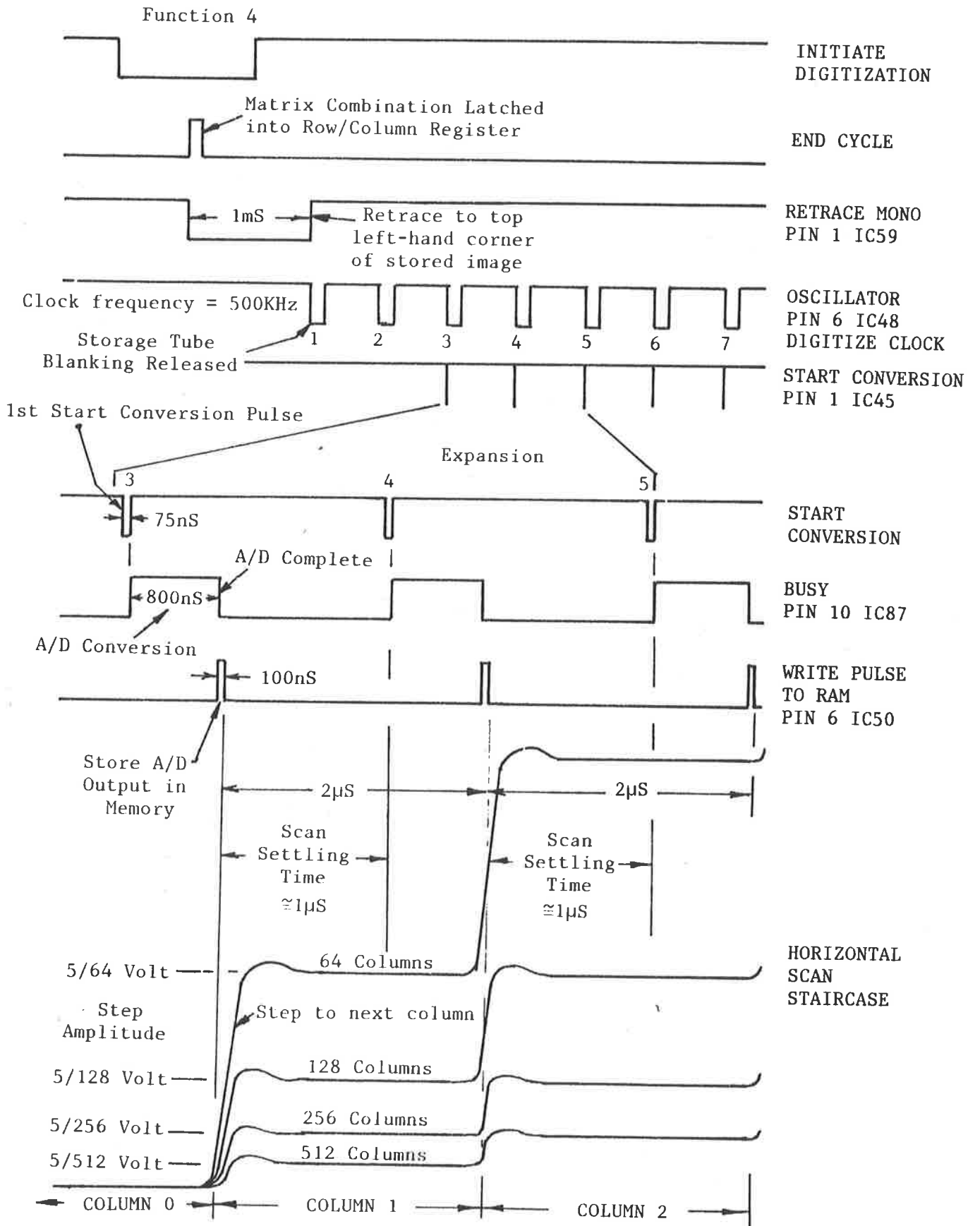


FIGURE 6. COLUMN COUNTER WAVEFORMS - DIGITIZE MODE

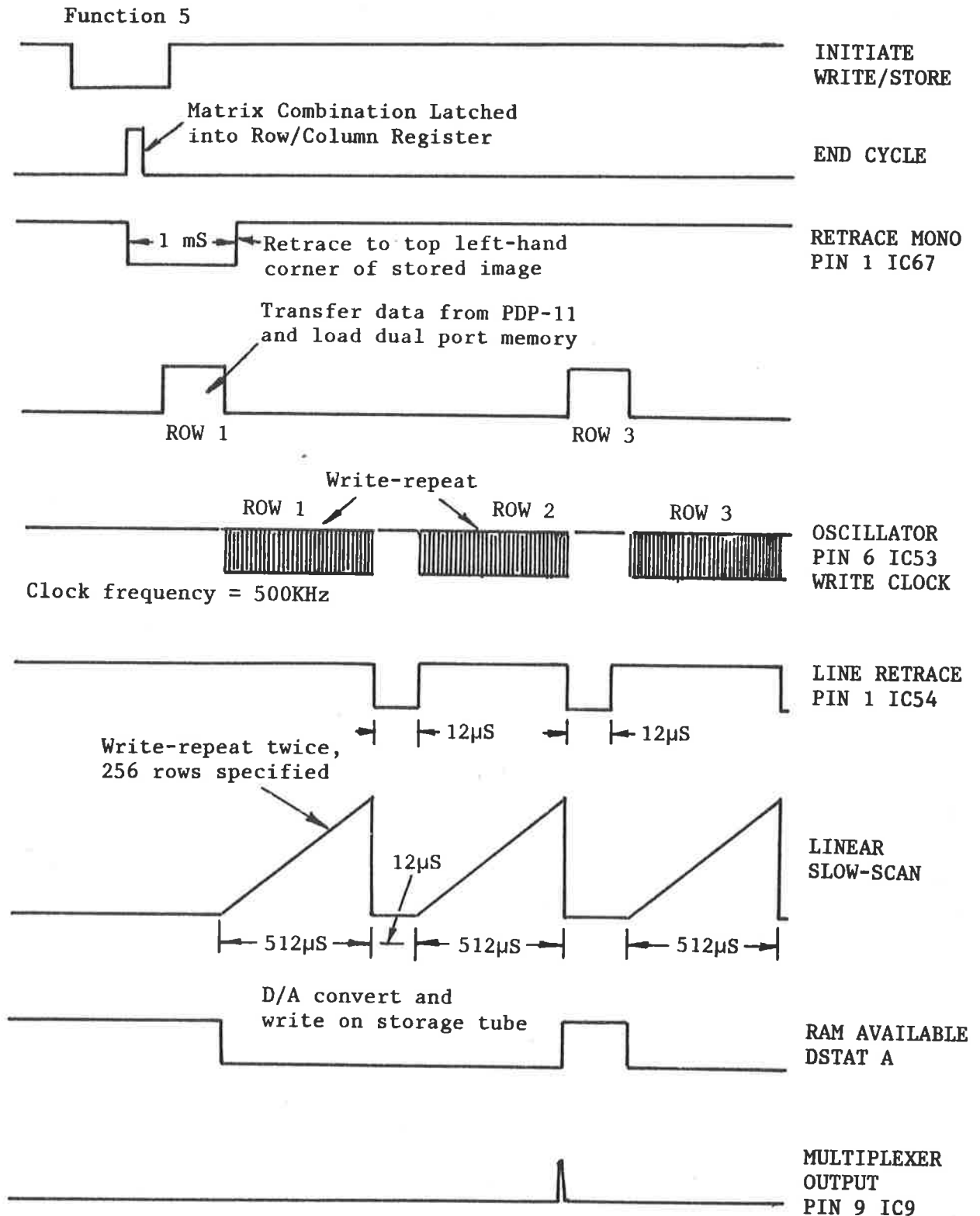


FIGURE 7. COLUMN COUNTER WAVEFORMS - WRITE DIGITAL MODE

### 7.3 Row counter

A second binary counter controls the vertical positioning of the electron beam within the storage tube. The binary output or present row number may be read by the computer or alternatively, the electron beam may be positioned on any row by loading the row number into the binary counter. Refer to figure II-5.

#### 7.3.1 Vertical staircase generator

The vertical staircase waveform causing the electron beam to step row by row down the storage tube is generated by coupling the outputs from a binary counter to a D/A converter. The least significant nine bits of the ten-bit counter (IC26-28) are coupled either directly to the D/A converter (IC43) or alternatively shifted one, two or three bits right when 512, 256, 128 or 64 rows respectively have been selected. Selection is controlled by loading two bits, ROW SELECT-0 and 1 into the row/column register when either initiating image digitization or writing digitally processed rows on the storage tube. The shift network is enabled only when digitizing an image and writing digitally processed rows on the storage tube. At all other times, the VERTICAL STAIRCASE ENABLE input, generated by the scan control/interlock circuitry, disables the shift network and holds the VERTICAL SCAN STAIRCASE OUTPUT at zero volt.

When storing a digitally processed image the shift network is disabled by ORing (IC10) the MODE input with the ROW SELECT inputs. The binary counter is then coupled

directly to the D/A converter irrespective of the selected number of rows. If for example, 64 rows were specified, the system executes a write-repeat, writing the same data stored in memory over eight consecutive rows. Hence the system always writes over 512 rows.

A 10-bit D/A converter has been used which generates a 0 - 10 volt output by coupling an internal resistor in the feedback loop of the output operational amplifier (IC49). This voltage range has been halved to 0 - 5 volt by using the least significant nine bits and connecting the most significant bit to 5 volt. It should be noted that the D/A converter operates with complementary binary inputs, hence the requirement for nine inverting gates (IC41,42).

### 7.3.2 Digitization

When digitizing an image, the MODE input is LOW. This enables the DIGITIZE gate (IC24c) and disables the WRITE/STORE gate (IC24b). The system has been designed such that the row number must be read by the PDP-11 computer before the binary counter is incremented. This logic operates in two modes, the row number may be read while the row is being digitized or alternatively, the row number may be read after row digitization is complete. In the first mode, clearing the DR11-B function bits causes the READ ROW NUMBER input to go LOW enabling 3-state buffers (IC34,35) and enabling a gate IC32a. Reading the row number generates an END CYCLE pulse which clocks a D-

type flip-flop (IC31) causing its output to go HIGH and enabling a gate, IC32b. Upon completion of row digitization, the RAM LOADED input goes HIGH, triggering a monostable multivibrator (IC33) whose output pulse resets the D-type flip-flop and increments the binary counter. In the second mode, the RAM LOADED input is already HIGH. Loading the DR11-B function bits with zero causes the READ ROW NUMBER input to go LOW, again enabling IC32a. Reading the row number generates an END CYCLE pulse which clocks the D-type flip-flop (IC31). An output from the flip-flop triggers the monostable multivibrator (IC33) which again resets the D-type flip-flop and increments the binary counter.

### 7.3.3 Write digital

When writing digitally processed rows on the storage tube, the MODE input is HIGH. This disables the shift network and connects the binary counter outputs directly to the D/A converter. The MODE input also disables the DIGITIZE gate (IC24c) and enables the WRITE/STORE gate (IC24b).

After each row is written on the storage tube, an END OF ROW pulse is generated by the column counter which increments the row counter. At the count of 512, the END OF DIGITIZATION output goes HIGH inhibiting further END OF ROW pulses from clocking the counter.

#### 7.3.4 Loading the row counter

The vertical scan may be positioned on any row by loading the row number into the binary counter. When the DR11-B function bits are loaded with binary one, the WRITE ROW NUMBER input goes LOW enabling the binary counter load inputs and enabling gate IC25c. The row number is then transmitted to the DR11-B data-out bus and synchronously clocked into the binary counter by the END CYCLE pulse.

#### 7.3.5 Reading the row number

Loading binary zero into the DR11-B function bits sets the READ ROW NUMBER input LOW, enabling ten 3-state buffers (IC34,35). These buffers place the binary counter outputs on the DR11-B data-in bus awaiting a read operation by the computer.

#### 7.4 Word transfer counter

As previously indicated, the binary outputs from the DR11-B word count register (DRWC) are not available to the user device. Instead, word transfers either to or from the PDP-11 computer are counted in a separate nine-stage binary counter (IC1-3), see figure II-6. During writing into, and reading from the dual port memory, END CYCLE pulses are gated (IC4c) to the word transfer counter clock inputs and the binary outputs are multiplexed onto the dual port memory address lines. Four outputs from the counter are coupled to a 4 to 1 line multiplexer (IC14) which is controlled by the COLUMN SELECT 0 and 1 code stored in the row/column register. The multiplexer output is inverted (IC4a) and applied to the input gate (IC4c). Further counting is inhibited and an END OF WORD TRANSFER pulse is generated when the number of words transferred by the PDP-11 computer, either to or from the dual port memory, is equal to half the number of columns defined by the column select code.

Resetting of the counter is controlled by the MODE input which multiplexes (IC63) the RAM LOADED input or the RAM AVAILABLE input onto the reset line. The counter is held reset by the RAM LOADED input as each row is digitized. Immediately the row is digitized, the RAM LOADED input goes HIGH, releasing the reset line and allowing END CYCLE pulses to clock the counter. When writing on the storage tube, the RAM AVAILABLE input is HIGH. Upon transferring the number of words to the dual port memory, the END OF WORD TRANSFER pulse goes HIGH, clocking flip-flop IC68b, figure II-4, and causing

the RAM AVAILABLE input to go LOW. Reset on the counter is not released until the specified number of write-repeats has been completed. The counter is also reset during power-on and by setting the maintenance bit (MAINT), see section 6.4.6 .



## 7.5 Row/Column register

Logic circuits within the Image Processing Terminal which set the number of steps in the vertical and horizontal staircase waveforms and the number of write-repeats are controlled by the ROW SELECT 0,1 and COLUMN SELECT 0,1 outputs from the row/column register (IC29), see figure II-7. When initiating digitization (function four) or writing the digitized image on the storage tube (function five), a row/column matrix code is simultaneously transmitted across the least significant four bits of the DR11-B output data bus. Binary 0, 1, 2 or 3 is transmitted as the least significant two bits when specifying 64, 128, 256 or 512 rows and the same code is transmitted as the next least significant bits when specifying 64, 128, 256 or 512 columns.

Loading binary four or five into the DR11-B function bits causes the INITIATE DIGITIZATION or the INITIATE WRITE/STORE input to go LOW enabling a gate (IC32d). At the same time, the four-bit matrix code is applied to the data inputs of a four-bit latch (IC29). This data is valid when the END CYCLE pulse is issued by the DR11-B. The END CYCLE pulse clocks a D-type flip-flop (IC31) which in turn clocks the row/column matrix code into the four-bit latch. The status of flip-flop IC31 and the row/column matrix code are indicated by five light emitting diodes.

## 7.6 Dual port memory

The dual port memory, figure II-8, is partitioned into two 256 x 8-bit memories (IC77,78 and 79,80) which appear as a 256 x 16-bit memory to the DR11-B interface bus and as a 512 x 8-bit memory to the A/D and D/A converters.

When digitizing an image, the 8-bit output from the A/D converter (IC87) is applied to the data inputs of both memory partitions and the most significant 8-bits from the column counter are multiplexed (IC12,13) to the memory address lines. The memory write pulse, WRITE PULSE TO RAM, is multiplexed (IC88) alternately to each memory partition by the least significant bit from the column counter. As the electron beam steps across the stored image at two microsecond intervals, the data generated by digitizing the even columns is stored in one memory partition and the data from the odd columns is stored in the other memory partition.

After digitizing each row, the data stored in memory is transferred to the PDP-11 computer. Loading function two into the function bits, see section 7.1.3, causes the READ FROM RAM input to go LOW, directing the outputs from both memory partitions onto the DR11-B data-in bus. It simultaneously multiplexes (IC12,13) the binary output from the word transfer counter to the memory address lines. The data is transferred to the PDP-11 computer and each END CYCLE pulse clocks the word transfer counter, accessing the next data word. It can be seen that the number of word transfers is always half the number of digitized columns.

A similar process occurs when transferring digitally processed rows back to the dual port memory before they are written on the storage tube. Loading function one into the DR11-B function bits sets WRITE INTO RAM, LOW which multiplexes the 16-bit DR11-B data-out bus into both memory partitions and multiplexes the binary output from the word transfer counter to the memory address lines. Unlike the digitization mode, the END CYCLE pulse is simultaneously directed to the write enable inputs of both memory partitions. Data on the DR11-B data-out bus is loaded into memory by the END CYCLE pulse. The trailing edge of the END CYCLE pulse then clocks the word transfer counter in anticipation of storing the next data word.

Immediately each row of data is loaded into memory, the data is clocked out of memory, converted to an analogue signal and written on the storage tube. In this mode, the binary output from the column counter is applied to the memory address lines and the least significant bit from the column counter multiplexes (IC72,74) the output from alternate memory partitions into the D/A converter (IC73,75,76). If less than 512 rows are specified, the system executes a write-repeat, writing the same data over consecutive rows. The number of write-repeats is equal to 512 divided by the number of rows. Hence, the system always writes 512 rows on the storage tube.

## 7.7 Scan control/interlock

The scan circuits operate in the following modes;

### (a) Frame scan

- (i) Linear scan with a period of 20ms.
- (ii) Staircase scan with 64, 128, 256 or 512 steps. Each step duration is determined by the selected number of columns and the speed at which data is transferred either to or from the Image Processing Terminal by the PDP-11 computer.

### (b) Line scan

- (i) Linear scan with a period of 64 $\mu$ S.
- (ii) Linear slow-scan of 128, 256, 512 or 1024 $\mu$ S duration.
- (iii) Staircase scan with 64, 128, 256 or 512 steps each of 2 $\mu$ S duration.

Correct selection and operation of these scanning modes is controlled by the scan control/interlock circuit, see figure II-9. Table 1 outlines the operational characteristics of the scan control/interlock circuit. When digitizing an image the MODE input is LOW, and when storing a digitally processed image on the storage tube, the WRITE DIGITAL input is HIGH.

TABLE 1. LOGIC CHARACTERISTICS - SCAN CONTROL/INTERLOCK CIRCUIT

FUNCTION	INPUTS		OUTPUTS		
	MODE	WRITE DIGITAL	1	2	3
READ	$\overline{\text{DIGITIZE}}\text{-(H)}$	$\overline{\text{WRITE}}\text{-(L)}$	H	L	H
WRITE DIGITAL	$\overline{\text{DIGITIZE}}\text{-(H)}$	WRITE-(H)	H	H	L
DIGITIZE	DIGITIZE-(L)	$\overline{\text{WRITE}}\text{-(L)}$	L	L	L
ERROR	DIGITIZE-(L)	WRITE-(H)	H	L	H

where; OUTPUT 1 =  $\overline{\overline{\text{MODE}} \cdot \overline{\text{WRITE DIGITAL}}}$   
 OUTPUT 2 =  $\text{MODE} \cdot \text{WRITE DIGITAL}$   
 OUTPUT 3 =  $\text{MODE} \oplus \text{WRITE DIGITAL}$

A LOW on output 1 enables the horizontal staircase generator, see figure II-4, and disables both the horizontal TV scan and slow-scan generators. It also switches the horizontal staircase waveform to the line scan driver, see figure II-14. It can be seen from Table 1 that the horizontal staircase scan is enabled only in the DIGITIZE mode.

A HIGH on output 2 enables the horizontal slow-scan circuits, hence from Table 1 the horizontal slow-scan circuits are enabled only in the WRITE DIGITAL mode.

A LOW on output 3 disables the vertical linear ramp generator and enables the vertical staircase generator, see figure II-5. At the same time, the vertical staircase waveform is switched to the frame scan driver. It can be seen that the vertical staircase scan is enabled during the DIGITIZE and WRITE DIGITAL modes.

If an error condition develops where the MODE input is LOW and the WRITE DIGITAL input is HIGH, the scans revert to the normal or READ mode.

## 7.8 Read-write-erase timing

Storing an image from a conventional TV source and erasure of the storage tube may be initiated either manually by front panel switches or by the computer with the write and erase durations generated by the read-write-erase timing circuit. Both the write and erase timing circuits are identical with the exception that the write timing circuit generates a pulse whose duration is in multiples (1-99) of 20 millisecond TV frames and the erase timing circuit generates a pulse whose duration is in multiples (1-99) of ten TV frames or 200 millisecond. Only the write timing circuit is described in the following sections, refer to figure II-10.

### 7.8.1 Manually initiated write

In the manually initiated write mode, the number of TV frames over which the video signal is stored is controlled by two front panel thumbwheel switches. The binary coded decimal (BCD) codes on these two switches are coupled through multiplexers (IC18,19) to two programmable decade down-counters (IC22,23). Operating a front panel 'WRITE' switch clocks a D-type flip-flop (IC17b) which transfers the logic level from the D input to the Q output. The write and erase timing circuits are electronically interlocked by coupling the outputs from the write and erase timing circuits to the D input. Hence, the Q output will not change state and a write cannot be initiated if an erase or a previously initiated write is in progress i.e., the write timing is non-retriggerable.

The  $\bar{Q}$  output of IC17b is applied to the D input of a second D-type flip-flop (IC17a) which is clocked by the frame synchronizing pulses. The output from this flip-flop changes state on the next frame sync pulse after operating the 'WRITE' switch. This transition triggers a monostable multivibrator (IC11) whose pulse output both loads the contents of the thumbwheel switches into the two decade counters and resets the first D-type flip-flop. The counter then down counts the number of TV frames set on the thumbwheel switches and stops on the count of zero. The write pulse is equal in duration to the thumbwheel switch setting times 20 milliseconds.

#### 7.8.2 Computer initiated mode

Loading the DR11-B function bits with binary six or seven sets the INITIATE WRITE or INITIATE ERASE input LOW. The number of frames over which a write or an erase will occur is transmitted as two BCD digits on the low order 8-bits of the DR11-B data bus. This data is valid when the END CYCLE pulse is generated. With either INITIATE WRITE or INITIATE ERASE LOW, the END CYCLE pulse is gated to two 4-bit latches (IC1,2) which store the data on the data bus. The END CYCLE pulse also clocks a D-type flip-flop (IC13a) whose output is coupled to a NAND gate (IC14d). If any number other than zero is stored in the latches (IC1,2), the output from the 8-input OR gate (IC5) is HIGH which forces the contents of these latches to be multiplexed (IC18,19) to the programmable down-counters (IC22,23). The END CYCLE pulse is gated to the appropriate WRITE or ERASE



timing circuit and NANDed with the switch input to perform the same initiating function as the front panel switch.

If a zero is transmitted, the output from the OR gate (IC5) is LOW, forcing the thumbwheel switch settings to be applied to the programmable down-counters (IC22,23). Upon completion of the number of WRITE or ERASE frames, the WRITE/ERASE COMPLETED output goes HIGH clocking a D-type flip-flop (IC13b) which resets itself through the RC network (R9 and C1) and generates a short pulse which resets the first flip-flop (IC13a). This again multiplexes the contents of the thumbwheel switches to the down-counters allowing correct manual operation after the computer initiated mode.

### 7.8.3 Read amplifier clamp pulse generator

The read amplifier must be protected by clamping its input to a low impedance source before the storage target is elevated to the write or erase potential. The clamp must also remain operative for a short duration after returning to the read potential.

The write pulse generated by the write timing circuit is coupled through an integrator network (R16 and C4) to a Schmitt trigger (IC21). The integrator time constant is selected to generate a pulse approximately equal in duration to the original write pulse but delayed by 200 $\mu$ S. The inverted write pulse and the inverted delayed pulse are NANDed (IC20b) to generate a WRITE CLAMP pulse whose leading edge is coincident with the leading edge of the

original write pulse and the trailing edge is delayed by 200 $\mu$ S. The non-inverted write pulse is ANDed (IC20a,IC16a) with the non-inverted delayed pulse to generate a WRITE pulse whose leading edge is delayed 200 $\mu$ S and its trailing edge coincident with the trailing edge of the original write pulse. Hence, two pulses are generated, the WRITE CLAMP pulse commencing 200 $\mu$ S before the start of the WRITE pulse and its trailing edge delayed 200 $\mu$ S with respect to the WRITE pulse. Read, write or erase status is displayed by a light emitting diode.

## 7.9 Read amplifier

The signal current produced by the storage tube is typically 200nA which must be amplified in a high-gain, broad-bandwidth amplifier to produce a video signal of two volts peak-to-peak. At this point, the video signal is DC restored and the composite synchronizing signals added to generate a composite video output signal which may be displayed on any conventional television monitor. Such an amplifier is extremely sensitive to the point where it must be enclosed in a shielded box to prevent interference from external sources, see photographs 6 and 7. In conflict with the video amplifier's sensitivity, the storage target to which the amplifier is connected must be switched rapidly from 7 volt in the read mode to 17 volt in the erase mode, and to 200 volt in the write mode without destroying the amplifier.

### 7.9.1 Bandwidth considerations

The resolution of a TV system, expressed in TV lines, is the number of vertical black and white lines which are displayed in a width equal to the vertical height of the display. For example, 100 TV lines is represented by 50 black and 50 white vertical lines in a width equal to the vertical height. The total number of lines displayed in the active display width must be increased by the display aspect ratio of 4:3. Ideally, the video signal required to display these lines is a square wave as shown in figure 8. If the bandwidth was limited, then these lines could be approximated by a sine wave. The active horizontal scan

time is  $64\mu\text{s}$  minus the retrace blanking of  $12\mu\text{s}$ . If it is assumed that the storage tube has a limiting resolution of 600 TV lines, then there are  $(600/2 * 4/3)$  cycles in  $52\mu\text{s}$  resulting in a frequency of approximately 8MHz. Hence, the video amplifier must have a bandwidth in excess of 8MHz.

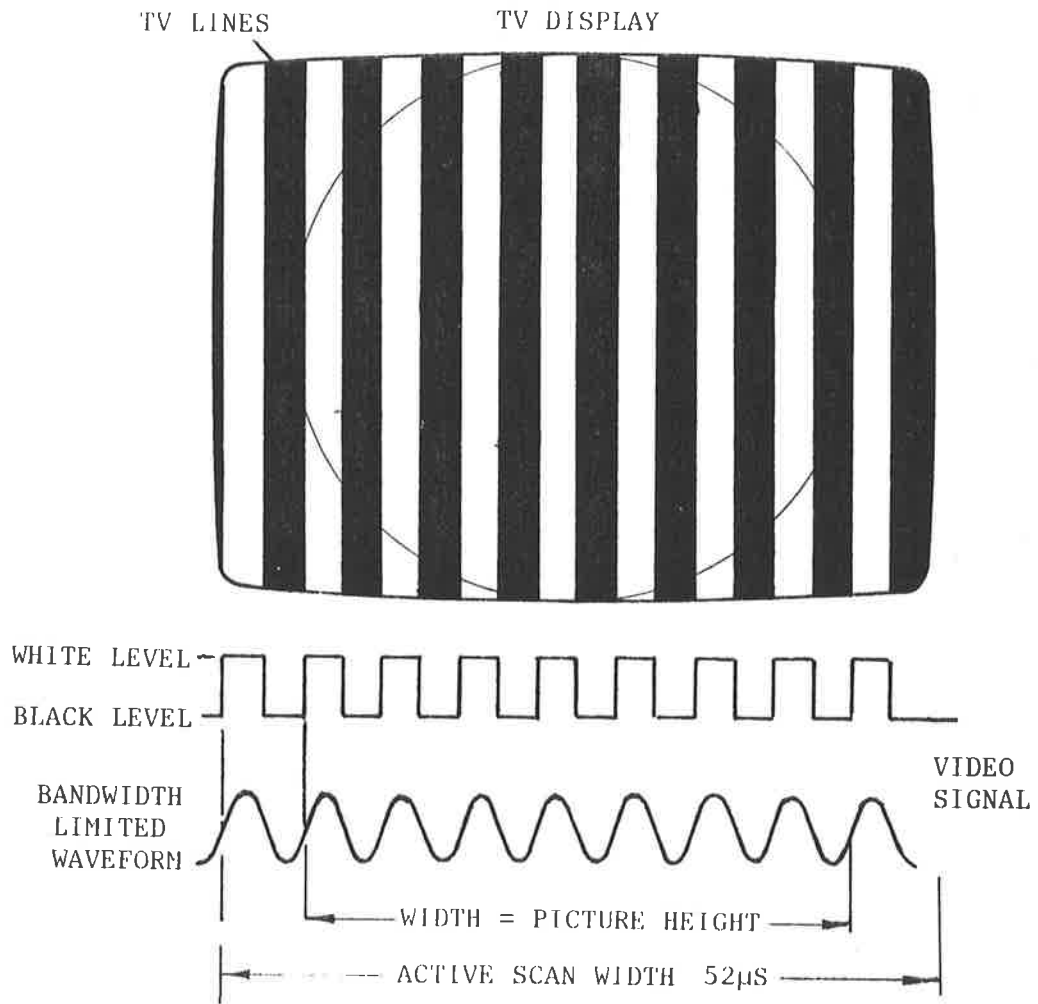


FIGURE 8. TV RESOLUTION TERMINOLOGY

### 7.9.2 FET video amplifier

The storage tube output impedance is similar to that of a conventional vidicon camera tube which is a high resistance shunted by the target capacitance, see figure 9. It is shown coupled to a video amplifier which is simplified as an input resistance shunted by the amplifier input capacitance and stray wiring capacitance. One approach in designing the video amplifier was to make the video amplifier input resistance low and combine it with a high-gain, broad-bandwidth amplifier. At the other extreme was a high input resistance design with unique amplifier characteristics.

The problems in designing a suitable video amplifier are highlighted by way of an example. If the amplifier input resistance is  $100K\Omega$ , as in the final design, and it is assumed that;

$$R_{\text{Target}} \gg 100K\Omega \quad \dots(1)$$

and  $C_{\text{Total}} = C_{\text{Target}} + C_{\text{Stray}} + C_{\text{Amplifier}} \quad \dots(2)$

$$= 20 \text{ pF} \quad \dots(3)$$

Then the frequency ( $f_{\text{RC}}$ ) at which the voltage developed across the amplifier input RC network is attenuated by 3db is given by;

$$f_{\text{RC}} = \frac{1}{2\pi} * \frac{1}{R_{\text{Amplifier}} * C_{\text{Total}}} \quad \dots(4)$$

$$= \frac{1}{2\pi} * \frac{1}{100 \times 10^3 * 20 \times 10^{-12}} \quad \dots(5)$$

$$\cong 80\text{KHz} \quad \dots(6)$$

Assuming a single pole network, the rate of attenuation is 20db per decade resulting in 20db attenuation at 800KHz and 40db attenuation at the minimum bandwidth of 8MHz as shown in figure 9. By comparison, an amplifier with a 1K $\Omega$  input resistance and the same capacitance has an input network bandwidth of 8MHz. Superficially, this may seem the best approach. However, the author's approach was to develop a high input impedance (HIGH-Z) design for the following reasons. Based on the assumption that the peak storage tube signal current is 200nA and the amplifier input resistance is 100K $\Omega$ , the video amplifier must provide 40db of gain over a minimum bandwidth of 8MHz to produce a two volt amplitude video signal. While the input network of the low input impedance design (LOW-Z) achieves the required bandwidth, the video amplifier must now have a gain of 80db. It can be seen that the attenuation caused by the input network of the high impedance design must be compensated for in the video amplifier with a gain characteristic which increases from 40db at 20db per decade from 80KHz to 8MHz. This biases the input amplifier noise towards the high frequency end of the spectrum where it is less discernible to the eye.

More importantly, the video amplifier required less DC gain, in this case 100 compared with a broadband gain of  $10^4$  for a 1K $\Omega$  input resistance design. Because of the unusual voltages applied to the storage target during the write and erase modes, the amplifier input was clamped to a

reference voltage. The low gain design ensured that slight variations in the clamp voltage did not saturate following stages when the clamp was applied.

Every attempt was made to reduce the amplifier input capacitance by use of a FET-transistor cascode amplifier (TR2,3), see figure II-11. Special consideration was given to printed circuit layout and placement of the printed circuit card to minimize lead length between the target electrode and the video amplifier, see photographs 6 and 7. Also, the gain-bandwidth product was maximized by coupling the amplifier output through an emitter follower (TR4) enabling a collector resistor of  $3K\Omega$  to be used. Measured bandwidth of the FET video amplifier is shown in photograph 8.



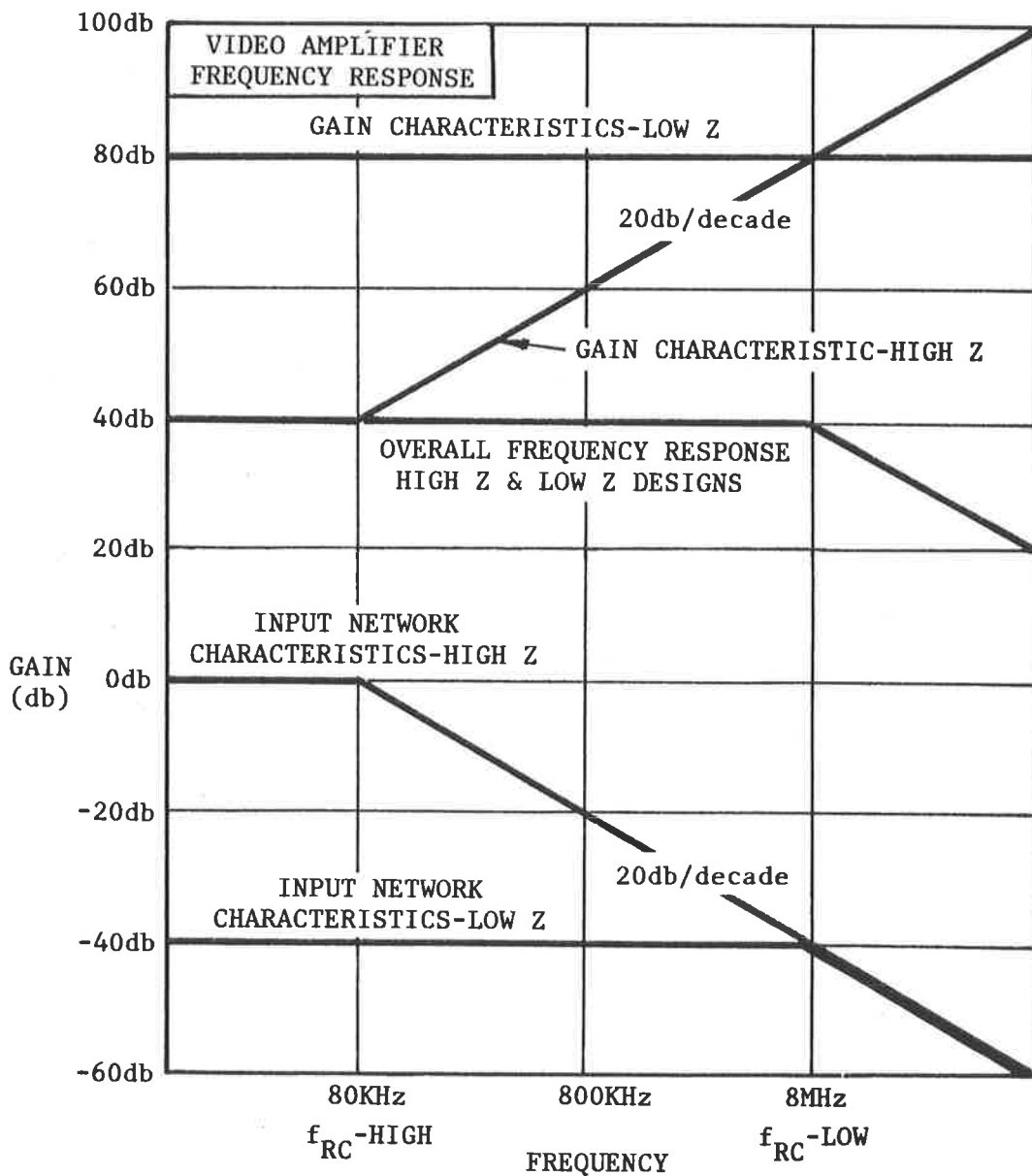
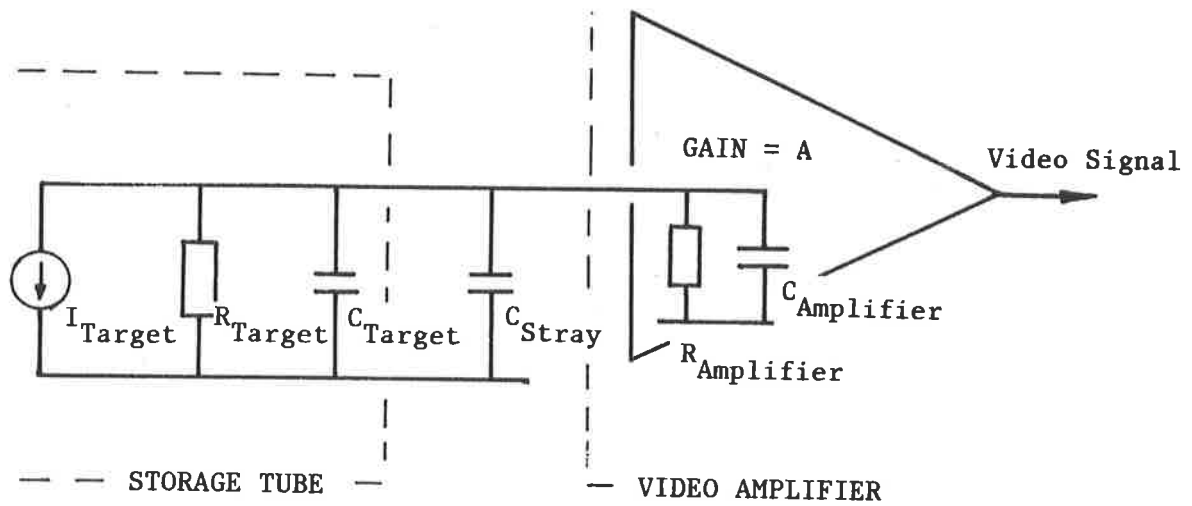


FIGURE 9. READ AMPLIFIER CHARACTERISTICS

### 7.9.3 Second-stage video amplifier

Output from the FET video amplifier is AC coupled (C10, C11) to a second-stage video amplifier (TR7-9) whose low frequency gain is approximately twelve. The purpose of this amplifier is to compensate for the input circuit attenuation by providing a gain characteristic which increases at 20db per decade from 80KHz, see figure 9. Additional gain in excess of 20db per decade is also provided to effectively reduce the scanning electron beam spot size (aperture correction). Not all of this gain can be achieved in one stage so that the frequency response is fabricated by decoupling a number of emitter resistors in the amplifier.

### 7.9.4 Sync/Video assembly

Output from the video amplifier is AC coupled (C16) to a FET source follower (TR10). Bias for the source follower is established by switching (IC1a) the FET gate to a DC potential during the line synchronizing period. In this way, the video signal, retrace blanking level is DC restored to a reference potential. Transients occurring during the retrace period are isolated from the video output section by a second analogue switch (IC1b) which is switched to its high impedance state during the composite blanking period. At this point, the synchronizing signals are added to the video waveform by a third analogue switch (IC1c) which shorts resistor R30 during the composite synchronizing period. The composite video signal is

buffered by a unity-gain amplifier (IC2) and coupled to a conventional TV monitor, see photograph 9.

#### 7.9.5 Storage target switching

One major consideration in designing the video amplifier was to protect the input FET (TR2) from voltage transients generated by switching the storage target to the erase or write potential. The approach was to connect the FET gate to the storage target via a diode (D1) and to clamp the FET gate to a low impedance source during these modes. The reasoning behind this is that the electron beam within the storage tube can be regarded as a piece of resistance wire which is connected to zero volt at the cathode. Since the FET gate is held at approximately 7.7 volt, the diode is always forward biased in the read mode. In the write and erase modes, the FET gate is clamped approximately 200 $\mu$ S both before and after the target is elevated to 200 volt and 17 volt respectively. Diode D1 is then reversed biased.

#### 7.9.6 Erase-write switching

Transistors TR5 and TR6 are switched off in the write mode and the storage target is connected to the 200 volt supply via resistor R12 and diode D2. A resistor (R11) has been added to discharge diode D2 when switching from the write mode to the read mode. In the erase mode, transistor TR5 is switched off and TR6 switched on, causing the collector of TR6 to bottom at the emitter voltage established by zener diodes D7 and D8 (17V). An EXCLUSIVE-

OR gate (IC8) has been added to force the system into the read mode if both erase and write are applied simultaneously.

#### 7.9.7 A/D converter video amplifier

As each row is digitized, the electron beam steps across each column of the stored image at  $2\mu\text{s}$  intervals. Simultaneously, the video output signal is applied to an A/D converter and converted to its digital equivalent. The A/D converter has a dynamic range of 0 to 10 volt, hence additional gain is required to interface the video signal from the second-stage video amplifier with the A/D converter. Output from the collector of transistor TR9 is buffered by an emitter follower (TR11) and AC coupled (C19) to a non-inverting amplifier (TR12,13). The video signal from this amplifier is AC coupled (C22) to a second emitter follower (TR15). At this point, the video signal blanking level is DC restored to zero volt by a transistor switch (TR14) which switches the base of transistor TR15 to the forward biased potential across diode D6. The diode compensates for the base-emitter voltage across transistor TR15. Transistor switch TR14 is normally operated and switched off as each row is digitized. In the worst case when digitizing 512 columns, the bias established across capacitor C22 must remain stable for  $1024\mu\text{s}$ . Transistor TR15 is a high gain transistor which minimizes discharge of capacitor C22. Output from the emitter follower (TR15) is applied to the analogue input of the A/D converter via a unity-gain buffer amplifier (IC11).

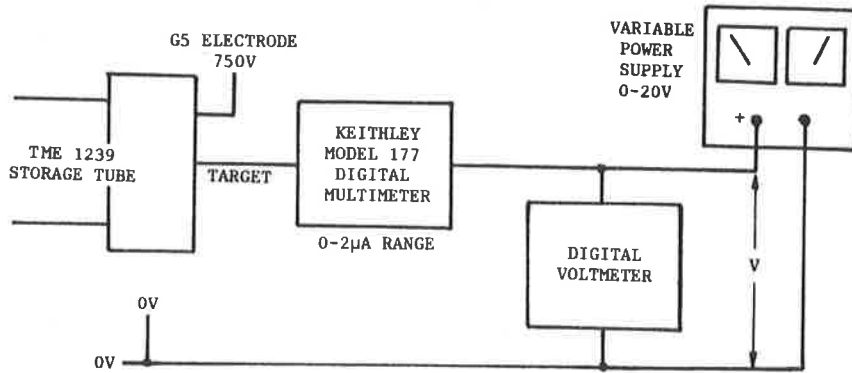
#### 7.9.8 Storage tube characteristics

Each storage tube is accompanied by a manufacturer's data sheet which specifies its optimum operational voltages. These voltages were adhered to in the design, however it was found that the stored image was compressed into the black level, i.e., the darker shades of grey were reproduced as black. Consequently, the storage target characteristics were investigated by measuring the target current with a digital microammeter. The microammeter was connected in series with the target and a variable power supply as shown in figure 10. The measured impedance of the microammeter on its  $2\mu\text{A}$  range was insignificant, approximately  $1.1\text{K}\Omega$ , and the voltage applied to the storage target electrode was measured at the power supply.

In operation, the power supply voltage was raised to 10 volt and the surface of the silicon dioxide blocks stabilized to cathode potential (0V) by erasing the storage tube. With the tube in the read mode, the target voltage was quickly lowered and target currents tabulated against the power supply voltages. The difference between the power supply voltage and the initial starting voltage was taken as the target surface potential. These values were then plotted as shown in figure 10. The process was repeated for a number of other voltages.

Operational voltages specified with the storage tube were 17 volt for erase and 5 volt for read, giving a black level target surface potential of -12 volt. The reason for

compressed black levels is obvious from the measured characteristics. Linear operation is best achieved with a maximum negative surface potential of -10 volt or a 7 volt read potential combined with a 17 volt erase potential. Appropriate measures were taken to incorporate this modification in the read amplifier design.



SCHEMATIC - MEASUREMENT CIRCUIT

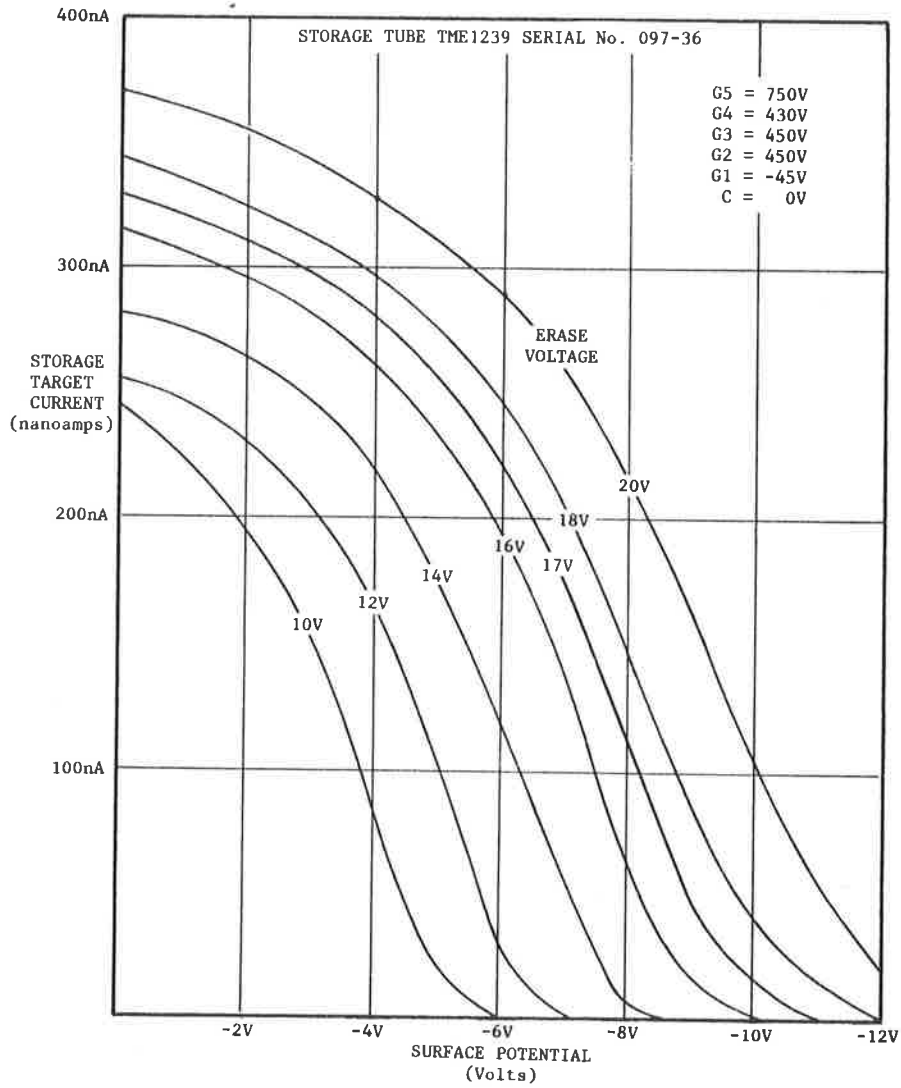


FIGURE 10. STORAGE TARGET CHARACTERISTICS

## 7.10 Write amplifier

Storing an image either from a conventional TV source or from data stored in the dual port memory, erasure and blanking are controlled by the write amplifier, see figure II-12.

### 7.10.1 Input video amplifier

A video input signal from any conventional TV source is coupled through a 'video level' potentiometer to a video amplifier which has a gain of approximately six. A small amount of high frequency peaking has been added by way of R6 and C2. Output from this amplifier is AC coupled (C4) to the gate of a FET source follower (TR3). Bias for the FET is established by an active clamp (IC11a) which charges capacitor C4 by shorting the FET gate to a reference potential during the line back porch period. The back porch clamp pulse is generated by triggering a monostable multivibrator (IC21) from the trailing edges of the line synchronizing pulses. In this way, the video signal blanking level is restored to a DC potential which is adjusted to correspond with the main video amplifier cut-off potential.

### 7.10.2 Programmable attenuator

Immediately after each digitally processed row is transferred from the PDP-11's central memory to the dual port memory, the Image Processing Terminal executes a linear horizontal scan as the data is clocked from memory, converted to an analogue signal and written on the storage



tube. Data is accessed at a  $2\mu\text{S}$  clock rate, hence the horizontal scan times are  $128\mu\text{S}$ ,  $256\mu\text{S}$ ,  $512\mu\text{S}$  or  $1024\mu\text{S}$  when either 64, 128, 256 or 512 columns of data respectively are returned for storage. Accordingly, the analogue signal applied to the storage tube must be attenuated in the ratio of 1:2:4:8.

The COLUMN SELECT 0 and 1 inputs are coupled to a 3 to 8 line decoder (IC20) which enables one of four transistors (TR4-TR7). Resistor R33 and the appropriate collector resistor (R35, R37, R39 or R41) then form a voltage divider network with the central point buffered by a high-impedance, unity-gain amplifier (IC15). Collector resistors R35, R37, R39 and R41 are adjusted to provide the necessary attenuation. Output from the buffer amplifier is coupled to a second non-inverting, unity-gain amplifier (IC16) which has a bias network (R44-R46) to bias an input voltage of zero volt to the cut-off voltage of -85 volt on the grid of the storage tube.

### 7.10.3 Video switching network

The control grid  $G_1$  operates over a wide range of voltage levels. For example, it is normally held at a DC potential of between -35 and -50 volt during the read mode and zero volt in the erase mode. When storing a conventional TV image, a video signal of approximately 30 volt peak superimposed on the grid cut-off potential of -85 volt is applied to the control grid. Proportionately less video signal is applied when storing a digitally

processed image on the storage tube. Also, electron beam blanking is applied during retrace by switching the control grid to a potential in the range -85 to -100 volt.

All of these voltages are derived from different sources. The appropriate input signal is selected from each source and coupled to the main video amplifier by one of six analogue switches (IC11b,c and IC13). One switch is enabled at any one time with selection controlled by the switching logic (IC1-8,10 & 12), see section 7.10.4 .

During the erase mode, the main video amplifier input is switched (IC13c) to a DC potential established across a potential divider network (R24-R26). A potentiometer (R25) is then adjusted for a grid potential of zero volt. Similarly, the main video amplifier input is switched (IC13a) to a second potential divider network (R27-R29) which allows adjustment of the grid potential from -35 to -50 volt in the read mode. When storing a conventional TV signal, the video input amplifier's output (TR3) is coupled to the main video amplifier by switch IC11b for the selected number of TV frames. The write blanking is applied by disabling switch IC11b and switching IC11c to the DC potential established across potentiometer R16. This voltage is adjusted for a blanking level of between -85 and -100 volt. It should be noted that there are two blanking adjustment potentiometers (R16 & R31). The video output transistor collector resistor (R54) is switched out of circuit in the write mode to achieve adequate bandwidth. This also changes the DC gain whereby the DC potential

applied to the input of the main video amplifier to maintain the same blanking level, differs for the write and erase modes. Switch IC13b is activated in the write-digital mode when coupling the output from amplifier IC16 to the main video amplifier.

#### 7.10.4 Video switching logic

Selection of the appropriate analogue switch is controlled by the video switching logic. In the read mode, the inputs WRITE TV, WRITE DIGITAL and ERASE are LOW and the output of gate IC4c is also LOW. A LOW on this output enables analogue switch IC13a which couples the DC potential on the 'READ' potentiometer (R28) to the main video amplifier. With any one input HIGH, the output of IC4c is HIGH and NAND gates IC5a, c and d are enabled. Application of the WRITE TV input over the selected number of TV frames then enables IC11b which interfaces the conventional TV video input signal with the main video amplifier. A HIGH on the WRITE DIGITAL input couples the video output from IC16 to the main video amplifier, while a HIGH on the ERASE input enables IC13c and switches the DC 'ERASE' potential to the main video amplifier. If any two or all three inputs are HIGH simultaneously, an error condition results and the output of IC4c goes LOW inhibiting the NAND gates and forcing the system into the read mode.

During the WRITE TV mode or WRITE DIGITAL mode, the main video amplifier bandwidth is increased by reducing the

video output transistor (TR10) collector resistance. A HIGH on either of these inputs causes the output of NAND gate IC7d to go LOW, switching the Darlington transistor in the optically coupled isolator (IC17) to its off state. Pull-up resistor R55 causes transistor TR11 to saturate, thereby switching collector resistor R54 out of circuit.

Conventional TV blanking or digital blanking is selected by a two-input multiplexer (IC2). When either the  $\overline{\text{MODE}}$  or the WRITE DIGITAL input is HIGH, digital blanking is multiplexed to the video switching logic. The  $\overline{\text{MODE}}$  input is HIGH during image digitization. During blanking, analogue switches IC11b, IC13a, b and c are disabled and switch IC11c or IC13d is enabled.

Since the DC gain of the main video amplifier is changed in the write mode, a different blanking level is required to establish the same cut-off potential of -85 volt on grid  $G_1$ . When in either the WRITE TV or WRITE DIGITAL mode, the output of IC5b is HIGH. This enables AND gate IC8a and directs blanking pulses to analogue switch IC11c which controls the blanking level in the write mode. In any other mode, the AND gate IC8b is enabled and the read blanking is applied by analogue switch IC13d.

#### 7.10.5 Main video amplifier

The main video amplifier operates between the grid cut-off potential of -85 volt during blanking and zero volt during erasure. For this reason, the video amplifier was designed to operate from -100 volt and +18 volt power

supplies. The storage tube normally operates in the read mode and is switched to the write or erase modes for short periods only. In the read mode, grid  $G_1$  operates at a DC potential of between -35 and -50 volt. Unfortunately this is close to the point of maximum dissipation for the video output transistor (TR10) and is exacerbated by the fact that the collector resistance must be low to achieve a bandwidth in excess of 8MHz.

The problem has been overcome by using two collector resistors, R53 and R54, which in the read or erase mode presents a  $5.7K\Omega$  load resistor to the video output transistor (TR10). However, in the write mode, resistor R54 is shorted by a transistor switch (TR11) which is operated by an optically coupled isolator (IC17). This opto-isolator is activated only in the write mode causing the video output transistor to operate into a  $1K\Omega$  collector resistance. Measured frequency responses of the main video amplifier are shown in photographs 10 & 11.

#### 7.10.6 Storage tube electrode potentials

The electron beam within the storage tube is focused either by varying the potential on grid  $G_4$  or by varying the current flowing through the magnetic focus coil. In adherence with the manufacturer's specified operating potentials, the electrostatic focus potential on grid  $G_4$  is maintained at 430 volt by a resistive divider network, R59 and R60 coupled to the 450 volt supply. The accelerator grid  $G_2$  is maintained at a potential of 450 volt, with

resistor R63 and capacitors C18 and C19 providing a filter network.

Unlike a vidicon electron gun assembly, the storage tube incorporates an additional grid  $G_3$ , which when grounded, defocuses the electron beam and greatly increases the beam current to minimize the erasure time. If this electrode is maintained at 450 volt, the electron beam is neither defocused nor is the beam current increased. The potential for this electrode is derived from the collector of a high voltage transistor (TR12). With the SLOW/FAST ERASE input HIGH, grid  $G_3$  is maintained at the collector-emitter saturation voltage, approximately zero volt, and with the SLOW/FAST ERASE input LOW, grid  $G_3$  is maintained at 450 volt. This mode is used when slowly erasing the tube or when erasing selected areas of the stored image.

The cathode is maintained at zero volt and the filament is supplied from the unregulated 5 volt supply, see figure II-16.

## 7.11 Sync separator/generator

During normal operation, the video input signal is coupled to the sync separator which recovers the line and frame synchronizing pulses for synchronization of the Image Processing Terminal. Alternatively, the Image Processing Terminal may be synchronized from an internal sync pulse generator. A circuit diagram of the sync separator/generator is shown in figure II-13.

### 7.11.1 Line sync separator

An integrated circuit synchronization pulse separator (IC1) recovers the composite synchronization pulses from the video input signal. Included in the integrated circuit is a line oscillator and phase locked loop (PLL) which recover the line synchronization pulses. The leading edges of these pulses are phased by means of the 'PHASE' control to be coincident with the commencement of the line blanking signal.

### 7.11.2 Frame sync. separator

Frame synchronizing pulses are recovered from the composite synchronizing pulse waveform by an integrator-clipper circuit (R20,21,C12,13,TR2 & 3), see figure 11. The recovered frame synchronizing pulses then reset an astable multivibrator (IC11). When the video input signal is disconnected, the composite synchronizing pulse waveform is not generated by the integrated circuit sync separator (IC1) and the astable multivibrator functions as the frame

oscillator. The multivibrator must be set to a frequency of less than 50Hz for correct synchronization.

By convention, the frame blanking is applied 160 $\mu$ S before the frame sync pulse. This duration is commonly referred to as the frame front porch. The frame blanking pulse is recovered by a phase locked loop (IC12) which anticipates the frame synchronizing pulse. With reference to figure 11, the positive edge of the PLL's voltage controlled oscillator triggers a monostable multivibrator whose output pulse width is set to 160 $\mu$ S. The trailing edge of this pulse is maintained coincident with the leading edge of the recovered frame sync pulse by the edge sensitive phase locked loop. Hence, the voltage controlled oscillator output is locked to the leading edge of the frame blanking signal.

### 7.11.3 Synchronization pulse generator

The Image Processing Terminal incorporates an industrial standard synchronization pulse generator. A combined oscillator, binary divider (IC2) divides a 4MHz crystal frequency in binary stages to produce 31.25KHz and 15.625KHz. The 31.25KHz is further divided by 625 to arrive at a 50Hz frame frequency. Generation of the 15.625KHz line frequency and 50Hz frame frequency by this technique results in the necessary half-line offset between alternate frames to produce a 2:1 interlace.



#### 7.11.4 Sync pulse multiplexer

Line and frame frequencies from either the internal sync pulse generator or the sync separator are selected by a quad two input multiplexer (IC8). Selection is controlled by the INT/EXT SYNC switch. When in the INT SYNC position, the write timing circuit is inhibited, see figure II-10.

#### 7.11.5 Pulse generation

Two monostable multivibrators (IC6,7), one of 12 $\mu$ S pulse duration (line blanking) and one of 1.5 $\mu$ S duration (line front porch) are triggered by the positive edge of either the line sync pulse or the line frequency. The trailing edge of the 1.5 $\mu$ S pulse triggers a third monostable multivibrator (IC6) of 5 $\mu$ S pulse duration (line synchronization). Similarly, the positive edge of the frame frequency triggers two monostable multivibrators (IC7,9), one of 1mS duration (frame blanking) and one of 160 $\mu$ S (frame front porch) which triggers a third monostable multivibrator (IC9) generating a 200 $\mu$ S frame synchronization pulse. Line and frame synchronization and blanking pulses are ANDed (IC10) to generate the composite synchronization and composite blanking waveforms.

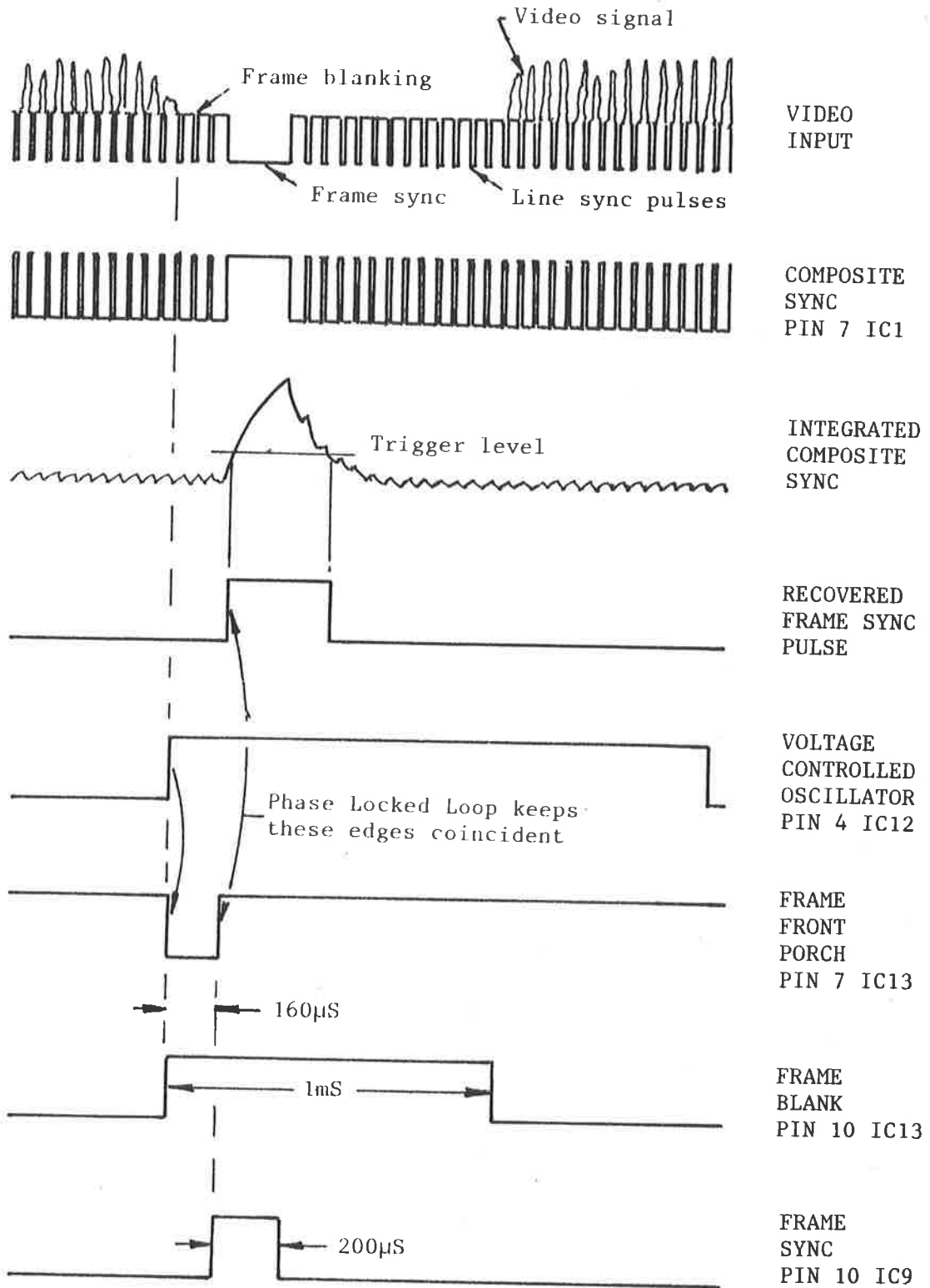


FIGURE 11. SYNC SEPARATOR WAVEFORMS

## 7.12 Frame scan

The frame or vertical scan operates in either a normal TV scan mode which is a linear ramp of approximately 19.8ms duration and 20ms period or a staircase mode. In the staircase mode, the vertical scan may be positioned on any row by loading the row counter and it remains stationary when digitization is in progress or when digital data is being loaded into the dual port memory. For this reason, the vertical scan was DC coupled, see figure II-14.

### 7.12.1 TV frame scan generator

The normal TV frame scan waveform is generated by charging a capacitor (C28) from a constant current source (T13) and discharging the capacitor through a transistor switch (T12) driven by the frame synchronization pulses. Capacitor C28 is held at zero volt when either digitizing an image or writing a digitized image on the storage tube. The scan waveform is coupled to the frame switching network by a high input impedance buffer amplifier (IC12).

### 7.12.2 Frame scan switching

Scan selection is implemented in a dual emitter follower (T14,15) with a common emitter resistor (R60). Bias for the emitter followers is established by connecting the base resistors (R59,R61) to the open collector outputs of two voltage comparators (IC13). Comparator switching levels are made TTL compatible by connecting their reference inputs to a potential divider network (R63,R64).

A HIGH on the FRAME SYNC INHIBIT input enables gate IC11c which directs frame synchronizing pulses to the capacitor reset switch (T12) and switches the output of comparator IC13a to its high output impedance state. Simultaneously, the output of IC13b is switched to -5 volt reverse biasing transistor T15. The normal TV scan waveform is then coupled to the emitter resistor (R60) by emitter follower T14.

The FRAME SYNC INHIBIT input is LOW when digitizing an image or when writing digitally processed images on the storage tube. Comparator IC13a is switched to its low output impedance state, reverse biasing transistor T14. Capacitor C28 is held at zero volt by transistor switch T12 and the vertical scan staircase waveform is coupled to emitter resistor R60 through emitter follower T15.

### 7.12.3 Frame scan driver

The frame scan driver has the appearance of a conventional operational amplifier with feedback resistor (R69 + R70) and gain determined by the ratio of  $[(R69 + R70)/R65]$ , see figure 12. One difference exists, the vertical deflection coil is coupled between the amplifier output and a sense resistor (R74) with feedback taken from the sense resistor.

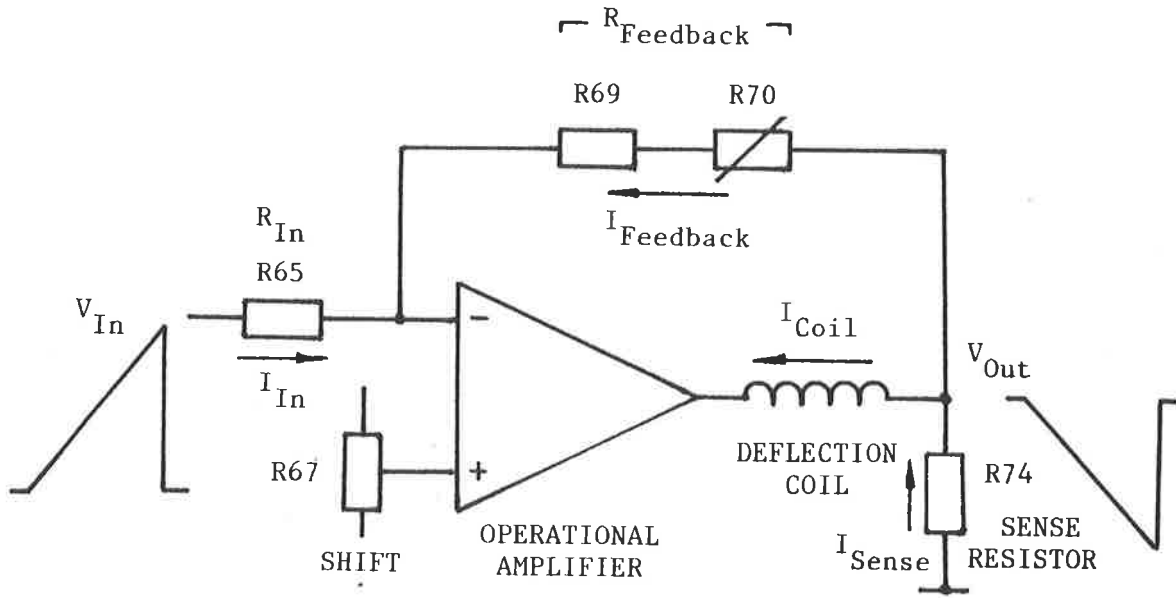


FIGURE 12. FRAME SCAN DRIVER

Applying simple operational amplifier techniques, the output voltage of this circuit is given by;

$$V_{Out} = -A * V_{In} \quad \dots(7)$$

where,

$$A = [(R69 + R70)/R65] \quad \dots(8)$$

and the current flowing in the sense resistor is;

$$I_{Sense} = V_{Out}/R74 \quad \dots(9)$$

If it is assumed that the feedback current is insignificant, then the current flowing through the deflection coil is approximately equal to the current flowing through the sense resistor,

$$\text{and} \quad I_{Coil} \cong -A * V_{In}/R74 \quad \dots(10)$$

In essence, the circuit is a voltage to current converter which self generates the voltage waveform required to drive the deflection coil.

Most of the operational amplifiers examined in the developmental phase exhibited significant cross-over distortion. Finally, an LH0061 power amplifier was selected. Although this amplifier gave unnoticeable cross-over distortion when examined with a current probe, a slight amount of distortion was apparent when the storage tube was operational. The amplifier was replaced by a combination of an LM301A operational amplifier (IC15) driving an MC1438R unity-gain power amplifier (IC16). Typical voltage and current waveforms are shown in photographs 12 and 13. All currents were measured with a Tektronix P6302 Current Probe and AM503 Current Probe Amplifier.

### 7.13 Line scan

The line or horizontal scan operates in the following modes;

- (a) Normal TV scan during READ(TV), WRITE(TV) and ERASE which is a  $59\mu\text{S}$  linear ramp with a period of  $64\mu\text{S}$ .
- (b) Staircase during DIGITIZATION comprising either 64, 128, 256 or 512 steps, each of  $2\mu\text{S}$  duration.
- (c) Slow-scan during WRITE (DIGITAL) with linear ramps of 128, 256, 512 or  $1024\mu\text{S}$  duration.

Scan selection is controlled by the scan control/interlock circuit, see section 7.7 .

#### 7.13.1 Slow-scan/TV scan ramp generators

The horizontal slow-scan and TV scan waveforms are generated by charging a capacitor (C2) from one of five constant current sources (T2-T6) and discharging the capacitor with a transistor switch (T1), see figure II-14.

When the SLOW-SCAN ENABLE input is LOW, constant current source T2 is disabled and a 3 to 8 line decoder (IC2) is enabled. The two-bit code defining 64, 128, 256 or 512 columns applied to the COLUMN SELECT 0 and 1 inputs enables one of four constant current sources (T3-T6). Resistors R8, R12, R16 and R20 vary the current in each constant current source and are adjusted to charge capacitor C2 to 5 volt in 128, 256, 512 and  $1024\mu\text{S}$  respectively. Line synchronizing pulses are inhibited by

gate IC1a and the DIGITAL BLANKING is applied to the transistor switch (T2) via gate IC1b and c.

In the TV scan mode, the SLOW-SCAN ENABLE input is HIGH which disables the 3 to 8 line decoder and constant current sources T3-T6. Bias is applied to zener diode D1 and constant current source T2 is enabled. Simultaneously, gate IC1c is enabled and line synchronizing pulses operate transistor switch T1. Resistor R4 is adjusted for a ramp amplitude of 5 volt. The ramp waveform is coupled to the scan switching network by a high input impedance buffer amplifier (IC4).

#### 7.13.2 Line scan switching

Selection of either the slow-scan/TV scan waveforms or the horizontal scan staircase waveform is implemented by the scan switching network (IC5). Circuit operation is identical to the frame switching network with the exception that switching is controlled by the LINEAR SCAN INHIBIT input.

#### 7.13.3 Line scan driver

Development of the horizontal scan was complicated by the fact that the storage tube required a 1.5 inch deflection yoke. These yokes were developed for the 1.5 inch vidicon camera tube which did not gain the same level of commercial acceptance as the 1 inch and 2/3 inch vidicon camera tubes. As a result, the choice of a deflection coil was limited to designs which dated back to



the valve era. They characteristically operated at high voltage, i.e., high inductance and low deflection current as opposed to transistor circuits which operate at low voltage and high current. A 'Cleveland Electronics' Model 15VY-258 deflection coil was finally chosen because it offered centre tapped deflection coils which suited a deflection driver design outlined in U.S. Patent 3,426,241, reference 11. In this patent, an inductor with approximately 50 times the inductance of the deflection coil couples the centre tap of the coil to a low voltage power supply. Each coil is driven in push-pull by two power transistors as shown in figure 13, and each transistor operates as a class-A amplifier with a bias current of  $I_{DC}$ . This results in a quiescent current of  $2 \cdot I_{DC}$  flowing through the inductor. In principle, during rapid deflection, one drive transistor saturates with the net result that the quiescent current cannot be maintained through the inductor. This current change is opposed by the inductor which then increases the voltage at the deflection yoke centre tap to accommodate the higher deflection rate.

In practice, difficulty was experienced in preventing the inductor from ringing during the horizontal retrace, and as a result, the circuit was evaluated without the inductor by coupling the centre tap of the deflection coil to a separate high voltage power supply. While this circuit gave promising results when monitored with a current probe, it proved useless in practice because the

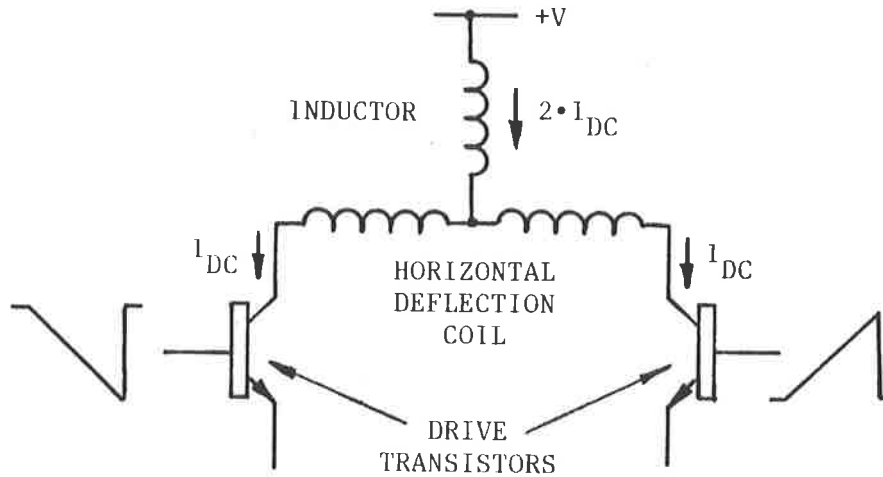


FIGURE 13. SCHEMATIC DEFLECTION COIL DRIVER U.S. PATENT 3,426,241

storage tube would not focus uniformly. Closer examination of the horizontal deflection coils showed them to be two sets of rectangular, concentric windings on diametrical sides of the former. While in theory the two magnetic fields cancelled each other, the windings were such that they were not precisely matched. Hence the magnetic field produced by the bias currents interacted with the magnetic field generated by the focus coil. At this stage, the horizontal deflection coil was modified by connecting the two windings in parallel to reduce the inductance and therefore the maximum voltage required for retrace.

A considerable amount of effort was expended in the search for a wide-bandwidth operational amplifier with high slew rate, high voltage and large current characteristics. Eventually, a hybrid amplifier was arrived at which incorporated a wide-bandwidth operational amplifier (IC7)

coupled to a high voltage, high current transistor amplifier (T9-T11) and employing the same feedback techniques as for the frame scan driver. Typical line scan voltage and current waveforms are shown in photographs 14 and 15.

#### 7.14 Magnetic focus

The scanning electron beam within the storage tube is both electrostatically and magnetically focused. Magnetic focus is achieved by maintaining a constant current through the focus coil. A  $\mu$ A723 precision voltage regulator (IC10) is used as a constant current source by configuring the internal series pass transistor as an emitter follower, with the focus coil and a sense resistor (R53) in the emitter circuit, see figure II-15. A voltage proportional to the current flowing through the focus coil is developed across the sense resistor. This voltage is compared in an internal operational amplifier with a voltage developed across a potential divider network (R49-R51) coupled to the internal reference voltage. Output from the operational amplifier is internally connected to the base of the series pass transistor thus closing a feedback loop which maintains a constant current through the focus coil.

#### 7.15 Magnetic alignment

The deflection coil assembly is fitted with vertical and horizontal alignment coils which correct for the angle of emission of electrons from the cathode of the electron gun assembly. Each alignment coil is driven by a unity-gain buffer amplifier (IC8,9), figure II-15, whose input voltage is variable over  $\pm 5$  volt resulting in a current adjustment of approximately  $\pm 30$ mA.

#### 7.16 Power supply.

The storage tube requires a relatively large number of operating voltages such as 750 volt for the  $G_5$  mesh electrode, 450 volt for the  $G_2$  accelerator electrode, 200 volt for the write switching circuit and 6.3 volt at 600 millamperes for the filament. Also, -100 volt is required for the write amplifier which drives the control grid  $G_1$ .

Because of a limited selection of 1.5 inch deflection yoke/focus coils, a minimum voltage of 45 volt is required to effect horizontal retrace in less than  $10\mu\text{S}$ , and 28 volt is required for the focus coil. In addition to this, the electronics operate from  $\pm 15$  volt, 12 volt and 5 volt supplies. All of these voltages are derived from a single 240 volt 50Hz transformer as shown in figure II-16. Integrated circuit voltage regulators are used for the 45 volt, 28 volt,  $\pm 15$  volt, 12 volt and 5 volt supplies. The unregulated 450 volt supply is obtained by a full-wave bridge (D7-D10) coupled to two 175 volt transformer windings connected in series. It can be seen that the centre tap of this winding (0V) is full-wave rectified at the transformer output by the action of the 450 volt supply diode bridge. This output is peak detected by a diode (D6) to generate a DC supply of approximately 250 volt which is regulated by a series pass transistor (TR3). Bias for the series pass transistor is established by two 100 volt zener diodes (D16,17). A similar circuit is employed for the 450 volt supply where a high voltage series pass transistor (TR2) is biased at 450 volt by a number of zener diodes (D11-D15). The 750 volt unregulated

supply is generated by AC coupling (C1) a 50Hz output from the transformer and diode clamping (D1) the most negative excursion to the unregulated 450 volt supply. This combined voltage is then peak detected by a diode (D2) to give approximately 800 volt. Another high voltage series pass transistor (TR1) with its base biased 300 volt above the base of TR2 provides the regulated 750 volt supply.

A separate -100 volt supply is provided by full-wave rectification of the voltage output from secondary winding No. 2 and regulating the voltage in a series pass transistor (TR4) with its base biased by a 100 volt zener diode (D25). Currents drawn by each power supply are shown in Table 2.

TABLE 2. POWER SUPPLY OPERATING CURRENTS

SUPPLY	READ	ERASE	WRITE
750V	1 $\mu$ A	50 $\mu$ A	0.5 $\mu$ A
450V	460 $\mu$ A	2.8mA	400 $\mu$ A
200V	4.3mA	4 $\mu$ A	4mA
45V	36mA	36mA	36mA
28V	184mA	201mA	192mA
15V	200mA	200mA	200mA
12V	55mA	55mA	55mA
5V	1.45A	1.45A	1.45A
-15V	210mA	210mA	210mA
-100V	7.5mA	16mA	21mA

### 7.17 H.T. inverter

Voltages for the storage tube were initially generated by a DC to DC inverter, see figure II-17. Switching transients were isolated to the line blanking period by dividing the line blanking input by two and driving the switching transistors (TR1,2) at half line frequency ( $\cong 7.8\text{KHz}$ ). The switching transistors were protected against loss of drive by AC coupling the complementary outputs from the divider to the bases of the switching transistors. The primary winding centre tap was coupled to the emitter of a series pass transistor (TR3) which was controlled by a  $\mu\text{A723}$  voltage regulator (IC4). Feedback was applied by comparing a proportion of the 450 volt output voltage, derived from a potential divider network (R6-R8), with the internal reference voltage of the  $\mu\text{A723}$  regulator. Additional supplies of -100 volt, 750 volt, 200 volt and 6.3 volt were also generated. While the circuit gave excellent regulation, the system still required additional power supplies such as 45 volt, 28 volt and the low voltage power supplies. Also, switching transients during the line blanking period upset the video clamp circuitry, see section 7.9.4, producing a DC offset between alternate scan lines. For these reasons, the H.T. inverter was replaced with a single, mains operated power supply which generated all the operational voltages.

## 8. TESTING

The electronics design was isolated into a number of subsections which were constructed on individual printed circuit cards. All printed circuit artwork and assembly of the printed circuit cards were performed by the author. Most of the analogue circuits were developed and tested as small prototype units before being taped onto larger printed circuit cards.

A major proportion of the digital interface electronics was taped on one large printed circuit card without prior testing of individual circuits. Figure II-20 shows a reduced version of the printed circuit artwork. While this approach represented a considerable amount of effort on the author's part, this was offset by the time needed to debug the card due to easier component identification, easy to follow track layout and its robustness i.e., wires not falling off due to mechanical stress. Invariably, any printed circuit card of this magnitude may have track layout errors, faulty components, logic errors and timing errors, any one of which would prevent the system from functioning. Commissioning of the card was approached in three stages, by manually exercising the card, exercising the card with an Intel SDK-85 microcomputer kit and finally, proving the system against the DR11-B interface bus.

### 8.1 Manual testing

A system for simulating the DR11-B interface bus was devised which proved invaluable in checking the printed circuit card for layout errors, logic errors and faulty components, see figure II-18. The 16-bit data bus out of the



DR11-B was simulated by four hexadecimal switches and the 16-bit data bus into the DR11-B was displayed on four hexadecimal displays. Additionally, the three function bits were generated by using the first eight positions of a hexadecimal switch. The interface electronics were reset by an 'INITIALIZE' switch. An END CYCLE pulse, simulating the end of each data transfer, was generated by triggering a 100ns monostable multivibrator from an output of two cross-coupled NAND gates. The gates were toggled by a front panel 'END CYCLE' switch.

A significant proportion of the electronics was tested with the aid of this device without connecting the storage tube, thereby minimizing the risk of damage to the tube during the developmental phase. For example, the row number was set on the hexadecimal switches and loaded into the row counter by exercising function one. The contents of the row counter were then displayed on the hexadecimal displays by selecting function zero. Any discrepancy between these two values pointed to an obvious fault which could be traced by applying static logic levels.

It was possible to load data into consecutive memory locations within the dual port memory by setting the data on the hexadecimal switches, selecting function three, and operating the END CYCLE switch. The END CYCLE pulse stored the data and incremented the word transfer counter to the next memory location. Again, the integrity of the stored data could be checked by resetting the electronics within the Image Processing Terminal and selecting function two - READ FROM

RAM. The contents of each memory location were displayed on the hexadecimal displays by sequentially stepping through the memory with the END CYCLE switch. It was also possible to initiate digitization but instead of using the video output from the storage tube, either one binary output from the column counter or the horizontal staircase waveform was applied to the video input of the A/D converter. The contents of the memory were then interrogated by exercising function two to ensure that the stored data alternated between a high and a low value or alternatively incremented in an ascending order.

## 8.2 Microcomputer testing

While the manual system proved invaluable for testing the Image Processing Terminal, it could not be used to check the system dynamically. This task was fulfilled by an Intel SDK-85 microcomputer kit which offered a large number of Input-Output (I/O) ports for simulating the DR11-B interface bus. Connections to these ports are shown in Table 3.

Instead of using separate I/O ports for the two 16-bit data buses, a technique similar to the internal connections within the DR11-B interface bus is employed, see figure II-19. Two 8-bit microcomputer I/O ports are connected to sixteen bi-directional buffers which separate the I/O ports into a 16-bit output bus and a 16-bit input bus. Data direction is controlled by the DATA DIRECTION bit. Additionally, the microcomputer generates the same outputs as the manual interface tester i.e. INITIALIZE, END CYCLE and the three

TABLE 3. SDK-85 MICROCOMPUTER I/O PORT ALLOCATION

(A) PORT 21H-DATA

BIT	DESCRIPTION
7	DRDB 07
6	DRDB 06
5	DRDB 05
4	DRDB 04
3	DRDB 03
2	DRDB 02
1	DRDB 01
0	DRDB 00

(B) PORT 22H-DATA

BIT	DESCRIPTION
7	DRDB 15
6	DRDB 14
5	DRDB 13
4	DRDB 12
3	DRDB 11
2	DRDB 10
1	DRDB 09
0	DRDB 08

(C) PORT 23H-FUNCTION

BIT	DESCRIPTION
5	Not Used
4	DATA DIRECTION
3	FNCT 3
2	FNCT 2
0	FNCT 1

(D) PORT 00H-COMMAND

BIT	DESCRIPTION
7	Not Used
6	Not Used
5	Not Used
4	DSTAT A
3	DSTAT B
2	DSTAT C
1	INITIALIZE
0	END CYCLE

DATA DIRECTION:  
 0 = Read into SDK-85  
 1 = Output from SDK-85

function bits FNCT 1, 2 and 3. In order to operate dynamically, the microcomputer has access to the three device status bits DSTAT A, B and C.

Assembly language programs for exercising the Image Processing Terminal are shown in Appendix III. Superficially these programs may seem complex but in fact, the annotation proved more time consuming than writing the programs. The programs were used to erase the storage tube, store an image from a conventional TV source, write a series of black and white vertical bars or a staircase function on the storage tube and digitize an image. Before attempting to use any of

these programs, the stack pointer and I/O ports were defined by executing the 'START' program which commenced at address 2036.

The greatest advantage of the microcomputer was the ability to change quickly from executing a program once to operating in a continuous loop. Timing sequences within the Image Processing Terminal could then be observed on an oscilloscope by triggering the oscilloscope from pulses generated by specific events. For example when executing the program 'WRCOL', the WRITE ROW NUMBER output (figure II-3) goes LOW just before transmission of data to the dual port memory. Programs 'WRCOL', 'WRST' and 'DIGIT' are written as continuous loops by jumping back to the start of each program. When operating in their normal modes, the jump instruction (C3) is changed to the restart instruction RST1(CF) and each program is executed once before the microcomputer returns to the monitor program.

Photograph 16 shows the square wave output from the video D/A converter (IC73, 75 and 76, figure II-8), resulting from using the program 'WRCOL' to write a series of black and white vertical bars on the storage tube. Photograph 17 shows the stored image.

## 9. COMPUTER PROGRAMMING - IMAGE PROCESSING TERMINAL

Communication between the Image Processing Terminal and the PDP-11 computer is controlled by the four DR11-B interface bus registers. Each register has a specific address within the I/O page, see figure 5. The computer's operating system prevents a non-privileged or general user from making direct access to any registers within the I/O page. Also, the bus address register (DRBA) and extended bus address bits (XBA16 & 17) are loaded with 18 bits which specify a physical address in the PDP-11's central memory where data transfers will commence. Since the PDP-11 word is 16 bits in length, it can address 32K words of memory. These addresses are virtual addresses which are mapped into 18-bit physical addresses by the Memory Management Unit and the user program may be loaded into any memory segment/s which is/are unknown to the user. It can be seen that the data buffer in central memory must be linked with the Image Processing Terminal program.

Both of these problems have been overcome by declaring the I/O page and the data storage area as COMMON blocks. One COMMON block 'EXT' maps over the I/O page, octal address 760000 to 777777, and a second COMMON block 'IDATA' maps over 1024 words of central memory commencing at octal address 216600.

### 9.1 FORTRAN programming

FORTRAN IV is the most convenient programming language for addressing the Image Processing Terminal, see Appendix IV. Access to the DR11-B registers is gained by declaring a 4K word integer array IARRAY(4096) COMMON with the previously

installed COMMON block, 'EXT'. Since the array is integer, each variable is stored as a 16-bit word, hence variable IARRAY(1) has the address 760000 octal. In general, the variable IARRAY("N) has the address ["760000 + 2\*("N-1)]. Thus IARRAY ("5205) has the same address as the DR11-B word count register (DRWC). The three consecutive array variables have the addresses of the remaining DR11-B registers. Use of the FORTRAN EQUIVALENT declaration enables the four array variables to be defined by their mnemonic names as shown in Table 4.

TABLE 4. VARIABLES DEFINING DR11-B INTERFACE REGISTERS

ARRAY VARIABLE	PHYSICAL ADDRESS	MNEMONIC
IARRAY ("5205)	"772410	DRWC
IARRAY ("5206)	"772412	DRBA
IARRAY ("5207)	"772414	DRST
IARRAY ("5208)	"772416	DRDB

#### 9.1.1 Integer constants

A number of integer constants are defined in Appendix IV which are 16-bit words with one or two bits set. Again, for ease of comprehension, the integer constants have mnemonic names which equate with functions in the command and status register, see Table 5.

-----  
" specifies an octal number



the appropriate mask with the command and status register. For example, the FORTRAN statement,

```
IF((DRST.AND.DSTAT A).EQ.0) Statement 1 ...(12)
Statement 2
```

tests the status of DSTAT A. If DSTAT A is clear, statement 1 is executed and if DSTAT A is set, the program executes statement 2.

#### 9.1.5 Loading the word count register

If the variable COLS is set to the number of columns over which digitization will be implemented, then the number of words transferred to the PDP-11 computer is equal to half the number of columns, i.e.,

```
WORDS = COLS/2 ...(13)
```

The word count register is loaded with the two's complement of the number of word transfers by the FORTRAN statement,

```
DRWC = -WORDS ...(14)
```

#### 9.1.6 Loading the bus address register

The data buffer is located at a physical address of 216600 octal and the low order 16-bits of this 18-bit address are loaded into the bus address register by the FORTRAN statement,

```
DRBA = IBASE ...(15)
```

where

```
IBASE = "16600 ...(16)
```

In order to define address "216600, the extended bus address bits XBA16 and XBA17 must be set to 1 and 0



respectively. These bits are loaded into the command and status register by the FORTRAN statement:

```
DRST = XBA + .....                               ...(17)
```

The extended bus address bits are aligned in the command and status register by combining XBA16 and XBA17 and setting,

```
XBA = "20                                         ...(18)
```

#### 9.1.7 Executing a function

The statement

```
DRST = XBA + (FNCT * 2) + GO                       ...(19)
```

sets the extended bus address bits, enters the function code into the function bits and sets the GO bit in the command and status register.

#### 9.1.8 Creating a PDP-11 executable program

Firstly, the FORTRAN source program is compiled to create the object program. The object program is then submitted to a PDP-11 system program called the Task Builder which creates a machine executable program. Program references to the COMMON storage areas 'EXT' and 'IDATA' are resolved by including the following Task Builder options;

```
 /  
COMMON = EXT:RW:7  
RESCOM = IDATA/RW:6                               ...(20)  
 //
```

Appendix IV shows a FORTRAN IV program which exercises all eight functions within the Image Processing



Terminal. Firstly, the program erases the storage tube over 100 TV frames and then stores a conventional TV image. The image is digitized over 128 rows by 64 columns and stored on disk after which, the storage tube is again erased and the digitized image returned from disk to the storage tube for viewing at normal TV scan rates. Photograph 21 shows the result of executing this program to digitize a chequer-board pattern from a video test pattern generator.

## 10. SYSTEM PERFORMANCE

An evaluation of the Image Processing Terminal is presented in the following sections. Where possible, the descriptions are supplemented by photographs of the TV display. It should be noted that photography of a TV display is often difficult to achieve without some loss in picture quality. Additional degradation results from photographing the original prints for the purpose of publication.

### 10.1 Image integration

One outstanding feature of the storage tube is its ability to integrate images with very low signal to noise ratios. Photographs 3 and 4 show the effect of integrating the video output from a low light level television camera over 0.2 second (10 TV frames) and 1 second (50 TV frames) respectively. The benefit of this technique is obvious when it is considered that a result similar to that of photograph 2 would have been obtained if the image was stored for 40 millisecond (2 TV frames).

### 10.2 Deflection circuit distortion

Barrel distortion in photographs of the TV display is caused primarily by photographing a small 125 millimetre television monitor with an oscilloscope camera. The application of operational amplifier techniques for the storage tube deflection circuits has resulted in highly linear deflection currents. Although this does not guarantee linear

scanning of the storage target because of possible non-linearity introduced by the deflection coils, it is assumed that any geometric distortion caused by the scans is negligible because the same deflection circuits are used for both writing and reading.

### 10.3 Microcomputer generated image

Aside from being a valuable tool for testing the Image Processing Terminal, the microcomputer highlighted a few deficiencies in the electronics design, in particular the instability in the write clock frequency. It can be seen from photograph 17 that the vertical bars generated by the microcomputer are not straight lines. This is the result of jitter in the write clock frequency and variation in the oscillator starting point. The former is caused by the Schmitt trigger write clock oscillator while the latter may be caused by a combination of the oscillator circuit and variation in the horizontal retrace monostable multivibrator output (IC54, figure II-4). Ideally the Schmitt trigger oscillator should be replaced by a gated 500KHz crystal oscillator.

### 10.4 Image retention

#### 10.4.1 Storage tube operational

In theory the storage tube has a non-destructive read mechanism but in practice, residual gas molecules within the tube are ionized through collisions with the electron beam. These positive ions discharge the surface of the

target. Photographs 18 and 19 show the effect on the stored image over a period of an hour. Figure 14 shows the relative video output signal amplitude over the same period.

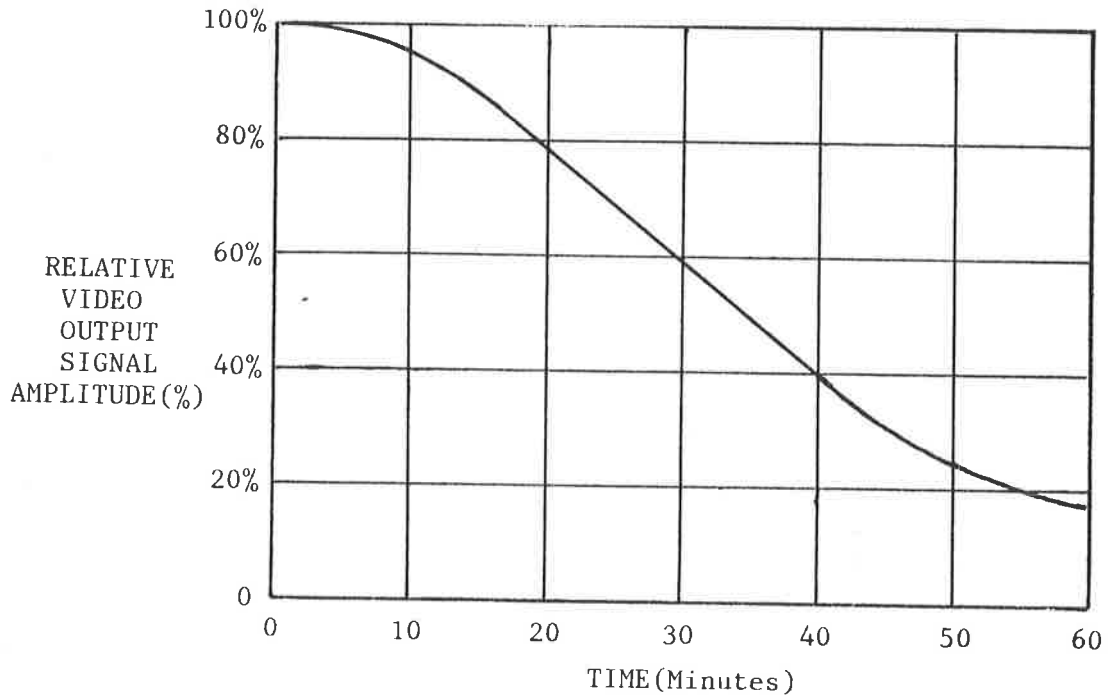


FIGURE 14. IMAGE RETENTION

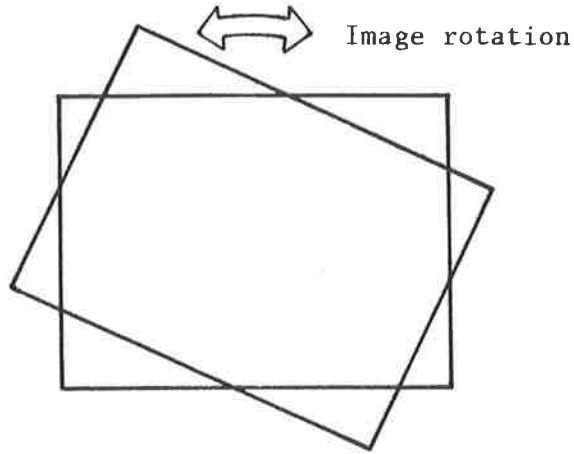
#### 10.4.2 Storage tube inoperative

The image is not degraded over a longer period of time if the electron beam is gated off or the tube is switched off. Negligible degradation in picture quality was observed after the tube had been switched off for 24 hours immediately after storing an image.

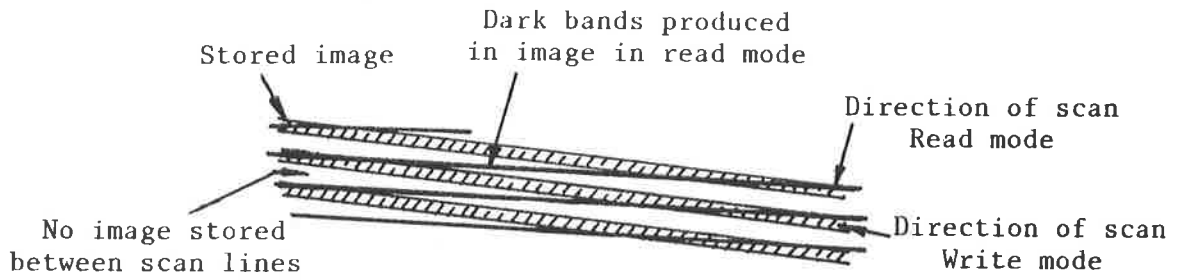
### 10.5 Moire patterns

Varying either the magnetic or electrostatic focus causes the scanned image to rotate about the central axis of the storage tube as shown in figure 15a. Elevation of the target to 200 volt in the write mode modifies the electrostatic field within the storage tube and affects the electrostatic focus. Hence, there is a slight variation in the direction of scan between the write and read modes. Since the TV image is composed of a number of spaced scan lines, traversing these lines at a slightly different angle as shown in figure 15b results in Moire patterns. This effect is greatly exaggerated from normal operating conditions, as shown in photograph 20, by storing a non-interlaced test pattern i.e., the second TV frame overwrites the first, effectively giving 312 scan lines instead of the usual 625, and by deliberately maladjusting the scan amplitudes after storing the test pattern.

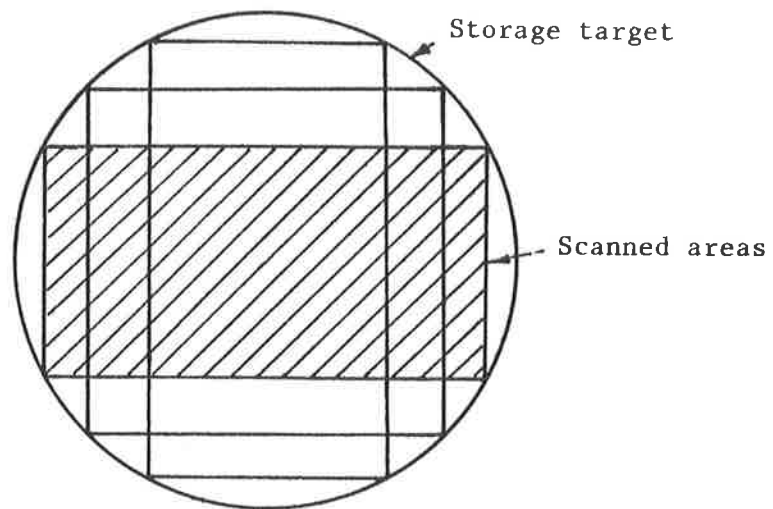
It can be seen from figure 15c that the horizontal and vertical scan amplitudes may be adjusted for a scanned area on the storage target of any aspect ratio. In order to minimize the possibility of generating Moire patterns, the scan amplitudes must be adjusted for an oblong scanned area to reduce the spacing between TV scan lines.



(a) ROTATION CAUSED BY FOCUSING



(b) SCANNING DIRECTION - READ/WRITE MODES



(c) SCANNED AREA ASPECT RATIO

FIGURE 15. MOIRE PATTERN GENERATION

## 10.6 Image shading

Aside from Moire effects, there are a number of causes for unwanted shading in the stored image, such as non-uniformity of the silicon dioxide layer, incorrect adjustment of the electron optics within the storage tube and non-linearity of the scanning circuits. With this particular storage tube, no noticeable shading has been attributed to variation in the silicon dioxide layer thickness. Also, a high degree of linearity is achieved by employing operational amplifier techniques for the deflection circuits.

Shading caused by the electron optics is minimized by careful adjustment of the magnetic focus and alignment circuits. Photograph 18 shows shading in the top left-hand corner of the stored image which is more apparent after continuously reading the image for an hour as shown in photograph 19.

## 10.7 Image digitization

The ultimate objective of the Image Processing Terminal was to digitize a conventional television image and to return a digitally processed image to the storage tube for viewing at normal TV scan rates. How well the hardware achieved this objective was evaluated by using two similar TV monitors side by side with one to display the digitally processed image from the Image Processing Terminal, and one to display the video input signal. A video signal from either a video test pattern generator or a conventional television camera was connected to the video input of the Image Processing terminal and also



displayed on one TV monitor.

A computer program shown in Appendix IV was then implemented by the PDP-11 computer to digitize the image. The program firstly erased the storage tube for two seconds and stored the video input signal over two TV frames. This image was then digitized over a selected matrix combination and stored on disk under the file name 'TWM.DAT'. The storage tube was again erased and the digitized image returned to the storage tube for viewing at normal TV scan rates and for comparing with the displayed video input signal. Photographs 21, 23 and 24 show typical results obtained from digitizing images from the two different sources.

#### 10.7.1 Test pattern

The microcomputer generated image shown in photograph 17 highlighted instability in the write clock frequency. Since the digitize clock frequency is generated by an identical circuit, it is not surprising that the oscillator exhibits the same instability. This instability is apparent when digitizing an image with sharp black and white transitions which are orthogonal to the horizontal scanning direction. Certain edges which are coincident with the clock frequency transitions are randomly digitized as white or black.

Black specks in the white areas of the digitally processed test pattern are attributed to Moire effects.

### 10.7.2 Conventional image

For the second part of the evaluation, a conventional television camera was coupled to the Image Processing Terminal and the camera focused on a colour photograph. Although the photograph's appearance to the eye was enhanced by virtue of it being in colour, its grey scale characteristics were not wide ranging when viewed with a black and white television camera. However, it was considered important to relate the system to a stored image of a prominent person as opposed to a general scene which may have presented better grey scale characteristics. Photographs 23 and 24 show the result of processing the image shown in photograph 22 over 128 rows by 64 columns and 256 rows by 128 columns respectively.

In general, the digitally processed image was considered a fair reproduction of the original stored image. Again, the random black specks have been attributed to Moire effects.

### 10.8 Resolution

The maximum resolution of the storage tube is determined by a combination of video amplifier bandwidth, technical adjustment of the electron optics and electron beam spot diameter. Ideally, the video amplifier should have sufficient bandwidth and the electron optics should be adjusted to have a minimal effect on the system resolution, with the main limitation being the physical diameter of the scanning electron beam. Photograph 25 shows the result of storing a

test pattern with square wave frequency components of 0.3125, 0.625, 1.25, 2.5, 4.43 and 5MHz. Figure 16 shows the modulation transfer function of the overall system obtained by plotting the relative video output signal amplitude of each square wave against its respective frequency.

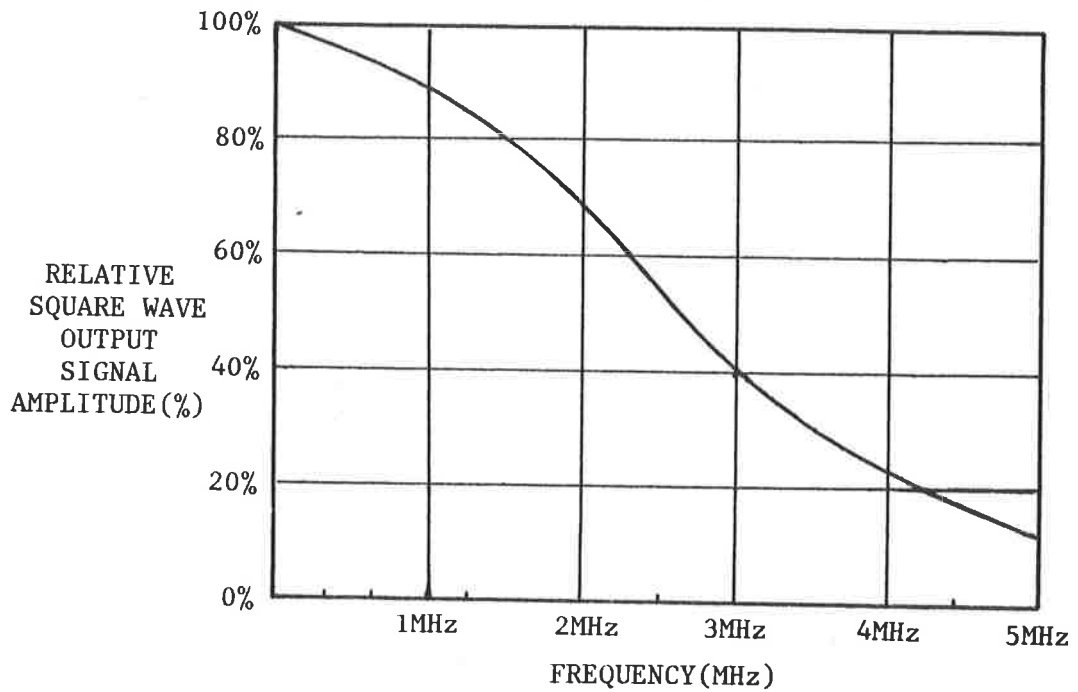


FIGURE 16. MODULATION TRANSFER FUNCTION - OVERALL SYSTEM

## 11. CONCLUSIONS

When this project was conceived, a storage tube represented an economical approach for developing an image processing terminal. Over the ensuing years the size of single integrated circuit dynamic memories has increased by almost two orders of magnitude and their cost has plummeted to approximately 0.01 cent per bit (16K dynamic RAM). The number of peripheral integrated circuits has also been reduced. An image processing terminal equivalent to the present design and employing digital memories requires a high speed analogue-to-digital converter to digitize the video input signal. Again, the cost of these units has steadily declined to less than one hundred dollars.

While today, an image processing terminal employing a digital memory may be comparable in price with the present design, the storage tube still has some unique features such as its ability to integrate images and to function as a non-volatile store. It does however suffer from image shading caused by the electron optics and non-uniformity of the silicon dioxide storage target. Also, the image is not stored as a series of discrete points but as discrete lines which may result in the generation of Moire patterns. These problems are minimized by careful adjustment of the deflection and alignment circuits.

The present Image Processing Terminal uses a small digital memory for temporarily storing one row of the digitized image. At the same time, the system may be supported by a small minicomputer with very limited memory capacity. The data generated by digitizing one or more images is held on a disk

unit. As shown in reference 7 the concept of storing data in row accessible order on disk does not prevent the system from engaging in two dimensional image processing techniques. These advantages are offset by the increase in processing time to transfer data either to or from disk when compared with a large computer with its central processor interfaced directly with a digital video store.

Data transfer between the Image Processing Terminal and the PDP-11 computer is controlled by four registers located in the DR11-B interface bus. The use of the FORTRAN COMMON statement to overlay an array over the I/O page with elements in the array having the same physical addresses as the interface registers has greatly simplified the techniques for programming the Image Processing Terminal. Although the system executes eight separate functions, the FORTRAN coding to implement these functions has been reduced to just a few instructions.

As with almost any project of this magnitude, the conceptual design may occupy a significant proportion of the total developmental time. This is particularly true with complex digital circuits where, by careful consideration of the timing requirements, it is often not necessary to prototype the design before proceeding with its construction. Such was the case with the printed circuit card shown in figure II-20.

This is not necessarily the case with analogue circuits which frequently require prototyping before proceeding with their construction. As in the case of the vertical deflection circuit, even this did not guarantee its satisfactory operation. While

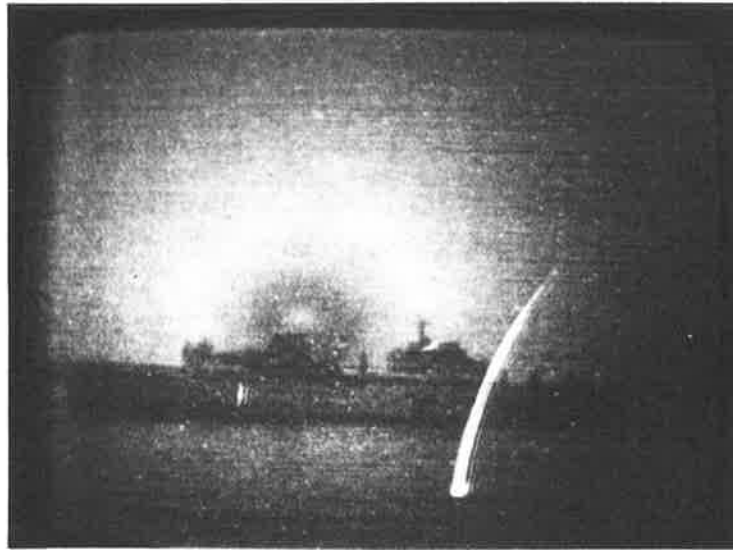
its linearity appeared excellent when examined with a current probe, the circuit showed signs of cross-over distortion when observing a stored image on the television monitor. An important aspect of any video system is the fact that the television monitor coupled to the system is itself a useful tool for diagnosing circuit deficiencies. Even low levels of external electrical interference are readily apparent on the display, hence the special attention paid in the design to minimize this interference by shielding and careful placement of certain printed circuit cards such as the read amplifier.

The present design has proved the conceptual and hardware designs for an Image Processing Terminal. At the same time, the functional system highlighted areas which require additional attention such as the write and digitize clock oscillators.

Not only has technology progressed in the field of semiconductor devices but possibly as a result of this explosion there has been increasing development of computer generated displays. It is believed that this trend will continue and display systems will play an ever increasing role in the interface between man and machine.

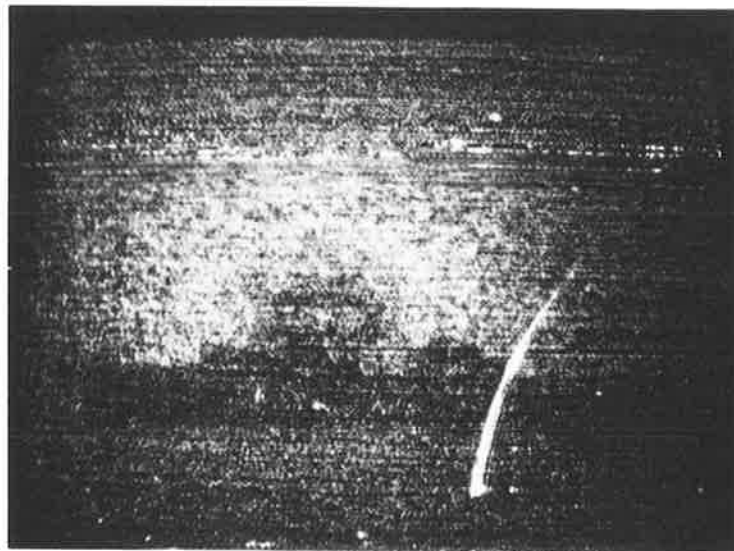
LIST OF PHOTOGRAPHS

1. IMAGE - REPLAY VTR
2. IMAGE - STOP FRAME VTR
3. STORAGE TUBE INTEGRATION - 0.2 SECOND
4. STORAGE TUBE INTEGRATION - 1.0 SECOND
5. THE IMAGE PROCESSING TERMINAL
6. READ AMPLIFIER LOCATION
7. READ AMPLIFIER
8. FET VIDEO AMPLIFIER FREQUENCY RESPONSE
9. COMPOSITE VIDEO SIGNAL
10. MAIN VIDEO AMPLIFIER FREQUENCY RESPONSE - READ & ERASE MODES
11. MAIN VIDEO AMPLIFIER FREQUENCY RESPONSE - WRITE MODE
12. FRAME SCAN CURRENT/VOLTAGE WAVEFORMS - NORMAL TV SCAN
13. FRAME SCAN CURRENT WAVEFORM - STAIRCASE SCAN
14. LINE SCAN CURRENT/VOLTAGE WAVEFORMS - NORMAL TV SCAN
15. LINE SCAN CURRENT/VOLTAGE WAVEFORMS - STAIRCASE SCAN
16. D/A CONVERTER OUTPUT - TEST MODE
17. STORED IMAGE GENERATED BY MICROCOMPUTER
18. STORED IMAGE - 0 MINUTES
19. STORED IMAGE AFTER 60 MINUTES
20. MOIRE PATTERNS
21. DIGITIZED TEST PATTERN
22. STORED IMAGE FOR DIGITIZATION
23. DIGITIZED IMAGE 128 ROWS X 64 COLUMNS
24. DIGITIZED IMAGE 256 ROWS X 128 COLUMNS
25. STORED MULTI-BURST TEST PATTERN



Camera shutter speed 0.25 second

PHOTOGRAPH 1. IMAGE - REPLAY VTR



Camera shutter speed 0.25 second

PHOTOGRAPH 2. IMAGE - STOP FRAME VTR





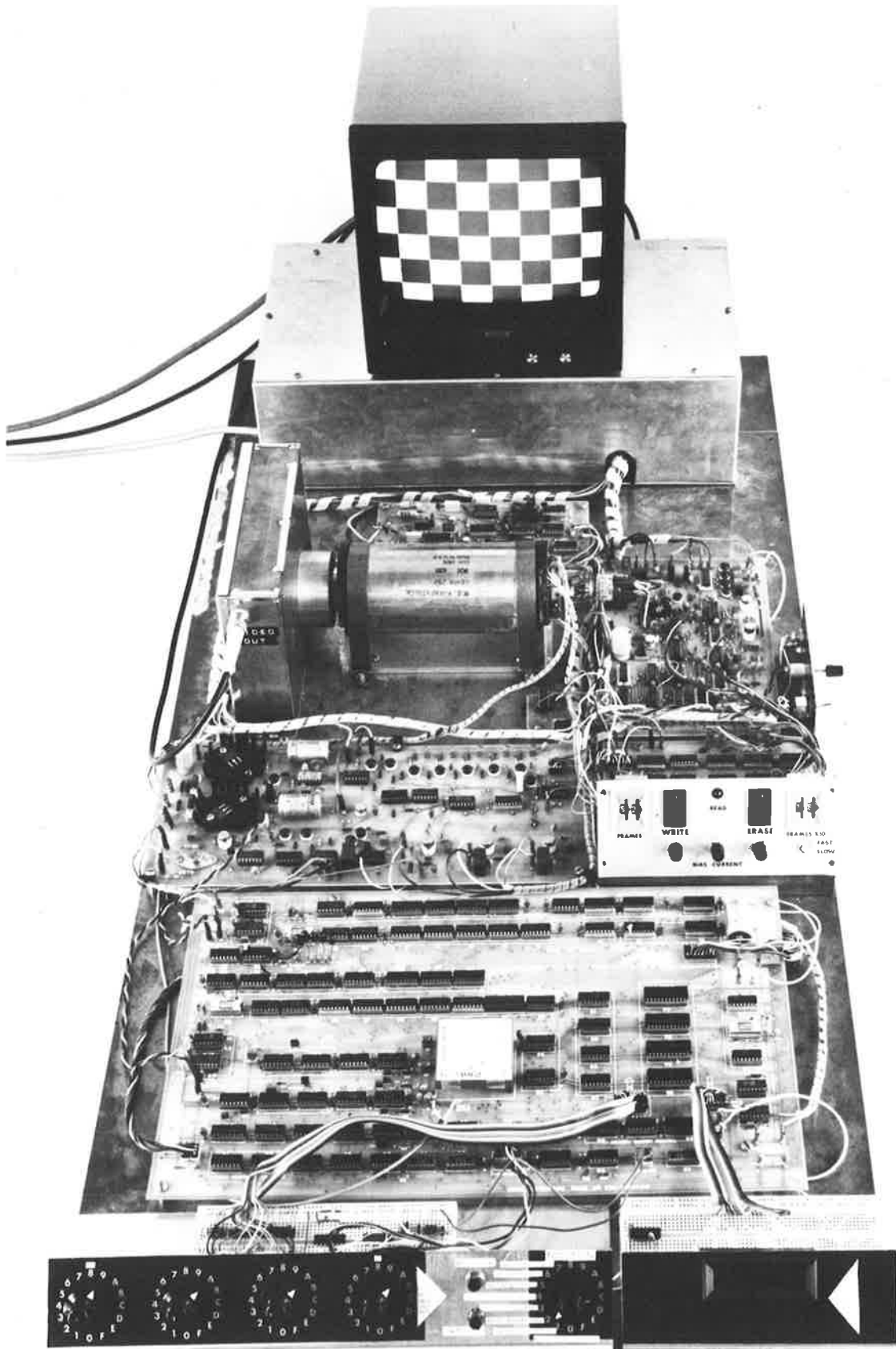
Integration over 10 TV Frames

PHOTOGRAPH 3. STORAGE TUBE INTEGRATION - 0.2 SECOND

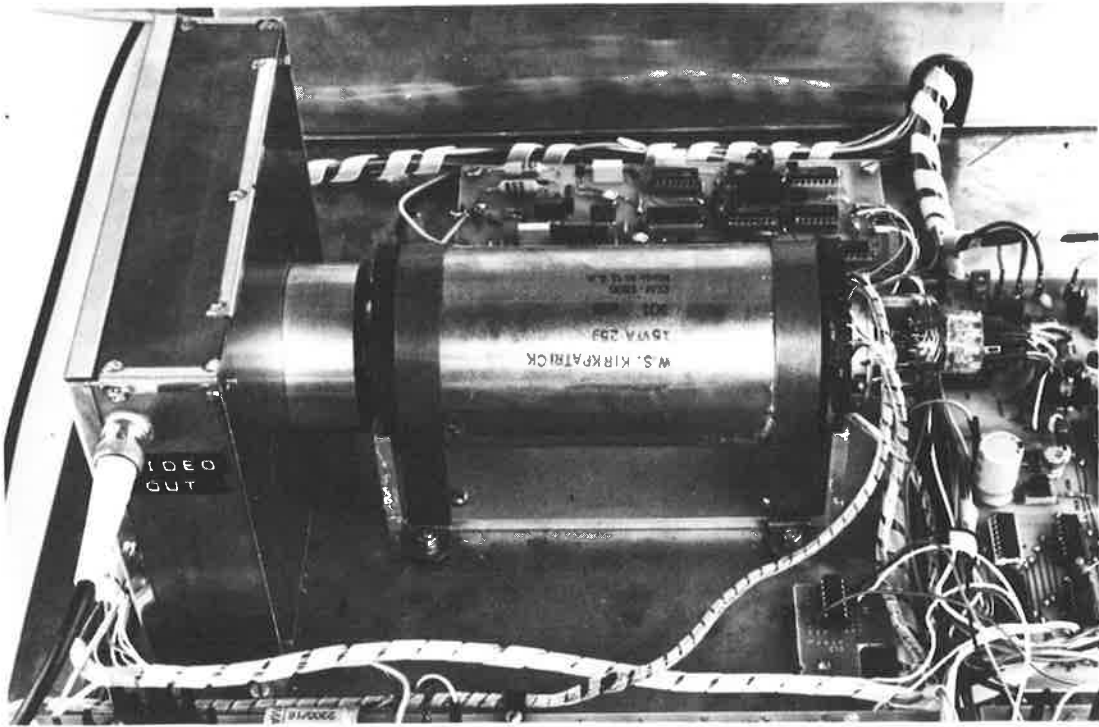


Integration over 50 TV Frames

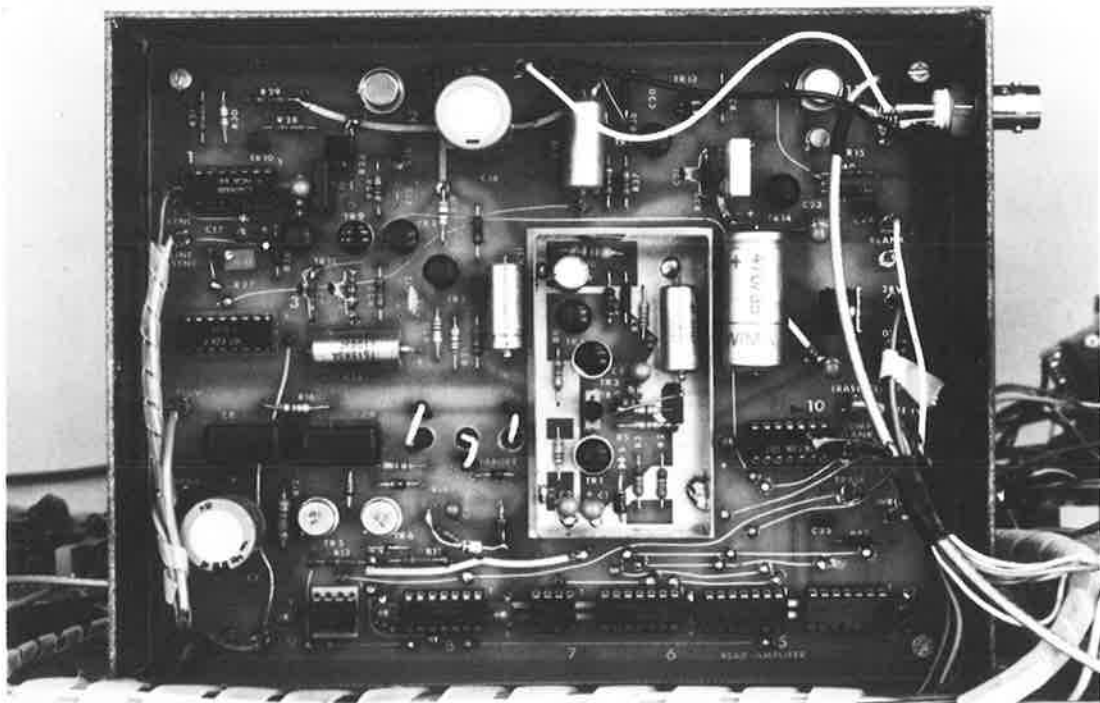
PHOTOGRAPH 4. STORAGE TUBE INTEGRATION - 1.0 SECOND



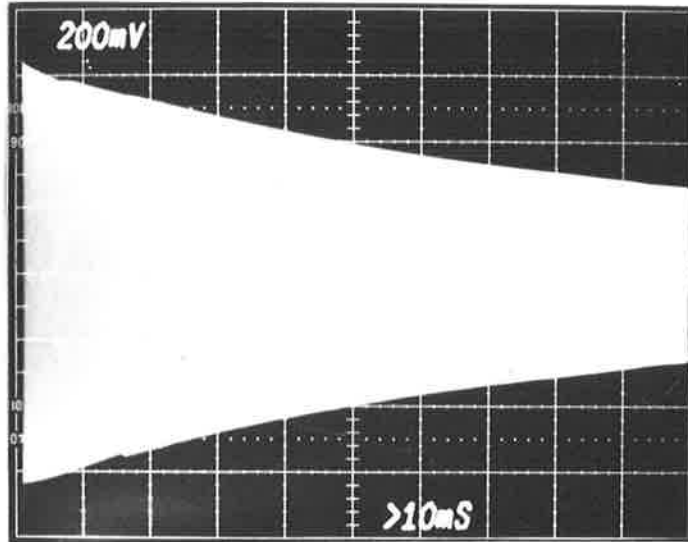
PHOTOGRAPH 5. THE IMAGE PROCESSING TERMINAL



PHOTOGRAPH 6. READ AMPLIFIER LOCATION

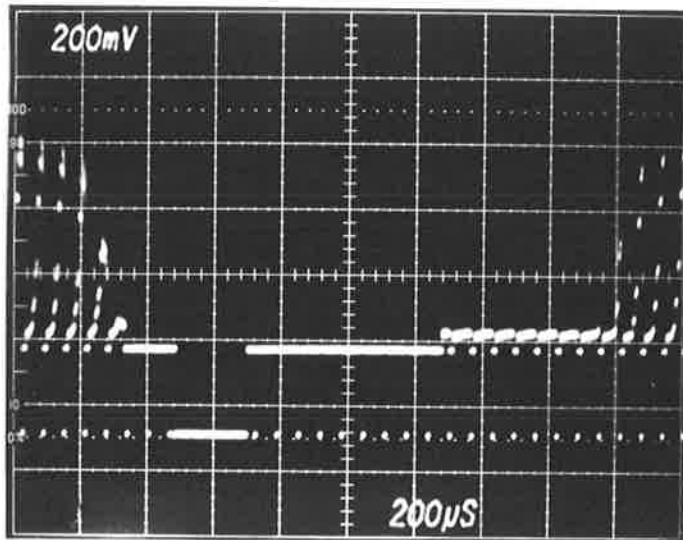


PHOTOGRAPH 7. READ AMPLIFIER

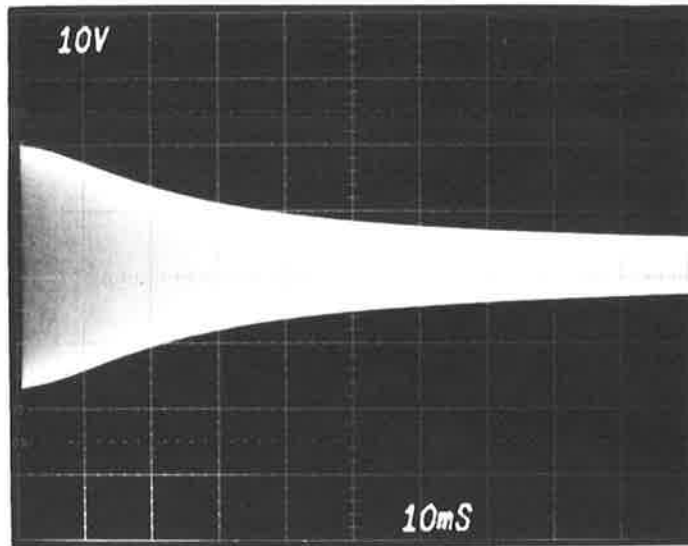


Low frequency gain  $\cong 8$   
Linear sweep 10KHz - 15MHz

PHOTOGRAPH 8. FET VIDEO AMPLIFIER FREQUENCY RESPONSE

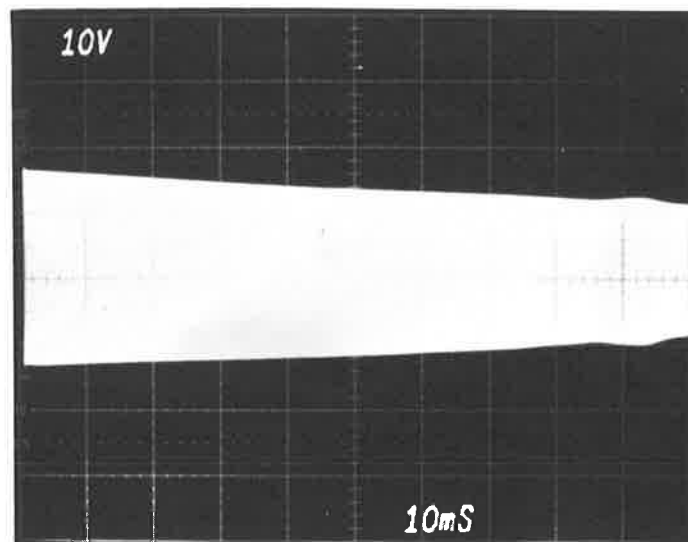


PHOTOGRAPH 9. COMPOSITE VIDEO SIGNAL



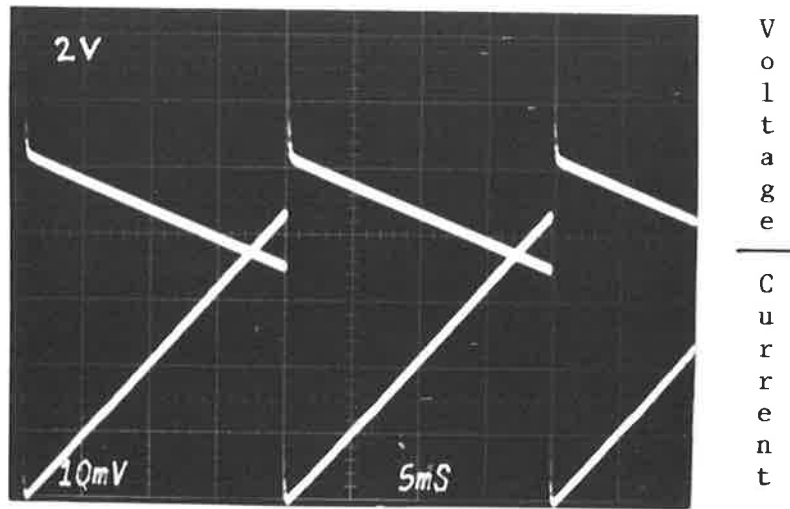
Low frequency gain  $\cong 100$   
Linear sweep 10KHz - 5MHz

PHOTOGRAPH 10. MAIN VIDEO AMPLIFIER FREQUENCY RESPONSE - READ & ERASE MODES



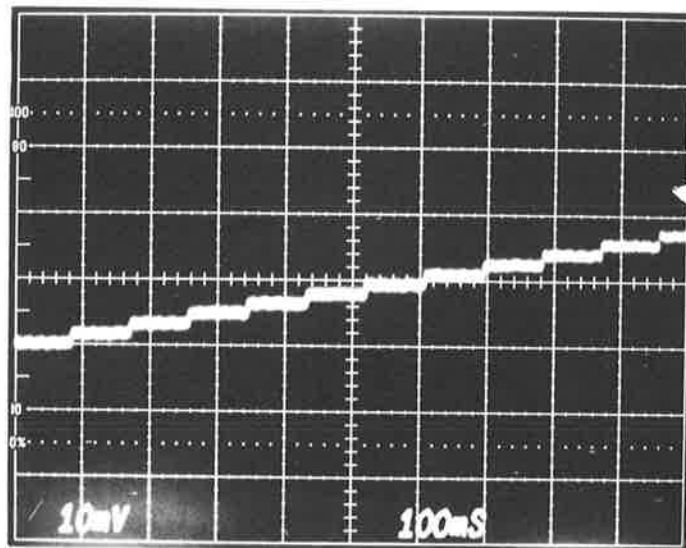
Low frequency gain  $\cong 20$   
Linear sweep 10KHz - 15MHz

PHOTOGRAPH 11. MAIN VIDEO AMPLIFIER FREQUENCY RESPONSE - WRITE MODE



Current 5mA/Div

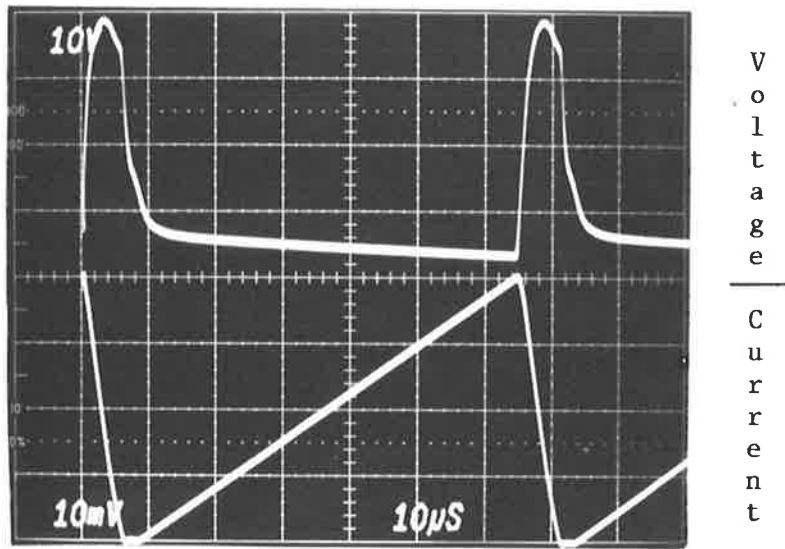
PHOTOGRAPH 12. FRAME SCAN CURRENT/VOLTAGE WAVEFORMS - NORMAL TV SCAN



64 Rows

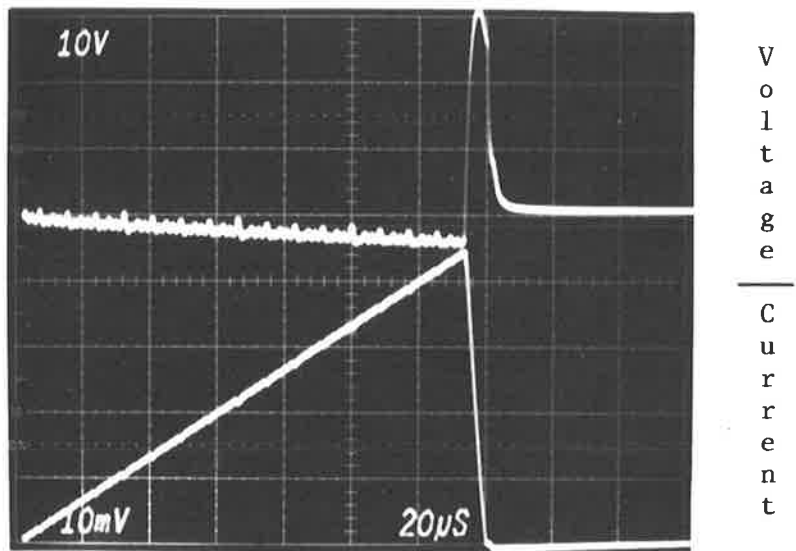
Current 2mA/Div

PHOTOGRAPH 13. FRAME SCAN CURRENT WAVEFORM - STAIRCASE SCAN



Current 50mA/Div

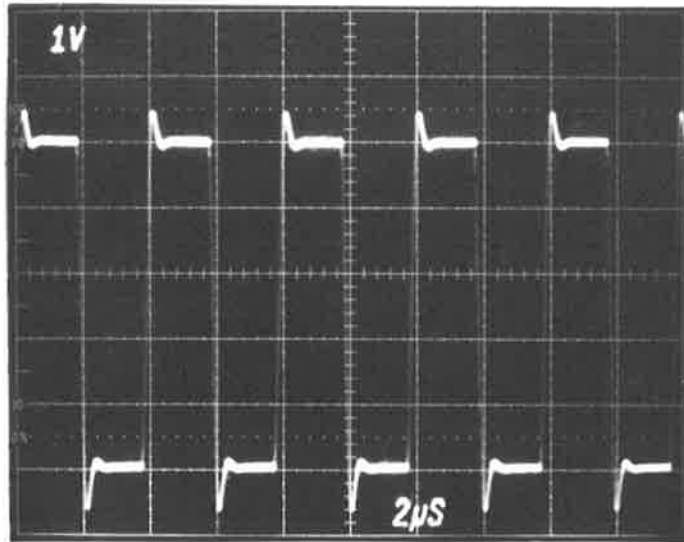
PHOTOGRAPH 14. LINE SCAN CURRENT/VOLTAGE WAVEFORMS - NORMAL TV SCAN



64 Columns

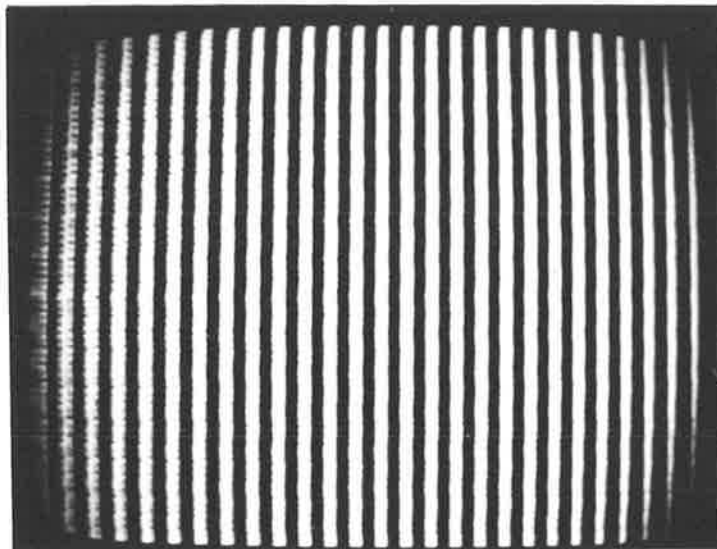
Current 50mA/Div

PHOTOGRAPH 15. LINE SCAN CURRENT/VOLTAGE WAVEFORMS - STAIRCASE SCAN



128 Rows x 64 Columns

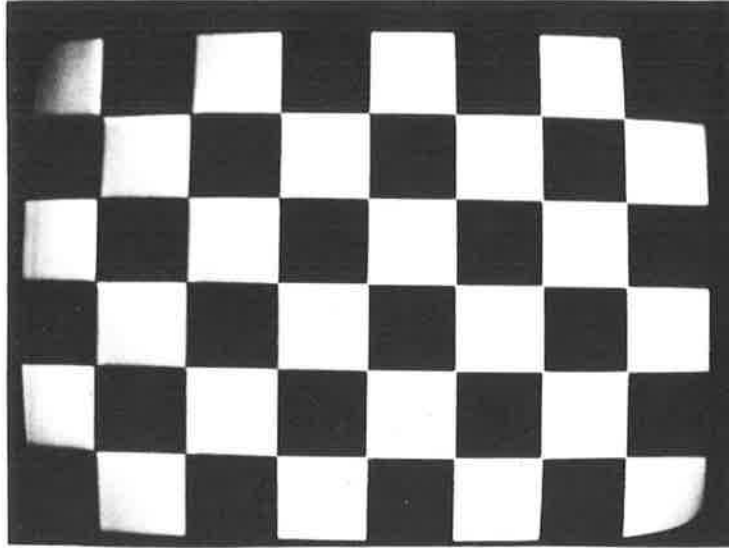
PHOTOGRAPH 16. D/A CONVERTER OUTPUT - TEST MODE



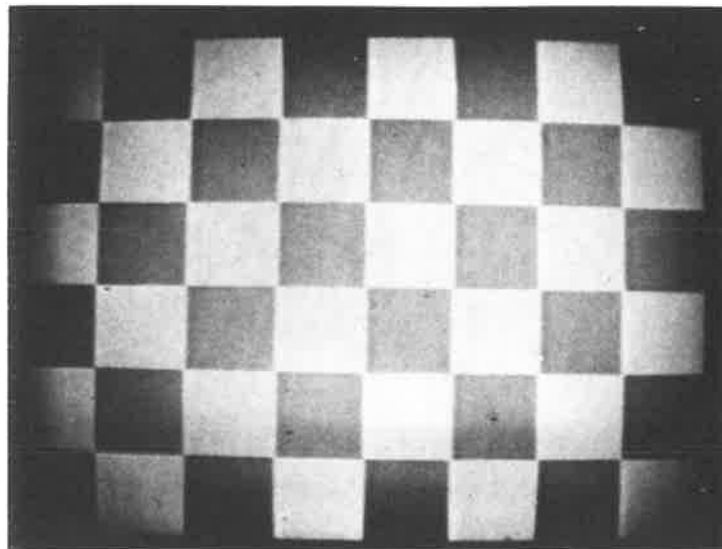
128 Rows x 64 Columns

PHOTOGRAPH 17. STORED IMAGE GENERATED BY MICROCOMPUTER

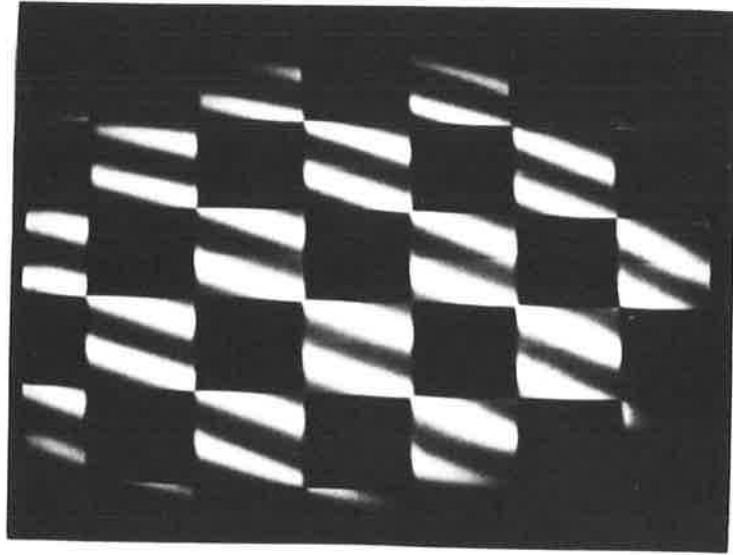




PHOTOGRAPH 18. STORED IMAGE - 0 MINUTES

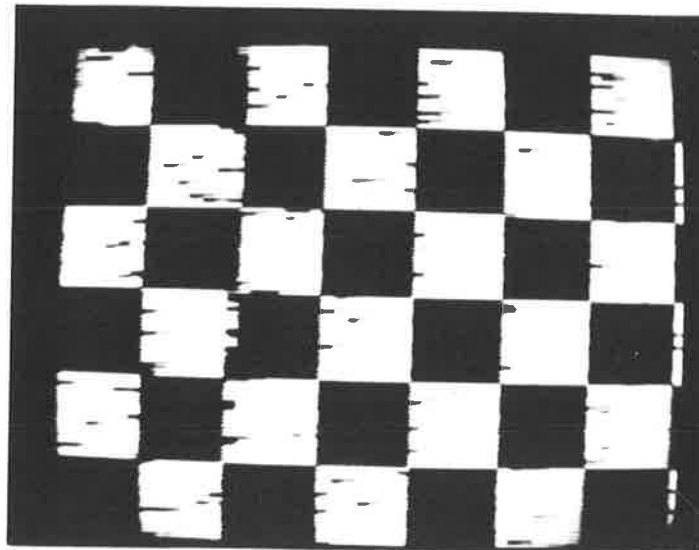


PHOTOGRAPH 19. STORED IMAGE AFTER 60 MINUTES



System deliberately maladjusted  
to highlight the effect

PHOTOGRAPH 20. MOIRE PATTERNS



128 Rows x 64 Columns

PHOTOGRAPH 21. DIGITIZED TEST PATTERN



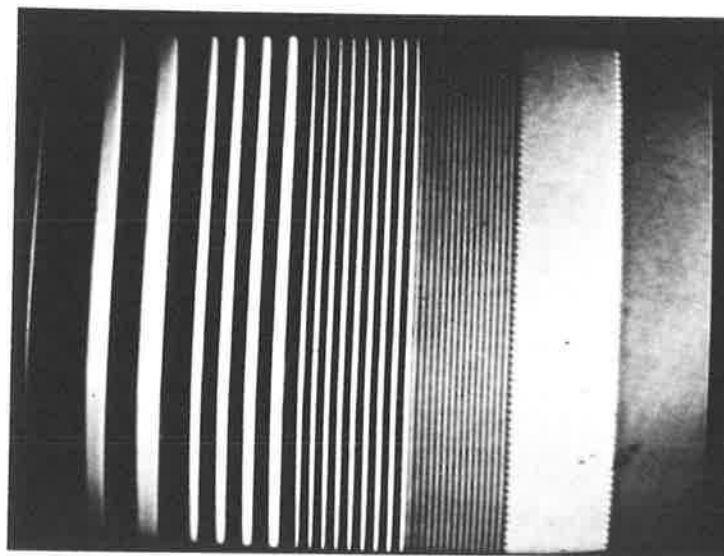
PHOTOGRAPH 22. STORED IMAGE FOR DIGITIZATION



PHOTOGRAPH 23. DIGITIZED IMAGE 128 ROWS X 64 COLUMNS



PHOTOGRAPH 24. DIGITIZED IMAGE 256 ROWS X 128 COLUMNS



0.3125MHz    0.625MHz    2.5MHz    5.0MHz

PHOTOGRAPH 25. STORED MULTI-BURST TEST PATTERN

APPENDIX I

THE SILICON DIOXIDE STORAGE TUBE

I.1 Storage tube

The silicon dioxide storage tube (ref. 1,2) differs from most other storage tubes in that it can reproduce shades of grey and is therefore ideally suited to storing television images. It is mechanically and electrically similar to a conventional magnetically focused and deflected vidicon camera tube but with the photosensitive target replaced by a fabricated silicon dioxide storage target. This target has been made possible by advances in integrated circuit technology.

I.1.1 Electron gun

The electron gun (figure I-1) consists of an indirectly heated cathode C, a control grid G1, an accelerating electrode G2, an erasing electrode G3, a focusing electrode G4 and a field mesh electrode G5. The G5 electrode is a fine wire mesh located in close proximity to the target.

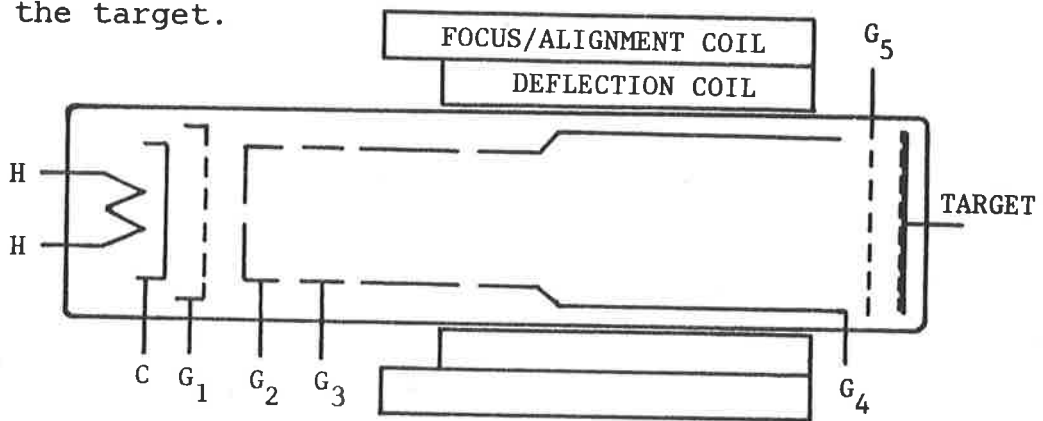


FIGURE I-1 SCHEMATIC SILICON DIOXIDE STORAGE TUBE

### I.1.2 Storage target

The storage target consists of a mosaic of silicon dioxide dielectric blocks on a conducting backplate (figure I-2). The backplate is a heavily doped P-type silicon wafer which is thermally oxidised to form a 1 micron ( $\mu\text{m}$ ) thick silicon dioxide layer. This layer is etched by standard integrated circuit techniques to form a mosaic of elemental dielectric blocks, each approximately  $10\mu\text{m}$  square and separated by  $4\mu\text{m}$ .

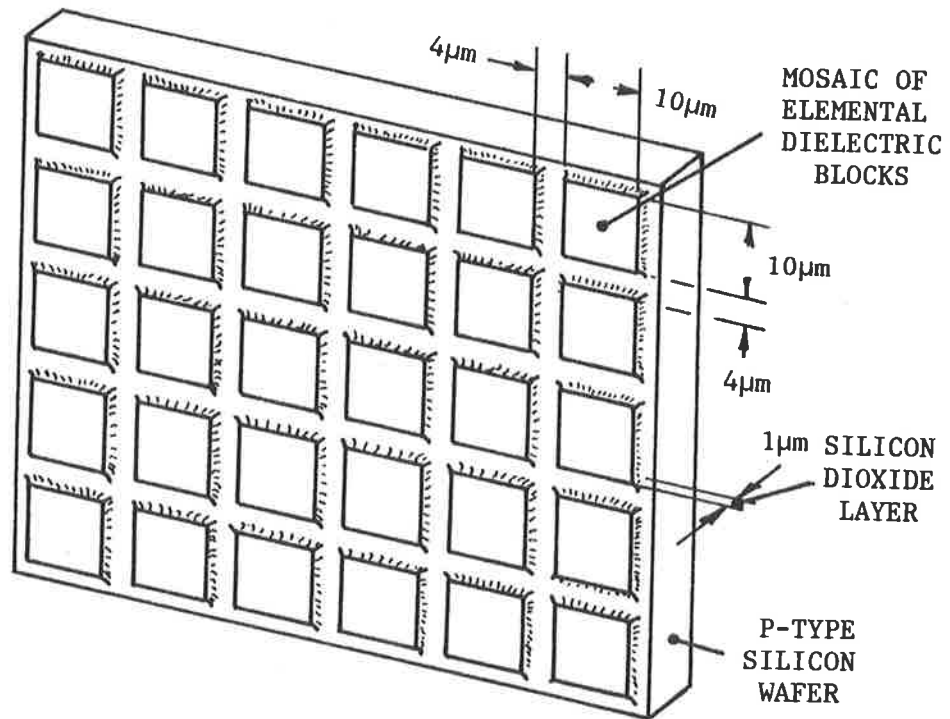


FIGURE I-2 SCHEMATIC STORAGE TARGET

### I.1.3 Principles of operation

Charges are stored on these elemental dielectric blocks and electrostatic interaction between adjacent blocks establishes a coplanar grid which controls the reading electron beam current flowing through to the

conducting backplate. Establishing this charge pattern (writing) on the storage target, reading and erasure are performed sequentially and each process is described separately.

#### I.1.4 Erasure

During erasure, the target backplate is held at approximately 17 volt and the silicon dioxide blocks are scanned by a constant electron beam current (figure I-3a). With a uniform decelerating field established between the G5 electrode (+750V) and the conducting backplate (17V), the electrons are decelerated and arrive at the target with low velocity. Charges are deposited on the surface of the silicon dioxide blocks and all are stabilized to cathode potential (0V). Stabilization requires approximately 360ms or 18 TV frames after which, each block acting as an elemental capacitor, is charged to 17 volt.

#### I.1.5 Writing

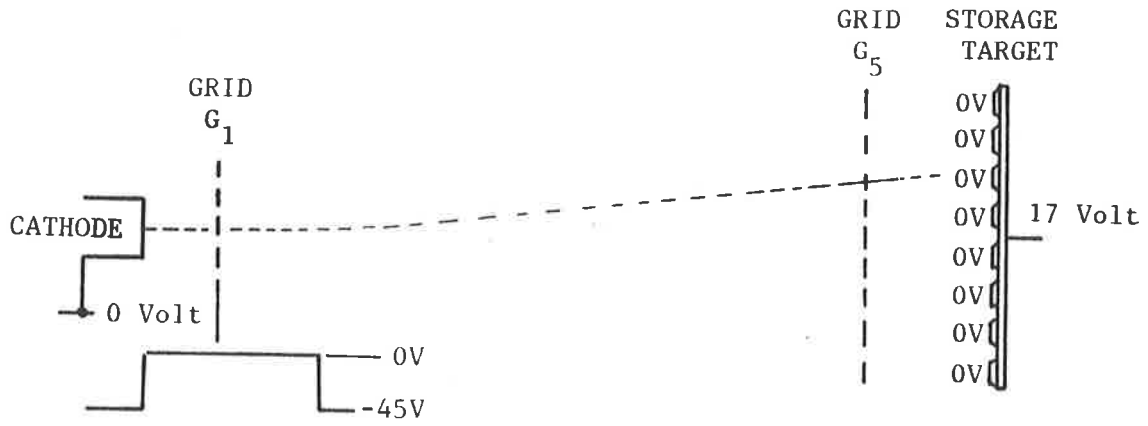
Prior to the writing mode, the target backplate potential is raised to 200 volt and by capacitive coupling, the cathode side of each dielectric block is elevated to 183 volt (200V minus the 17V stored on each elemental capacitor). Elevation of the target to this potential reduces the decelerating field whereby the beam electrons are not decelerated and arrive at the target with high velocity. These high energy electrons strike the silicon dioxide surface releasing secondary electrons in numbers proportional to the incident electron density, which in

turn is proportional to the video signal applied to the control grid, G1 (assuming unity gamma for the electron gun). Removal of electrons discharge the elemental capacitors taking them positive as shown in figure I-3b .

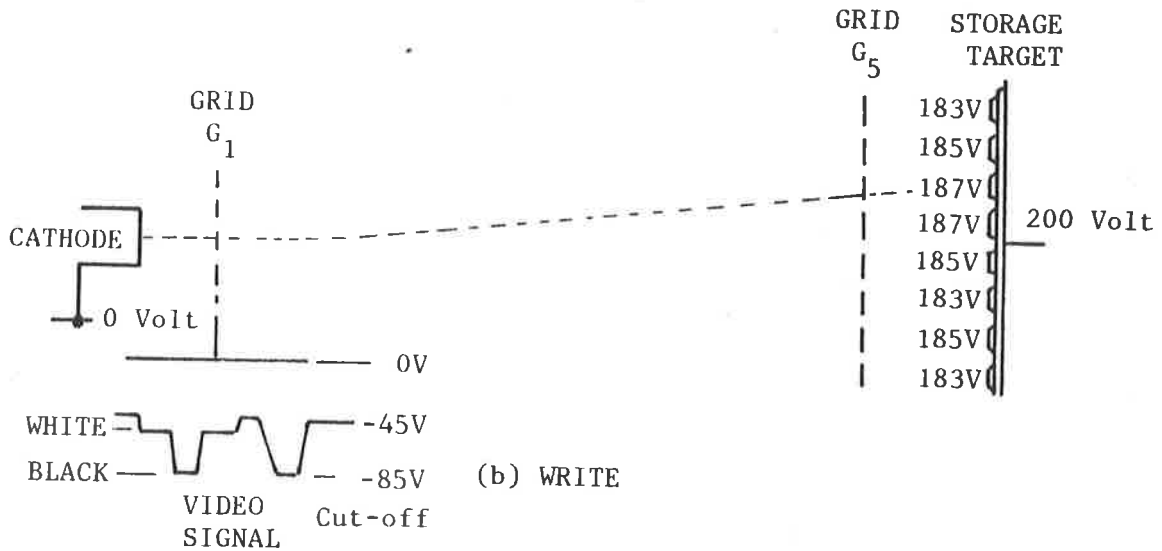
#### I.1.6 Non-destructive read

After writing, the target backplate is lowered to approximately 7 volt and by capacitive coupling, the cathode side of each dielectric block assumes a voltage in the range -10 to 0 volt, see figure I-3c. A uniform decelerating field is again established between the G5 electrode and the target. The target is scanned in the normal raster mode by a constant beam current and the electrons, under the influence of the decelerating field, arrive at the target with low velocity. The negative potentials on the dielectric blocks repel electrons and prevent target discharge (i.e. non-destructive read mechanism). Whereas the electrostatic interaction between adjacent blocks establishes a coplanar grid controlling the reading beam current flowing to the conducting backplate. The beam current reaching the backplate develops a voltage across the load resistor 'R' proportional to the stored charge.

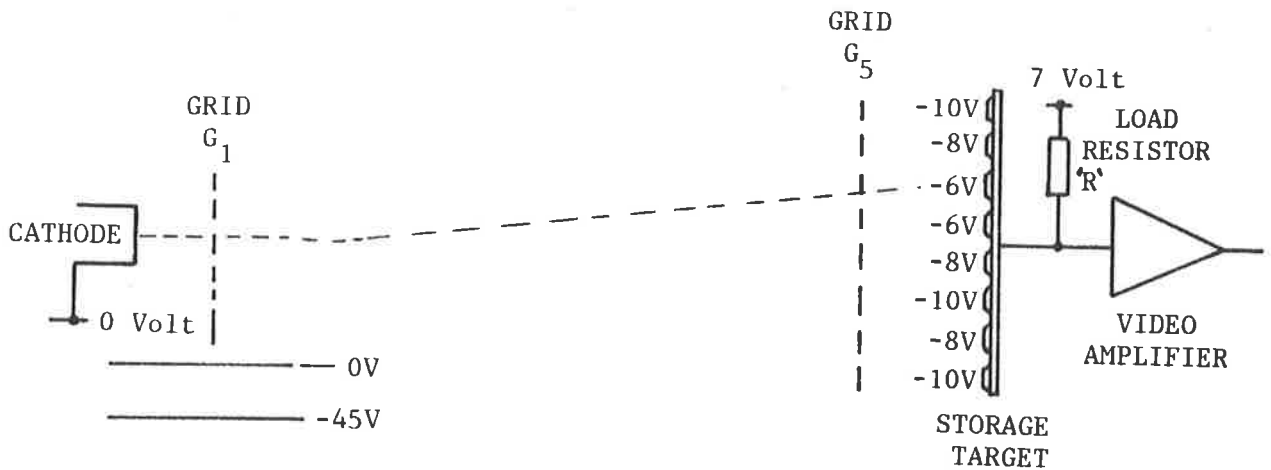




(a) ERASE



(b) WRITE



(c) READ

FIGURE I-3 STORAGE TUBE OPERATING PRINCIPLES

APPENDIX II

CIRCUIT DIAGRAMS

- FIGURE II-1 BLOCK DIAGRAM - IMAGE PROCESSING TERMINAL
- FIGURE II-2 DR11-B INTERFACE
- FIGURE II-3 FUNCTION DECODER
- FIGURE II-4 COLUMN COUNTER
- FIGURE II-5 ROW COUNTER
- FIGURE II-6 WORD TRANSFER COUNTER
- FIGURE II-7 ROW/COLUMN REGISTER
- FIGURE II-8 DUAL PORT MEMORY
- FIGURE II-9 SCAN CONTROL/INTERLOCK
- FIGURE II-10 READ-WRITE-ERASE TIMING
- FIGURE II-11 READ AMPLIFIER
- FIGURE II-12 WRITE AMPLIFIER
- FIGURE II-13 SYNC SEPARATOR/GENERATOR
- FIGURE II-14 LINE/FRAME SCAN
- FIGURE II-15 MAGNETIC ALIGNMENT/FOCUS
- FIGURE II-16 POWER SUPPLY
- FIGURE II-17 H.T. INVERTER
- FIGURE II-18 MANUAL INTERFACE TESTER
- FIGURE II-19 SDK-85 MICROCOMPUTER INTERFACE TESTER
- FIGURE II-20 DR11B - STORAGE TUBE INTERFACE CARD ARTWORK  
OVERLAY - COMPONENT SIDE - TRACK SIDE

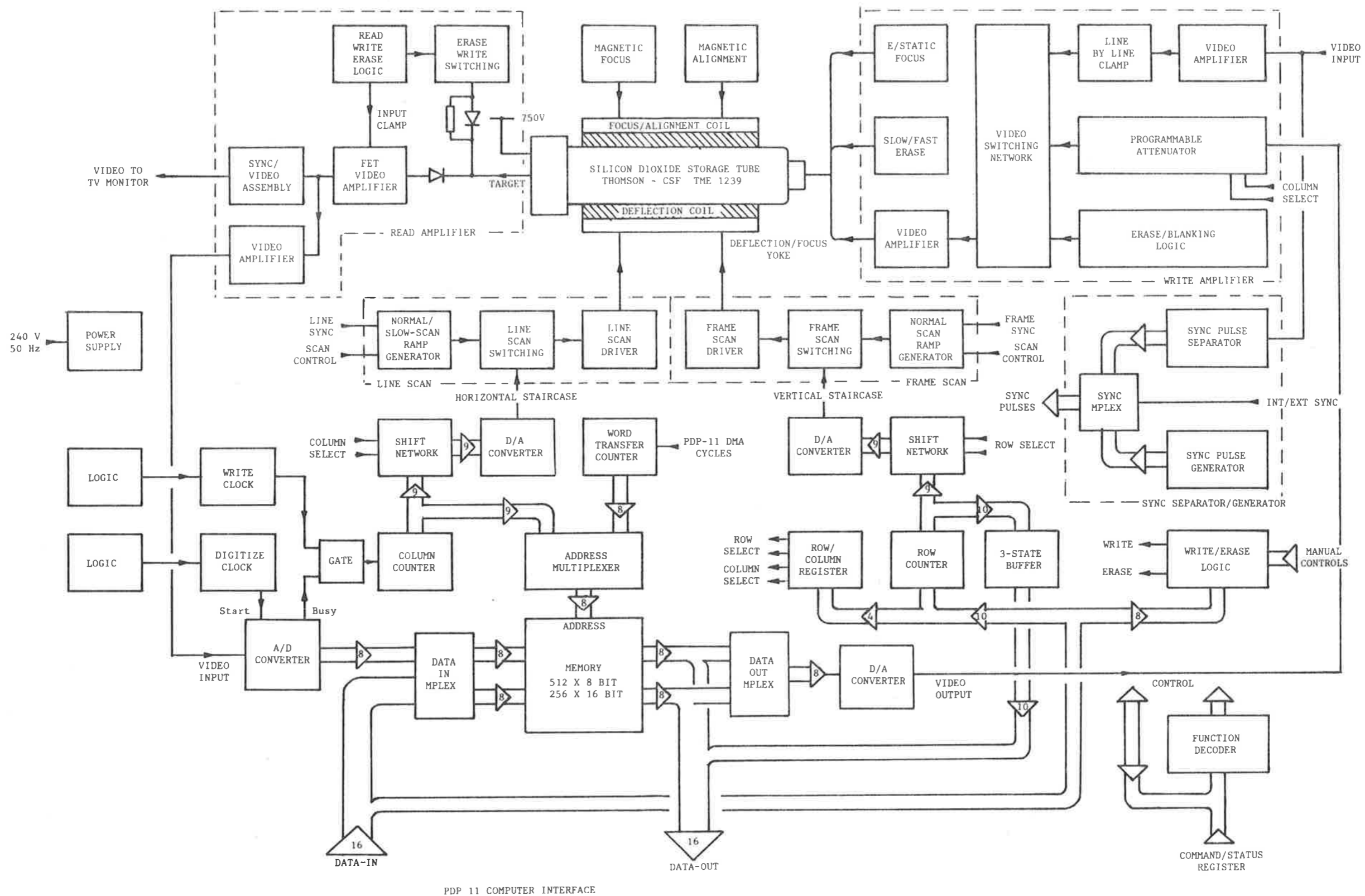


FIGURE II-1 BLOCK DIAGRAM - IMAGE PROCESSING TERMINAL

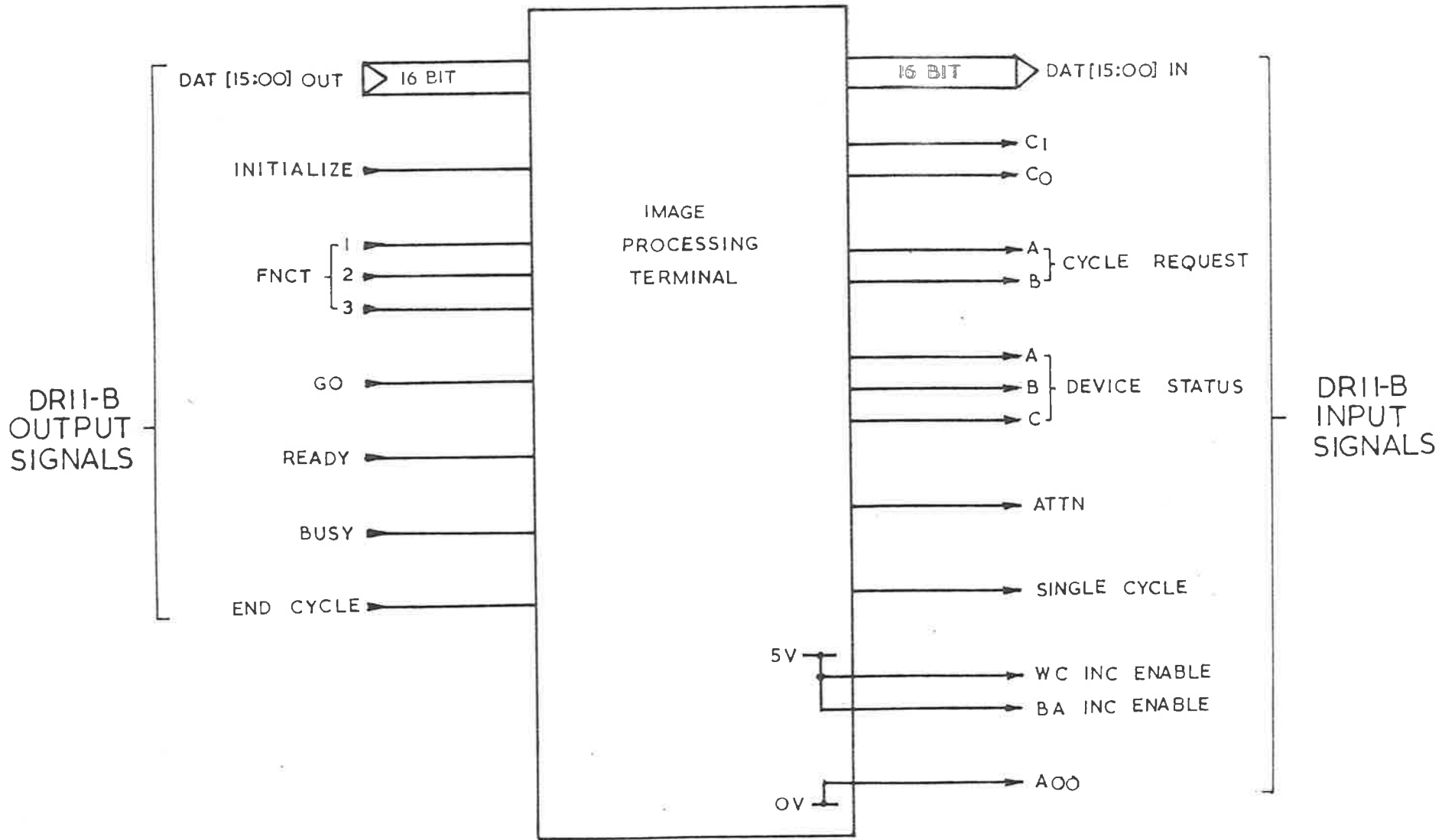
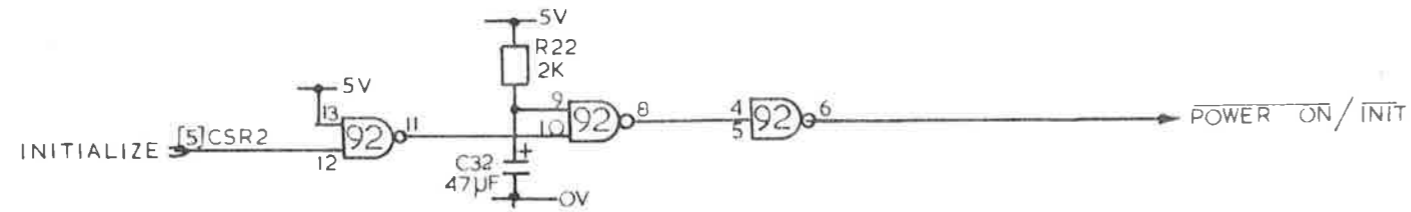


FIGURE II-2 DR11-B INTERFACE



POWER ON - INITIALIZE

CI	CO	DRIIB I/O CONTROL
0	0	FROM DRIIB TO USER DEVICE
1	0	TO DRIIB FROM USER DEVICE

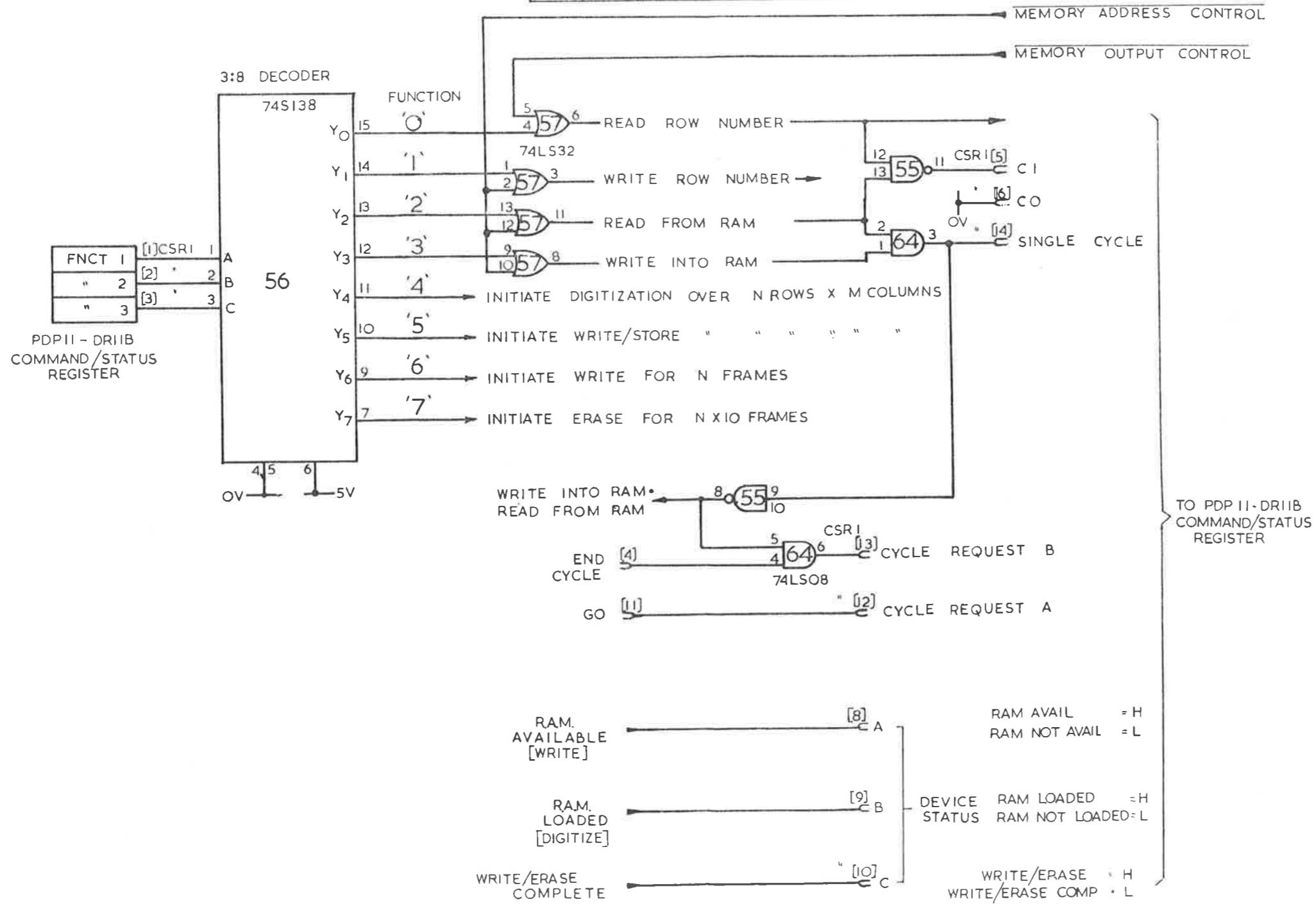


FIGURE II-3 FUNCTION DECODER

DR11B - STORAGE TUBE I/F CARD

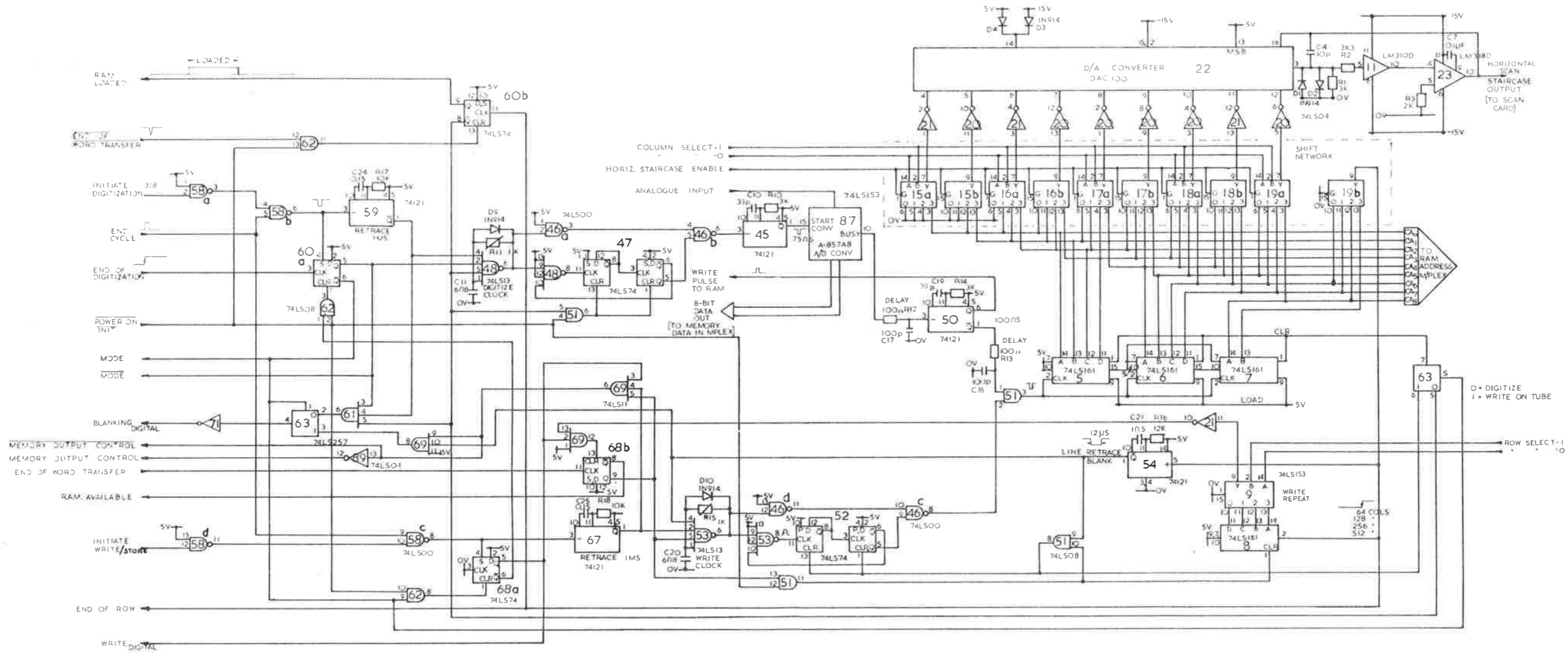


FIGURE II-4 COLUMN COUNTER

DR11B - STORAGE TUBE I/F CARD



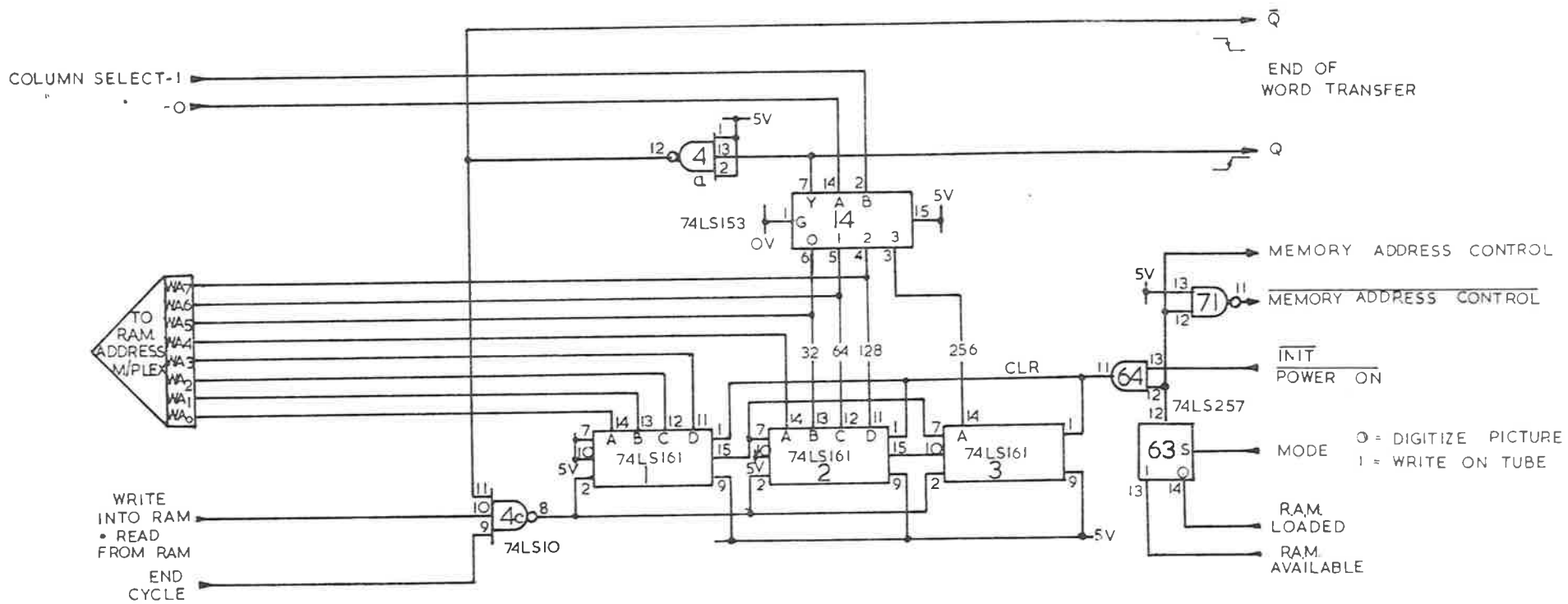
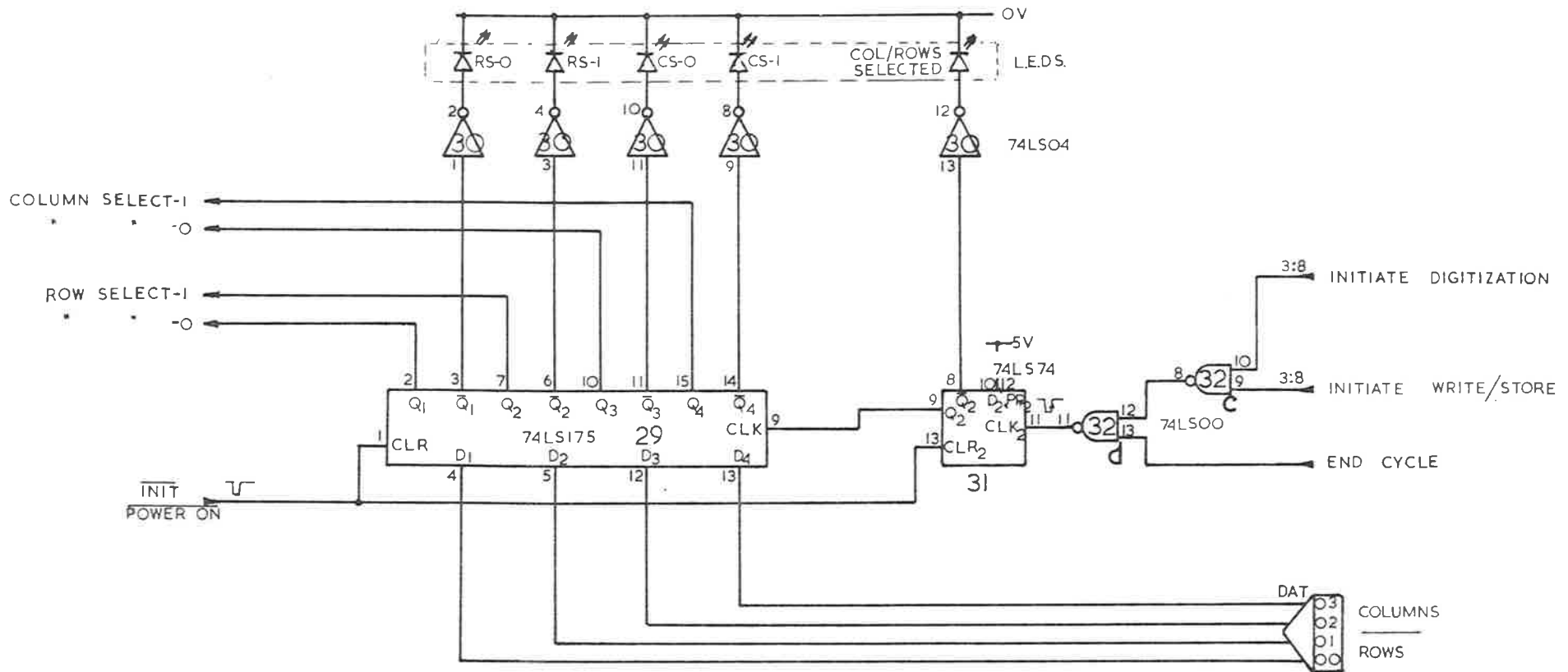


FIGURE II-6 WORD TRANSFER COUNTER DR11B - STORAGE TUBE I/F CARD

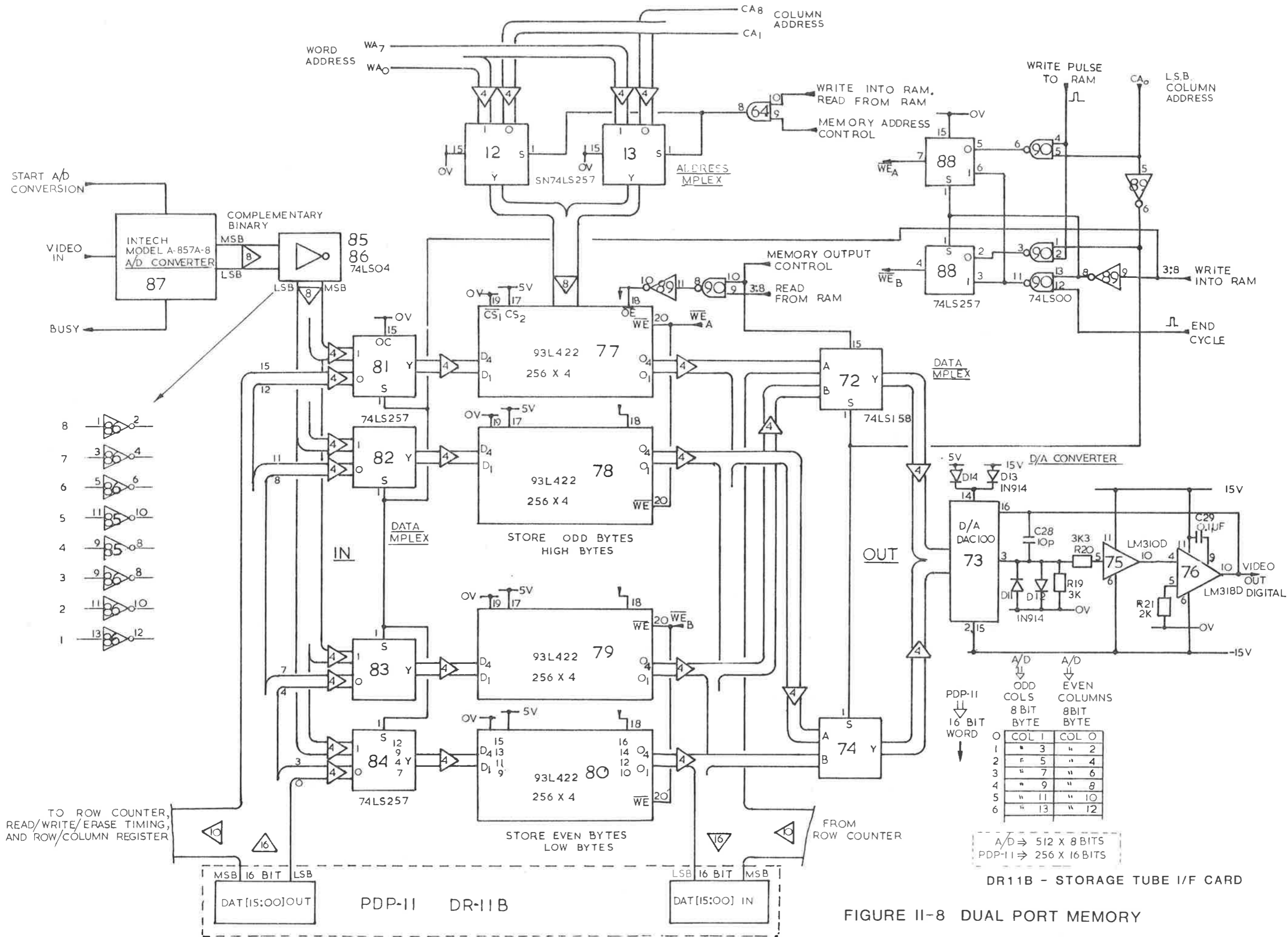


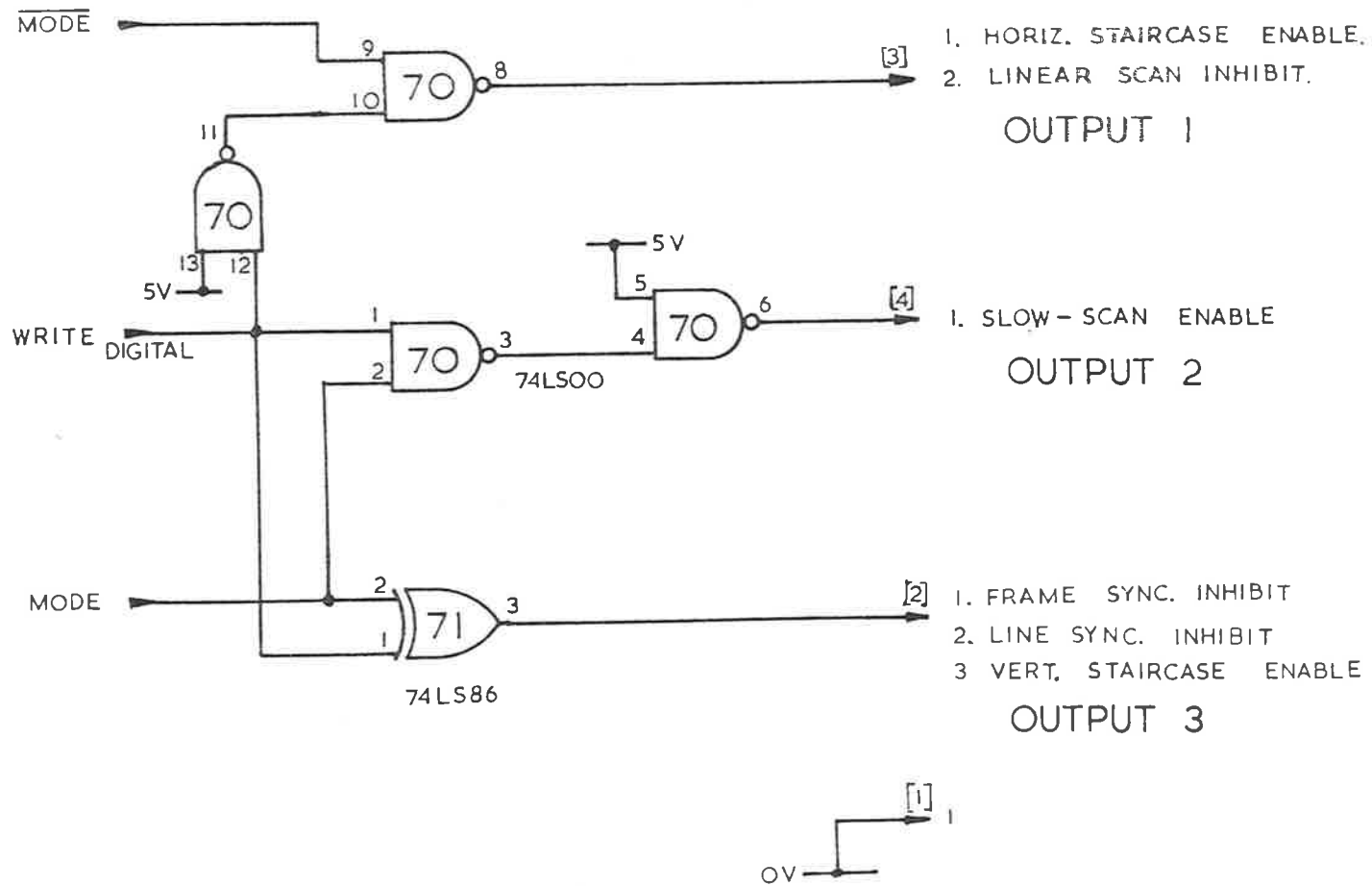


ROWS	RS-I	RS-O
COLUMNS	CS-I	CS-O
64	0	0
128	0	1
256	1	0
512	1	1

DAT <sub>O3</sub>	DAT <sub>O2</sub>	DAT <sub>O1</sub>	DAT <sub>O0</sub>
CS-I	CS-O	RS-I	RS-O

FIGURE II-7 ROW/COLUMN REGISTER DR11B - STORAGE TUBE I/F CARD





- 1. HORIZ. STAIRCASE ENABLE.
- 2. LINEAR SCAN INHIBIT.

OUTPUT 1

- 1. SLOW-SCAN ENABLE

OUTPUT 2

- 1. FRAME SYNC. INHIBIT
- 2. LINE SYNC. INHIBIT
- 3. VERT. STAIRCASE ENABLE

OUTPUT 3

FIGURE II-9 SCAN CONTROL/INTERLOCK DR11B - STORAGE TUBE I/F CARD

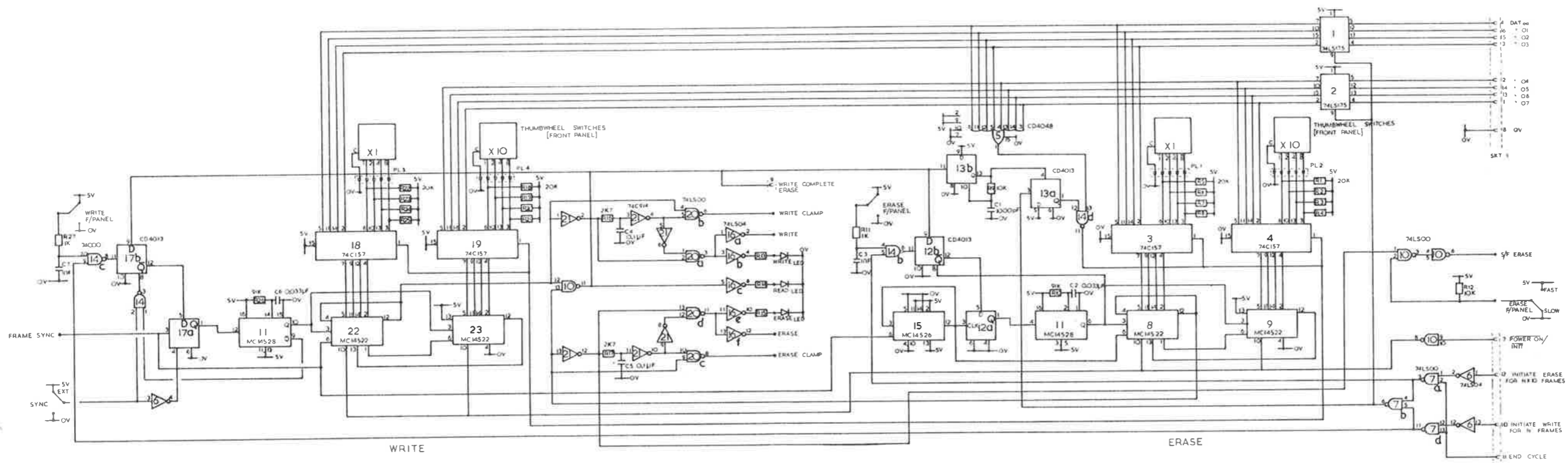


FIGURE II-10 READ-WRITE-ERASE TIMING

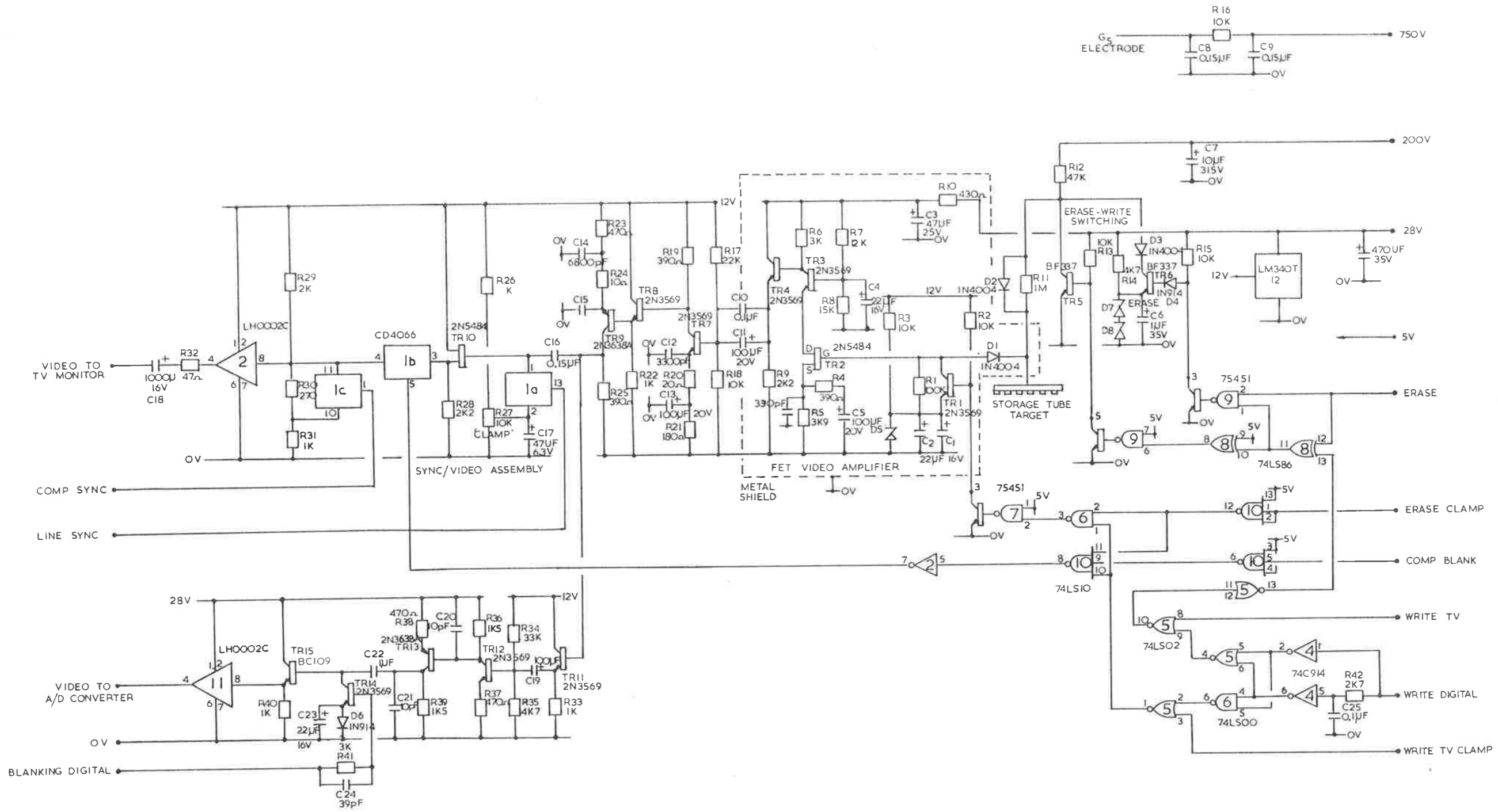


FIGURE II-11 READ AMPLIFIER

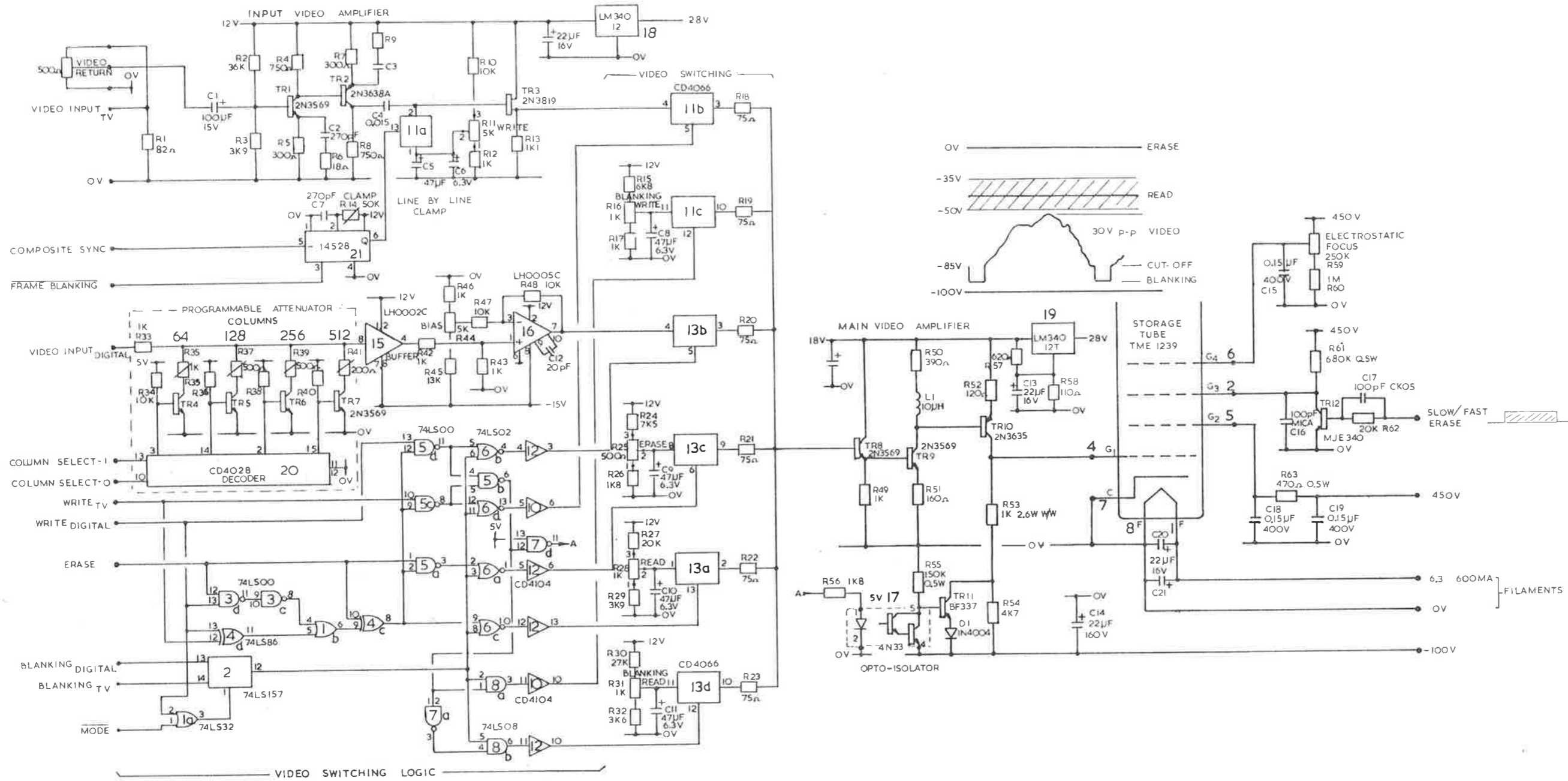


FIGURE II-12 WRITE AMPLIFIER

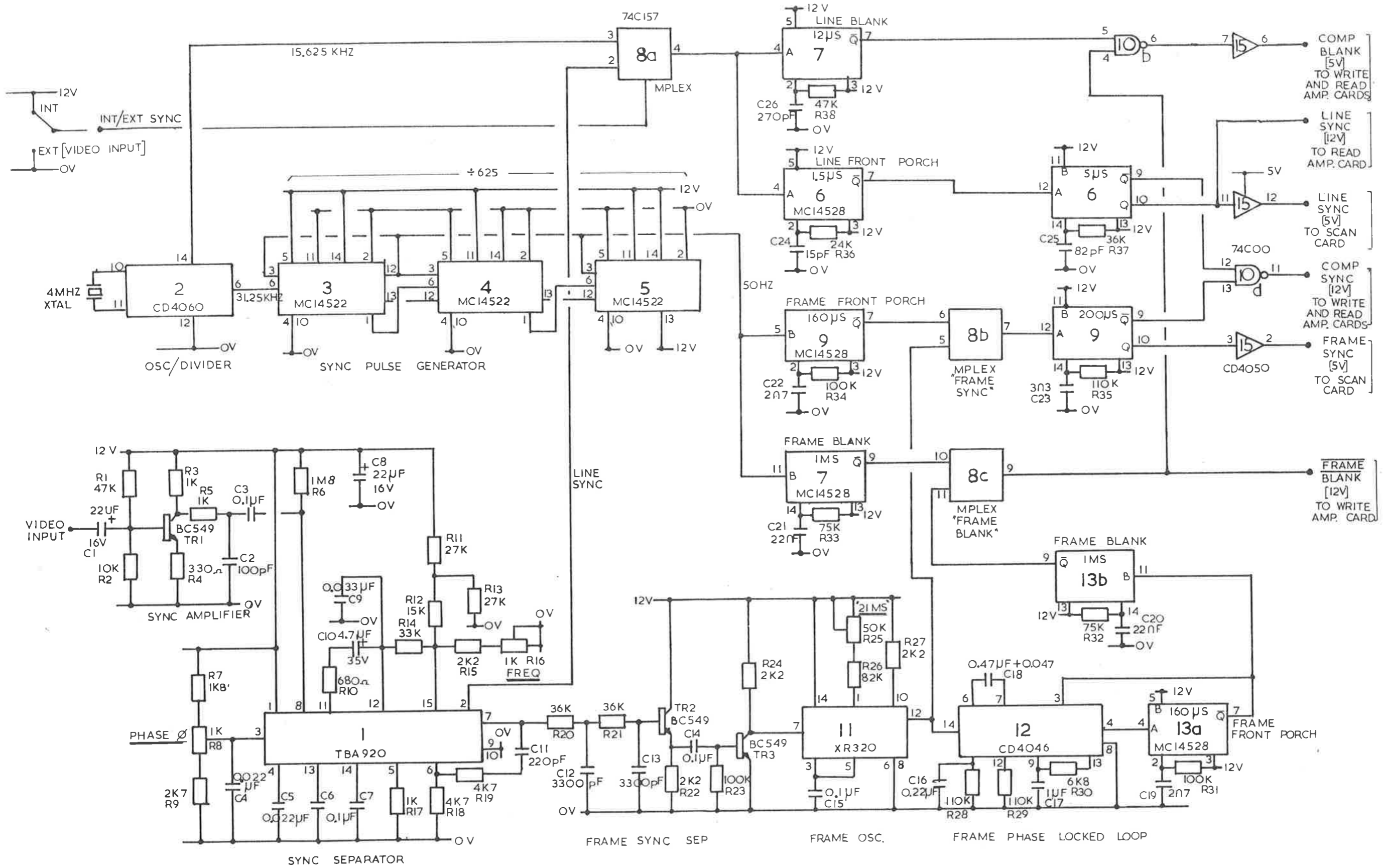
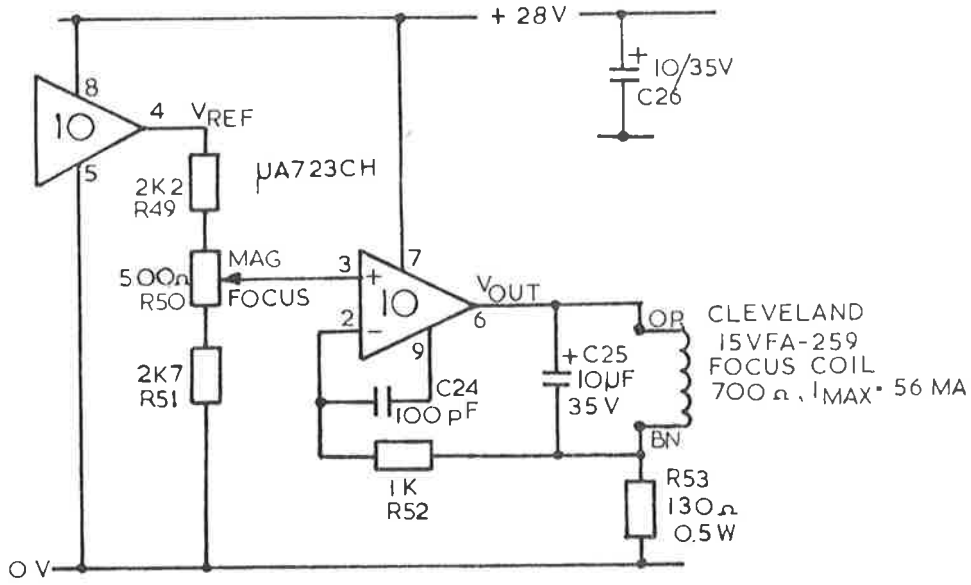


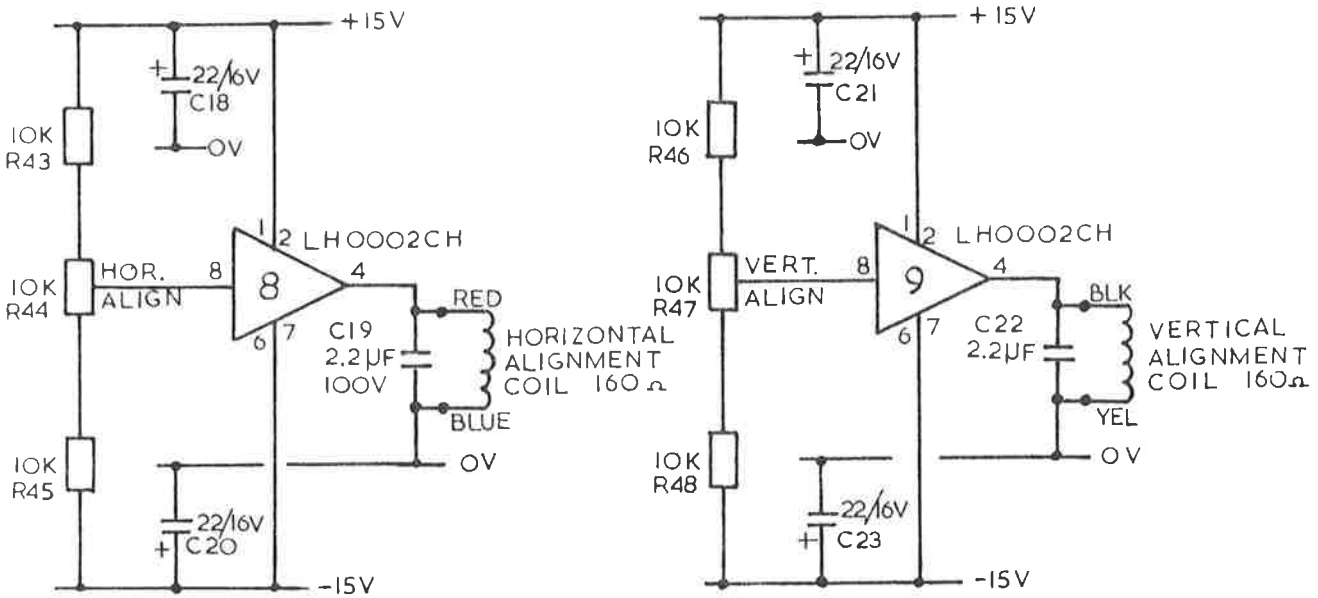
FIGURE II-13 SYNC SEPARATOR/GENERATOR







**MAGNETIC FOCUS**



**MAGNETIC ALIGNMENT**

FIGURE II-15 MAGNETIC ALIGNMENT / FOCUS

SCAN CARD

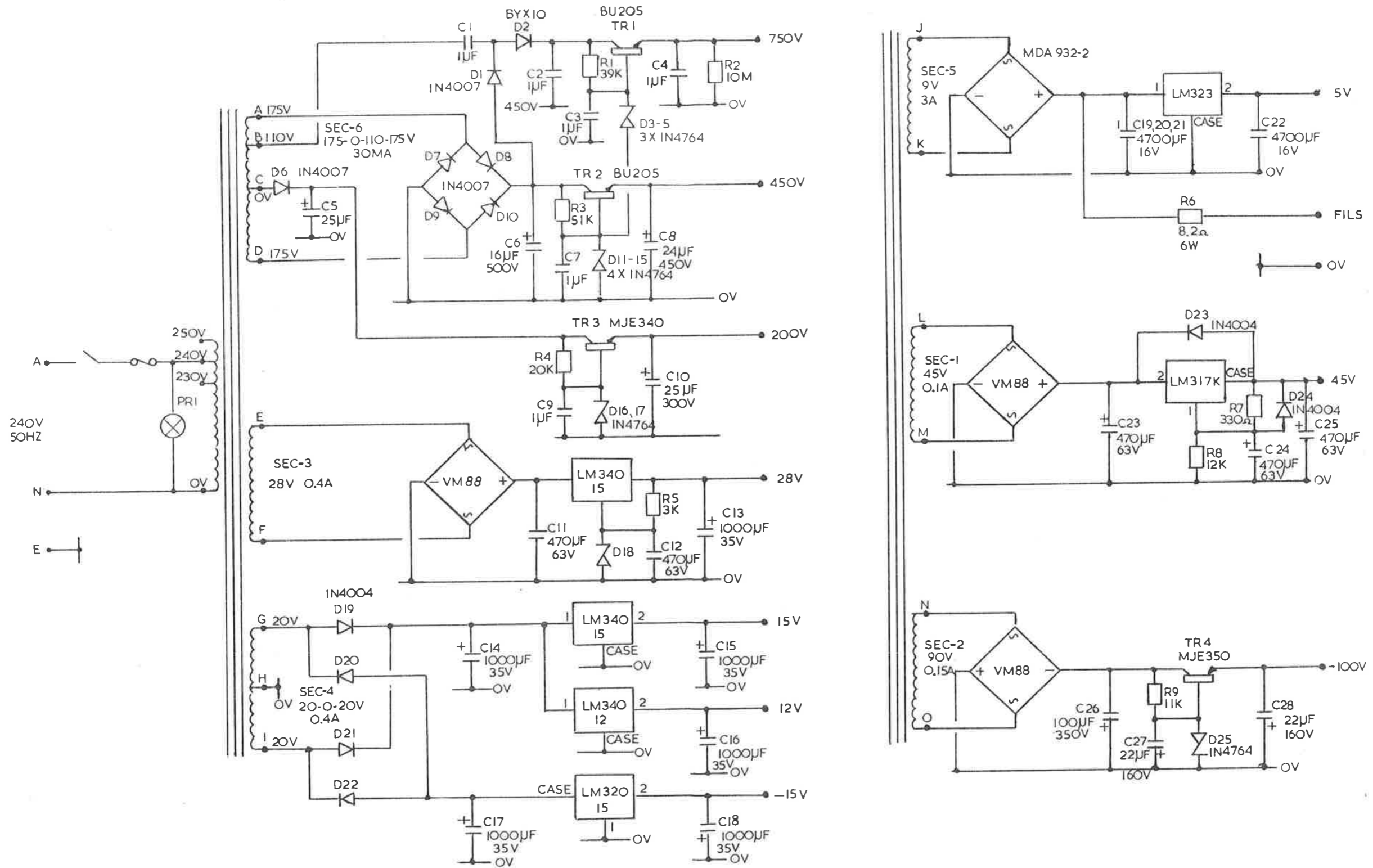


FIGURE II-16 POWER SUPPLY

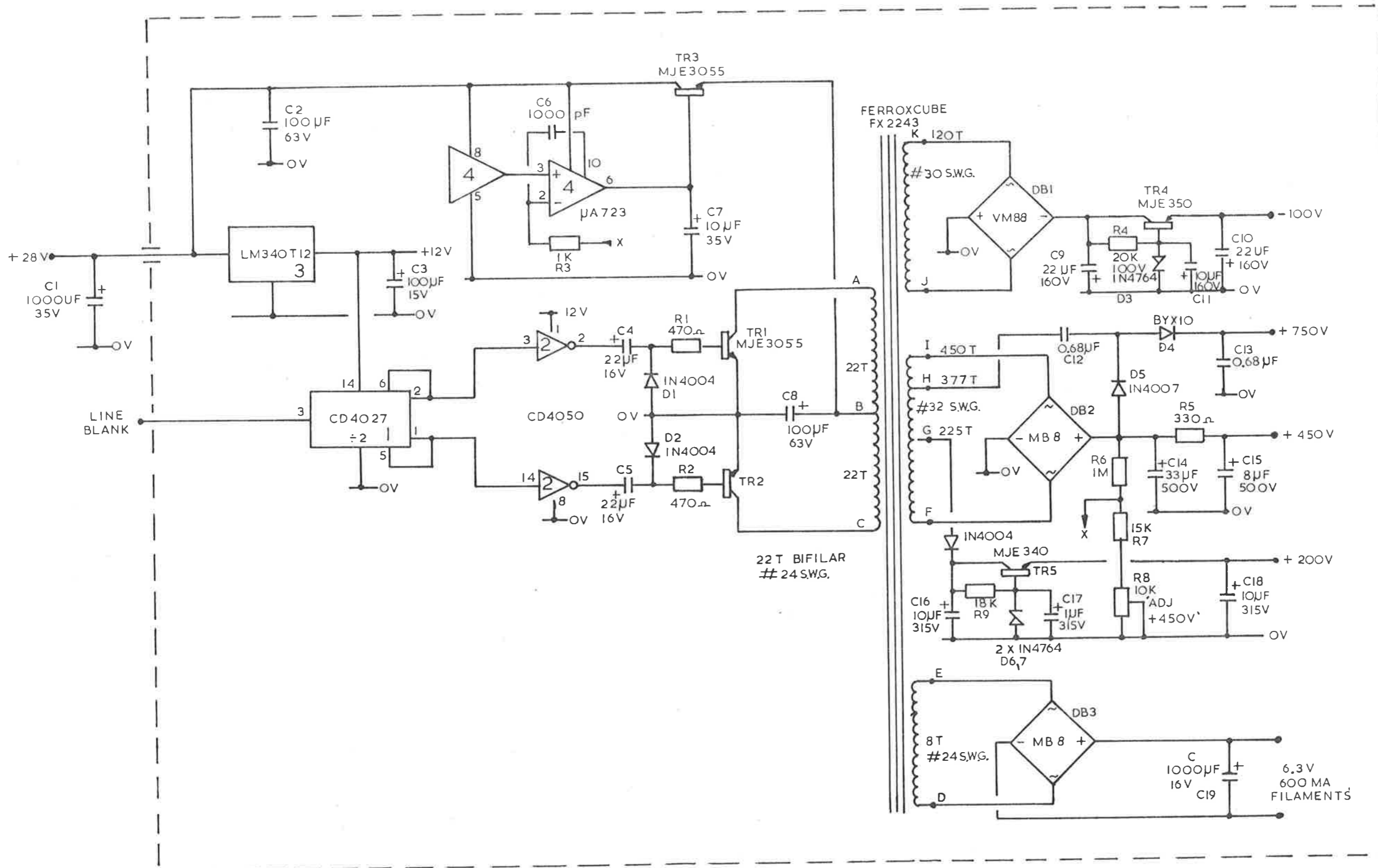


FIGURE II-17 H.T. INVERTER

DRIIB-STORAGE TUBE INTERFACE CARD

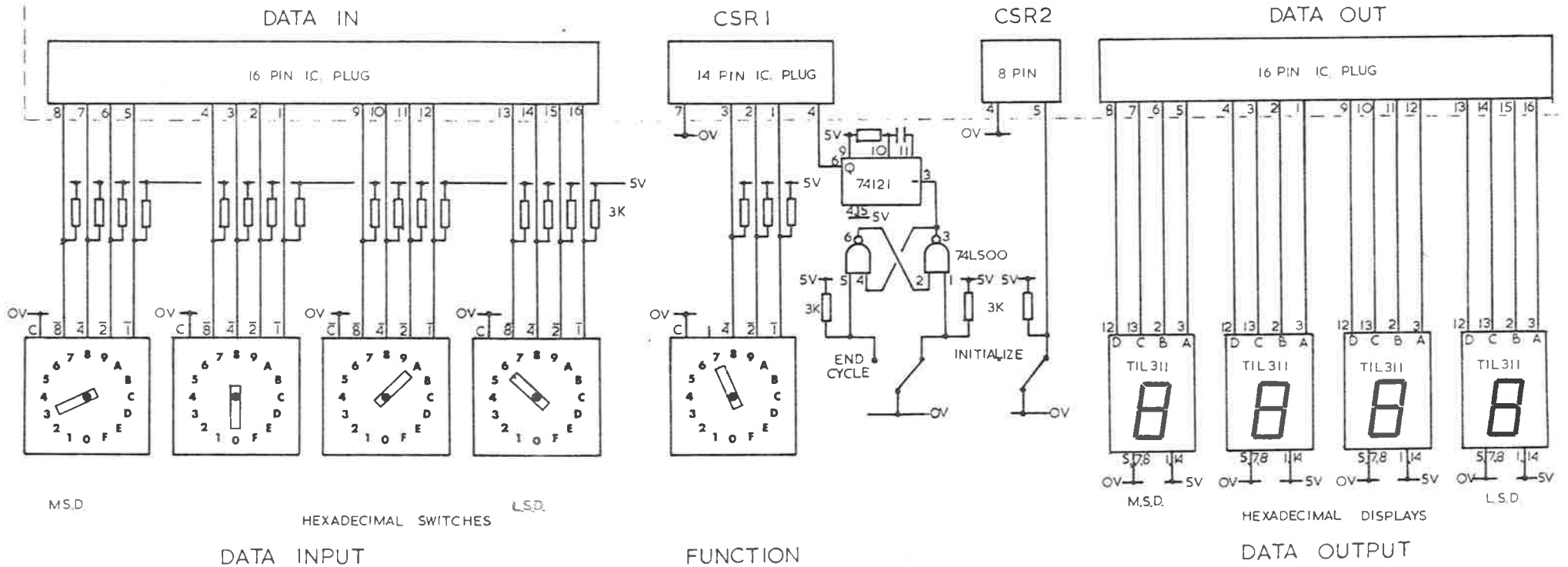


FIGURE II-18 MANUAL INTERFACE TESTER

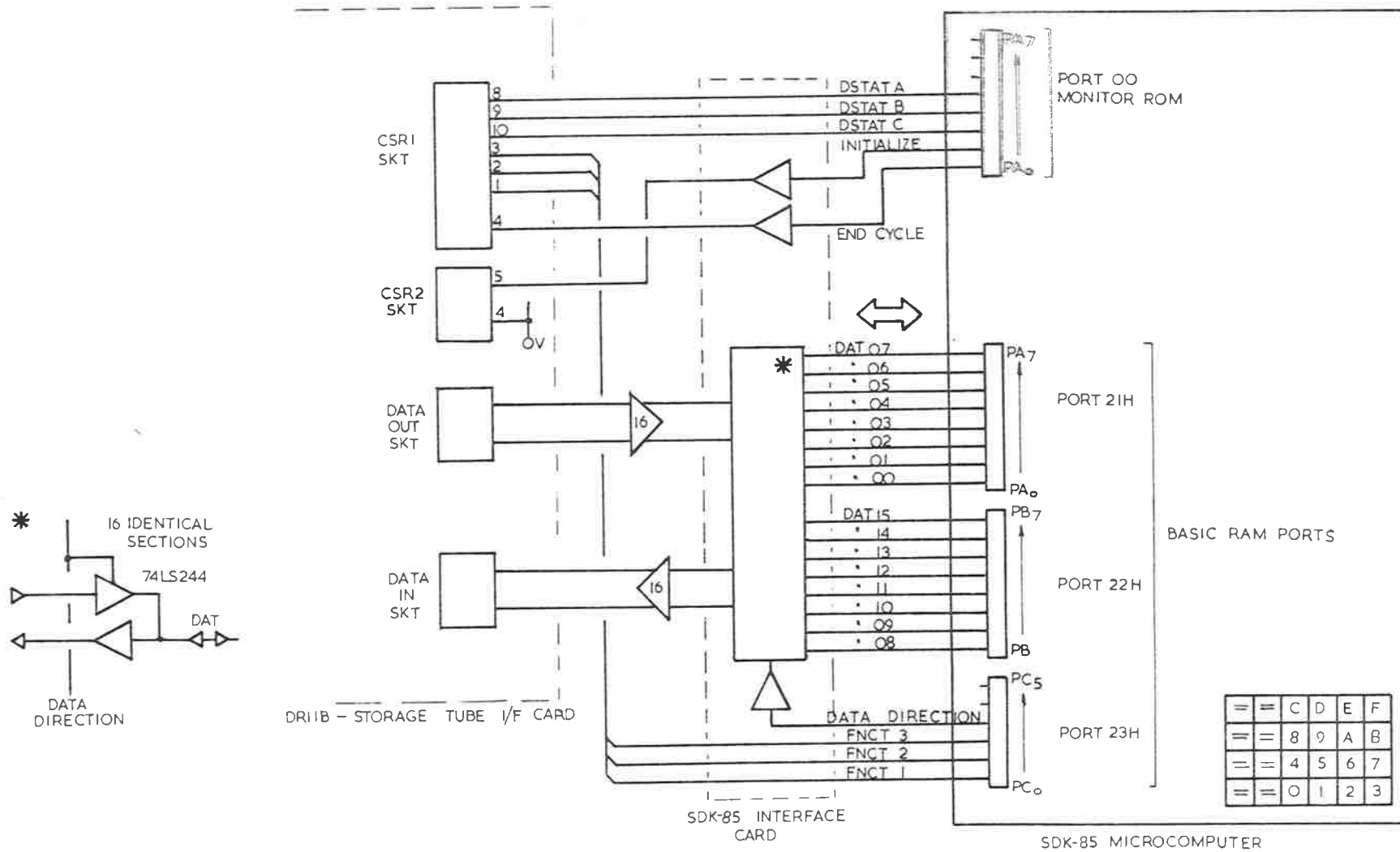
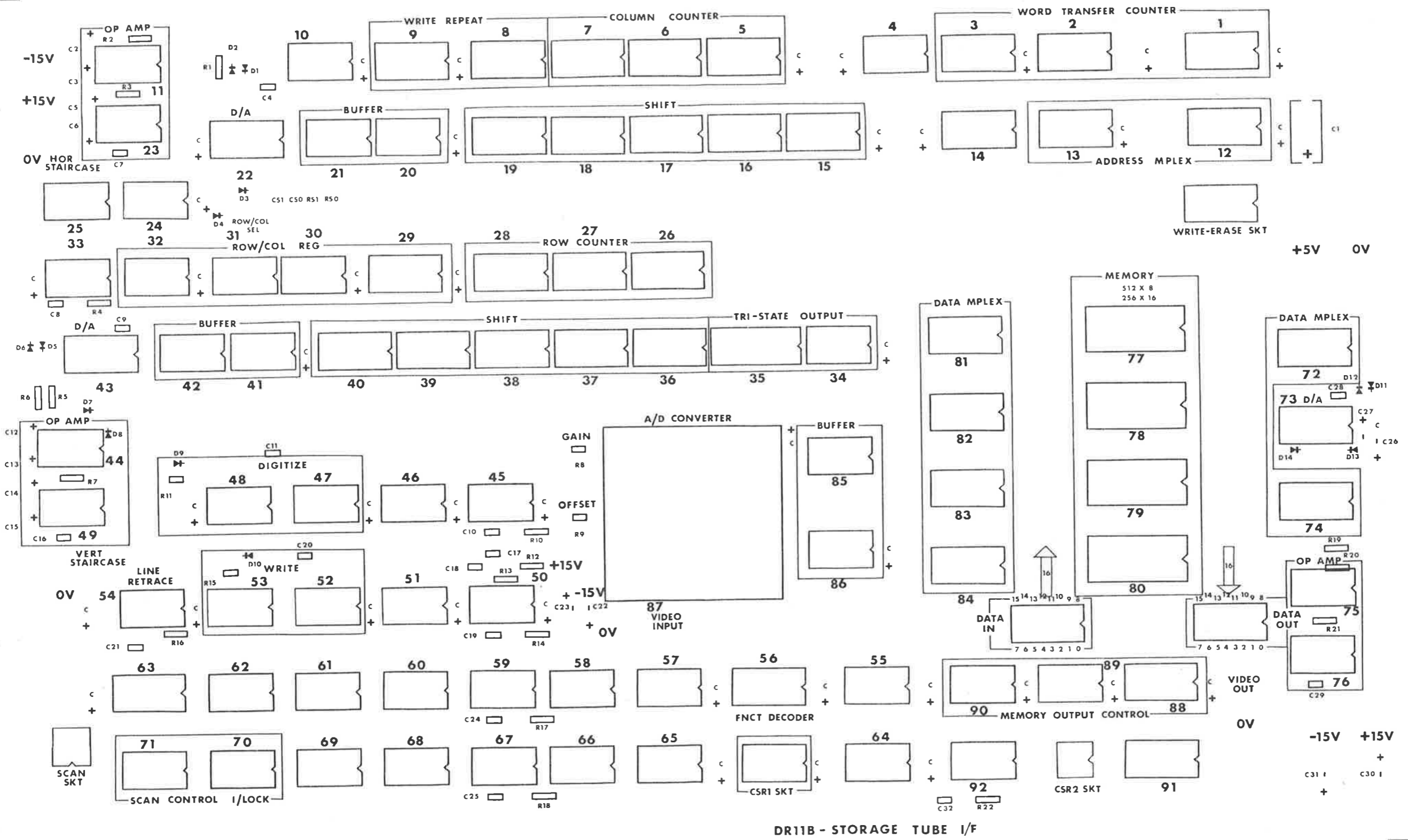


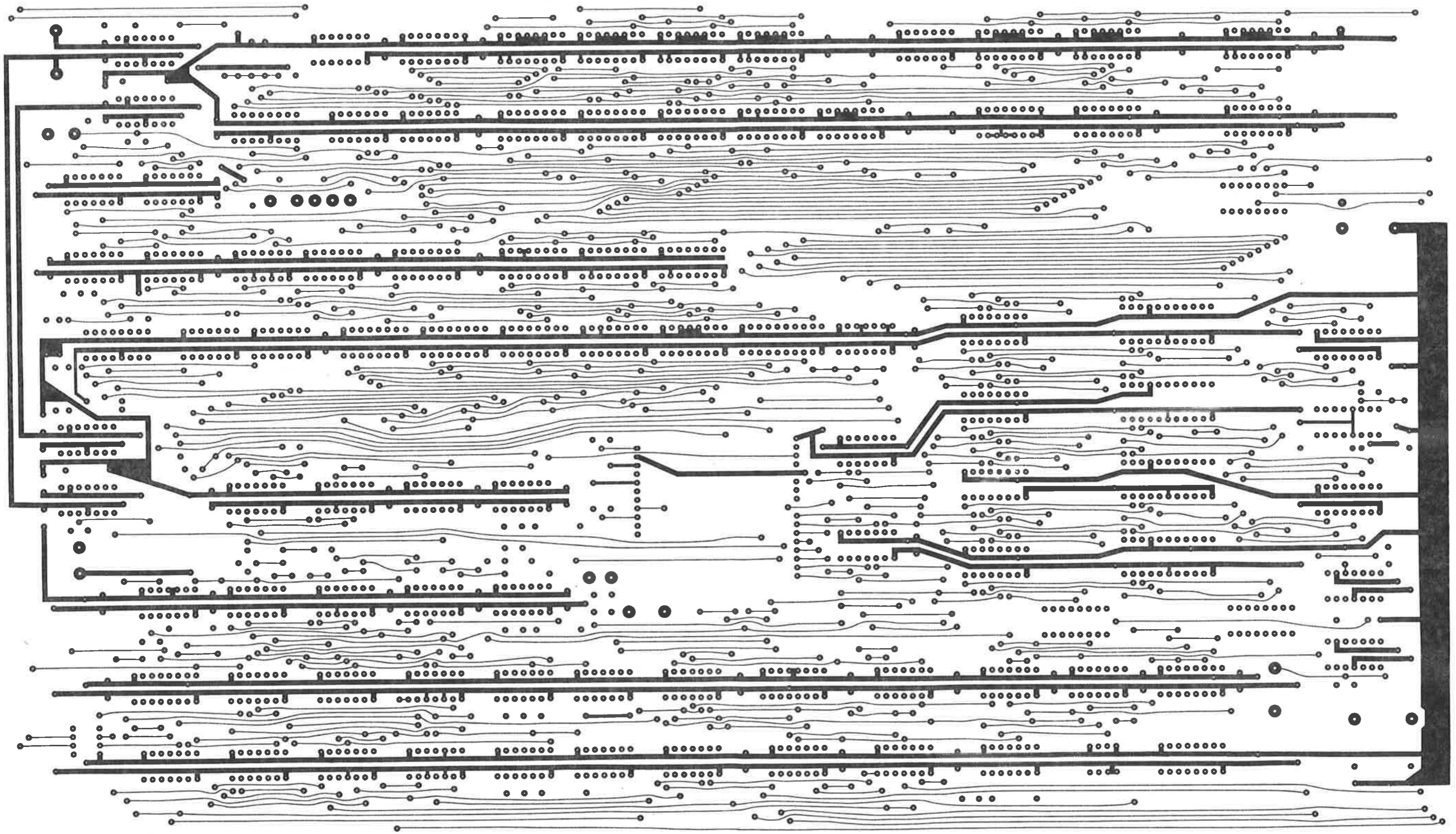
FIGURE II-19 SDK-85 MICROCOMPUTER INTERFACE TESTER



OVERLAY SILK SCREEN WHITE

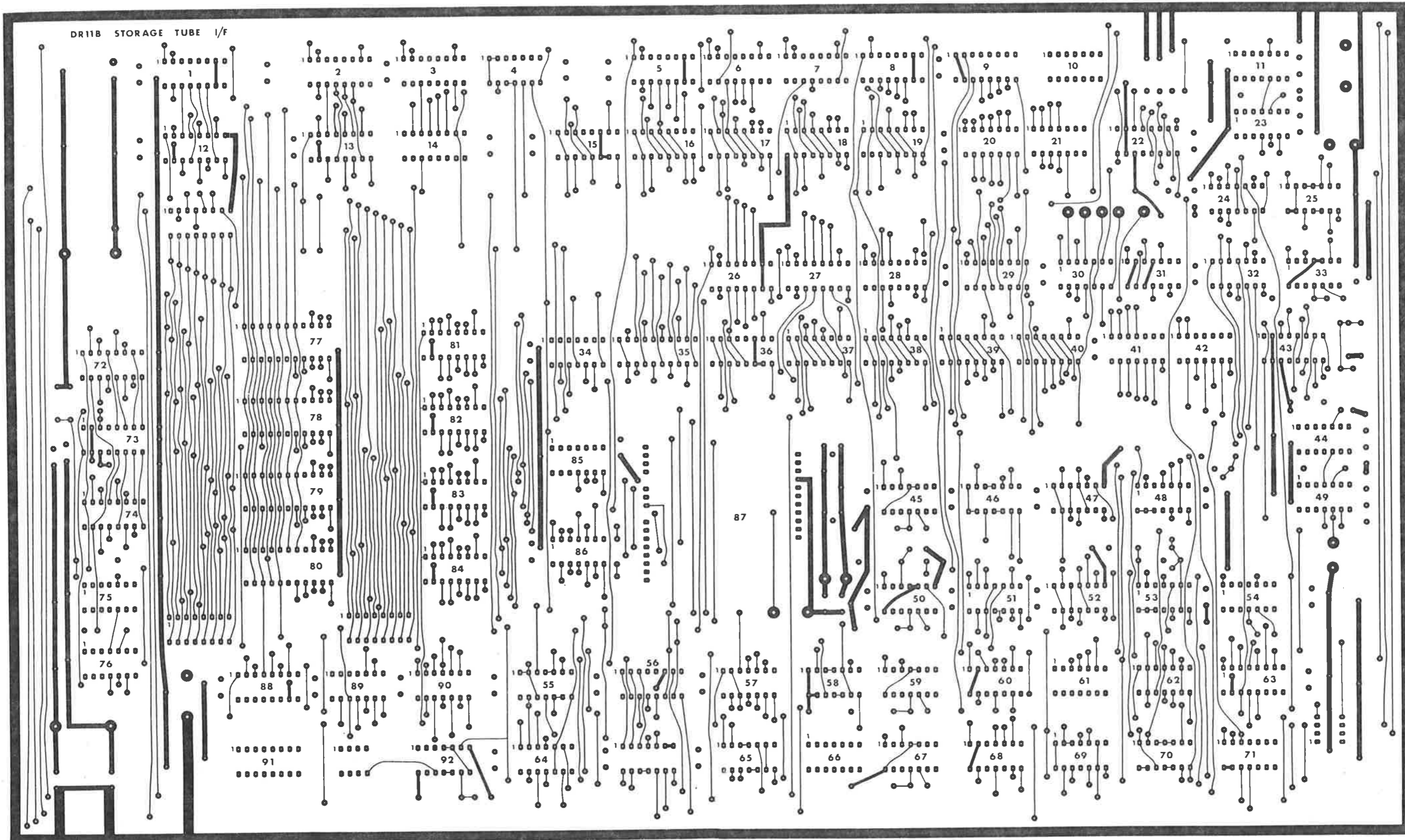
REDUCED 0.8:1

FIGURE II-20 DR11B - STORAGE TUBE INTERFACE CARD ARTWORK - OVERLAY



REDUCED 0.8:1

FIGURE II-20 COMPONENT SIDE



REDUCED 0.8:1

FIGURE II-20 TRACK SIDE



APPENDIX III

MICROCOMPUTER TEST PROGRAMS

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

;*****
; ADDRESS SPACE
;
; 1. 2000 - 20C9 AVAILABLE IN BASIC RAM
;                FOR PROGRAM DEVELOPMENT
; 2. 20C8 - 20FF RESERVED BY THE MONITOR PROGRAM
; 3. 2800 - 28F0 AVAILABLE IN EXPANSION RAM
;                FOR PROGRAM DEVELOPMENT
; 4. 28F1 - 28FF RESERVED FOR PROGRAM STACK
;*****
; TITLE:
; TITLE 'IMAGE PROCESSING TERMINAL
;        SDK-85 MICROCOMPUTER TEST PROGRAM'
;*****
;ASSIGN LABELS TO IMAGE PROCESSING TERMINAL
;MODES OF OPERATION
;*****
0000 FNCT0 EQU 00H ;FUNCTION 0 READ ROW NUMBER
0009 FNCT1 EQU 09H ;FUNCTION 1 WRITE ROW NUMBER
0002 FNCT2 EQU 02H ;FUNCTION 2 READ FROM RAM
000B FNCT3 EQU 0BH ;FUNCTION 3 WRITE INTO RAM
000C FNCT4 EQU 0CH ;FUNCTION 4 INITIATE DIGITIZATION
000D FNCT5 EQU 0DH ;FUNCTION 5 INITIATE WRITE (DIGITAL)
000E FNCT6 EQU 0EH ;FUNCTION 6 INITIATE WRITE (TV)
000F FNCT7 EQU 0FH ;FUNCTION 7 INITIATE ERASE
;*****
; MATRIX ROW/COLUMN CODES
; FOR: 1. DIGITIZATION - FUNCTION 4
;       2. WRITE(DIGITAL) - FUNCTION 5
;*****
0000 MAT01 EQU 00H ; 64 ROWS X 64 COLUMNS
0001 MAT02 EQU 01H ; 128 ROWS X 64 COLUMNS
0002 MAT03 EQU 02H ; 256 ROWS X 64 COLUMNS
0003 MAT04 EQU 03H ; 512 ROWS X 64 COLUMNS
0004 MAT05 EQU 04H ; 64 ROWS X 128 COLUMNS
0005 MAT06 EQU 05H ; 128 ROWS X 128 COLUMNS
0006 MAT07 EQU 06H ; 256 ROWS X 128 COLUMNS
0007 MAT08 EQU 07H ; 512 ROWS X 128 COLUMNS
0008 MAT09 EQU 08H ; 64 ROWS X 256 COLUMNS
0009 MAT10 EQU 09H ; 128 ROWS X 256 COLUMNS
000A MAT11 EQU 0AH ; 256 ROWS X 256 COLUMNS
000B MAT12 EQU 0BH ; 512 ROWS X 256 COLUMNS
000C MAT13 EQU 0CH ; 64 ROWS X 512 COLUMNS
000D MAT14 EQU 0DH ; 128 ROWS X 512 COLUMNS
000E MAT15 EQU 0EH ; 256 ROWS X 512 COLUMNS
000F MAT16 EQU 0FH ; 512 ROWS X 512 COLUMNS
;*****

```



IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

;
;          PORT 22H = INPUT
;          PORT 23H = OUTPUT
;          2.  ACCEPTS FNCT 1, 2 AND 3 IN B REGISTER,
;              AND OUTPUTS FUNCTION TO PORT 23H.
;
200E  3E0C  DIN:    MVI    A,0CH  ;SET I/O CODE FOR C/S REGISTER
2010  D320          OUT    20H  ;OUTPUT TO C/S REGISTER
2012   78          MOV    A,B   ;RETRIEVE FUNCTION CODE
2013  D323          OUT    23H  ;OUTPUT FUNCTION
2015  C9           RET          ;RETURN
;
;*****
;  SUBROUTINE          LOAD THE ROW COUNTER IN THE
;  'WRROW'            IMAGE PROCESSING TERMINAL
;                    (ROW NO. STORED IN REGISTER PAIR D+E)
;
2016  3E09  WRROW:  MVI    A, FNCT1 ;SET FUNCTION 1 - WRITE
2018  D323          OUT    23H  ;/ROW NUMBER
201A   7B          MOV    A,E   ;MOVE LOW BYTE
201B  D321          OUT    21H  ;/TO DATA BUS 00-07
201D   7A          MOV    A,D   ;MOVE HIGH BYTE
201E  D322          OUT    22H  ;/TO DATA BUS 08-15
2020  3E01          MVI    A,01H ;PULSE 'END CYCLE' TO
2022  CD0020        CALL   PULSE  ;/LOAD ROW NUMBER
2025  C9           RET          ;RETURN
;
;*****
;  SUBROUTINE          READ THE ROW COUNTER IN THE
;  'REROW'            IMAGE PROCESSING TERMINAL
;                    (ROW NO. MOVED TO REGISTER PAIR D+E)
;
2026  3E00  REROW:  MVI    A, FNCT0 ;SET FUNCTION 0 - READ
2028  D323          OUT    23H  ;/ROW NUMBER
202A  DB21          IN     21H  ;INPUT FROM DATA BUS 00-07
202C   5F          MOV    E,A   ;STORE LOW BYTE IN REGISTER E
202D  DB22          IN     22H  ;INPUT FROM DATA BUS 08-15
202F   57          MOV    D,A   ;STORE HIGH BYTE IN REGISTER D
2030  3E01          MVI    A,01H ;PULSE 'END CYCLE'
2032  CD0020        CALL   PULSE ;
2035  C9           RET          ;RETURN
;
;*****
;
;          PROGRAMS
;*****
;  'START'  1.  INITIALIZES STACK POINTER
;            2.  SETS DATA DIRECTION REGISTER, PORT 02H,
;                FOR PORT 00H  BITS 0,1 = OUTPUT
;                            BITS 2-7 = INPUT
;            3.  RESETS IMAGE PROCESSING TERMINAL LOGIC

```

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

;          4. RETURNS TO MONITOR PROGRAM
;
2036 31FF28 START: LXI SP,28FFH;DEFINE STACK POINTER AT 2800
2039 3E03      MVI A,03H ;
203B D302      OUT 02H ;SET DATA DIRECTION REGISTER
203D AF        XRA A ;CLEAR A REGISTER
203E D300      OUT 00H ;
2040 3E02      MVI A,02H ;SET BIT 1, A REGISTER
2042 CD0020    CALL PULSE ;INITIALIZE (RESET)
2045 CF        RST 1 ;RETURN TO MONITOR PROGRAM
;
;*****
; 'RESET' PULSES 'INITIALIZE' WHICH RESETS ALL LOGIC
; WITHIN THE IMAGE PROCESSING TERMINAL
;
2046 3E02      RESET: MVI A,02H ;SET BIT 1, A REGISTER
2048 CD0020    CALL PULSE ;PULSE 'INITIALIZE'
204B CF        RST 1 ;RETURN TO MONITOR PROGRAM
;
;*****
; 'WRTV' STORES AN IMAGE FROM A CONVENTIONAL TV SOURCE
;
; 1. SETS UP DATA DIRECTION REGISTER ASSOCIATED
; WITH I/O PORTS
; 2. SETS FUNCTION BITS TO BINARY 6 - WRITE(TV)
; 3. OUTPUTS WRITE FRAMES
; 4. WRITE(TV) INITIATED BY 'END CYCLE' PULSE
; 5. RETURNS TO MONITOR PROGRAM
;
204C 060E      WRTV: MVI B,FNCT6 ;SET FUNCTION 6 - WRITE(TV)
204E CD0620    CALL DOUT ;SET DATA DIRECTION REGISTERS
; /ASSOCIATED WITH SDK85 I/O PORTS
2051 3E02      MVI A,02D ;SET NUMBER OF TV FRAMES = 2
2053 D321      OUT 21H ;OUTPUT TO PORT 21H
2055 3E01      MVI A,01H ;SET BIT 0, A REGISTER
2057 CD0020    CALL PULSE ;TRANSMIT 'END CYCLE' PULSE
; /TO EXECUTE WRITE(TV)
205A CF        RST 1 ;RETURN TO MONITOR PROGRAM
;
;*****
; 'ERASE' ERASES STORAGE TUBE
;
; 1. SETS UP DATA DIRECTION REGISTER ASSOCIATED
; WITH I/O PORTS
; 2. SETS FUNCTION BITS TO BINARY 7 - ERASE
; 3. OUTPUTS ERASE FRAMES X 10
; 4. ERASE INITIATED BY 'END CYCLE' PULSE
; 5. RETURNS TO MONITOR PROGRAM
;
205B 060F      ERASE: MVI B,FNCT7 ;SET FUNCTION 7 - ERASE
205D CD0620    CALL DOUT ;SETS DATA DIRECTION REGISTERS

```

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

; /ASSOCIATED WITH SDK85 I/O PORTS
2060 3E0A MVI A,10D ;SET NUMBER OF TV FRAMES = 10 X 10
2062 D321 OUT 21H ;OUTPUT TO PORT 21H
2064 3E01 MVI A,01H ;SET BIT 0, A REGISTER
2066 CD0020 CALL PULSE ;TRANSMIT 'END CYCLE' PULSE
; /TO EXECUTE ERASE
2069 CF RST 1 ;RETURN TO MONITOR PROGRAM
;
; *****
; 'WRCOL' WRITES A SERIES OF BLACK AND WHITE
; VERTICAL BARS ON THE STORAGE TUBE
;
206A 110000 WRCOL: LXI D,0000H ;REGISTER PAIR D+E IS
; /16-BIT ROW COUNTER,
; /INITIALIZE TO ZERO
;
; INITIATE WRITING DIGITAL INFORMATION ON STORAGE TUBE
206D 060D MVI B, FNCT5 ;SET FUNCTION 5 - WRITE(DIGITAL)
206F CD0620 CALL DOUT ;SET UP I/O PORTS FOR OUTPUT
2072 3E02 MVI A, MAT03 ;INITIATE WRITE OVER
; /256 ROWS X 64 COLUMNS
2074 D321 OUT 21H ;OUTPUT TO DATA BUS 00-07
2076 3E01 MVI A,01H ;SET BIT 0, A REGISTER
2078 CD0020 CALL PULSE ;PULSE 'END CYCLE'
;
; TEST FOR MEMORY AVAILABLE
207B ROWS:
207B DB00 NORAM: IN 00H ;READ DEVICE STATUS BITS
207D E610 ANI 10H ;MASK DSTAT A - (BIT 4)
207F CA7B20 JZ NORAM ;WAIT FOR RAM AVAILABLE
;
; WRITE ROW NUMBER
;
2082 CD1620 CALL WRROW ;WRITE ROW NUMBER
;
; OUTPUT ONE ROW OF DATA
; WRITE 00H IN EVEN COLUMNS
; WRITE FFH IN ODD COLUMNS
;
2085 AF XRA A ;CLEAR A REGISTER
2086 D321 OUT 21H ;OUTPUT 00 TO DATA BUS 00-07
2088 2F CMA ;SET A REGISTER TO FF
2089 D322 OUT 22H ;OUTPUT FF TO DATA BUS 08-15
;
; INITIATE WRITE INTO DUAL PORT MEMORY
208B 3E0B MVI A, FNCT3 ;SET FUNCTION 3 - WRITE INTO RAM
208D D323 OUT 23H ;
208F 3E01 MVI A,01H ;SET BIT 0, A REGISTER
2091 CD0020 CALL PULSE ;PULSE 'END CYCLE'
;
2094 010000 LXI B,0000H ;REGISTER PAIR B + C
```

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

;
; /IS COLUMN COUNTER
; /INITIALIZE TO ZERO
;
2097 3E01 COLS: MVI A,01H ;SET BIT 0, A REGISTER
2099 CD0020 CALL PULSE ;PULSE 'END CYCLE' AND
; /TRANSMIT 00-FF
;
209C 03 INX B ;STEP TO NEXT COLUMN PAIR
209D 79 MOV A,C ;NOTE: IF 512 COLUMNS MOV A,B
209E FE20 CPI C64 ;TEST FOR END OF COLUMNS
20A0 C29720 JNZ COLS ;NO, TRANSMIT NEXT
; COLUMN PAIR
20A3 13 INX D ;MOVE TO NEXT ROW
20A4 13 INX D ;
20A5 7A MOV A,D ;
20A6 FE02 CPI R512 ;TEST FOR END OF ROWS
20A8 C27B20 JNZ ROWS ;NO, GO TO NEXT ROW
;
; RESET IMAGE PROCESSING TERMINAL LOGIC
20AB 3E02 MVI A,02H ;SET BIT 1, A REGISTER
20AD CD0020 CALL PULSE ;PULSE 'INITIALIZE'
;
20B0 C36A20 JMP WRCOL ;REPEAT THE PROCESS
; REPLACE THIS STATEMENT WITH
; /RST 1 (CF) WHEN EXECUTING
; /THE PROGRAM ONCE
;
; *****
; PROGRAM CONTINUES IN EXPANSION RAM
;
2800 ORG 2800H ;SET ASSEMBLER LOCATION COUNTER
; TO ADDRESS 2800
;
; *****
; 'WRST' WRITES A STAIRCASE FUNCTION ACROSS
; STORAGE TUBE RANGING FROM BLACK
; ON THE LEFT TO WHITE ON THE RIGHT
;
2800 110000 WRST: LXI D,0000H ;REGISTER PAIR D+E IS
; /16-BIT ROW COUNTER,
; /INITIALIZE TO ZERO
;
; INITIATE WRITING DIGITAL INFORMATION ON STORAGE TUBE
2803 060E MVI B, FNCT6 ;SET FUNCTION 6 - WRITE(DIGITAL)
2805 CD0620 CALL DOUT ;SET UP I/O PORTS FOR OUTPUT
2808 3E06 MVI A, MAT07 ;INITIATE WRITE OVER
; /256 ROWS X 128 COLUMNS
280A D321 OUT 21H ;OUTPUT TO DATA BUS 00-07
280C 3E01 MVI A,01H ;SET BIT 0, A REGISTER
280E CD0020 CALL PULSE ;PULSE 'END CYCLE'
;

```

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

; TEST FOR MEMORY AVAILABLE
2811 RWS:
2811 DB00 NRAM: IN 00H ;READ DEVICE STATUS BITS
2813 E610 ANI 10H ;MASK DSTAT A - (BIT 4)
2815 CA1128 JZ NRAM ;WAIT FOR RAM AVAILABLE
;
; WRITE ROW NUMBER
;
2818 CD1620 CALL WRROW ;WRITE ROW NUMBER
;
; OUTPUT ONE ROW OF DATA BY NORMALIZING THE COLUMN COUNT
; TO 512 AND OUTPUT COLUMN COUNT TO
; DUAL PORT MEMORY
;
; INITIATE WRITE INTO DUAL PORT MEMORY
281B 3E0B MVI A, FNCT3 ;SET FUNCTION 3 - WRITE INTO RAM
281D D323 OUT 23H ;
281F 3E01 MVI A, 01H ;SET BIT 0, A REGISTER
2821 CD0020 CALL PULSE ;PULSE 'END CYCLE'
;
2824 010000 LXI B, 0000H ;REGISTER PAIR B + C
; /IS COLUMN COUNTER
; /INITIALIZE TO ZERO
;
2827 79 COL: MOV A, C ;
2828 D321 OUT 21H ;OUTPUT EVEN COLUMN
282A 03 INX B ;STEP TO NEXT COLUMN
282B 03 INX B ;
;
282C 79 MOV A, C ;
282D D322 OUT 22H ;OUTPUT ODD COLUMN
282F 3E01 MVI A, 01H ;SET BIT 0, A REGISTER
2831 CD0020 CALL PULSE ;PULSE 'END CYCLE'
;
2834 03 INX B ;STEP TO NEXT COLUMN
2835 03 INX B ;
;
2836 78 MOV A, B ;
2837 FE02 CPI 02H ;TEST FOR END OF COLS
2839 C22728 JNZ COL ;NO, GO TO NEXT COLUMN PAIR
;
283C 13 INX D ;MOVE TO NEXT ROW
283D 13 INX D ;
283E 7A MOV A, D ;
283F FE02 CPI R512 ;TEST FOR END OF ROWS
2841 C21128 JNZ RWS ;NO, GO TO NEXT ROW
;
2844 C30028 JMP WRST ;REPEAT THE PROCESS
;REPLACE THIS STATEMENT WITH
; /RST 1 (CF) WHEN EXECUTING
; /THE PROGRAM ONCE
```



IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

```

;
;*****
;
; INITIATE IMAGE DIGITIZATION
;
2847 060C DIGIT: MVI B, FNCT4 ;SET FUNCTION 4 - DIGITIZATION
2849 CD0620 CALL DOUT ;SET UP I/O PORTS FOR OUTPUT
284C 3E05 MVI A, MAT06 ;INITIATE DIGITIZATION OVER
; /128 ROWS X 128 COLUMNS
284E D321 OUT 21H ;OUTPUT TO DATA BUS 00-07
2850 3E01 MVI A, 01H ;SET BIT 0, A REGISTER
2852 CD0020 CALL PULSE ;PULSE 'END CYCLE' TO
; /INITIATE DIGITIZATION
;
; TEST FOR MEMORY LOADED
2855 DB00 NOTLD: IN 00H ;READ DEVICE STATUS BITS
2857 E610 ANI 10H ;MASK DSTAT B - (BIT 3)
2859 CA5528 JZ NOTLD ;WAIT UNTIL ROW DIGITIZATION
; /IS COMPLETE
;
; READ DATA FROM DUAL PORT MEMORY
285C 0602 MVI B, FNCT2 ;SET FUNCTION 2 - READ FROM RAM
285E CD0E20 CALL DIN ;PREPARE TO INPUT DATA
;
; INPUT ONE ROW OF DATA
2861 010000 LXI B, 0000H ;REGISTER B IS COLUMN COUNTER
2864 DB21 COLMN: IN 21H ;INPUT EVEN COLUMN
2866 DB22 IN 22H ;INPUT ODD COLUMN
2868 03 INX B ;STEP TO NEXT COLUMN PAIR
;
2869 79 MOV A, C ;NOTE: IF 512 COLS MOV A, B
286A FE40 CPI C128 ;TEST FOR END OF COLUMNS
286C C26428 JNZ COLMN ;NO, READ NEXT COLUMN PAIR
;
; READ ROW NUMBER
286F CD2620 CALL REROW ;READ ROW NUMBER
2872 7B MOV A, E ;NOTE: IF 256 OR 512 ROWS MOV A, D
2873 FE80 CPI R128 ;TEST FOR END OF ROWS
2875 C25528 JNZ NOTLD ;NO, WAIT FOR DIGITIZATION
;
2878 C34728 JMP DIGIT ;REPEAT THE PROCESS
;REPLACE THIS STATEMENT WITH
; /RST 1 (CF) WHEN EXECUTING
; /THE PROGRAM ONCE
;
END ;END OF PROGRAM
```

NO PROGRAM ERRORS

IMAGE PROCESSING TERMINAL SDK-85 MICROCOMPUTER TEST PROGRAM

SYMBOL TABLE

\* 01

A	0007	B	0000	C	0001	C128	0040
C256	0080 *	C512	0010 *	C64	0020 *	COL	2827
COLMN	2864	COLS	2097	D	0002	DIGIT	2847
DIN	200E	DOUT	2006	E	0003	ERASE	205B *
FNCT0	0000	FNCT1	0009	FNCT2	0002	FNCT3	000B
FNCT4	000C	FNCT5	000D	FNCT6	000E	FNCT7	000F
H	0004	L	0005	M	0006	MAT01	0000 *
MAT02	0001 *	MAT03	0002 *	MAT04	0003 *	MAT05	0004 *
MAT06	0005	MAT07	0006	MAT08	0007 *	MAT09	0008 *
MAT10	0009 *	MAT11	000A *	MAT12	000B *	MAT13	000C *
MAT14	000D *	MAT15	000E *	MAT16	000F *	NORAM	207B
NOTLD	2855	NRAM	2811	PSW	0006	PULSE	2000
R128	0080	R256	0001 *	R512	0002	R64	0010 *
REROW	2026	RESET	2046 *	ROWS	207B	RWS	2811
SP	0006	START	2036 *	WRCOL	206A	WRROW	2016
WRST	2800	WRTV	204C *				

APPENDIX IV

IMAGE PROCESSING TERMINAL FORTRAN PROGRAMS

```
C   DEFINE THE ARRAY IDATA(1024) COMMON WITH THE INSTALLED
C   COMMON BLOCK 'IDATA'
C   COMMON /IDATA/ IDATA(1024)
C   DEFINE THE ARRAY IARRAY(4096) COMMON WITH THE INSTALLED
C   COMMON BLOCK 'EXT'
C   COMMON /EXT/ IARRAY(4096)
C
C   DECLARE THE FOLLOWING VARIABLES AS INTEGER
C   INTEGER DRWC,DRBA,DRST,DRDB
C   INTEGER ERROR,MAINT,DSTATA,DSTATB,DSTATC,READY,XBA,GO,FNCT
C   INTEGER ROWS,COLS,WORDS,WRITE,ERASE,MATRIX
C
C   DEFINE THE MEMORY ADDRESS FOR THE DATA BUFFER
C   DATA IBASE /"16600/
C
C   ASSIGN MNEMONIC NAMES TO ARRAY VARIABLES
C   EQUIVALENCE (IARRAY("5205),DRWC),(IARRAY("5206),DRBA)
C   EQUIVALENCE (IARRAY("5207),DRST),(IARRAY("5208),DRDB)
C
C   OPEN DISK FILE FOR DATA STORAGE
C   OPEN (UNIT=2,ACCESS='DIRECT',NAME='TWM.DAT',RECORDSIZE=64,
1  BLOCKSIZE=256,FORM='UNFORMATTED',TYPE='NEW')
C   DEFINE INTEGER CONSTANTS
C   ERROR = "100000
C   MAINT = "10000
C   DSTATA = "4000
C   DSTATB = "2000
C   DSTATC = "1000
C   READY = "200
C   XBA = "20
C   GO = "1
C
C   DEFINE IMAGE PROCESSING TERMINAL OPERATING CHARACTERISTICS
C   DIGITIZE OVER 128 ROWS X 64 COLUMNS
C   MATRIX = 1
C   ROWS = 128
C   COLS = 64
C   WORDS = COLS/2
C   ERASE FOR 10 X 10 TV FRAMES
C   ERASE = 10
C   WRITE OVER 2 TV FRAMES
C   WRITE = 2
C
C   RESET ELECTRONICS WITHIN THE IMAGE PROCESSING TERMINAL
C   BY SETTING AND THEN CLEARING THE 'MAINTENANCE' BIT
C   DRST = MAINT
C   DRST = 0
C
C   INITIATE 'ERASE'
C   SET THE WORD COUNT REGISTER TO -1
C   DRWC = -1
C   STORE NUMBER OF ERASE FRAMES X 10 IN IDATA(1)
C   IDATA(1) = ERASE
C   LOAD THE BUS ADDRESS REGISTER
C   DRBA = IBASE
C   SET FUNCTION 7 - 'ERASE'
C   FNCT = 7
```

```
C      INITIATE ERASURE OF THE STORAGE TUBE
C      DRST = XBA + (FNCT*2) + GO
C      INDICATE ERASE INITIATED
C      TYPE 1
C      WAIT FOR ERASURE (IDELAY MILLISECONDS)
C      IDELAY = ERASE*200
C      CALL WAIT(IDELAY,1)
C
C      TEST DEVICE STATUS DSTATC FOR ERASE COMPLETE
C      IF ERASE NOT COMPLETE AFTER 1000 LOOPS, EXIT
C      ITIME = 0
2      ITIME = ITIME + 1
C      IF(ITIME.EQ.1000) GOTO 70
C      IF(DRST.AND.DSTATC).EQ.DSTATC) GOTO 2
C
C      STORE A CONVENTIONAL TV IMAGE ON THE STORAGE
C      TUBE BY INITIATING A 'WRITE(TV)'
C      SET THE WORD COUNT REGISTER TO -1
C      DRWC = -1
C      STORE NUMBER OF WRITE FRAMES
C      IDATA(1) = WRITE
C      LOAD THE BUS ADDRESS REGISTER
C      DRBA = IBASE
C      SET FUNCTION 6 - 'WRITE(TV)'
C      FNCT = 6
C      INITIATE WRITE
C      DRST = XBA + (FNCT*2) + GO
C
C      INDICATE WRITE INITIATED
C      TYPE 3
C      WAIT FOR WRITE (IDELAY MILLISECONDS)
C      IDELAY = WRITE*20
C      CALL WAIT (IDELAY,1)
C
C      TEST DEVICE STATUS DSTATC FOR WRITE COMPLETE
C      ITIME = 0
4      ITIME = ITIME + 1
C      IF(ITIME.EQ.1000) GOTO 70
C      IF(DRST.AND.DSTATC).EQ.DSTATC) GOTO 4
C
C      INITIATE DIGITIZATION OVER SELECTED MATRIX COMBINATION
C      SET THE WORD COUNT REGISTER TO -1
C      DRWC = -1
C      STORE THE MATRIX COMBINATION
C      IDATA(1) = MATRIX
C      LOAD THE BUS ADDRESS REGISTER
C      DRBA = IBASE
C      SET FUNCTION 4 - 'INITIATE DIGITIZATION'
C      FNCT = 4
C      INITIATE DIGITIZATION
C      DRST = XBA + (FNCT*2) + GO
C      INDICATE DIGITIZATION INITIATED
C      TYPE 5
C
C      SET UP LOOP TO READ ALL ROWS
C
C      DO 90 IROW = 1,ROWS
```

```
C
C   TEST FOR RAM LOADED
C   ITIME = 0
6   ITIME = ITIME + 1
C   IF(ITIME.EQ.1000) GOTO 70
C   IF(DRST.AND.DSTATB).EQ.0) GOTO 6
C
C   READ DATA FROM RAM
C   LOAD WORD COUNT REGISTER WITH WORDS TRANSFERRED
C   DRWC = -WORDS
C   LOAD THE BUS ADDRESS REGISTER
C   DRBA = IBASE
C   SET FUNCTION 2 - 'READ FROM MEMORY'
C   FNCT = 2
C   LOAD WORDS STORED IN RAM INTO CENTRAL MEMORY
C   DRST = XBA + (FNCT*2) + GO
C   TRANSFER DATA FROM CENTRAL MEMORY TO DISK
C   WRITE(2'IROW) (IDATA(K),K=1,WORDS)
C
C   READ ROW NUMBER
C   DRWC = -1
C   DRBA = IBASE
C   SET FUNCTION 0 'READ ROW NUMBER'
C   FNCT = 0
C   DRST = XBA + (FNCT*2) + GO
C   MASK LEAST SIGNIFICANT 9 BITS OF ROW NUMBER
C   IDATA(1) = IDATA(1).AND."000777
C   INDICATE WHICH ROW IS DIGITIZED
90  TYPE 7,IDATA(1)
C
C   RESET THE ELECTRONICS WITHIN THE IMAGE PROCESSING TERMINAL
C   DRST = MAINT
C   DRST = 0
C
C   WAIT FOR 10 SECONDS
C   CALL WAIT(10,2)
C
C   INITIATE 'ERASE'
C   DRWC = -1
C   IDATA(1) = ERASE
C   DRBA = IBASE
C   FNCT = 7
C   DRST = XBA + (FNCT*2) + GO
C   TYPE 1
C
C   WAIT FOR 5 SECONDS
C   CALL WAIT (5,2)
C
C   INITIATE 'WRITE DIGITAL' OVER SELECTED MATRIX COMBINATION
C   SET THE WORD COUNT REGISTER
C   DRWC = -1
C   STORE THE MATRIX COMBINATION
C   IDATA(1) = MATRIX
C   LOAD THE BUS ADDRESS REGISTER
C   DRBA = IBASE
C   SET FUNCTION 5 - 'WRITE DIGITAL'
C   FNCT = 5
```

```
C      INITIATE 'WRITE DIGITAL'
      DRST = XBA + (FNCT*2) + GO
C      INDICATE 'WRITE DIGITAL' INITIATED
      TYPE 8
C
C      SET UP ROW COUNTER
      DO 60 IROW = 1,ROWS
C
C      RECOVER ROW OF DATA FROM DISK
      READ (2'IROW) (IDATA(K),K=1,WORDS)
C
C      TEST FOR RAM AVAILABLE
      ITIME = 0
30     ITIME = ITIME + 1
      IF(ITIME.EQ.1000) GOTO 70
      IF((DRST.AND.DSTATA).EQ.0) GOTO 30
C
C      WRITE ROW NUMBER
      DRWC = -1
      DRBA = IBASE
      FNCT =1
C      NORMALIZE ROW NUMBER TO 1 IN 512 ROWS
      IDATA(1) = (512/ROWS)*IROW
      DRST = XBA + (FNCT*2) + GO
C
C      TRANSFER ROW OF DATA TO RAM
      DRWC = -WORDS
      DRBA = IBASE
      FNCT = 3
      DRST = XBA + (FNCT*2) + GO
60     CONTINUE
      GOTO 80
C
C      INDICATE TEST OF DEVICE STATUS FAILED
70     TYPE 10
C      RESET ELECTRONICS WITHIN THE IMAGE PROCESSING TERMINAL
80     DRST = MAINT
      DRST = 0
C
C      CLOSE THE DISK FILE
      CLOSE(UNIT=2,DISP='DELETE')
C
C      FORMAT STATEMENTS
1      FORMAT(' ERASE INITIATED')
3      FORMAT(' WRITE INITIATED')
5      FORMAT(' DIGITIZATION INITIATED')
7      FORMAT(' ROW',I5,'DIGITZED')
8      FORMAT(' WRITE DIGITAL INITIATED')
10     FORMAT(' DEVICE STATUS NOT OPERATING')
C
      END
```

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