

Monolithic Photonic Integrated Circuit Based on Silicon Nitride and Lithium Niobate on Insulator Hybrid Platform

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Lithium niobate on insulator (LNOI) has been demonstrated as a promising platform for photonic integrated circuits (PICs), thanks to its excellent properties such as strong electro-optic effect, low material loss, and wide transparency window. Herein, a monolithic PIC for high-speed data communication application on a lithium-niobate-etchless platform with silicon nitride (Si_3N_4) as a loading material is proposed and demonstrated. The fabricated PIC consists of four racetrack resonator modulators and a pair of four-channel mode (de)multiplexers, which shows high data modulation rate of 70 Gbps for single channel and the total data throughput reaches up to 280 Gbps. To the best of knowledge, this is the first demonstration of PIC consisting of high-speed electro-optical modulators and (de)multiplexers with such high data capacity on Si_3N_4 -LNOI hybrid platform, which opens up new avenues for achieving large-scale monolithic integration on LNOI platform in future.

1. Introduction

Photonic integrated circuits (PICs) play a key role in optical interconnections, optical computing, and optical neural networks due to their high speed and large capacity.^[1,2] Lithium niobate on insulator (LNOI) has been demonstrated as one of the most promising platforms for PICs due to its inherent advantages, such as strong Pockels effect ($r_{33} = 33 \text{ pm V}^{-1}$), large optical nonlinear coefficients ($d_{33} = 27 \text{ pm V}^{-1}$), and wide transparency window ($0.35 \sim 5 \mu\text{m}$).^[3-5] However, lithium niobate has stable chemical properties, and common chemical etching methods are ineffective in forming low-loss waveguides.^[5] In recent years, the physical dry etching with Ar^+ milling has been verified

as an effective method for directly etching lithium niobate to realize integrated photonic devices on the LNOI platform.^[6] Various high-performance integrated photonic devices such as modulators,^[7-9] optical frequency combs,^[10,11] and wavelength converters^[12,13] have been demonstrated experimentally. Except for direct etching on the LNOI platform, the hybrid platform with a readily etched loading material on the top of the LNOI chip is another good choice for realizing large-scale PICs, where one can fabricate hybrid waveguides on the LNOI platform conveniently without etching the lithium niobate thin film.^[6,14]


Compared with other loading materials such as silicon,^[15,16] tantalum pentoxide,^[17] polymer,^[18] silicon nitride (Si_3N_4) is one of the most promising loading materials for the hybrid LNOI platform.^[19-24] First, the fabrication processes for silicon nitride material are commercially available, which means it is convenient to realize large-scale PICs with good scalability on the Si_3N_4 -LNOI hybrid platform. Secondly, Si_3N_4 has a slightly lower refractive index than lithium niobate,^[25] and thus the optical mode in hybrid waveguides can be mostly confined in the lithium niobate layer to take full advantage of its excellent material properties. At last, Si_3N_4 has low material loss and an optical transparency window similar to that of lithium niobate,^[25] which also means the performance of PICs based on such a hybrid platform will not suffer significant degradation caused by the introduction of loading material. Currently, various active and passive devices have been proposed and demonstrated on the Si_3N_4 -LNOI hybrid platform.^[19-30]

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As a proof of concept, a monolithic PIC is proposed and demonstrated for on-chip data communication application based on the Si₃N₄-LNOI hybrid platform, which consists of four racetrack-resonator modulators (RRMs) and a pair of four-channel mode (de)multiplexers (MMUXs). The fabricated PIC shows excellent performance with a single-channel data communication rate of 70 Gbps, and the total data capacity can reach up to 280 Gbps. To the best of our knowledge, this is the first demonstration of a monolithic PIC on the Si₃N₄-LNOI hybrid platform with such high data capacity. The proposed PIC has excellent potential for the applications of high-speed and large-capacity on-chip optical interconnection in the future.

2. Principle and Design

2.1. General Architecture

Figure 1a shows the 3D schematic diagram of the proposed PIC consisting of four RRMs and a pair of MMUXs on an X-cut Si₃N₄-LNOI hybrid platform. The principle of the PIC is described as follows. The four light beams at the resonances of four racetrack-resonators are coupled from single-mode fibers to the chip by means of grating couplers, and then modulated by the corresponding RRMs respectively. The modulated optical signals are transferred to different mode channels in the multimode bus waveguide by the MMUX. After transmitting a distance, the signals carried on different modes are demultiplexed to different output ports and coupled out of the chip via grating couplers and single-mode fibers for characterizing the performances of the proposed PIC.

Here, the Si₃N₄-LNOI hybrid platform is formed by the silicon substrate, the buried oxide layer, the lithium niobate thin film, and the Si₃N₄ loading layer. The thicknesses of the buried oxide layer, the lithium niobate thin film, and the Si₃N₄ loading layer are chosen as 4.7 μm, 300, and 300 nm respectively, following our previous work.^[29] The proposed PIC is designed along the crystallographic Z direction, for full use of the strongest electro-optic coefficient of lithium niobate. By using the finite element method (FEM),^[31] the simulated mode profile in the hybrid waveguide with a Si₃N₄ width of 1 μm is shown in

Figure 1b. The anisotropy of lithium niobate has been considered carefully in our simulation, with an extraordinary refractive index (n_e) of ~2.14 for the crystallographic Z direction and an ordinary refractive index (n_o) of ~2.21 for the crystallographic X/Y directions, at the wavelength of 1550 nm. As aforementioned, the Si₃N₄ has a slightly lower refractive index (~1.99) when compared with lithium niobate. Hence, it can be seen that the optical mode is mostly confined in the lithium niobate thin film, which is vital for electro-optical modulation.

2.2. Design and Static Performance of RRM

RRM is one of the key building blocks of the proposed PIC, which determines the data communication rate of each channel. Figure 2a shows the 3D schematic diagram with a cross-sectional view of the proposed RRM. The widths of the racetrack resonator waveguides are chosen to be $w = 1 \mu\text{m}$, which have been demonstrated to be under the single-mode condition for quasi-transverse electric (TE) modes.^[22] The coupling gap between the straight waveguide and racetrack waveguide is designed as $g = 750 \text{ nm}$ to satisfy the critical coupling condition for obtaining a relatively high extinction ratio.^[32] It can be seen that the racetrack waveguide consists of two long straight tracks connected by bending waveguides. The straight track length is designed as $L = 1.5 \text{ mm}$, and the radius of the bending waveguides is chosen to be $r_1 = 300 \mu\text{m}$. To realize high-efficiency electro-optical modulation, travelling-wave electrodes in the form of ground-signal-ground (G-S-G) are designed along one of the two straight long tracks. The electrode metal is selected to be gold with a thickness of $d = 500 \text{ nm}$. Figure 2b shows the simulated impedance of the electrodes as a 2D function of the width of the signal electrode (w_s) and the gap between signal and ground electrodes (g_1), by using a FEM eigenmode solver.^[33] The impedance of the electrodes is designed to be 50Ω for the impedance matching, as indicated by the solid black line in Figure 2b. In contrast, the optical loss induced by the electrodes and the index matching between the RF signal and optical signal should also be considered carefully. Thus, the width of the signal electrode is designed to be $w_s = 23 \mu\text{m}$, and the gap between signal and ground electrodes is designed to be $g_1 = 5.8 \mu\text{m}$. According to our calculation,

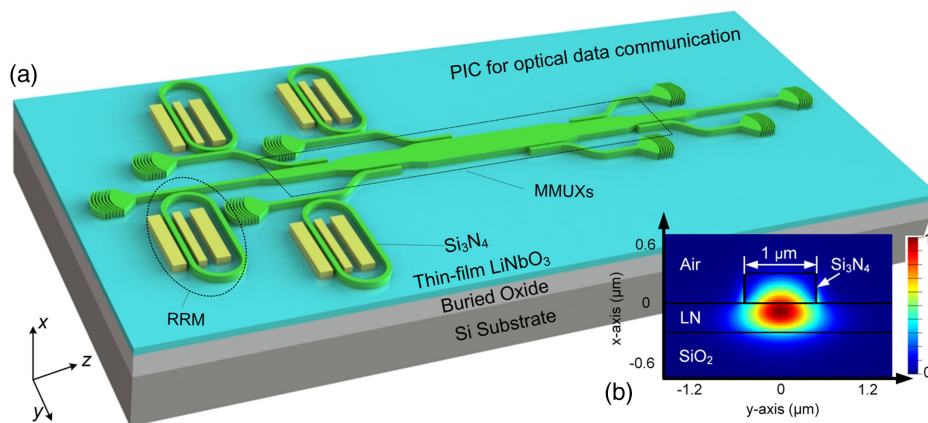


Figure 1. a) The 3D schematic diagram of the proposed photonic integrated circuit (PIC) for high-speed data communication. b) The simulated mode profile in the hybrid waveguide with a Si₃N₄ width of 1 μm.

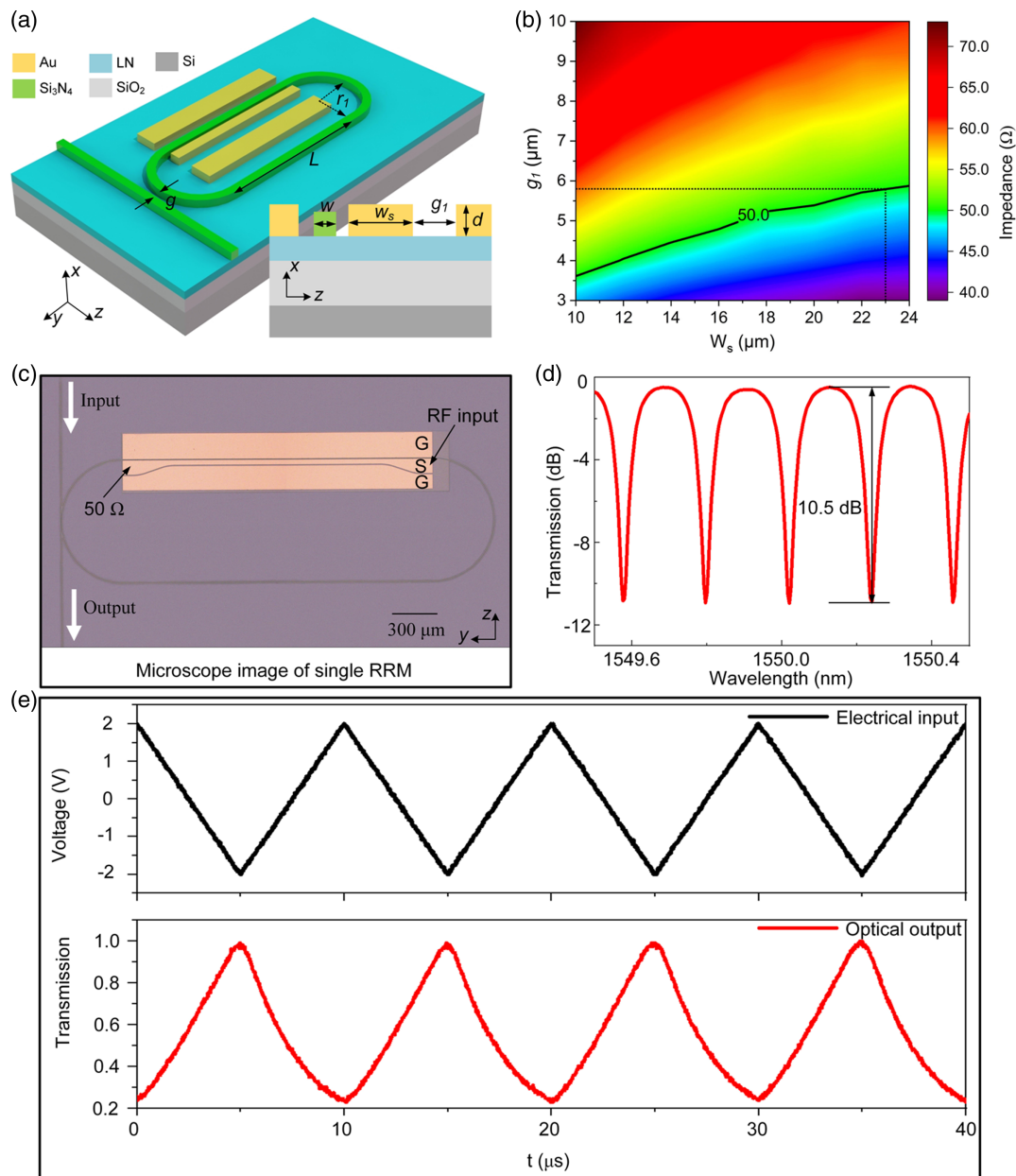


Figure 2. a) The 3D schematic diagram of the proposed racetrack-resonator modulator (RRM). b) Simulated impedance of the electrodes as a 2D function of the width of the signal electrode (w_s) and the gap between signal and ground electrodes (g_1). c) Microscope image of the fabricated RRM. d) Measured transmission spectrum of the fabricated RRM. e) Measured optical response of the fabricated RRM to the applied voltages.

the group index of TE_0 mode in the optical waveguide and the effective index of RF signal are both around 2.3.

Figure 2c shows the microscope image of the fabricated single RRM with the measured transmission spectrum shown in Figure 2d. In the experiment, the light is transmitted by an amplified spontaneous emission source, which is coupled in and out of the chip by using a pair of standard single-mode fibers. The output light is directed to an optical spectrum analyzer for transmission spectra plotting. The coupling angle of the fibers is $\approx 10^\circ$, and the transmission spectrum of the device is normalized by that of a straight waveguide fabricated closely on the same

chip. The measured optical insertion loss and extinction ratio are about 0.5 and 10.5 dB, respectively. To characterize the static EO performance of the RRM, a 100 kHz triangular voltage sweep is applied to the electrodes by using an RF probe, with the peak voltages of ± 2 V due to the limitation of our equipment. At the other end, the electrodes are terminated by a 50Ω load applied to another RF probe for impedance matching. The input wavelength is fixed at around 1550 nm. The measured optical response of the fabricated RRM is shown in Figure 2e. Up to $\sim 80\%$ difference is observed for the optical power when the induced phase shift changes from the most positive to the most

negative. We can obtain a higher excitation ratio of the fabricated RRM by increasing the applied voltage amplitude in the future.

2.3. Design and Static Performance of MMUX

MMUX is the other critical component of the proposed PIC, which should be designed carefully to reduce insertion loss and inter-modal crosstalk. In this work, we chose asymmetric directional couplers (ADCs) to realize MMUXs, as shown in **Figure 3a**, and its detailed principle can be found in our previous work.^[22]

Here, the width of the single-mode waveguide is decreased to be $w_0 = 0.8 \mu\text{m}$ to further reduce the inter-modal crosstalk. To satisfy the phase-matching condition,^[34] the widths of the multimode waveguides supporting TE_1 , TE_2 , and TE_3 modes are designed to be $w_1 = 2.164 \mu\text{m}$, $w_2 = 3.537 \mu\text{m}$, and $w_3 = 4.903 \mu\text{m}$, respectively. All of the coupling gaps in the ADCs are designed to be $g_2 = 0.3 \mu\text{m}$, considering our fabrication limitation. The radius of the bending waveguides is designed to be $r_2 = 150 \mu\text{m}$ to reduce transmission loss. After that, the coupling lengths are optimized by using the finite-difference time-domain (FDTD) method to achieve the highest mode coupling efficiency,^[35] which are designed to be $L_1 = 4 \mu\text{m}$, $L_2 = 12 \mu\text{m}$, and $L_3 = 18 \mu\text{m}$ for TE_1 , TE_2 , and TE_3 modes, respectively. The simulated transmission

spectra of TE_0 -to- TE_1 , TE_0 -to- TE_2 , and TE_0 -to- TE_3 mode conversions in the ADCs are shown in **Figure 3b–d**. The simulated mode conversion efficiencies are larger than -0.53 , -0.61 , and -0.62 dB, while inter-modal crosstalk is below -28.9 , -22.1 , and -17.9 dB for TE_1 , TE_2 , and TE_3 modes, respectively, at a wavelength range of 1525–1565 nm.

Similarly, we fabricated the MMUXs with the designed parameters on the same chip, with the microscope image shown in **Figure 4a**. The input and output ports for $\text{TE}_0 \sim \text{TE}_3$ modes are indicated as $I_0 \sim I_3$ and $O_0 \sim O_3$, respectively. **Figure 4b–d** shows the measured transmission spectra of the fabricated device. The transmission spectra of the device are also normalized by that of a reference straight waveguide fabricated closely on the same chip. It can be seen that the experimental results match the simulations well. The measured insertion loss and inter-modal crosstalk for all mode channels is lower than 1.83 and -15.3 dB, respectively, at a wavelength range of 1525–1565 nm.

3. High-Speed Data Communication

The microscope image of fabricated PIC is shown in **Figure 5a**, with the close-up images of the coupling region of RRM, the

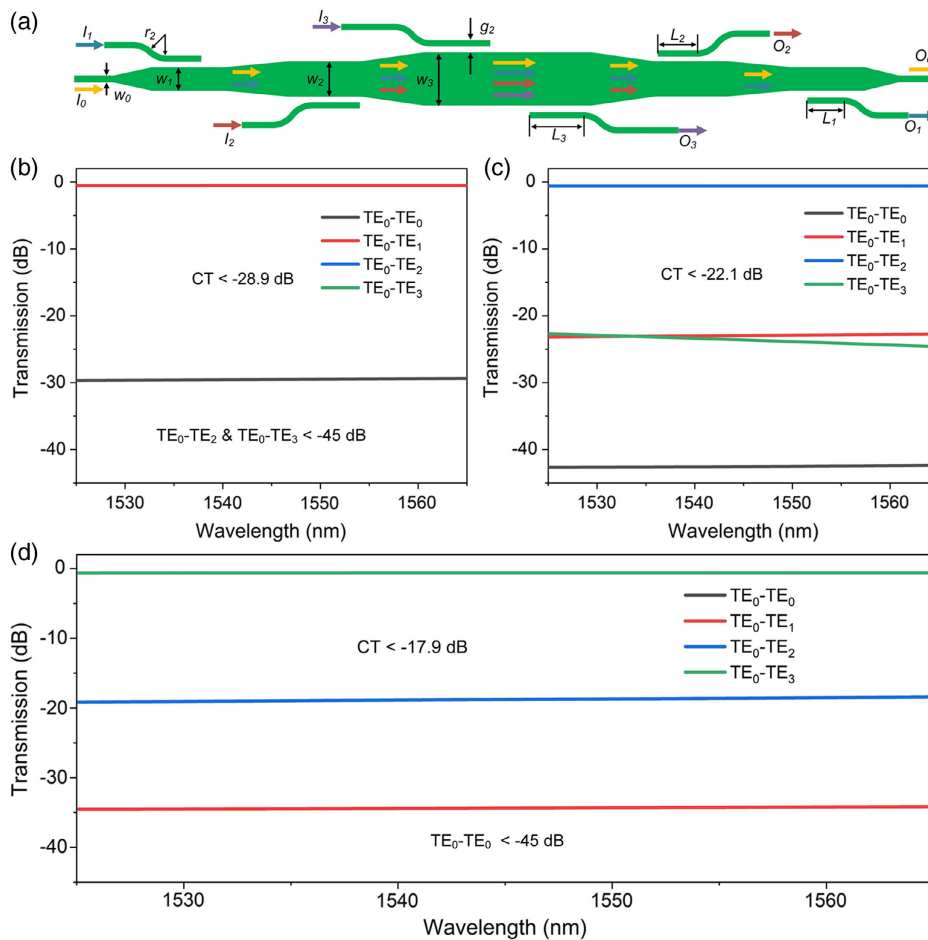


Figure 3. a) Schematic image of the four-channel mode (de)multiplexer (MMUX). Simulated transmission spectra for b) TE_0 -to- TE_1 , c) TE_0 -to- TE_2 , and d) TE_0 -to- TE_3 mode conversions in the ADC-based mode converters, respectively.

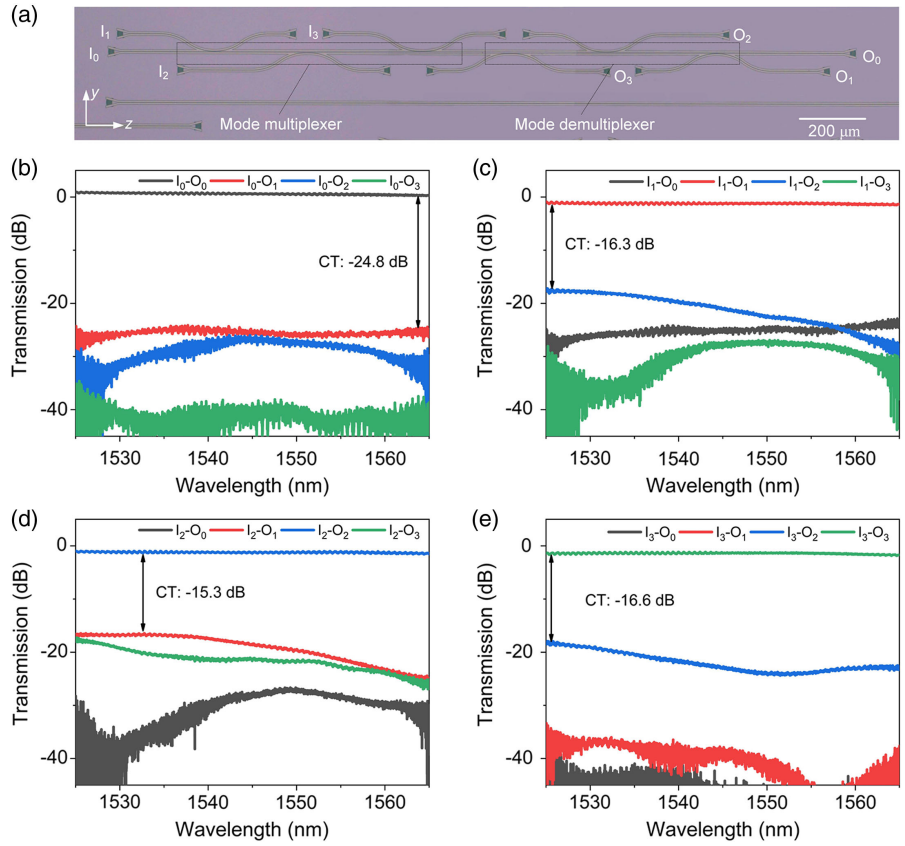


Figure 4. a) Microscope image of the fabricated MMUX. b–e) Measured transmission spectra from input ports I_0 – I_3 to different output ports.

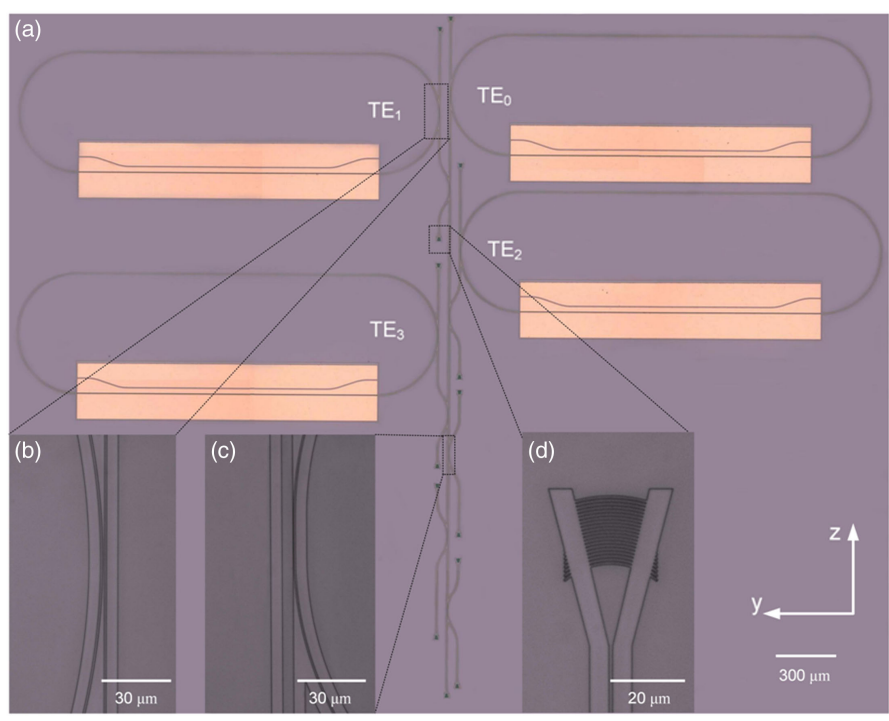


Figure 5. a) Optical microscope image of the fabricated PIC. b–d) Close-up images of the coupling region of RRM, the coupling region of ADC-based mode converter, and the grating coupler, respectively.

coupling region of ADC-based mode converter, and the grating coupler shown in Figure 5b–d, respectively. The experimental setup for the demonstration of on-chip high-speed data communication is shown in **Figure 6a**. The light input to the chip is first modulated by RRM with PRBS $2^{10}-1$ on-off key (OOK) electrical signals, then coupled to the corresponding mode channels, and finally demultiplexed from the bus waveguide to different output ports for dynamic measurements (see Experimental Section). The measured eye diagrams of different modulated data rates for TE₀–TE₃ mode channels are shown in Figure 6b. The measured single-channel data modulation rate can reach up to 70 Gbps, which is temporarily limited by the output voltage attenuation of our arbitrary waveform generator (AWG) with the increase in data rate. We believe the data modulation rate can be further increased with the improvement of our equipment in the near future. For 56, 64 and 70 Gbps modulated data rates, the measured extinction ratio of the eye diagrams for four-mode channels are 3.62, 2.90, and 2.04 dB, respectively. In addition, we also measured the bit-error rates (BERs) of TE₀–TE₃ mode channels with a data modulation rate of 56 Gbps, as shown in Figure 6c. It can be seen that the BERs decrease with the increased received power. To our knowledge, the measured BERs are lower than the limit of soft-decision forward error correction (SD-FEC) of 4×10^{-2} .^[8]

4. Discussion

In this work, we have successfully verified the high-speed data communication of fabricated PIC. The modulated data rate of the single RRM reaches up to 70 Gbps, and the total data throughput reaches 280 Gbps. The maximum modulation rate of our racetrack modulator and the ER of eye diagrams are curbed by equipment since the voltage applied to the chip has obvious attenuation. In **Table 1**, we compare the reported micro-ring resonator modulators, racetrack resonator modulators, and the same type of PICs on the LNOI platform. It can be seen that the modulator in the fabricated PIC has the highest

Table 1. Comparison of reported similar devices on the LNOI platform.

Platform	Channel number	ER [dB]	On chip data modulation rate	Total rate
Si-LN ^[15]	1	~11	9 Gbps	9 Gbps
LN ^[39]	1	~7	40 Gbps	40 Gbps
Si ₃ N ₄ -LN ^[40]	1	>30	NA	NA
Polymer-LN ^[18]	4	NA	100 Mbps	400 Mbps
This work	4	~9	70 Gbps	280 Gbps

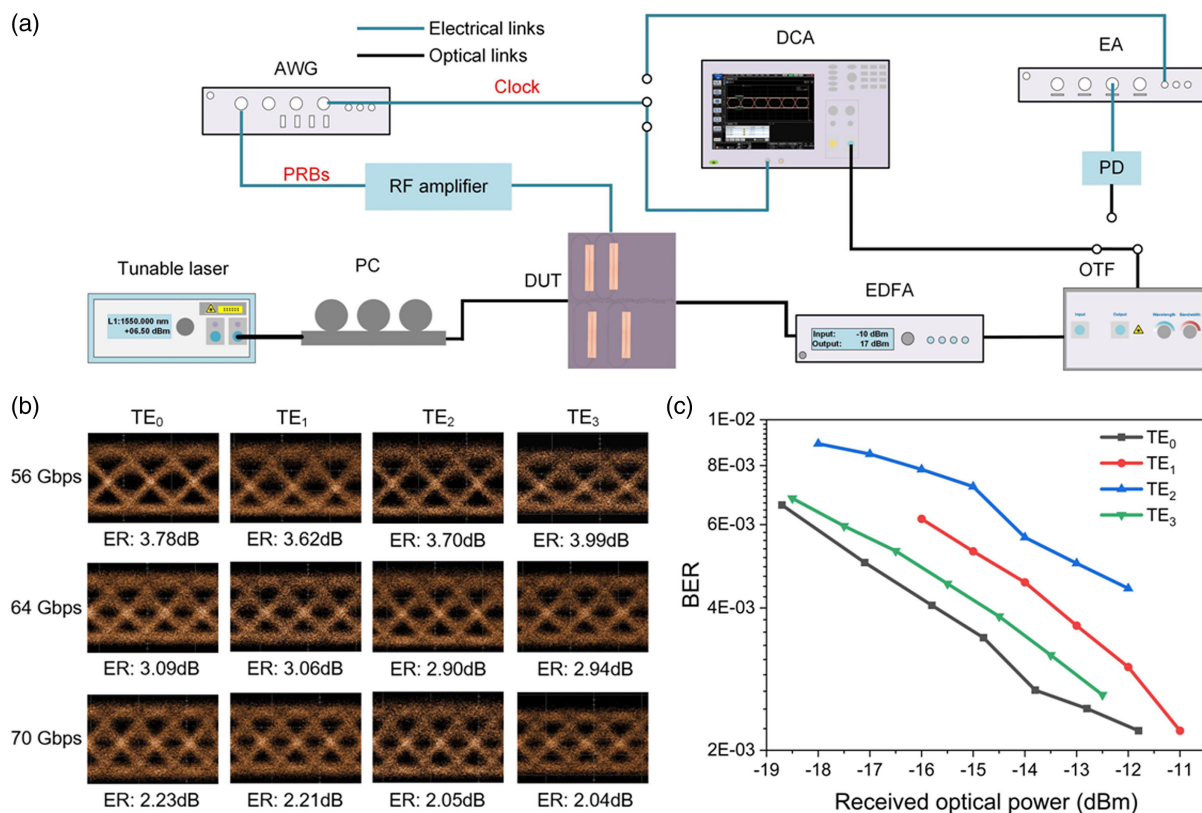


Figure 6. a) Experimental setup for demonstration of high-speed data communication based on the fabricated PIC. PC: polarization controller; DUT: device under test; EDFA: erbium-doped fiber amplifier; OTF: optical tunable filter; AWG: arbitrary waveform generator; DCA: digital-communication analyzer; EA: error analyzer; PD: photodetector. PRBS: pseudo-random bit sequence. b) Measured eye diagrams for TE₀–TE₃ mode channels with different modulation rates (the input light wavelengths are around 1550 nm). c) Measured BERs for TE₀–TE₃ mode channels with a data modulation rate of 56 Gbps.

modulated data rate compared with the reported same type of modulators on the LNOI platform. Although, the single MZI modulator based on LNOI can support very high data rates.^[7,8] However, with the continuous growth of data capacity, the performance of a single MZI modulator will be difficult to meet the application demands. Thus, combining modulators with MDM technology is a promising scheme to meet the challenges for future data capacity growth.

5. Conclusion

In summary, we propose, design, and demonstrate a PIC consisting of RRM and MMUXs for on-chip data communication based on the Si₃N₄-LNOI hybrid platform. The static and dynamic measurements are carried out successfully. For high-efficiency electro-optical modulation, the G-S-G traveling-wave electrodes are designed and fabricated for the RRM, leading to an excellent static EO performance. The MMUX has been further optimized based on our previous work,^[22] with low insertion losses below 1.83 dB and low inter-modal crosstalk below -15.3 dB over the whole C band. By combining the modulators with the MMUXs, the application for on-chip high-speed data communication with the 280 Gbps total data throughput has been verified. The communication capacity of our proposed PIC can be further improved greatly by combining other multiplexing technologies such as wavelength-division multiplexing and polarization-division multiplexing.^[36,37] This work is expected to serve as guidelines for fabricating large-scale PICs for data communication applications based on the LNOI platform.

6. Experimental Section

Fabrication: The x-cut LNOI wafer with a thickness of 300 nm is provided by "NanoLN," and then a 300 nm-thick Si₃N₄ thin film is deposited on the top of the LNOI wafer by using the reactive sputtering process, in accordance with our previous work.^[38] After that, the waveguides are patterned and etched by using electron beam lithography (EBL) and inductively coupled plasma (ICP) processes, respectively. The grating couplers are formed during the same (single) process that is used for the fabrication of the waveguides, with a grating period of 910 nm and a filling factor of 0.4. The detailed principle and performance of the grating couplers can be found in our previous work.^[26] Finally, the gold electrodes with a thickness of 500 nm are deposited and formed by using e-beam evaporation deposition, laser direct writing, and lift-off processes.

Dynamic Measurement: The light generated by a tunable laser source (EXFO FLS-2800) passes through the polarization controller (PC, Thorlabs-FPC561) for reducing the fiber-to-chip coupling loss. At the other end of the chip, the modulated optical signals are amplified by an erbium-doped fiber amplifier (EDFA, Keopsys CEFA). The undesired wavelengths are filtered out by the following optical tunable filter (OTF, Santec OTF-350). Finally, the optical signals are directed to the digital-communication analyzer (DCA, Keysight DCA-X-86100D) and error analyzer (EA, SHF 1104 A) for eye diagrams and BERs observation, respectively. For the electrical signal, the PRBS 2¹⁰⁻¹ OOK signal is generated by AWG (Keysight M8196A) and amplified by the RF amplifier (SHF S807C). An RF probe (GGB, 67 GHz) is used to apply the RF signal to the chip, and another probe (GGB, 67 GHz) with 50 Ω terminations is applied to the other end of the electrode for impedance matching. For 56, 64, and 70 Gbps modulated data rates, the calculated energy consumptions of the fabricated RRM are 789, 391, and 212 fJ bit⁻¹ respectively.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

lithium niobate on insulator (LNOI), mode-division multiplexing (MDM), racetrack ring modulator, silicon nitride

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