An Experimental System for Evaluating Cache Coherence Protocols in Shared Memory Multiprocessors

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Abstract

This thesis examines cache coherence protocols designed for use in bus connected shared memory multiprocessors. The cache coherency problem is discussed, and several previously published protocols are described in a new uniform framework, allowing ready comparison between them to be made. The issue of protocol correctness is also addressed. The protocol mechanisms proposed for the IEEEE P896.2 Futurebus are described, and the way they may be used to implement the published protocols is illustrated. Two approaches for verifying correctness of the Futurebus mechanisms are described. A brief survey of techniques for evaluating relative performance of cache coherence protocols is presented, covering three main techniques: analytical, simulation based, and measurement of real systems. It is argued that the last of these is the most accurate, and that the results of such measurements are needed to validate evaluations based on the other two techniques. A brief description is presented of an early prototype multiprocessor, the Leopard-1, and a detailed description is presented of a full-scale multiprocessor system, Leopard-2. The Leopard-2 is an experimental platform which includes programmable cache controllers, designed to allow performance measurements of cache coherence protocols. Attention is focussed on the design of the cache attached to each processor, and the way in which the coherence protocols are implemented is described. A detailed behavioural model of the programmable cache controller is presented. The model is driven by two workloads: a synthetic workload to exercise specific aspects of system behaviour, and a pseudo-random workload to provide comprehensive test coverage. The model is used to verify correct maintenance of coherence by the caches operating under different coherence protocols. The thesis concludes with

a discussion of ways in which the experimental platform is used to measure relative performance of coherence protocols.