Fast Asynchronous VLSI Circuit Design Techniques and their Application to Microprocessor Design

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Addenda

Section 2.2 - Asynchronous hardware

This thesis is focussed on practical asynchronous circuit design with an emphasis on microprocessors, and therefore only those processors which have been designed to fabrication have been included in the literature discussion. Fabricated test structures and coded microprocessors do not provide enough reliable data to justify their discussion in this context, although in Section 8.1 a description of coded superscalar processors, as compared to the author's, is given.

Section 2.2.2 - AMULET I and II

The AMULET I design was the first generation attempt at implementing a sixth generation commercial ARM6 processor, and was built with significantly less man-power and resources. This makes comparisons between them difficult, and the performance gap of 50% should be treated cautiously. The subsequent AMULET II processor has since demonstrated improved performance over the ARM6.

Section 3.5 - The ECS representation

The ECS representation is intended to enable asynchronous circuits to be specified in a clear and concise format which models the interaction of data and control wires. It is not intended as a formal tool for synthesis, and as such has not been developed using formal methods. Instead, an intuitive description of the representation has been presented based on the practical implementation of asynchronous circuits, as this is the major focus of the thesis.

Section 4.1 - Algebraic improvements of a TS

The simplifications described in this section are synonymous with those of boolean logic.

Section 5.3.1 - Dynamic logic

The nature of the data stream will also impact the power dissipation of a dynamic versus a static gate.

Section 5.3.3.2 - Self-timed pseudo-nmos logic

This circuit has a fast completion detection time compared to the static logic tree, as evidenced in Table 6.8. Compared to a typical dynamic gate however, it will be slow.

Chapter 6 - Self-timed Architectures

The pseudo self-timed architectures presented in this chapter do not require additional safety margins. The computation and completion paths are closely matched in layout, and an implicit margin is already included in the handshaking overhead to compensate for any variations.

Contents

Abstract

Over the past decade a variety of asynchronous synthesis techniques have been proposed. The majority of these have been concerned with generating provably correct circuits with high reliability, whereas others have focussed on producing circuits with low power dissipation. However in taking such approaches the resulting circuits are usually swamped with a large number of gates in the critical paths and are consequently inefficient in terms of speed.

This thesis describes a collection of novel design techniques engineered for high speed operation (such as fast pipeline control circuits and pseudo self-timed computations). In addition, a new gate representation is proposed to better reflect their functionality in an asynchronous domain. As an illustration of these design techniques two microprocessors have been implemented:

- *ECSTAC* is styled as a linear pipeline with a load/store architecture and an 8 bit data path and a 24 bit address path. It employs fast pipeline control circuits and utilizes some interesting asynchronous techniques for bypassing stages, controlling data hazards, and register fetching. *ECSTAC* has been fabricated using ES2's 0.7μm DLM CMOS process and demonstrated a peak operating speed of 28 Mips.

- *ECSCESS* is structured to take advantage of self-timed data dependent computations and to employ functional parallelism. It has a 32 bit data path and can provide for up to 32 single precision (16 double precision) functional units which interact directly with each other, thus enabling out-of-order execution and global results forwarding. Their operation is fully decoupled from branches and interrupts to minimize stalling. Emphasis has been placed on maintaining a high throughput to the functional units. It employs novel design techniques for rapid data hazard detection between units, PC updating, and decoupled branch evaluation and branch target determination. *ECSCESS* has been simulated in VHDL with delays comparable to those of the 0.7μm standard cell library used in *ECSTAC*, and demonstrated a peak operating speed of 181 Mips.