



Performance-Directed Design of Asynchronous VLSI Systems

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Abstract

Asynchronous system design has been subject to a resurgence of interest over the past decade due to the mounting problems with synchronous design approaches. Asynchronous systems eliminate or obviate many difficulties with large, complex VLSI systems encountered when using synchronous design techniques. Nevertheless, asynchronous design is still not widely accepted for a number of reasons, perhaps the most critical of which is the performance limitation imposed.

This thesis describes a new method for designing asynchronous systems that breaks with traditional techniques commonly believed to be essential. The method, called **Free-Flow Asynchronism (FeFA)** eliminates all unnecessary signalling to open the performance bottleneck, while still retaining many inherent advantages of both synchronous and asynchronous design approaches. The method is based around an existing engineered design approach for two-phase asynchronous systems, *Event Controlled Systems (ECS)*. ECS is shown to outperform existing asynchronous control methodologies by significant factors.

Powerful techniques are developed to compose complex systems, describe solutions to problems that occur in implementations, and give performance figures based on simulation. A method for utilising variable latency in FeFA pipelines to significantly improve average performance is developed.

The method is demonstrated through two applications. An channel signalling system, which can be used in FeFA or traditional asynchronous systems, is described. This application demonstrates the basic techniques of the FeFA approach and design trade-offs. Amedo, an asynchronous microprocessor based around the DLX architecture, is then described. This serves to illustrate some of the more advanced aspects of FeFA system design, as well as demonstrating the potential performance benefits.

Contents

Abstract	iii
List of Figures	ix
List of Tables	xv
List of Abbreviations	xvii
Declaration	xix
Acknowledgments	xxi
1 Introduction	1
1 Asynchronous Systems	1
2 Thesis Outline	5
3 Contribution and Concluding Remarks	8
2 Background	9
1 Asynchronous System Design	9
2 Related Work	25
3 Conclusion	27
3 The Event Controlled Systems Design Methodology	31
1 Two-Phase Design	32
2 Two-Phase Gates	37
3 A Complete Syntax	46
4 Conclusion	55
4 Pipelines	57
1 Pipeline Control	57
2 Pipeline Test	74

3	Conclusion	80
5	The ECSTAC Microprocessor	81
1	Architectural Overview	81
2	Processor Design	85
3	Device Test	108
4	Bottlenecks and Challenges	112
5	Conclusion	118
6	Free-Flow Asynchronous Systems	121
1	Free-Flow Concepts	122
2	Pipeline Design	126
3	Advanced Design Issues	146
4	Delay Design	158
5	System Test	169
6	Multi-rate pipelines	172
7	Conclusion	178
7	Free-Flow Communications	181
1	Asynchronous Channel Communication	181
2	Free-Flow Communication Architecture	184
3	Channel Control	186
4	Conclusion	195
8	Amedo — A Free-Flow Microprocessor	197
1	Base Architecture	198
2	Amedo Architecture	210
3	Amedo Performance	239
4	Conclusion	246
9	Conclusion	249
1	The Path Onwards	251
	Publications	255
A	Delay Design	257
1	Delay Performance and Self-Timed Units	257
2	Loading Effects	260

B Amedo ISA	263
1 Register Transfer Operation	263
C Gate Delay Data	267
Bibliography	269