Performance-Directed Design of Asynchronous VLSI Systems

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Abstract

Asynchronous system design has been subject to a resurgence of interest over the past decade due to the mounting problems with synchronous design approaches. Asynchronous systems eliminate or obviate many difficulties with large, complex VLSI systems encountered when using synchronous design techniques. Nevertheless, asynchronous design is still not widely accepted for a number of reasons, perhaps the most critical of which is the performance limitation imposed.

This thesis describes a new method for designing asynchronous systems that breaks with traditional techniques commonly believed to be essential. The method, called **Free-Flow Asynchronism** *(FeFA) eliminates all unnecessary signalling to open the performance bottleneck, while still retaining many inherent advantages of both synchronous and asynchronous design approaches. The method is based around an existing engineered design approach for two-phase asynchronous systems, Event Controlled Systems (ECS). ECS is shown to outperform existing asynchronous control methodologies by significant factors.*

Powerful techniques are developed to compose complex systems, describe solutions to problems that occur in implementations, and give performance figures based on simulation. A method for utilising variable latency in FeFA pipelines to significantly improve average performance is developed.

The method is demonstrated through two applications. An channel signalling system, which can be used in FeFA or traditional asynchronous systems, is described. This application demonstrates the basic techniques of the FeFA approach and design trade-offs. Amedo, an asynchronous microprocessor based around the DLX architecture, is then described. This serves to illustrate some of the more advanced aspects of FeFA system design, as well as demonstrating the potential performance benefits.

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