THE CIRRUS STORAGE SYSTEM

by

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I hereby state that this thesis contains no material which has been accepted for the award of any other degree or diploma in any University and to the best of my knowledge and belief, no material previously published or written by another person without due reference being made in the text of the thesis.

PREFACE

The design study leading to the CIRRUS computer was initiated during 1959 in an attempt to design a low cost computer providing, as far as possible, the power and flexibility normally associated with large and much more expensive machines. This work followed two separate but inter-related lines of development: the investigation of machine structures and programming systems, and hardware feasibility and evaluation studies. The results of these studies showed considerable promise in meeting this objective and during 1961, sufficient finance became available to commence construction of a machine. Construction and testing were largely completed by the end of 1962, although the machine did not become operational until late 1963, mainly due to delays in the delivery of the peripheral units.

The computer has a 36 bit word length and a repertoire of 200 orders, with arithmetic functions provided for 18 and 36 bit words in integral, fixed point and/or floating point form. Comprehensive indexing facilities are available and a powerful set of orders is provided for logical operations on whole or part words. Typical execution times, including order extraction, indexing and store accesses are: addition, 27 μsec (18 bit) and 210 μsec (36 bit fl. pt.) and multiplication, 110 μsec (18 bit) and 350 μsec (fl. pt) Extensive multi-programming facilities provide time-sharing of the computer during input and output and allow up to 7 programs to be held in the machine simultaneously. Each program has access to the machine via separate and independent operating consoles, each equipped with a basic set of peripherals. The normal input/output medium is paper tape but a full range of peripherals can be attached with a minimum of external buffering, this being provided partly by the general machine hardware and partly by the multi-programming system. Any of the peripherals may be allocated to a program if not committed to use with another. The basic machine with 4096 words of storage and a single operating console required

an expenditure of approx. £15,000 for components and a further £10,000 for labour.

During the period 1959-60, a small team from the University and the C.S.I.R.O. was assembled to carry the project through. Those involved were: M.W. Allen and G.A. Rose, faculty members of the Electrical Engineering Department; J.G. Sanderson, Maths Department; J.P. Penny and T. Pearcey, C.S.I.R.O.; and M.R.Haskard and I.R.Butcher, post-graduate students in the Electrical Engineering Department. With the exception of the last two, the personnel were only engaged on the project on a part-time basis. In many respects, the group worked as a team, but broadly the work was subdivided as follows: M.W. Allen, T.Pearcey and G.A.Rose, system design and logical design; J.G.Sanderson, general programming aspects; J.P.Penny, multi-programming system; and M.W.Allen, I.R.Butcher and M.R.Haskard, engineering design. The author was primarily responsible for the design and construction of the storage units, but was involved to a varying degree in most aspects of the engineering design.

The logical design of the machine requires four storage units: two coincident current core stores, the main store with a capacity of 16,384 19 bit words and the register store of 1,024 20 bit words and two fixed stores of a type developed by the author, one with a capacity of 4,096 38 bit words and the other of 8,192 19 bit words.

The two core stores use the same circuit techniques and both operate on a 6 μsec cycle. By current standards these are rather slow and do not in fact represent the maximum speed possible with the cores used, partly due to the need to fit in with the general machine timing and partly to the deliberate provision of substantial timing margins in the store cycle. Faster stores could have been built using either linear-

selection or coincident-current selection, but the available finance was limited and the speed and cost of the stores had to be compatible with the rest of the machine hardware. The objective in the design of the stores was a reliable low cost unit rather than high speed.

Both fixed stores had the same bit capacity and are identical mechanically, the different word capacities and word lengths being achieved by a minor change in the selection circuits. Two forms of fixed storage were developed, both using linear inductive coupling with the information represented by the manner in which the selection wires are threaded through the store. The Mkl form, using E-cores, was not particularly successful mechanically or electrically although it was completed and temporarily installed in the machine. This store did, however, provide a great deal of information on the behaviour of this type of unit which simplified the design of MK ll. using ferrite rods. Consequently, the Mkl store, although the less significant of the two is discussed first in the presentation of the thesis. Both stores were designed to operate on a 1.5 μsec cycle and the parameters of the system were chosen with this in mind. However, both would operate on a 1 μsec cycle and Mk ll would probably be capable of an 0.5 μsec cycle with suitable changes in the system parameters. The Mk ll fixed store has a 20:1 advantage over the core stores in cost/bit/μsec.

Both the core stores and the fixed stores were designed for a specific application rather than as a separate research venture, a fact which had a considerable influence on the design objectives and the techniques employed. The Mk ll fixed store in particular is capable of much better performance but circumstances unfortunately did not permit the full potential of this unit to be investigated. When the circuits were developed for the core stores and Mk 1 fixed store, transistors were relatively expensive and circuit techniques were aimed at minimising the

number required. The situation has now changed markedly and a different design approach would almost certainly be used if the work were to be repeated. The circuit techniques employed in Mk II fixed store reflect this attitude to a certain extent. Some restrictions were also placed on techniques by the desire to use components readily available locally and to use methods of production and assembly suited to the facilities at hand. The latter in particular eliminated printed circuit techniques and placed considerable restrictions on the design of the fixed stores.

The description of the store hardware is confined largely to that portion of the machine directly associated with the storage arrays, with only brief reference to the peripheral circuitry, static registers, power supplies, timing, etc. The treatment throughout the thesis is descriptive rather than mathematical, with a minimum of analysis, to keep the overall length to a reasonable limit.

A number of papers on the work contained in the thesis have been published or accepted for publication. Copies are not bound in with the thesis since the contents of the papers largely duplicate the appropriate section of the thesis. The papers are:

(a) "The CIRRUS Coincident-Current Core Store"
Accepted for publication in Electronic Engineering
(The main core store)

(b) "A Prewired Storage Unit"
Accepted for publication in IRETEC
(Mk II fixed store)

(c) "A Survey of High Speed Random Access Storage Techniques"
Presented at I.R.E. (Aust) Convention Melbourne 1963
(Appendix 3)

(d) "A Low Cost Driving System for a Coincident Current Core Store"

Presented at Australian Computer Conference Sydney 1961

(Appendix 2)

A fifth paper, "The Engineering Design of CIRRUS", co-authored with M.W. Allen, G.A. Rowe and M.R. Haskard is in preparation.

SUMMARY

The CIRRUS computer is a low cost machine of unusual power and flexibility. The main features of the machine design and hardware are described first to provide a background to the thesis. Four storage units are required: two coincident-current core stores, the main store of 16,384 19 bit words and the register store of 1024 20 bit words, and two fixed stores, the control fixed store of 4096 38 bit words and the machine language fixed store of 8192 19 bit words. The register store is only a reduced form of the main store and only the latter is discussed in detail. The drive system is based on the load-sharing switch and is temperature compensated to optimise operation over the range $10^{\circ}C$ - $45^{\circ}C$. The drive currents are controlled by transistors operating as non-saturating current switches. The store circuits are integrated into the overall machine hardware and do not require separate input, output or address registers. The stores are not fast, 6 μsec cycle, but are a low cost design conservative in both hardware ratings and timing. Another type of drive system using a new type of magnetic switch is also discussed in Appendix 2. Both fixed stores have the same bit capacity and are identical mechanically, the different word capacities and word lengths being achieved by a minor change in the addressing circuits. Two forms of fixed store developed by the author are described, both using a prewired inductively coupled array in which the information is stored by the mechanical arrangement of the selection wires within the array. The first using E cores was not particularly successful mechanically or electrically and was replaced by the second using ferrite rods. Both were designed to operate on a 1.5 μsec cycle but the second form is probably capable of an 0.5 μsec cycle with minor modifications. The stores are relatively cheap to construct and have a 20:1 speed/cost advantage over the core stores. A feature of the stores is the low drive

and large output in comparison with other types of fixed store described in the literature. Some other forms are discussed and briefly compared with the CIRRUS stores. The fixed store is then considered as a logical network and the application of this device to the design of complex switching networks is discussed. The control unit of the CIRRUS computer is taken as an example of this design approach. Finally some possible changes in the store circuits are considered in view of the improved and cheaper semiconductors now available and the possible future development of the storage system is discussed.

ACKNOWLEDGEMENTS

The author wishes to acknowledge the assistance and support of Professor E.O. Willoughby, of his colleagues in the project, particularly Dr. M.W. Allen, for discussions and criticism during the course of the project and of the workshop staff for their efforts in the construction of the equipment. The author is also indebted to the Postmaster General's Department for the opportunity to undertake this work and for assistance in the preparation of the thesis.

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SECTION A

THE CIRRUS COMPUTER.

(1) GENERAL DESCRIPTION

In recent years, considerable effort has been directed towards the development of faster and more powerful computers, both by increasing the internal speed of the computer and by providing more powerful order codes and operating facilities. The gains in speed have in most cases resulted in considerable increases in cost and hardware, although the cost per operation has fallen rapidly. The design study leading to the CIRRUS computer was directed towards a somewhat different objective, to derive the maximum possible computing power from a low cost machine.

The CIRRUS computer has a 36 bit word length and a repertoire of 200 orders with arithmetic functions provided for 18 and 36 bit words in integral, fixed point and/or floating point form. Comprehensive indexing facilities are available and a powerful set of orders is provided for logical operations on whole or part words. Typical execution times including order extraction, indexing and store accesses are : addition 27 μsec (18 bit) and 210 μsec (36 bit floating point) and multiplication 110 μsec (18 bit) and 350 μsec (fl. pt.). Extensive multi-programming facilities provide time-sharing of the computer during input and output and allow up to 7 programs to be held in the machine simultaneously. Each program has access to the machine via separate and independent operating consoles, each equipped with a basic set of peripherals. The normal machine input/output medium is paper tape, but a full range of peripherals can be attached with a minimum of external buffering, this being provided partly by the general machine hardware and partly by the multi-programming system. Any of the peripherals may be allocated to a program if not committed to use with another. The basic machine with 4096 words of storage and a single operating console required an expenditure of approximately £15,000 for components and a further £10,000 for labour.

At the hardware level, the main feature of the machine is the use of a control unit designed around a fixed store. The organisation of the control unit and the behaviour during the execution of the various machine functions is similar to that of an elementary computer. In the case of CIRRUS, this subcomputer is capable of executing 8 basic sub-orders. The machine order code and overall behaviour are defined by sub-programs held in the control fixed store.

The machine structure is shown in Fig. 1. The S register performs the combined functions of address register for the control fixed store and sequence counter for the sub-computer. The pattern set into the C register when the store is interrogated specifies both the information flow and the timing sequence to execute the sub-order and, directly or indirectly, the address to be set into S to extract the following sub-order. S is normally incremented after each sub-order is set into C, but the contents of the C register may indicate that S is to be conditionally or unconditionally set from another source, allowing jumps within or between the sub-programs held in the fixed store.

The rest of the machine consists basically of two independent core stores, and addition/logical network and a set of general purpose registers, time shared between a number of different functions during the various phases of the machine behaviour. The four main registers M, R, N and Z and the two stores are nominally of half-word length, the A register 6 bits and the E register 9 bits. Information processing within this hardware is half-word parallel, operations on longer word lengths being developed from a number of half-word operations. This procedure was adopted as a compromise between speed and cost.

The main function of the M and R registers is to provide temporary storage for the information read from the main and register stores respectively. N and A normally hold the required addresses

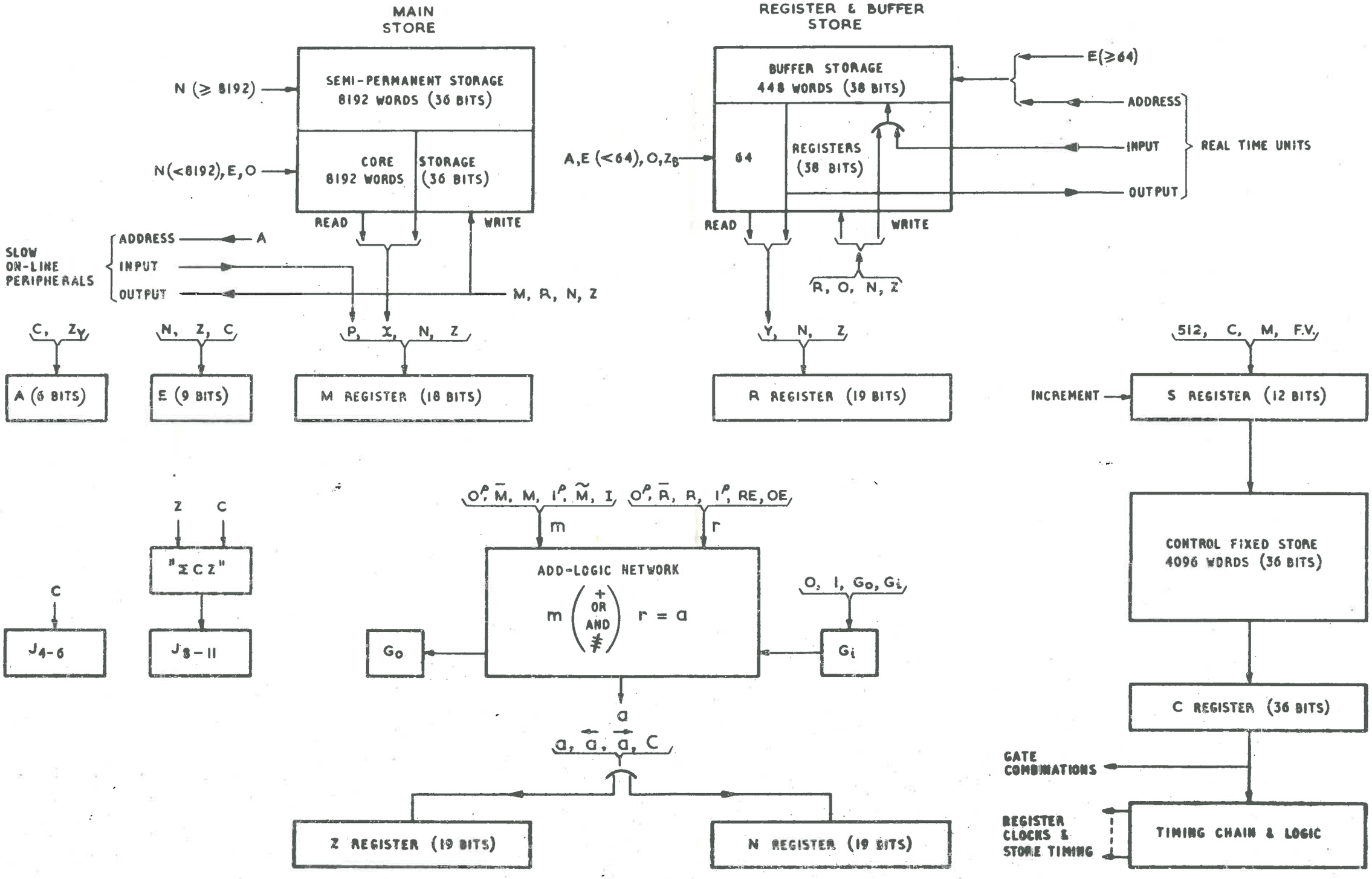


FIG. 1. CIRRUS STRUCTURE

and Z is most commonly used to buffer the output from the add/logical network, with, if required, a single place shift to left or right. The functions of sequence counter, index register and accumulator for each program are allocated to storage locations, the first in the main store and the other two in the register store. A total of 64 registers are provided in the register store, up to 32 of which can be allocated to a program. The address of the sequence counter for the current program is normally contained in the E register. The add/logical network is capable of addition and the logical operations of AND, OR, and NOT EQUIVALENT. By the appropriate choice of inputs and function, binary addition, subtraction or any of the 16 logical operations on two binary variables can be achieved.

The contents of the C register for each sub-order define a particular interconnection of these units via 1 of n gates as shown in Fig. 1. The gates deriving register inputs, store addresses and store inputs provide a 1 of 4 selection and those deriving the input to the add/logical network provide a 1 of 6 selection. For register manipulations not involving store access, the sub-order is executed in 1.5μsec, the cycle time of the fixed store. If access to either or both stores is required, this is increased to 6μsec. In the latter sub-order, the information is extracted from store, processed and returned to store within the sub-order.

Two data channels are provided for input and output. In both cases the peripherals are treated on an interrupt basis, with the computer controlling the data transfer. The first is for slow asynchronous units such as card and paper tape units, printers, plotters and the keyboard of the operating consoles. These units

can gain access to the machine at the end of each machine order via a system of indicators. A request for attention causes the current program to be suspended and control is transferred to the "director" sub-program which identifies the source of the interruption and selects a sub-program to control the information transfer to or from the peripheral unit. The director will then return control to the suspended program or will initiate a switch to another program if this is necessary. The second data channel allows for high speed synchronous peripherals such as magnetic tape or drums or a real time interrupt situation. Access is permitted at the end of each sub-order. All machine registers are held and the information is transferred to the section of the register store reserved for use as a buffer. At the completion of the transfer, the machine proceeds with the current program at least to the end of the interrupted order.

Parity checking is provided on all transfers to and from the logical unit involving either the stores or the peripherals and transfers within the logical unit and the control unit are checked, including the fixed store patterns and the incrementing of the S register. Failure of the parity check on any information within the machine will cause the machine to stop no later than the end of the current sub-order. No data from the peripherals is allowed into the machine unless the parity is correct.

This brief discussion of the machine structure and facilities is intended only to provide a background to sections B and C of the thesis, a description of the various storage units used. The structure and control unit are discussed in more detail in Section E and further information on other aspects of the computer can be found through section O of the bibliography.

The mechanical construction of the computer can be seen from the photographs of Fig. 2. The hardware is mounted in two frames approx. 6' high, 3'6" wide and 7" deep. These are hinged together and can be opened out for service. Each frame contains two sub-units, the control unit and register store in the fixed frame and the add/logical network, registers & main store in the movable frame. The physical arrangement of the machine hardware closely follows the layout of Fig. 1. An engineering test panel on the end of the fixed frame allows comprehensive testing of the machine hardware. The power regulators for the two lower units are mounted immediately beneath the units while the two stores each have their own set of regulators. A monitoring system detects incorrect voltages or excess load current, throwing the machine off if trouble develops. Switched marginal check facilities are provided on the sensitive voltages.

A packaged construction is used throughout the machine. Low level circuits are mounted in a polythene card enclosed by a stainless steel band with a 25 pin plug attached. The packages are approximately 6" x 2½" with the component leads cut to an overall length of 1". The packages then slide into a stainless steel framework screwed to an aluminium chassis. The high power circuits, store drivers and regulators, are mounted directly on sections of heat sink and treated as a plug-in assembly. Some typical packages are shown in Fig. 3.

Direct coupled diode-transistor logic is used with nominal voltages of -3.5 for '0' and O V for '1'. All circuits have been designed for 10% or 1 V. variation in power supplies, 10% resistor values and a realistic minimum β for each transistor type but 5% resistors were used and power supplies held to within 2.5%

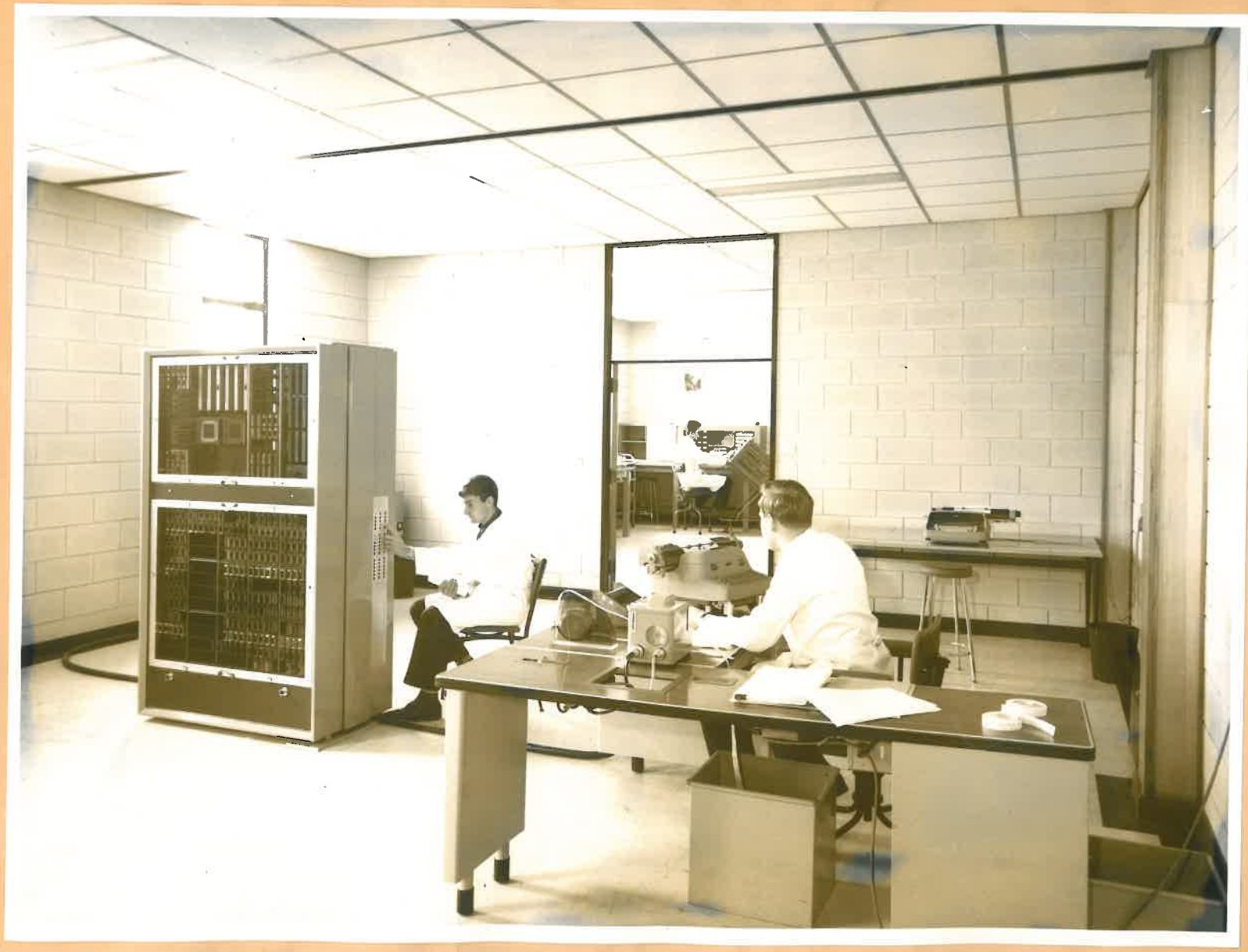


FIG. 2(a) OVERALL VIEW OF MACHINE

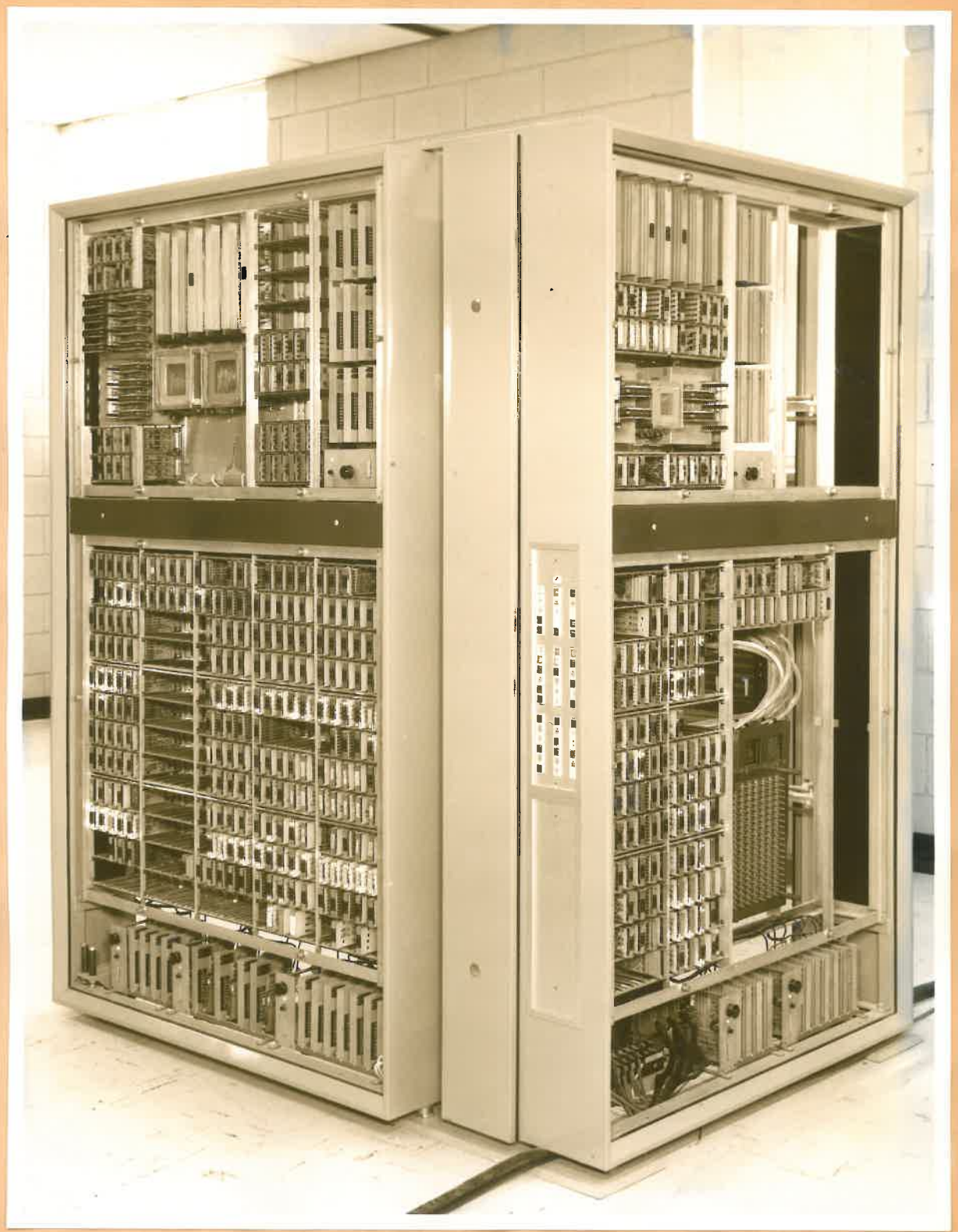


FIG. 2 (b). FRONT VIEW OF MAIN FRAME

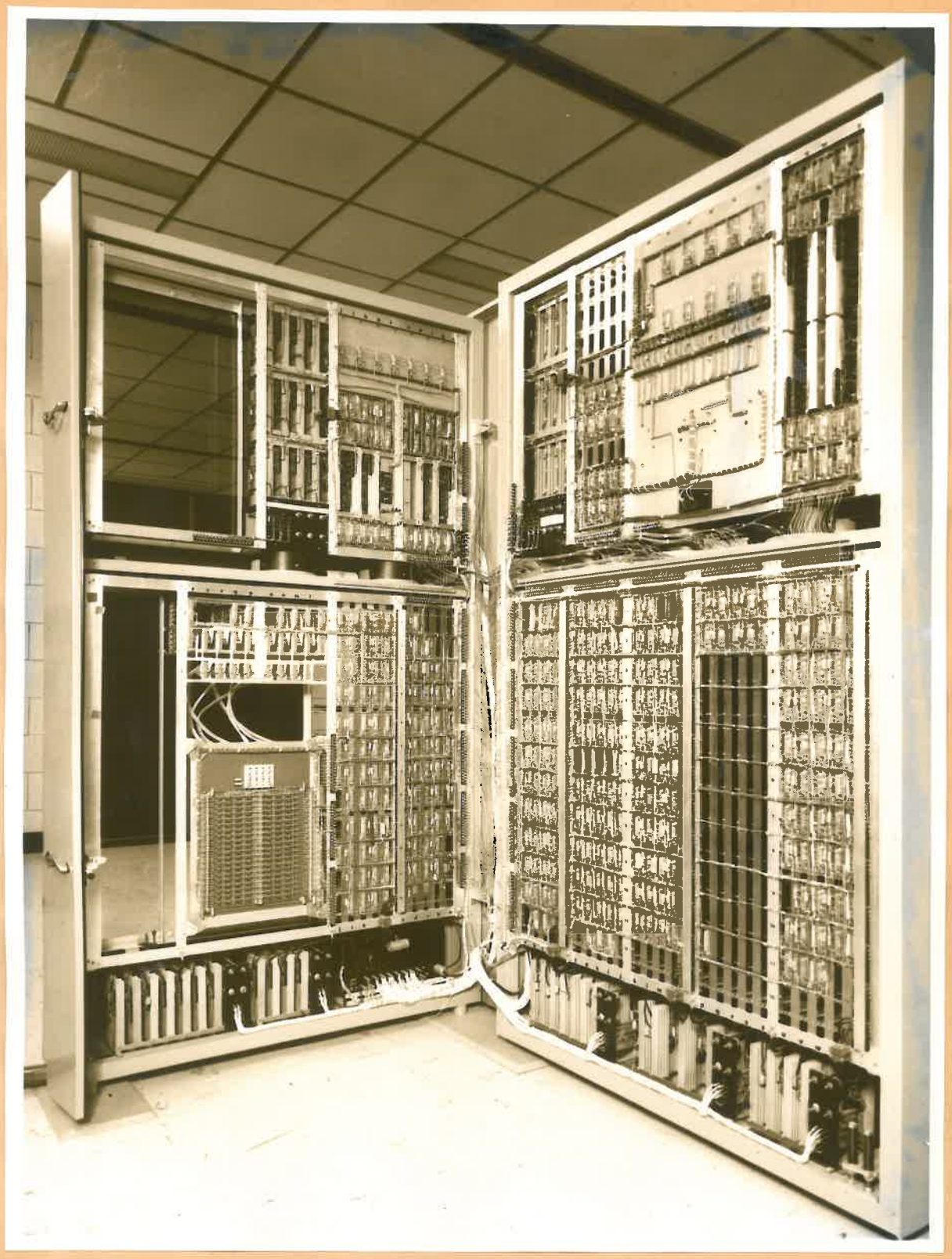


FIG. 2 (c) BACK VIEW OF MAIN FRAME

or 0.25 V. of the nominal voltage. A maximum ambient temperature of 45°C. was assumed.

The basic machine required approximately 400 packages and heat sink units, containing approx. 3500 transistors and 10,000 diodes.

(2) Storage Requirements

The CIRRUS order allows 14 bits for addressing the main store, providing for a store capacity of 16,384 words. Initial planning was on the assumption that addresses 0 - 8191 would refer to a core store and addresses 8192 - 16383 to a machine language fixed store similar to that used in the control unit. The latter store is intended to provide low cost storage for the assembler and compiler and the commonly used sub-routines. The permanent storage of these programs within the machine adds to the operating convenience of the system and since the various programs held in the machine can use the same fixed store routines, results in a decrease in the total storage requirements for multi-program operation. A capacity of 4096 words of fixed storage is expected to be sufficient for these programs. To maintain synchronism with the register store, the fixed store must operate on a 6 μsec cycle although capable of much greater speed. The register store has a capacity of 512 words, 64 for use as general purpose registers and the remainder for buffering of the high speed peripherals.

Although referred to externally as a full word of 36 bits, data is stored within the machine as 18 bit half-words. An extra bit is attached to the least significant end of the address by the control unit to specify whether the upper or lower half-word is required by the sub-order. A parity bit is added to each half-word to assist in the

detection of errors and/or store failure, and an extra bit is required in the register store to hold the overflow bit from the arithmetic unit. The main core store therefore has a capacity of 16,384 19 bit words, the register store 8,192 20 bit words and the machine-language fixed store 8192 19 bit words. Since the M and R registers serve as output buffers and the address and input are derived from the appropriate source by gating circuits, separate registers are not required to perform these functions.

The "word length" of the sub-computer is also 36 bits but in this case is read as a full word. Two parity bits are added to allow standardisation of the parity checking hardware. The control fixed store must therefore have a capacity of 4096, 38 bit words. For convenience both fixed stores use the same mechanical construction, providing storage for 8192 19 bit words. A simple variation is the selection circuits allows the information to be read as 19 or 38 bit words.

The development of the core stores was commenced during 1959 using 80 thou. cores and transistors operating close to the maximum ratings. The main store was then to be built in units of 4096 19 bit words. Towards the end of 1960, better cores and transistors became available and were incorporated in a new design described in Section B. The driving circuits for the earlier store which used a new form of drive switch are described in Appendix 2. Two forms of fixed storage have also been developed. The first store proved to be unsatisfactory mechanically and, in some respects electrically, but was completed and installed in the control unit to allow the testing of the machine to continue without interruption. This unit was subsequently replaced by the second type. Both stores are described in Section C. The two forms of storage are discussed

in chronological order of development since the experience gained with the first form had a considerable bearing on the design of the second.

SECTION B

THE CORE STORAGE UNITS.

(1) INTRODUCTION

Initially no firm specifications were placed on store speed or cost other than that it should be compatible with the rest of the machine. With an anticipated expenditure of £10-15,000 on components for the complete machine it was thought however, that the coincident current core store would be the most suitable. An investigation of the various alternative storage media, ferrite plates, twistors, multi-apertured cores and thin films showed that none of these was competitive with the core. Plates and multi-apertured cores were too expensive and twistors unavailable. Thin films were still under development but in any case were much faster and more expensive than necessary. A discussion of the current status of these devices in Appendix 3 suggests that under the same conditions this decision would still be valid although improvements in core technology and semiconductors would allow a better overall performance for the same expenditure.

In view of the large number and short length of the stored words, a linear selection core store was unattractive despite the higher speed since the increased cost lead to an unbalanced system. The coincident current store was therefore chosen, the cores selected allowing a conservative 6μ sec cycle within the restrictions of the overall machine timing.

(2) THE COINCIDENT CURRENT STORE

(2.1) SELECTION PRINCIPLE

The hysteresis loop of a square loop core is shown in Fig. 4. In the absence of an applied field, the core will be in either of the two remanent states P or N, defined as the '1' and '0' states respectively. As can be seen from the figure, there exists a current I m such that this current will, if applied in the right direction, cause the core to

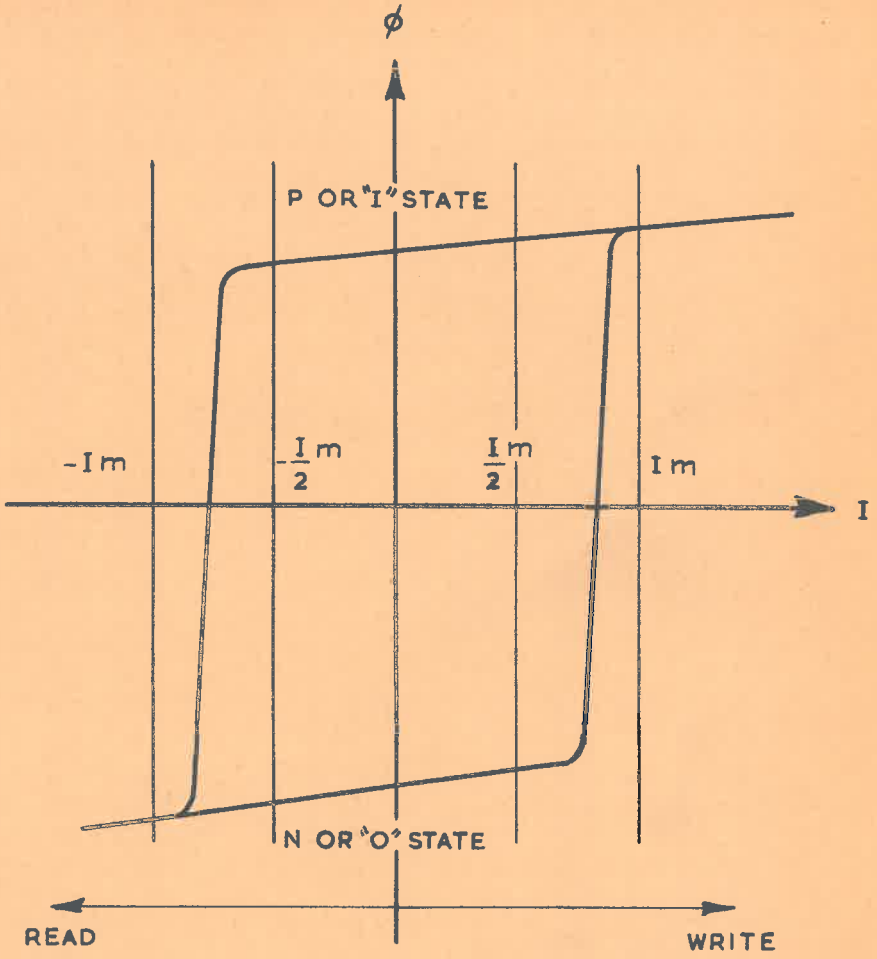


FIG. 4. HYSTERESIS CURVE OF A SQUARE LOOP CORE

change state but due to the rectangular hysterisis loop a current of ½ I m will leave the core unchanged. This property is the basis of the coincident current selection principle.

When wired into an array, a core is linked by four sets of wires (Figs. 6 and 7). One set links all cores along each X co-ordinate, another links all cores along each Y co-ordinate and the other two, the sense wire and the inhibit wire, link all cores in a plane. A store is normally a three dimensional stack operated in a parallel mode. If a word has W digits, W planes are used and a word is stored in the Z direction, occupying the same core position in each plane. The corresponding X and Y windings of each plane are connected in series so that each plane received the same drive currents. The store can then hold as many words as there are cores in a plane.

The block diagram and timing for a typical core store are shown in Fig. 5 During the read phase, currents of -½ I m are applied to the appropriate X and Y lines and the core on the intersection of these lines is set to the '0' state. No other core can change state since the drive is less than the switching threshold. If a selected core had been in the '1' state, the resulting flux change will induce a large voltage, 50 - 100 mV., in the sense wire. The flux change due to a '0' is very small and induces a small voltage 5 - 15 mV., of shorter duration in the sense wire. A word will therefore appear in parallel on the W sense wires. For the write phase, currents of + ½ I m are sent down the X and Y lines. This, however, would set all cores to the '1' state. If a '0' is to be written into a plane, the inhibit winding is energised with a current of - ½ I m. The selected core then receives a nett current of + ½ I m and will remain in the '0' state to which it was set during the

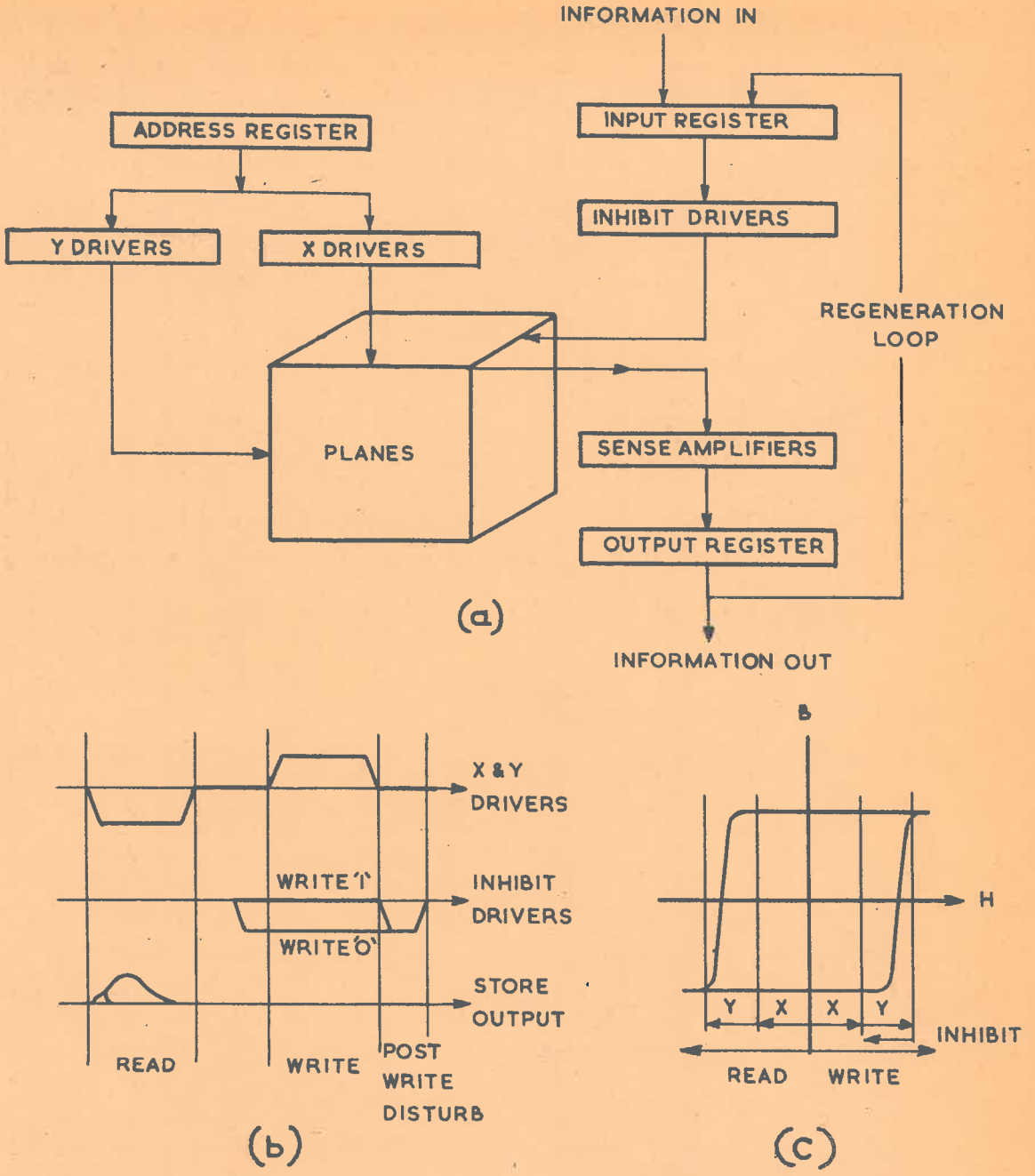


FIG.5 BLOCK DIAGRAM AND TIMING FOR A STORE WITH COINCIDENT CURRENT SELECTION

read phase. Since reading is destructive, if it is desired to retain the information in the core, it has to be restored during the following write period.

When operated in this manner, the cores perform both storage and switching functions, since the well defined switching threshold of square loop cores allows part of the selection to be performed within the array itself.

In practice the development of a store presents two main problems, spurious signals on the sense wire and the drive power required to deliver constant current drive pulses of several hundred milli-amps against the back e.m.f. generated by the inductive drive lines. The origin of these problems and their effect on store design are discussed below.

(2.2) DISTURBANCES ON THE SENSE WIRE

During the store cycle, various spurious signals, some of considerable amplitude, are coupled to the sense wire. These result from:

(a) signals generated by the half-selected cores

(b) magnetic and capacitive coupling between the drive and sense wires.

Those which introduce noise during the read phase are the most serious since it may be difficult to distinguish between a core output and a burst of spurious noise. Noise occurring during the rest of the cycle is an inconvenience which does not significantly affect store operation, but has a considerable influence on the design of the sense amplifier and can impose a limit on the store cycle.

(2-2.1) SIGNALS GENERATED BY HALF-SELECTED CORES

During the rise and fall of the drive currents, the small change in the flux state of the half-selected cores generates a signal in the sense wire. The magnitude of this signal is dependent on the states of the cores, the history of pulses which they have received and the rate of change of the drive current (B5, C26). The peak value of this disturb signal can be as high as 30% of that due to a switching core, although of much shorter duration. To minimise the cumulative effect of these signals, the sense wire is threaded so that equal numbers of cores produce positive and negative disturbs, providing a first order noise cancellation. Two winding configurations in common use are shown in Figs. 6 and 7. The diagonal sense winding has been most commonly used in the past but the rectangular pattern has some advantages for fast stores and is becoming more popular. To be fully effective the winding pattern should provide cancellation of signals occurring with a minimum time difference. With propagation times through the sense winding of 50 to 200 μ sec and drive rise times and hence disturb signals of similar duration, this can be quite significant and becomes more important as the store speed increases. The shorter physical and electrical length of the rectangular sense winding and the pattern of winding both contribute to better noise cancellation than is possible with the diagonal winding.

Apart from the inevitable spread in core characteristics, a limit is imposed on the effectiveness of the cancellation by the variable signal generated by a half-selected core. The reason for the variation can be shown by reference to Fig. 8. an expanded hysteresis loop. The idealised remanent states are A and B for a '1' and '0' resp. If the core is subject to a series of half

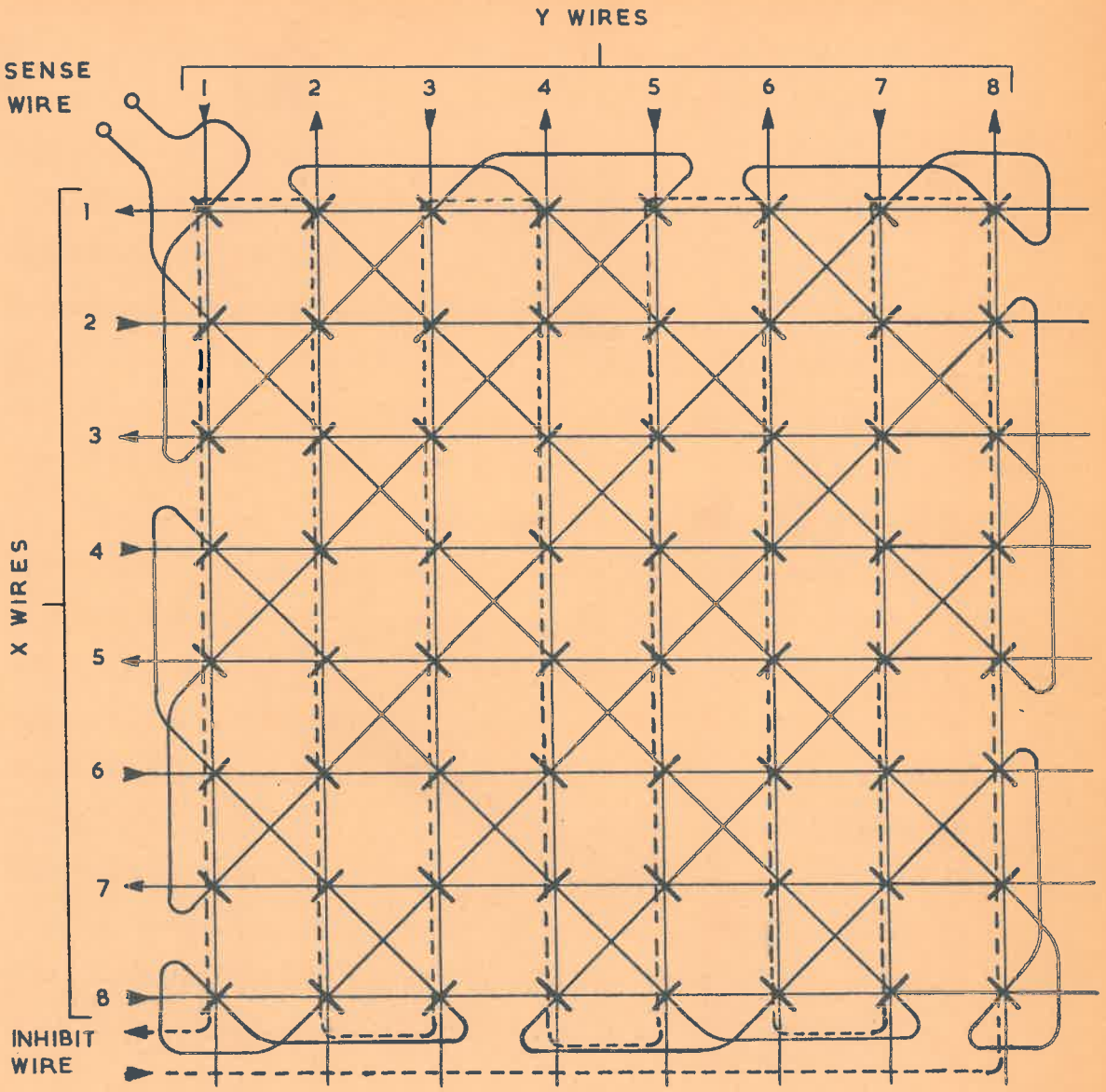


FIG.6 DIAGONAL SENSE WINDING

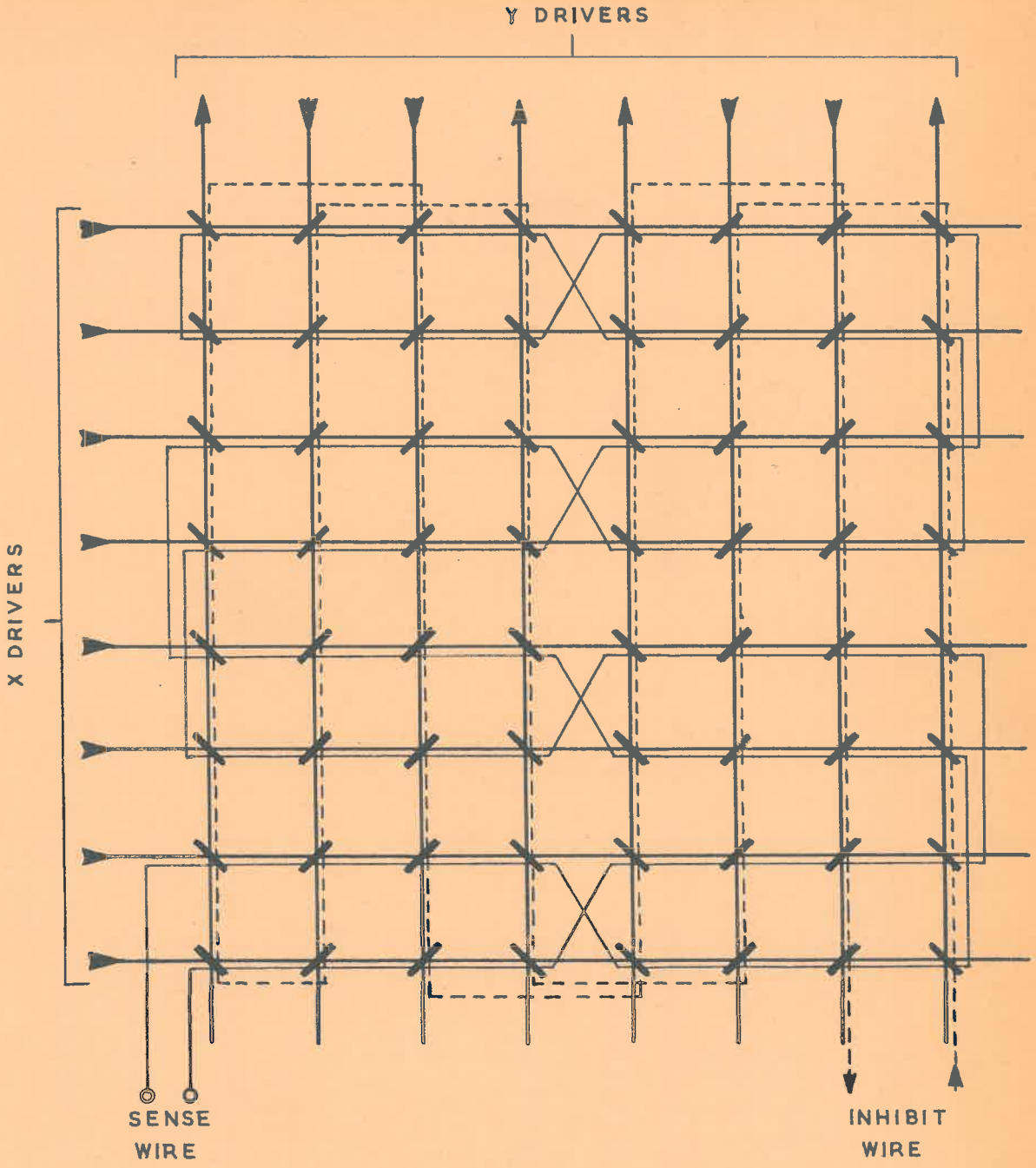


FIG. 7 RECTANGULAR SENSE WINDING

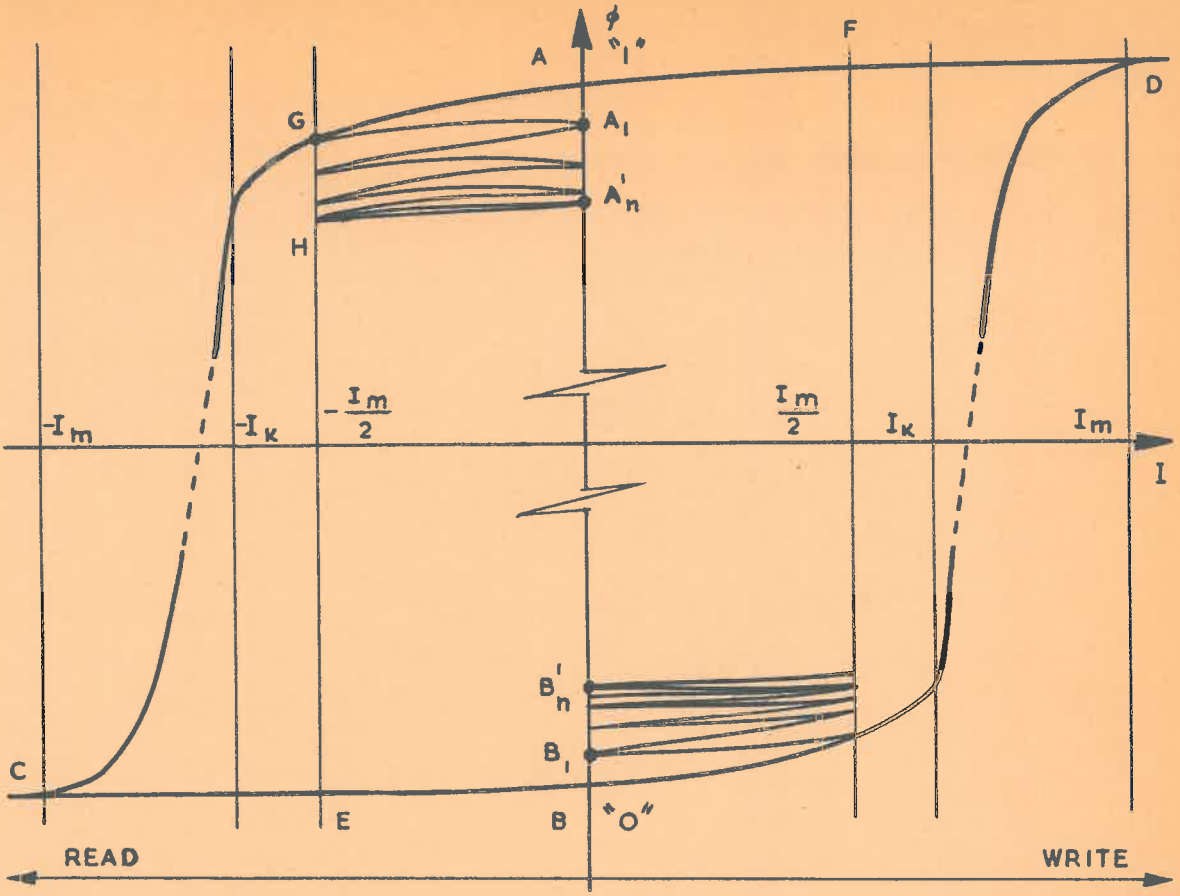


FIG. 8 MINOR LOOP BEHAVIOUR OF A STORAGE CORE

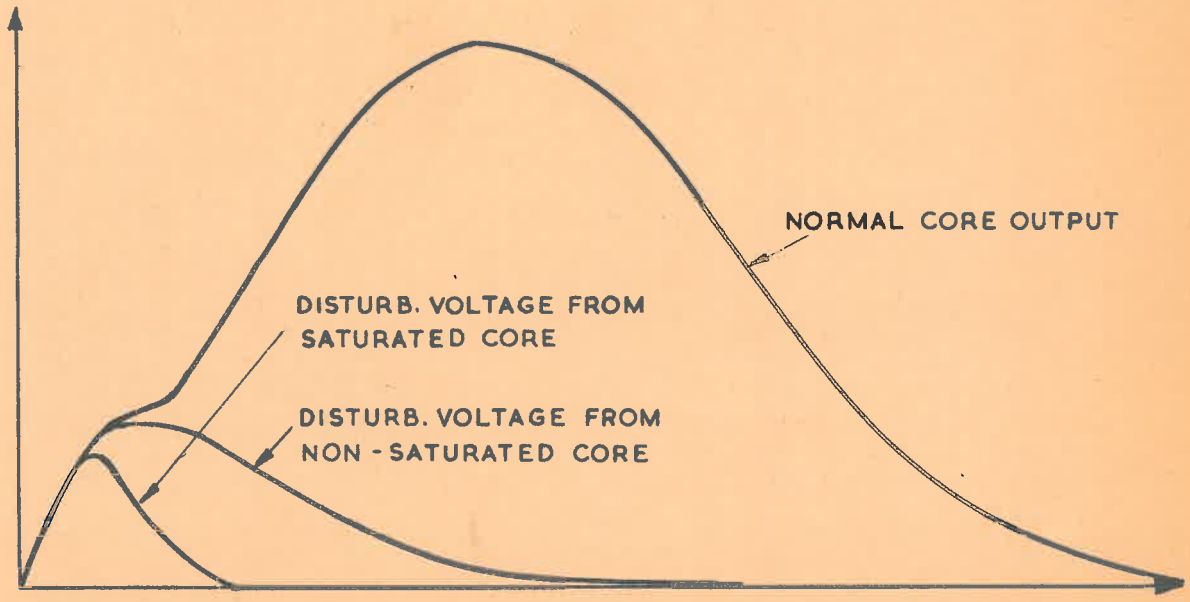


FIG. 9 CORE OUTPUTS FOR DIFFERENT REMANENT STATES

select pulses in the read direction, the remanent state for '1' will move downwards in a series of decreasing steps, finally reaching a stable loop such as A_n HA_n . A core in the '0' state will traverse the loop EBE and remain in the same position. Similarly a series of half write impulses will tend to move the operating points upwards from B to B_n and from A_n to A.

This process is reversible and the remanent states of the core may assume any value between A and A_n for a '1' and B and B_n for a '0'. The resulting disturb voltages will vary over the range shown in Fig. 9. A core on a stable saturated loop such as A_nH or BE will give a small signal present only during the rise of a half read current waveform, but a core in a remanent position such as A or B_n will give a signal of longer duration since some domain wall motion is involved in adjusting to the new operating point. Similar wave forms result from an undisturbed '0' point B, and a disturbed '0' such as B1 or Bn when the core is fully selected for a read.

Obviously cancellation of signals covering this range of wave forms cannot be particularly effective. However, in normal operation the cores will tend towards the states A_n and B since the effect of half read drive pulses in the inhibit winding, which affect all cores in the plane, will dominate the effect of the half read-half write pulses on the selected drive lines. This is sometimes accentuated by the use of a post-write-disturb pulse, a half read drive applied by the inhibit drivers at the end of each write period. The cores will therefore tend to settle into states which give smaller disturb signals of short duration and with less variation due to the state of the core.

Coupling between the inhibit and sense wiring via the cores can be particularly troublesome although this does not directly affect read discrimination. When the inhibit winding is energised, disturb signals are coupled into the sense winding by all the cores in the plane. Any unbalance between the disturb voltages will generate a large spurious signal in the sense winding which can paralyse the sense amplifier. The signal due to the trailing edge of the inhibit current can result in an increase in the store cycle to allow for amplifier recovery. Since the post-write-disturb pulse introduces the same transients, this is eliminated if possible to allow increased time for amplifier recovery. For each sense winding pattern, a worst case can be postulated in which all cores linking the sense winding in a positive sense are in one state and all those linking in a negative sense are in the other. For a plane with 4096 cores, only ½ mV. difference in the disturb voltages is required to generate a 1V noise signal in the sense wire.

(2.2.2) COUPLING BETWEEN DRIVE AND SENSE WINDINGS

Direct magnetic coupling between the drive wires and the sense wire is minimised by the two winding configurations shown above, since this was considered in the design of these patterns. The sense wire should be threaded so that the mutual inductance between drive and sense wires approaches zero for all drive wires. This is achieved by making the area of the sensing loops as small as possible, ensuring that cancelling components are equal in magnitude and time. Both configurations are capable of providing a high degree of noise rejection since both ideally have zero mutual inductance with the drive wires.

The capacitive coupling is normally much more significant since little can be done to reduce the capacity between the drive and sense wires. The aim is to balance the sense wire about the drive wires in such a manner that no nett difference signal appears at the output. The signals due to the cores can then be sensed by using a differential amplifier or a balanced transformer to reject the common mode capacitive coupling. The rectangular sense winding is superior to the diagonal winding in this regard since the wiring pattern of the latter allows a difference in the time and magnitude of the coupling to the various sections of the winding. The result is a high frequency ring on the sense wire. To minimise the capacitive coupling, the driving circuits should be arranged so that the voltage excursion of the driven wires is as small as possible. Some d.c. coupled drive systems are poor in this respect.

(2.2.3) METHODS OF REDUCING THE EFFECTS OF NOISE

The most significant reduction of noise is achieved by the appropriate design of the sense winding as discussed above. To ensure reliable sensing and/or further reduce noise, three other techniques are in common use.

The noise which tends to obscure the plane output, occurs during the rise of the drive currents, but the signal resulting from a switching core reaches a peak value $\frac{1}{4}$ - $\frac{1}{2}$ μsec later with typical storage cores. A narrow strobe pulse commencing at the peaking time of the core output will sample the output when the discrimination between a '1' output and a '0' output or noise is much better. Discrimination ratios in excess of 10:1 can be readily achieved. This favours a fast rise of current to ensure that the noise voltages will have decayed by strobe time. However, this increases the drive voltages and can

also accentuate the capacitive coupling between drive and sense windings. A satisfactory compromise is for the rise of the drive currents to be approx. ½ the peaking time of the core output.

The techniques described above are generally sufficient to provide adequate discrimination for planes with up to 4096 cores. If larger planes are to be used or a very high discrimination ratio is required the sense winding is normally sub-divided into a number of sections, each with a separate sense amplifier. The methods employed for the diagonal and rectangular sense windings are shown in Figs 10 and 11 for the case where each winding links ¼ of the total cores. Each section of the sense winding forms a self cancelling unit. For the diagonal pattern each winding has 4 sections chosen so that no two sections of any winding are common to the same X or Y drive line. This effectively reduces the noise by a factor of 4. The subdivision of the rectangular winding does not reduce the coupling from the X drive lines. Consequently to minimise the noise, the X drive should be applied slightly in advance of the Y drive so the noise coupled from the X drive has decayed before the Y drive is applied and the selected core switched. This technique can be used to advantage with either configuration with or without a subdivided sense winding if noise during read is excessive. The inhibit winding can also be subdivided into 4 sections such that only 1/16th of the total number of cores are common to any pair of sense and inhibit windings giving a substantial reduction in coupling between the two. The appropriate sense and inhibit windings can be simply derived from the address of the selected core.

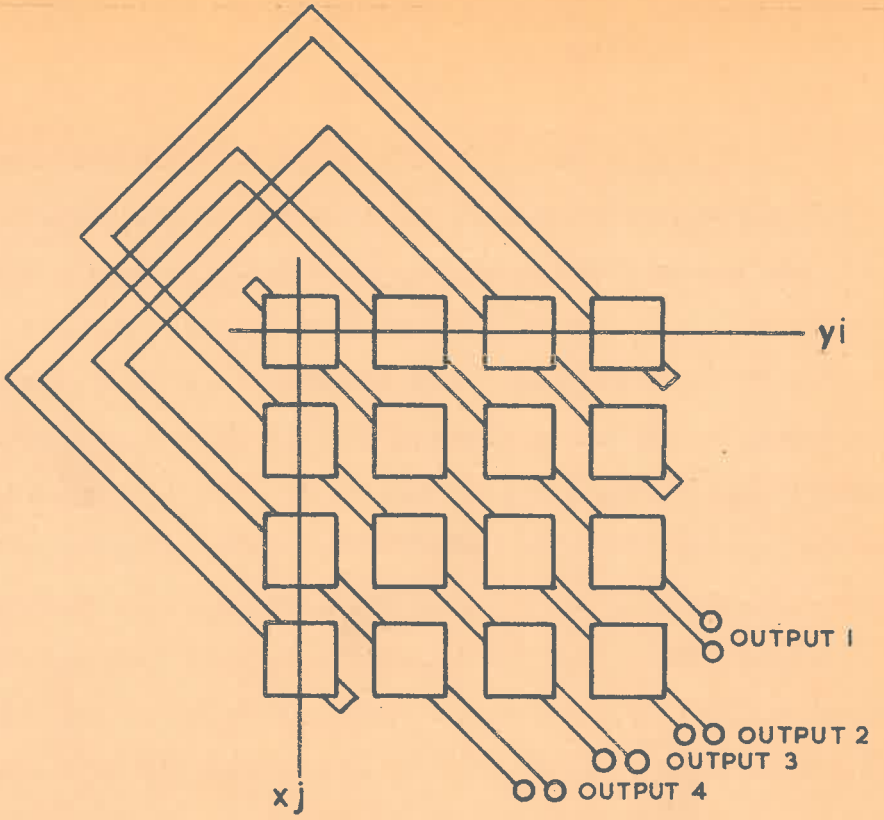


FIG. 10. SUBDIVISION OF DIAGONAL SENSE WINDING

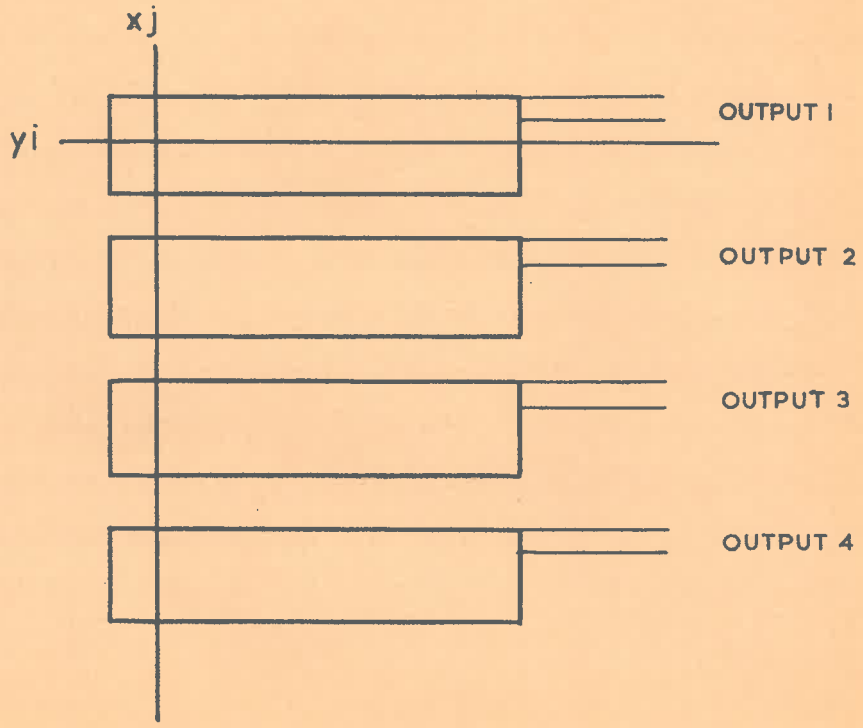


FIG. 11. SUBDIVISION OF RECTANGULAR SENSE WINDING

The design of the sense amplifier can also make a significant contribution to reducing the effects of the noise in the sense wire. A well designed sense winding with a transformer or difference amplifier input to the sense amplifier provides a very high common mode rejection and capacitively coupled noise can be reduced to a few millivolts. The input impedance of the sense amplifier should not be too low or the plane output will be reduced and the L/R time constant of the sense winding will limit the frequency response. The sense amplifier as a whole should have a frequency response sufficient to pass the core signal and the inductively coupled noise with a minimum of delay and distortion. If the frequency response is too low, the signal to noise ratio at strobe time is reduced and recovery from the inhibit transient is slower. The upper limit of the frequency response can still be chosen low enough to eliminate much of the higher frequency ringing which occurs with larger planes. To handle the large transients which can be present the amplifier should have a large dynamic range and a fast recovery from overload. A long train of noise on core signals of one polarity has a d.c. component which can cause a drift in the discrimination threshold. This pattern sensitivity can be minimised by avoiding the use of reactive elements in the amplifier. Within these restrictions the amplifier has to amplify and strobe the plane output and compare the strobed signal with a threshold to determine whether a '1' or '0' was read. The appropriate '1' and '0' outputs must then be generated to enable the information to be transferred to the rest of the computer.

(2.3) THE DRIVE CIRCUITS

(2.3.1) CIRCUIT BEHAVIOUR OF THE DRIVE LINES

When the drive lines of the store are energised by a half-select current, the operating points of the cores move along the saturated portion of the hysteresis loop. In this region the cores behave as a normal linear ferrite and produce an inductance of 3 n H/1000 cores in the impedance of the drive lines. The drive lines also have distributed capacity and a small series resistance and for a large store the drive lines resemble lossless transmission lines with a characteristic impedance of approx. 150 Ω and a velocity of propagation of 15-20 n sec./1000 cores. If the propagation time of the drive lines is comparable with the rise time of the drive pulse, the drive lines should be correctly terminated to prevent reflections and preserve the current waveform. However, for most stores the propagation time is considerably less than the rise and fall times of the drive pulses and the drive lines can be treated as a series R-L circuit.

For a typical store, with drive currents of 250 mA, rise and fall times of 0.2 μsec and an inductance of 15 μH, a back e.m.f. of 20 V. is generated by the drive lines during the rise and fall of the drive currents. Against this non-linear load, the drivers have to deliver a constant current controlled to approx. 5% in magnitude and with a minimum of overshoot. Two techniques are in common use. The first is to drive from a high voltage source with a large current defining resistor. This allows the use of the transistor as a saturated switch, minimising the power dissipated in the transistor but requiring a relatively high voltage rating. The other approach is to use the transistor as a non-saturating constant current source. If the circuit is designed so that the transistor does not saturate under the

voltage generated during the rise of the current pulse, then the voltage across the transistor during the remainder of the pulse will be high, resulting in a high dissipation in the transistor. Either approach is satisfactory, the choice between the two being largely determined by the type of drive system employed and the relative costs with the available transistors.

The impedance level of the drive lines is well suited to the use of transistor drivers but early stores using transistor drivers were restricted in size and speed by the limited ratings of the available high frequency transistors. These restrictions have been removed by improvements in both the transistor ratings and driving techniques, and transistor drive is now feasible for almost any store.

(2.3.2.) THE X AND Y SELECTION CIRCUITS :

This aspect of core storage has been subject to a great deal of ingenuity and development, since the choice of selection circuit has a considerable influence on the overall cost and performance of the storage system. The inhibit and output circuits must be provided on a per plane basis and little minimisation other than developing efficient circuits is possible. The function of the X and Y selection circuits is to provide a 1 of N selection and to deliver accurately controlled positive and negative current pulses to the selected drive line with low spurious outputs to the non-selected drive lines. Spurious outputs waste drive power and can have a cumulative destructive effect on the information stored in non-selected cores.

The many different selection circuits developed can be

divided into 2 classes[5], those using direct drive with or without transformer coupling and those using square loop magnetic switches. Direct drive using a driver for each line has been used but is expensive and some form of drive matrix using diode steering (C20, C37, C39) transistor steering (C19, C20) or a combination (C17) is normally employed. Some of these will only provide a unidirectional output and a dual set of wires or transformer coupling (C9) is necessary to provide the positive and negative currents required for read and write. Magnetic switches (A1, C3, C31, C35) can generate both polarities from unidirectional inputs and being transformer coupled can provide an impedance match between drivers and drive lines. The system best suited to a particular application depends on the store cycle required and the size of both the switch and the store. The choice of circuit technique i.e. saturated or non-saturated drivers can be influenced by costs and can in turn have a bearing on the choice of selection system. Direct coupled drive systems, using diode or transistor steering, normally favour the use of non-saturating drivers. For transformer coupled systems and magnetic switches, either can be used, the transformers normally being current driven.

It is desirable in most cases to choose a drive system employing the minimum number of active elements. This tends to reduce the cost of the selection circuits and increase reliability but in some cases this approach can lead to inferior switch performance and marginal operation of the system. Magnetic switches allow a considerable reduction in the driver count but due to switch losses and the added inductance of the non-selected switch cores, the individual drivers must be more powerful than those for direct drive and these switches are not well suited to high speed operation. The output from magnetic switches is gen-

erally not as well controlled as that from the various direct drive systems and spurious outputs can be troublesome. Direct drive on the other hand requires a greater number of transistors and/or diodes and consequently has a lower inherent reliability. This type of drive is preferred however for large and/or fast stores.

The systems so far discussed all suffer from a common disadvantage, only one driver effectively contributes to the switch output. Each driver must have a reserve power sufficient to allow continuous interrogation of one address, requiring a power rating far in excess of that necessary for normal usage. The drivers are therefore used rather inefficiently and some difficulty may be experienced if transistor drivers are to be used. Since there are a number of drivers idle during each phase of switch operation, it would be preferable to find some method by which these drivers could contribute to the switch output. The load sharing switch (Mi), a recent development in driving techniques, is capable of combining and distributing the power of a number of drivers. Each driver is used for either read or write during each cycle irrespective of the output selected, allowing efficient usage of the drivers. The worst case peak power required from each driver is therefore greatly reduced although the average power is unchanged. Cheaper transistors of reduced ratings can then be used to generate the same output power.

(2.3.3.) THE LOAD-SHARING SWITCH :

A load-sharing switch is based on an array of transformers each of which has multiple input windings. A 12 input-8 output switch is shown in Fig. 12. Eight transformers are required each of which has 12 identical input windings and 1 output

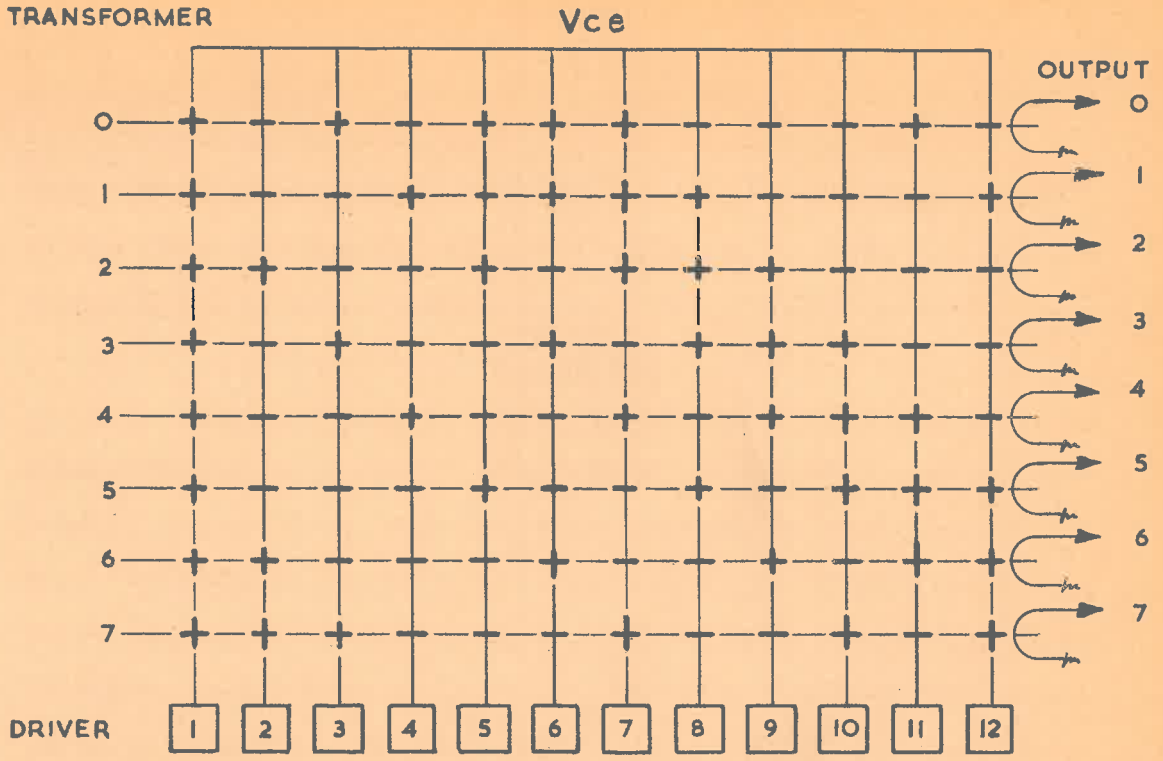


FIG.12. A 12 INPUT-8 OUTPUT LOAD-SHARING SWITCH

	DRIVERS REQUIRED											
OUTPUT	READ						WRITE					
0	1	3	5	6	7	11	2	4	8	9	10	12
1	1	4	6	7	8	12	2	3	5	9	10	11
2	1	2	5	7	8	9	3	4	6	10	11	12
3	1	3	6	8	9	10	2	4	5	7	11	12
4	1	4	7	9	10	11	2	3	5	6	8	12
5	1	5	8	10	11	12	2	3	4	6	7	9
6	1	2	6	9	11	12	3	4	5	7	8	10
7	1	2	3	7	10	12	4	5	6	8	9	11

FIG.13. DRIVER SELECTION FOR 12 INPUT LOAD SHARING SWITCH

winding. The input windings are interconnected with the polarities shown and connected to 12 drivers. The output windings are connected directly to the required load, an X or Y drive line of the store. Suppose now that drivers 1, 3, 5, 6, 7 and 11 are energised and deliver a defined current to the switch. Transformer O receives a positive excitation from each driver but all other transformers receive 3 positive and 3 negative excitations which cancel. Output O will therefore be energised by the combined power of the 6 drivers and will deliver a positive pulse to the memory drive line. Similarly by energising drivers 2, 4, 8, 9, 10 and 12, output O will deliver a negative pulse and all others ideally will produce no nett output. By choosing the appropriate 6 drivers (Fig. 13) any of the 8 outputs can be selectively energised with the combined power of 6 drivers to produce either positive or negative output.

Since the operation of the switch does not require any threshold in the switch cores, normal linear magnetic material can be used, resulting in a much higher switch efficiency. The principle of the load-sharing switch can be extended to switches with any reasonable number of outputs. For those of interest in the majority of storage applications, $n = 2^m$ outputs, the most efficient switch requires $n + 4$ inputs. One feature of the load-sharing switch which could be very relevant in some applications is that a small number of drivers can fail without seriously affecting store operation. If the normal output is m units, n failures will reduce this to m-n units and give a maximum spurious signal of n units on the non-selected outputs. In most cases, this will only be useful for switches with 16 or more outputs and 1 or perhaps 2 failures, but switch configurations with more than the minimum number of drivers could be used to accentuate this facility

if required. The load-sharing switch is discussed further in Appendix 1.

Although it is theoretically possible to construct a load-sharing switch with many outputs, this is frequently unattractive due to the low power required from each driver. In addition, the inductance of the non-selected transformers becomes excessive and the switch performance deteriorates. A 16 or perhaps 32 output switch is probably the maximum practical size depending on the speed and power required. In one store described (C38) the switch was extended by means of diode steering in the secondary circuit, in another (C22) by using a number of separate switches each with their own set of drivers. Two other methods have been developed. The first, using diode switching in the primary circuit, was used in the CIRRUS stores and is discussed below. The second uses a new form of magnetic switch which was developed to accept the bi-directional output of the load-sharing switch. This is discussed in Appendix 2.

(2.3.4.) TOLERANCE ON DRIVE CURRENTS (A.2)

The penalty paid for the more economical selection circuits of the coincident current store, is the reduced tolerance on the drive currents. The allowed tolerances can be derived by a consideration of 3 basic criteria: the effective writing of 1^s and 0^s and the restriction that the half select currents must be less than the switching threshold.

If

I_m = minimum full select current

I_k = knee current or maximum half select current

I_x = half select current in X or Y line

I_z = " " " inhibit "

then

$$2\,I_{w\,min} \geqslant I_m \text{ - write '1'}$$

$$2\,I_{w\,max} - I_{z\,min} \leqslant I_k \text{ - write '0'}$$

$$\left.\begin{aligned} I_{z\,max} &\leqslant I_k \\ I_{x\,max} &\leqslant I_k \end{aligned}\right\} \text{ - limit on half currents}$$

If the tolerance on X and Y currents is x and that on the inhibit current is z these inequalities can be written :

$$2\,(1 - x)\,I_x = I_m$$

$$2\,I_x\,(1 + x) - (1 - z)\,I_z = I_k$$

$$(1 + z)\,I_z = I_k$$

$$(1 + x)\,I_x = I_k$$

For $k = \frac{I_m}{I_k}$ the relation between the tolerances can be shown to be

$$\left(\frac{1 + x}{1 - x}\right) k - \left(\frac{1 - z}{1 + z}\right) = 1.$$

This relationship is shown graphically in Fig. 14. For $k = 1.6$, a typical value for a coincident current core, a tolerance of $\pm$ 7.5% is permitted for all currents. In practice this analysis is pessimistic in that it was assumed that the various drive currents could vary independently. If all are derived from a common power supply such freedom is unlikely to exist and the allowed tolerance would be increased. With some drive systems, the inhibit current will be more accurately defined that the X and Y currents and it may be better to take advantage of this by using say a 4% tolerance for I_z and 9% for I_x.

The values so determined for the X, Y and Z currents, although optimum from a tolerance aspect, may not be the most suitable for low noise. The balance between disturb voltages in the '1' and '0' states is dependent on the drive currents used and

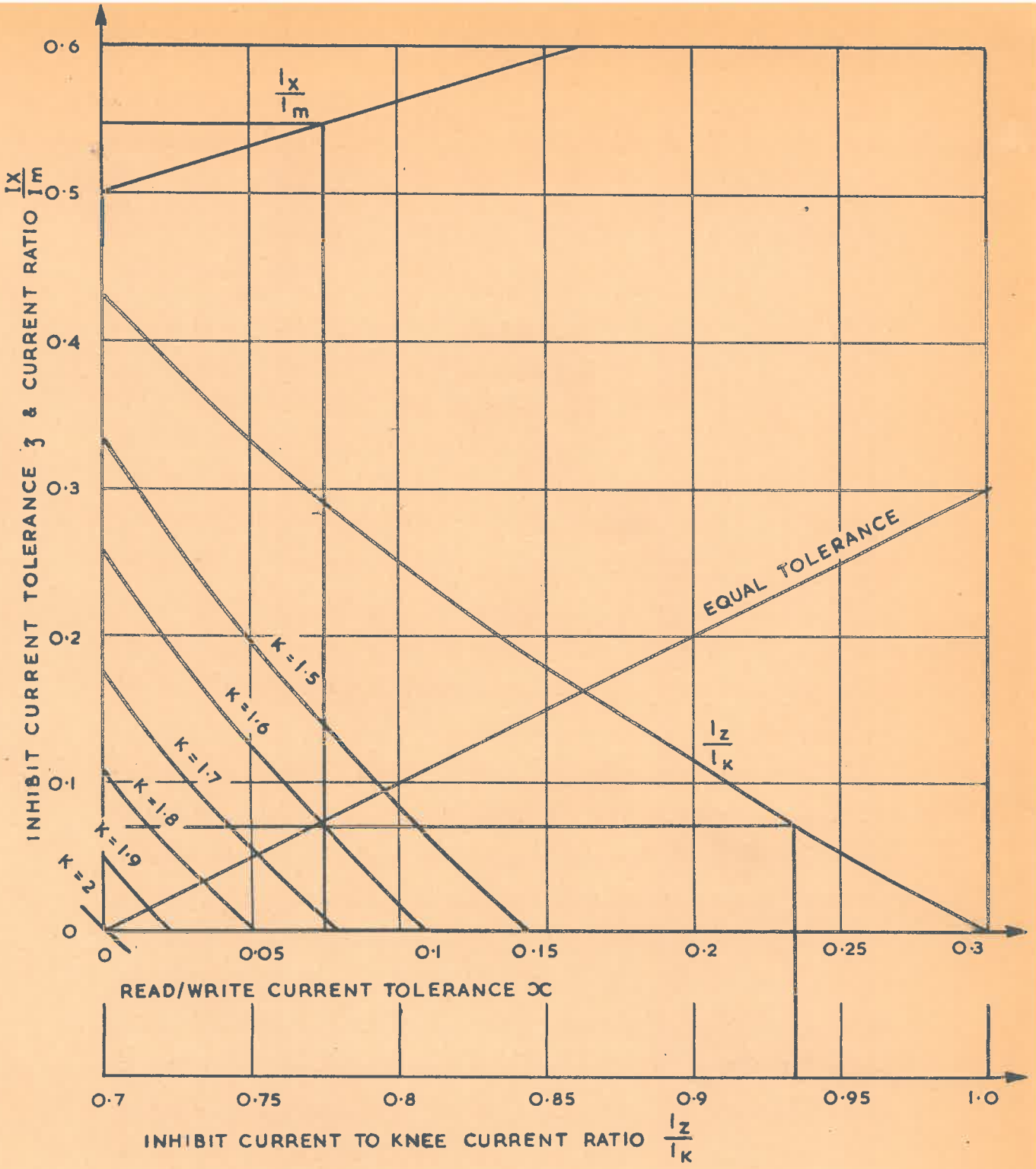


FIG.14 DRIVE TOLERANCE OF A COINCIDENT CURRENT STORE

minimum noise could well be achieved with higher or lower inhibit current or by an unbalance in read and write currents. The required unbalance in drive is generally quite small and can give a substantial reduction in noise although the drive tolerance is slightly reduced.

The drive tolerance should also be related to the range of ambient temperatures likely to be encountered. The majority of ferrites suitable for coincident current stores have a low Curie temperature (150 - 250° C) and consequently a temperature coefficient on drive currents of $\approx 0.5\%/^{\circ}$ C under normal operating conditions. Most cores have a knee current of 60 - 65% of the nominal drive current and allow operation over a range of up to 40° C provided the drive currents are held to very close tolerances. Adequate temperature compensation, however, ensures that the core will at all times be used under optimum conditions and gives a potentially more reliable system. Compensated drivers are satisfactory for a temperature range of up to 75° C but operation over a wider range requires either temperature control of the environment or the use of the recently developed wide range cores (C24).

(3) THE CIRRUS STORES :

The 16,384 half-word capacity for the main store was to be provided by four blocks of 64 x 64 x 19 cores with the X and Y drive lines interconnected to give a 128 x 128 array. There would then be in effect 4 sense and 4 inhibit windings for each plane. This was the largest size available when the planes were purchased but 128 x 128 arrays were subsequently produced at a considerably lower cost/bit. These also employed 4 sense and inhibit windings per plane so this had no effect on store design.

Only two blocks of store were initially installed but the hardware was designed to drive the full capacity. The register store used a single block of 32 x 32 x 20 cores.

In both cases the cores were Philips type 6 C1 with a nominal drive current of 500 mA, a switching time of 0.9 μsec and an output of 50 mV. In accordance with the previous section, the X and Y currents were chosen to be 250 mA $\pm$ 10 mA with a duration of 1.25 μsec and rise and fall times of <0.2 μsec. The inhibit current was chosen to be 265 mA $\pm$ 10 mA. Rise and fall times of <0.4 μsec were considered adequate with a nominal duration of 2.25 μsec giving 0.5 μsec overlap before and after the write pulse. An investigation of core characteristics indicated that drive voltages of 20 V and 15 V, resp. could be expected for the main store. The register store was to use the same basic driving hardware although the load was much smaller.

To provide reliable operation over the required temperature range of 10÷45° C, some form of temperature compensation was considered desirable. In view of the relatively small range, this could most conveniently be achieved by adjusting the drive currents. A drive system based on the load-sharing switch was chosen since it was one of the cheapest, provided efficient but conservative usage of the drive transistors and produced well controlled outputs with a high signal to noise ratio. With the available transistors, non-saturating drivers gave simpler and cheaper circuits with a better performance than those using saturated drivers.

Each store was to be a self-contained unit with its own power supplies and timing circuits. Sufficient space and drive

capacity were to be provided to allow expansion of the word length to 48 bits, requiring 25 bits/half word in the main store and 26 in the register store.

(4) THE MAIN STORE :

(4.1) THE X AND Y SELECTION CIRCUITS :

The block diagram of the selection circuit is shown in Fig. 15. Each load-sharing switch is of the type described earlier, requiring 12 inputs and providing selection of 1 of 8 outputs. The selection principle is extended from 8 to 128 outputs by employing 16 switches. The output of a common set of drivers (current sources) is steered to the appropriate switch by means of the 16 sink circuits and the diode network. An active (selected) sink has an output level of -20 V. which forward biasses the diodes on the selected switch. The switch then adds and distributes the power of the 6 active drivers to the selected output. All other diodes are reverse biassed by the voltage level, O V, of the non-selected sinks and the other switches produce no output. A particular output is therefore selected by selecting the appropriate 6 drivers, and 1 sink.

(4.1.1) THE DRIVING CIRCUITS :

The circuit of the load-sharing switch driver is shown in Fig 16. If all inputs are negative, T_1 will conduct and hold T_3 off. If any input goes positive, T_1 will be turned off and the base of T_3 taken to $\approx$ -3.5 V. Under these conditions T_3 conducts, reverse biassing D_4 and delivers a current of $\frac{\propto}{Re}$ $(6 + 3.2 + VD_3 - Vbe_2 - Vbe_3)$ amps to the switch. Allowing for reasonable variations in $\propto$ and the various diode drops, the current is defined to an accuracy of $\pm$ 2.5%. If required a greater accuracy can be achieved by increasing the voltage of the positive supply but this results in an undesirable

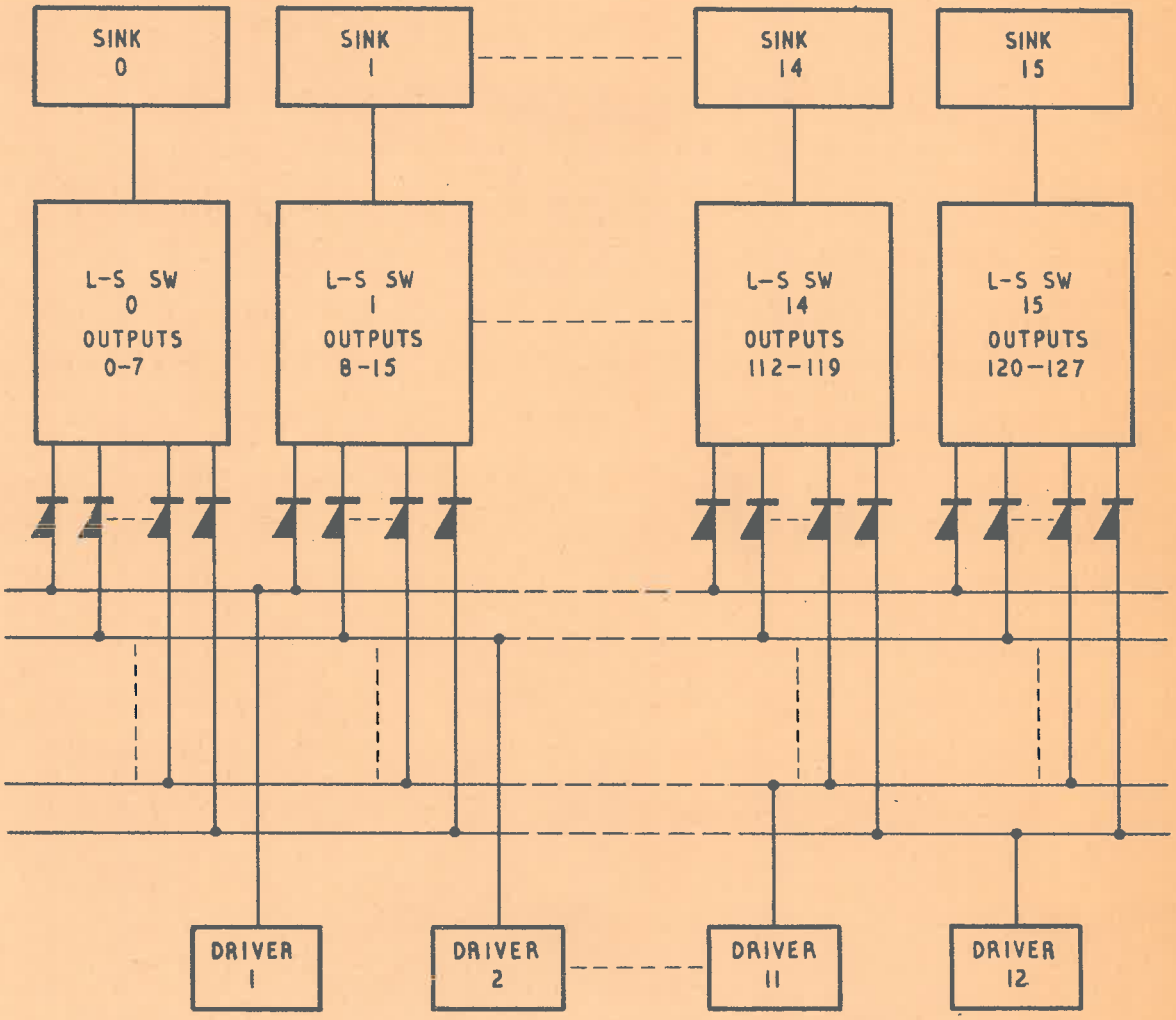


FIG. 15. BLOCK DIAGRAM OF X & Y SELECTION CIRCUITS

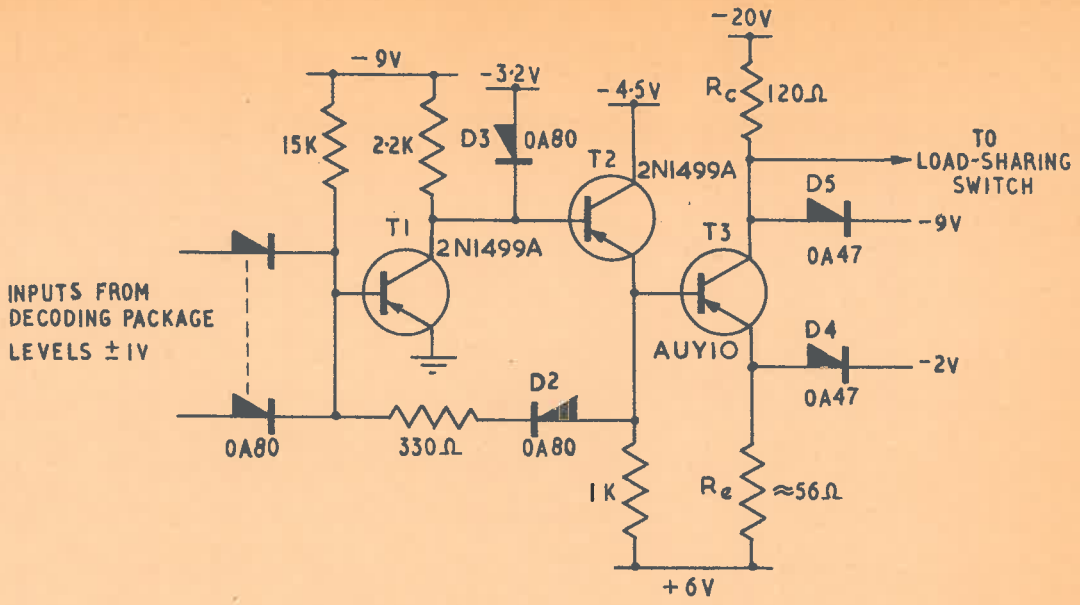


FIG. 16. SWITCH DRIVER

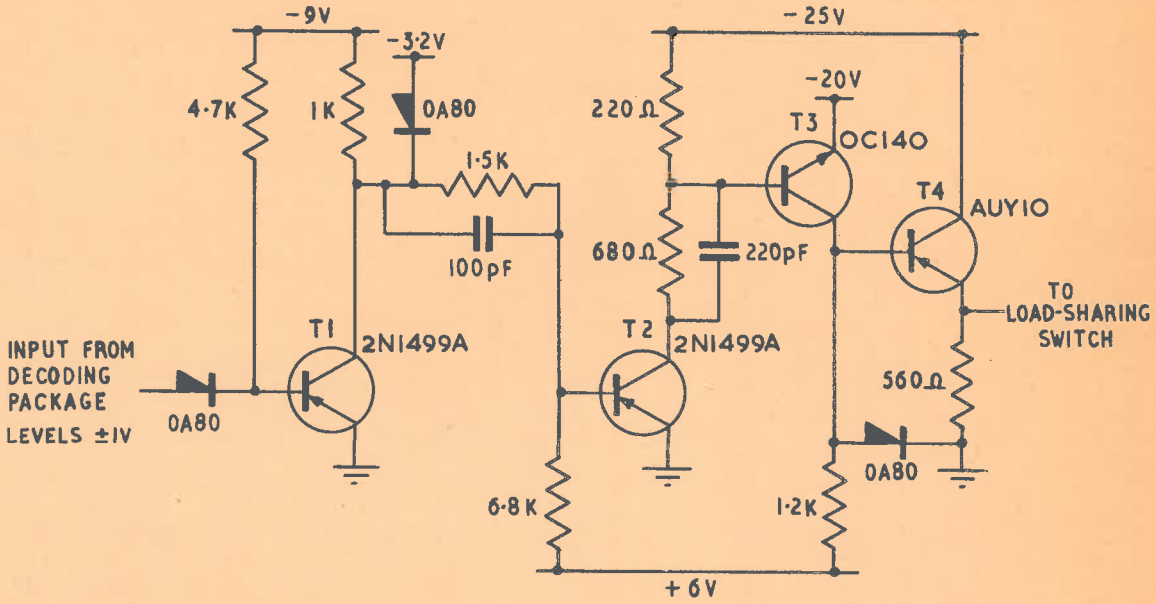


FIG. 17. SINK DRIVER

increase in the dissipation in Re and is not necessary in this application. A feedback action via D_2 prevents saturation in T_1, reducing both the magnitude and variation of storage time. Low spurious outputs from non-selected transformers requires that the individual drivers are well matched in amplitude and timing. D_5 ensures that T_3 maintains an operating point well out of saturation by conducting if a voltage transient takes Vc_3 more positive than -9V. Saturation could occur during the rise of the current pulse and results in a substantial overshoot on the current waveform. Rc provides shunt damping across the primary of the load-sharing switch, defining the time constant and back e.m.f. generated by the inductive load. A diode with low stored charge should be used for D4 to prevent overshoot of the drive currents.

Fig 17. shows the circuit of the sink driver. If the input is at -1 V, T_1 is conducting , T_2 and T_3 non-conducting and the output is at OV. When the input is taken to +1 V, T_2 and T_3 conduct and the output is taken to the -20V supply. In this condition T_4 must be capable of absorbing the pulse of 780 mA applied when the drivers conduct. The base impedance of T_4 must be very low since an initial base current of up to 250 mA can flow. The emitter resistor of T_4 is taken to O V rather than +6 V to reduce transistor dissipation. Eight of these transistors are mounted on one piece of heat sink material and a standing current of 10 mA in each transistor, necessary to handle the capacitive loading on the output of T_4, gives a total of 2W dissipation, doubling the dissipation in the heat sink. With the arrangement shown, T_4 in each of the seven non-selected sinks is reverse biassed minimising the dissipation in the heat sink and reducing the temperature rise in the sink drivers. This circuit would be improved if a saturated n.p.n. transistor were used in place of the T_3 - T_4

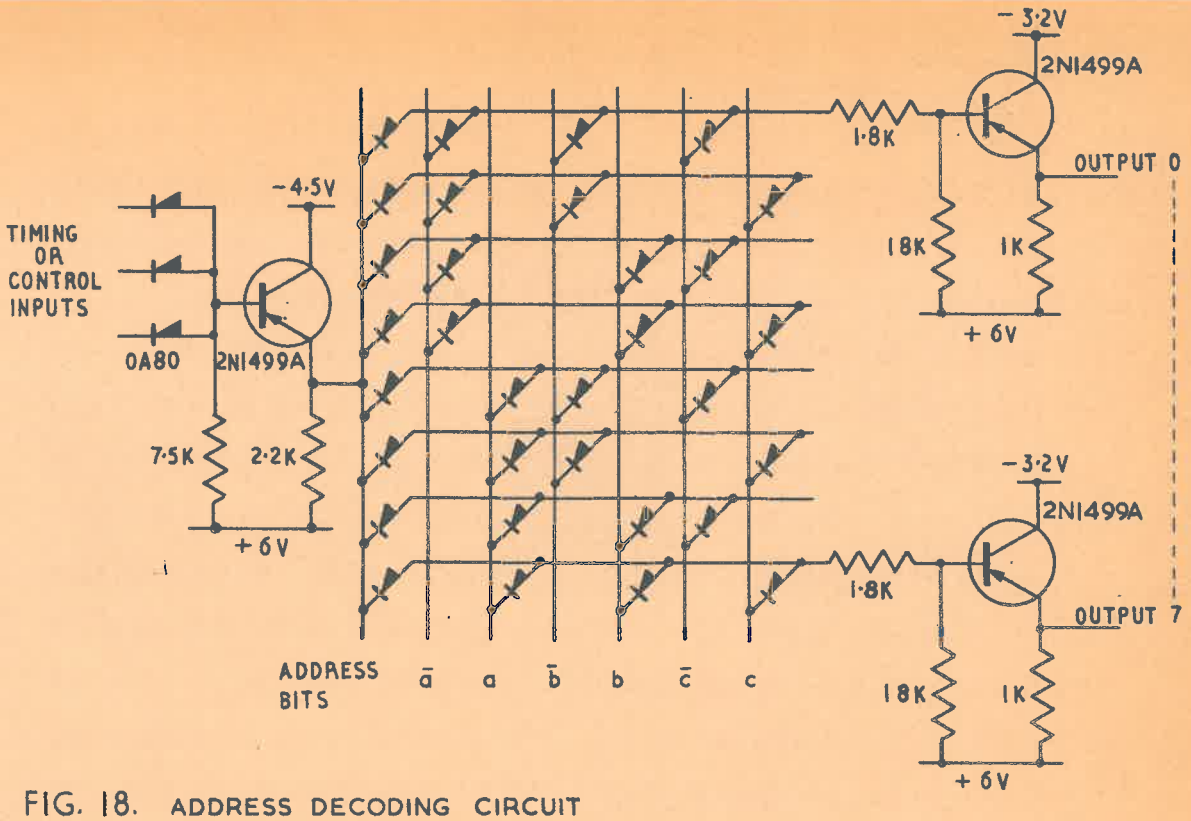


FIG. 18. ADDRESS DECODING CIRCUIT

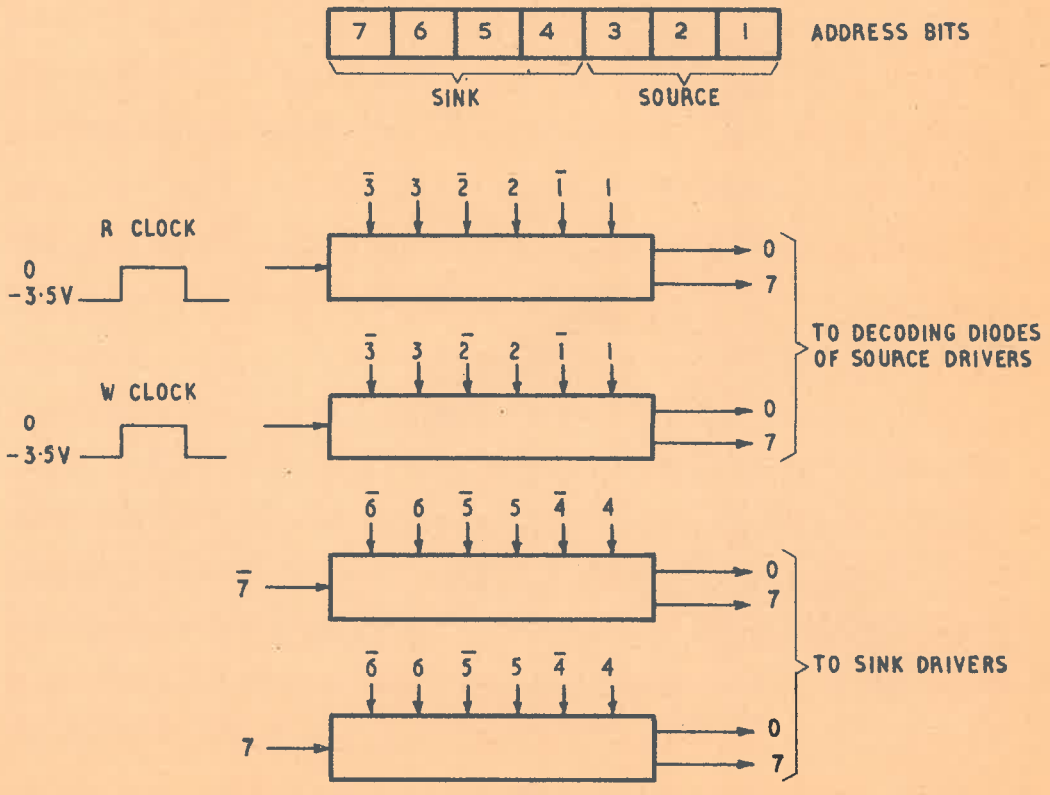


FIG. 19. BLOCK DIAGRAM OF ADDRESS DECODING.

combination, but no suitable transistors were available when the circuit was developed.

(4.1.2) ADDRESS DECODING :

The basic circuit used in address decoding is shown in Fig 18. This package provides a 1 of 8 decoding from 3 push-pull address bits with a controlling input gate for timing or logical functions. In the absence of a control or timing signal, the input gate is at -3.5V and all outputs are at -1 V. If the input gate goes to O V, 1 of the 8 outputs as decoded from the address bits will go to + 1 V. Fig. 19 shows how these packages are used to give the required 1 of 128 decoding from 7 address bits. The 16 outputs from the two packages providing the source decoding are connected to the OR diodes in the 12 source drivers. Each decoder output is therefore applied to 6 drivers and each driver has 8 input diodes. The appropriate decoding can be derived directly from Fig. 13. The Read and Write clocks are generated by the timing unit. The 16 outputs from the sink decoding packages are each connected to the input of a sink driver. One address bit applied in push-pull to the input gates allows the decoded output of only one package to rise to +1V so that only 1 of the 16 sinks is selected.

(4.1.3) SWITCH DESIGN :

In view of the impedance level of the loads, 250 mA and 20 V. back e.m.f., a transformer ratio of 1:3 was selected. Assuming perfect switch behaviour, this resulted in $\approx$7 V. back e.m.f. and 125 mA for each driver. Since each switch behaves as a current transformer, the magnetising current represents a loss which can vary with transformer, causing a variation in output current, or it can vary during the pulse, giving a droop in the output wave form. A maximum value of 40 mA, $\approx$5% of the total drive current,

was set to minimise these effects. To achieve low magnetising current with a small number of turns requires a magnetic circuit with a large cross-section and short path length. The transformers were therefore wound on 2 beads of A.1 ferrite, FX 1115, as shown in Fig. 20.

Assuming the load can be represented by a series R - L circuit, the flux change in the core during the pulse is given by

$$N \frac{d\phi}{dt} = i R + L \frac{di}{dt} + \frac{d\phi}{dt}$$

or $$N\Delta\phi = R\int^{t} idt + L.I + \phi c$$

where $\Delta\phi$ = change in flux in switch core

I = drive current (assumed 0 at t = 0)

ϕc = flux switched in the selected cores

R = the resistance of the drive line

L = the inductance of the drive line

(self inductance + effect of non-selected cores)

and N = the number of turns on the output winding of the switch core.

Measurements on one block of store and individual cores gave the following values for a 128 x 128 x 19 store.

ϕc = 0.5 V-μsec

R = 7.2 Ω → 1.5 x 7.2 x ¼ ≈ 3 V.-μsec.

$L I$ = 2 V. -μsec

$\therefore$ $N\Delta\phi$ = 5.5 V. -μsec

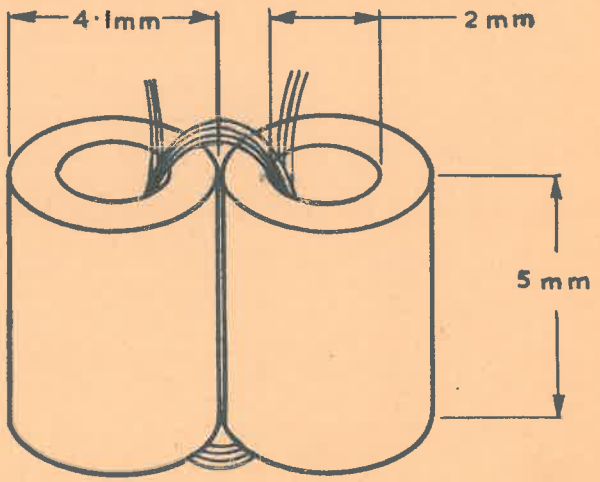
The c.s.a. of the magnetic path = $\frac{0.41-0.2}{2}$ .2.½

= 0.1 cm^2

B max = 3000 gauss

$\therefore$ $\Delta\phi$ max = 300 lines

= 3 V. -μsec



12 INPUT WINDINGS OF 8T.
1 OUTPUT WINDING OF 24 T.

FIG. 20 TRANSFORMER CONSTRUCTION

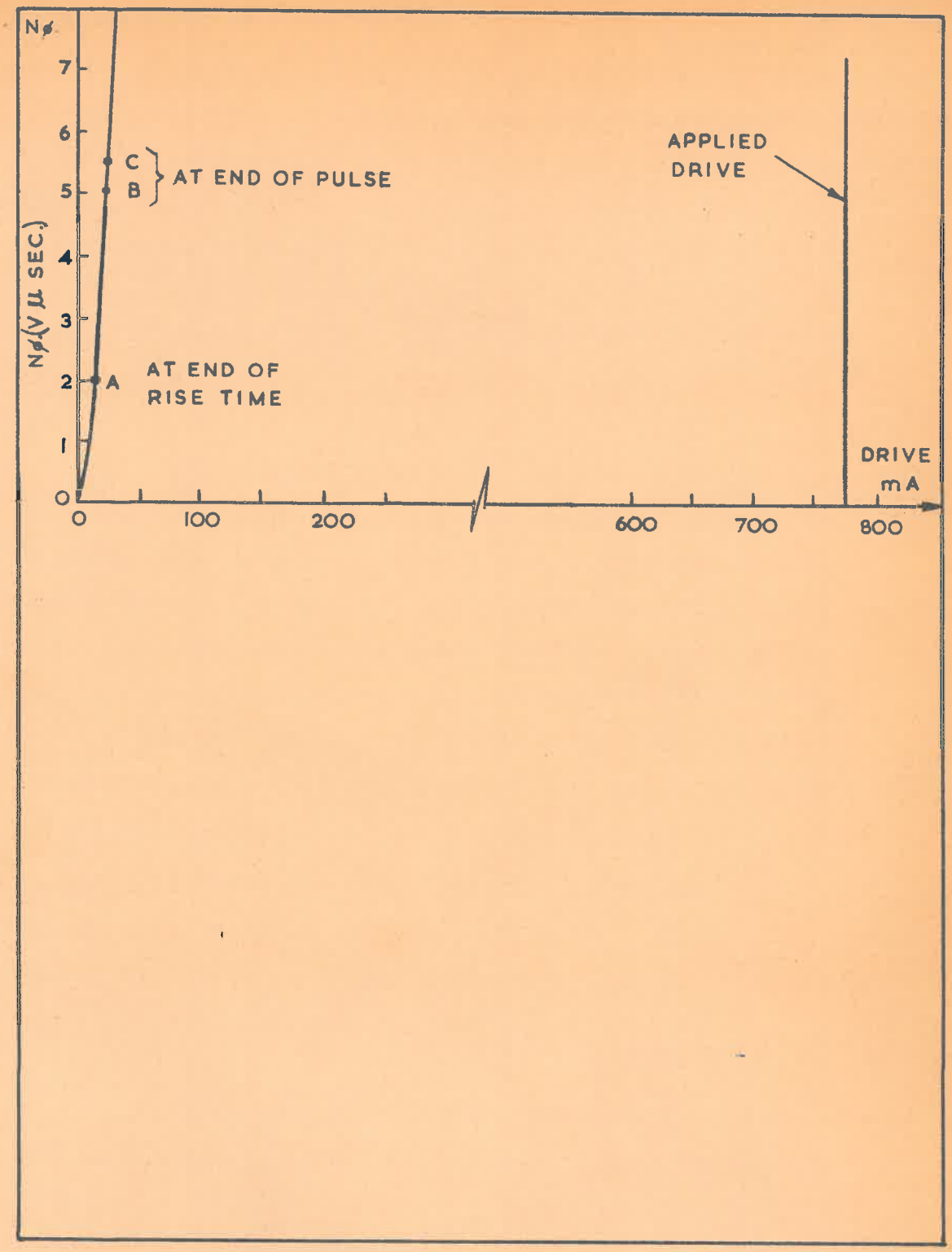


FIG. 21. OPERATING PATH OF LOAD SHARING SWITCH CORE

Even using the minimum N of 3, the flux available from the core is in excess of the required figure, allowing N to be selected for a suitable value of magnetising current. Using wire of 4 thou. diameter, 12 8 turn primaries and a 24 turn secondary could be easily accommodated on the beads. From the manufacturer's data, H at the end of the pulse is then $\approx$0.25 Oe, corresponding to a magnetising current of 25 mA, well within the desired limit.

The operating path of the switch core is shown in Fig 21. If the rise of the drive current is fast, no cores will switch and the effect of the resistance can be ignored. The core during the rise of the current waveform will therefore move up the hysteresis curve to a point where a quantity of flux $N\phi = L.Id$ has been transferred to the inductance of the drive lines. At the end of the rise time, the current is constant and the inductive term can be ignored. The core will then move up the hysteresis curve to satisfy the relation $N\frac{d\phi}{dt} = IR + \frac{d\phi c}{dt}$ These points plotted on Fig 21 indicate a droop of $\approx$ 1% in the current waveform. At the end of the pulse the flux OA stored in the half-selected cores is returned to the switch core and the remainder decays at a rate determined by the circuit time constant.

The transformers were initially would by simultaneously threading 15 windings of 8 turns each, the output winding being formed by connecting 3 in series. This reduced the wiring time considerably and minimised the possibility of errors in transformer ratio. The resulting close coupling between the windings gave a very low flux leakage and an excellent output waveform. It was found, however, that the capacity between the input and output winding increased the turn-off time of the sink driver due to the

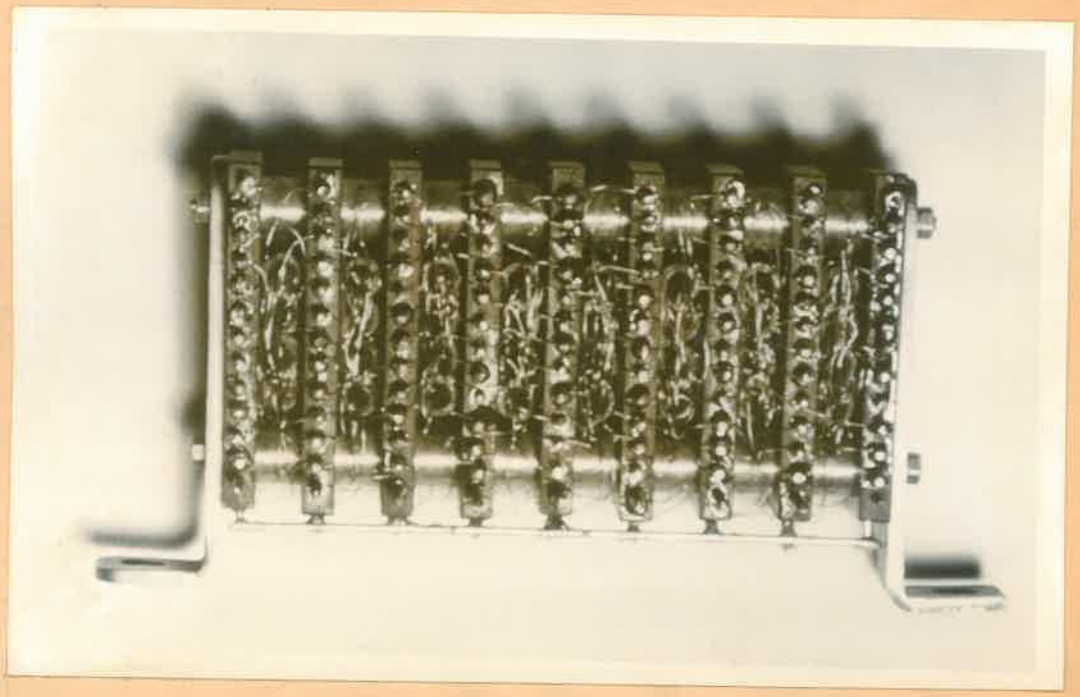


FIG. 22. A LOAD SHARING SWITCH ASSEMBLY

emitter circuit time constant. Winding the 24 turn secondary on first followed by the 12 primaries reduced this capacity from 500 to 150 p.f. and with a reduction in the emitter resistor of the sink circuit the performance was satisfactory. The construction of a switch is shown in Fig. 22. Each assembly contains two switches, one terminated down each side.

(4.2) THE INHIBIT DRIVERS :

The basic inhibit driver (Fig. 23) is very similar to the load-sharing switch driver. The input logic allows the driver to generate the required 265 mA output if both the Information input and the Inhibit clock are at O V or if the post-write-disturb clock is at O V. It will be noticed that this requires an inversion of "conventional" core operation, i.e. the core is set to '1' during read. A switching core therefore represents an '0' output instead of the conventional '1'.

As mentioned earlier the inhibit winding is split into 4 sections of 64 x 64 cores each. During either write or post-write-disturb it is only necessary to drive that section of the plane which contains the selected core. To avoid having 4 inhibit drivers per plane, a 1 of 4 steering circuit is attached to each driver as shown in Fig 24. By saturating the appropriate steering transistor, the inhibit current can be steered to the correct section of the inhibit winding. The diodes in the base circuit of the OC140[8] are necessary to prevent damping of the fall time of the inhibit current. At this time the collector voltage of the AUY10 and the unselected OC140[8] rises to $\approx$35 V, forward biassing the collector-base diode of the OC140[8]. The diodes prevent the current flow that would otherwise result. The 120 Ω resistor, and 0.01 μFd condenser are necessary to control the back e.m.f. generated by the inhibit winding.

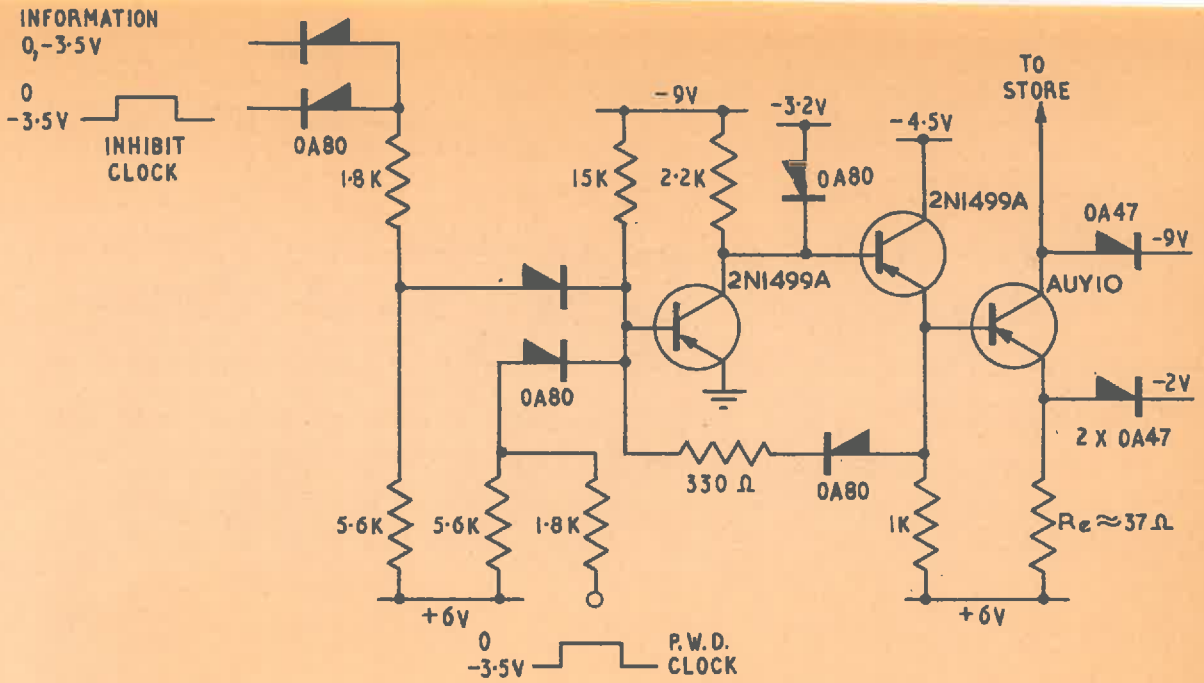


FIG. 23. INHIBIT DRIVER

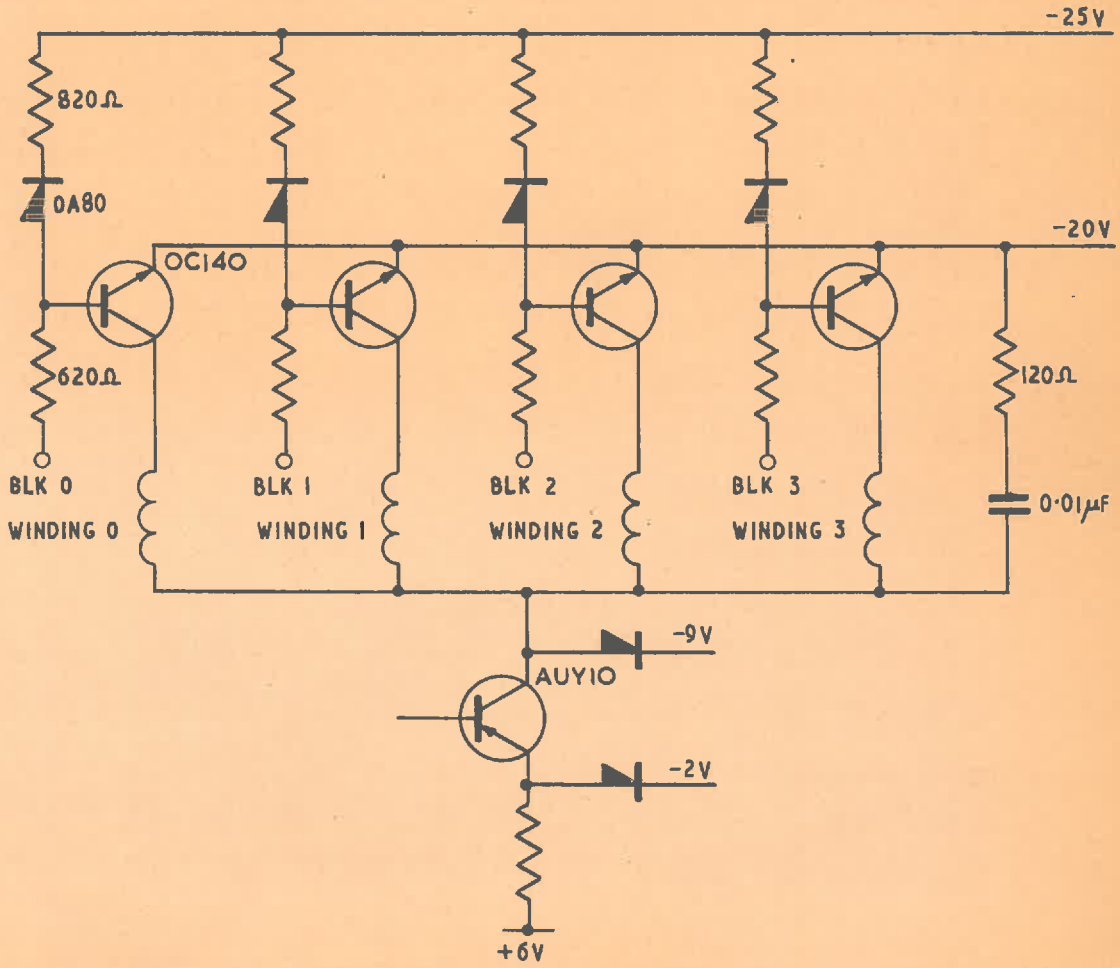


FIG. 24. STEERING CIRCUIT FOR INHIBIT CURRENT

The selection of the appropriate set of steering transistors is achieved by techniques identical to those described for the load-sharing and inhibit drivers. A 1 of 4 decoding from the 2 most significant address bits selects 1 of 4 possible BLK current switches to generate a 380 mA output. This is applied to the appropriate BLK input of each inhibit driver and due to the 620 Ω resistors in series, provides ≈ 20 mA to each of the 19 steering transistors. The steering transistors for the other 3 blocks have 5 V. reverse bias applied since an inactive current switch is very nearly open circuit.

(4.3) TEMPERATURE COMPENSATION :

As described above, temperature compensation was to be provided by variation of the drive currents. To provide the necessary information, tests were made on core characteristics at various temperatures. The hysteresis loops of the material (Fig. 25) were obtained by resetting the core to a defined state, negative saturation, and measuring the flux change resulting from various setting currents. The flux change was derived from the area of the voltage-time wave-form of a 10 turn output winding. The graphs of output voltages against drive current (Fig. 26) were obtained from the same waveforms.

The values of drive current for various temperatures can be derived directly from Fig 26. since a constant output voltage over the range of temperatures was required. This gives a temperature coefficient of -2.1 mA/^{o}C from the nominal 500 mA at 25^{o} C. With the current switching technique employed in the driving circuits, the drive currents can be adjusted by controlling the positive supply. Consequently the emitter resistors were

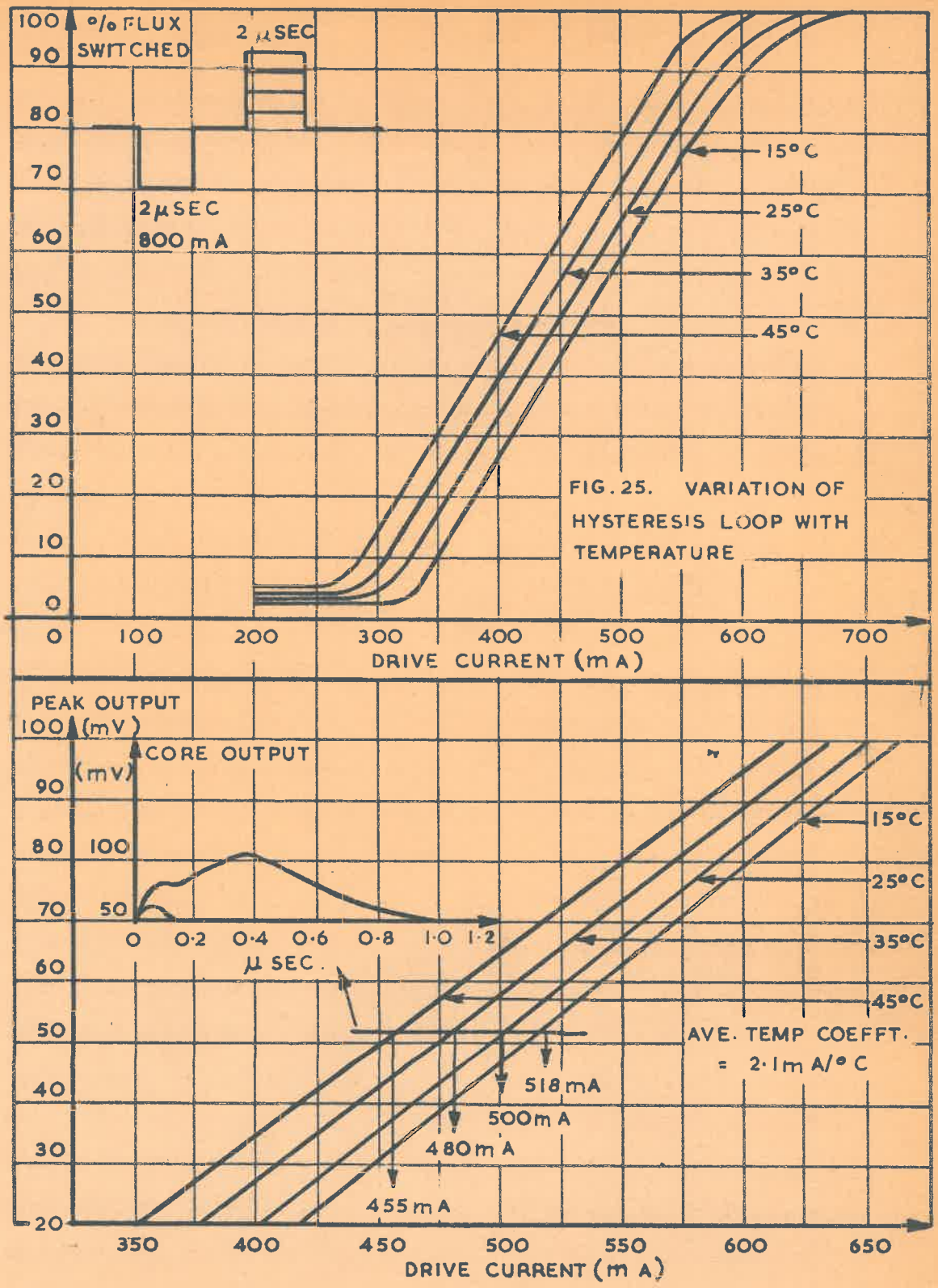


FIG. 25. VARIATION OF HYSTERESIS LOOP WITH TEMPERATURE

FIG. 26. CORE OUTPUT V DRIVE CURRENT FOR VARIOUS TEMPERATURES.

returned to a separate regulator, the voltage of which was varied by a thermistor network. The compensated core wave-forms shown as an inset in Fig. 26. were essentially constant over the range 5 - 50° C.

The information gained by these tests was also used to estimate the drive voltages. For repeated unidirectional drive pulses, conditions similar to those in a store using a post-write-disturb pulse, a reversible flux change of 7×10^{-4} V - μsec was measured. This gives total flux changes of 1.7 and 2.9 V - μsec for the X and Y and inhibit windings respectively. Driven with alternate positive and negative pulses, the half-select flux changes are much greater as discussed earlier. The flux change was measured to be 11×10^{-4} V - μsec. The storage planes were not available when the driving circuits were designed so values of 2 and 3 V - μsec based on these measurements were assumed in the design of the drivers. These proved to be quite close to the correct values.

(4.4) THE PERFORMANCE OF THE DRIVING CIRCUITS :

The circuit waveforms for a source driver and sink driver are shown in Figs. 27 and 28 resp. and a selection of switch outputs in Fig. 29.

The base current of the AUY10 current switch shows a considerable initial peak, being the current required to establish the base charge in this transistor. A low impedance source is therefore required if the turn-on delay of the driver is to be kept small. A similar peak occurs in the base current of the sink transistor when the 780 mA from the 6 active source drivers is

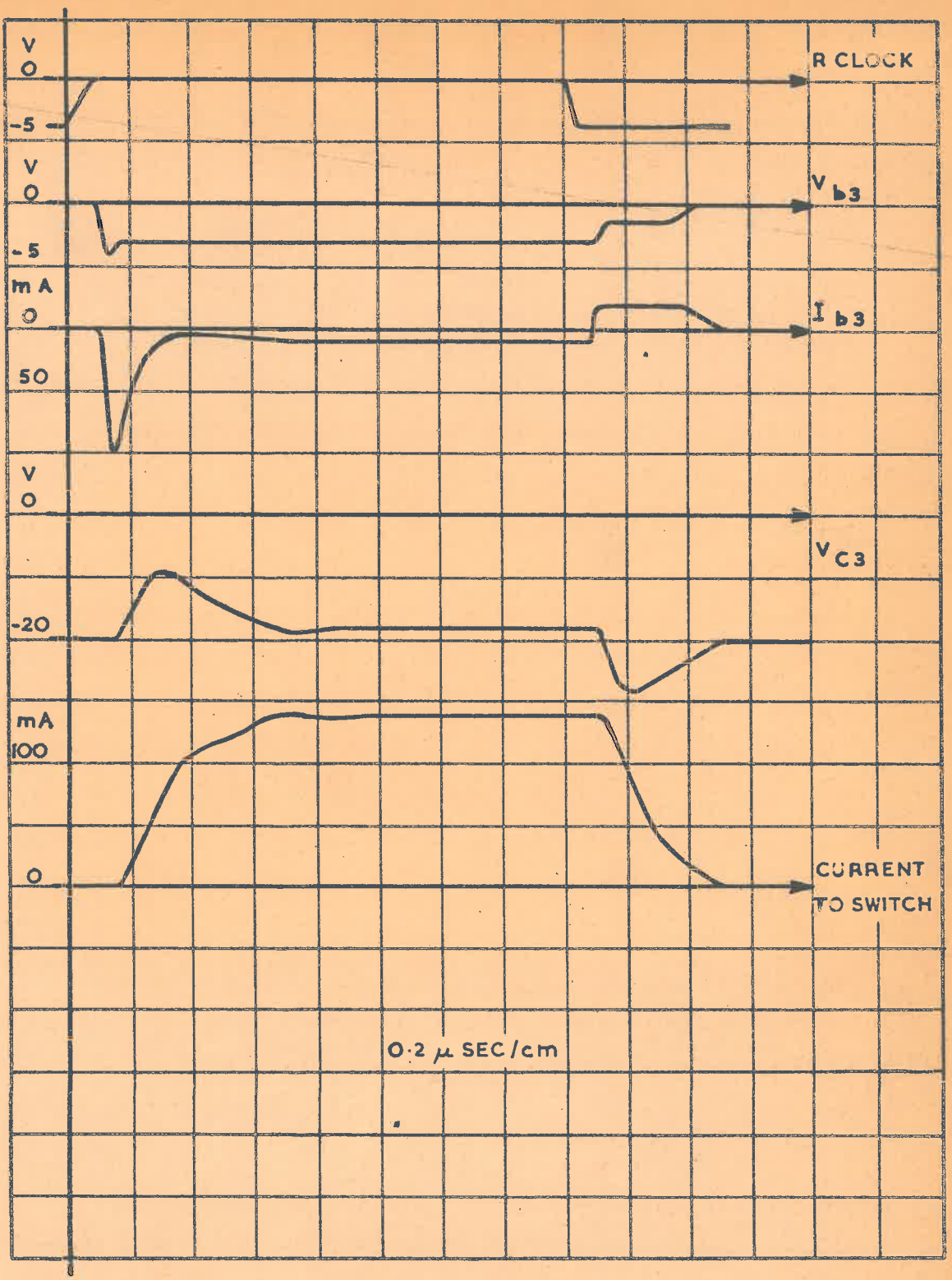


FIG. 27. CIRCUIT WAVEFORMS FOR SOURCE DRIVER

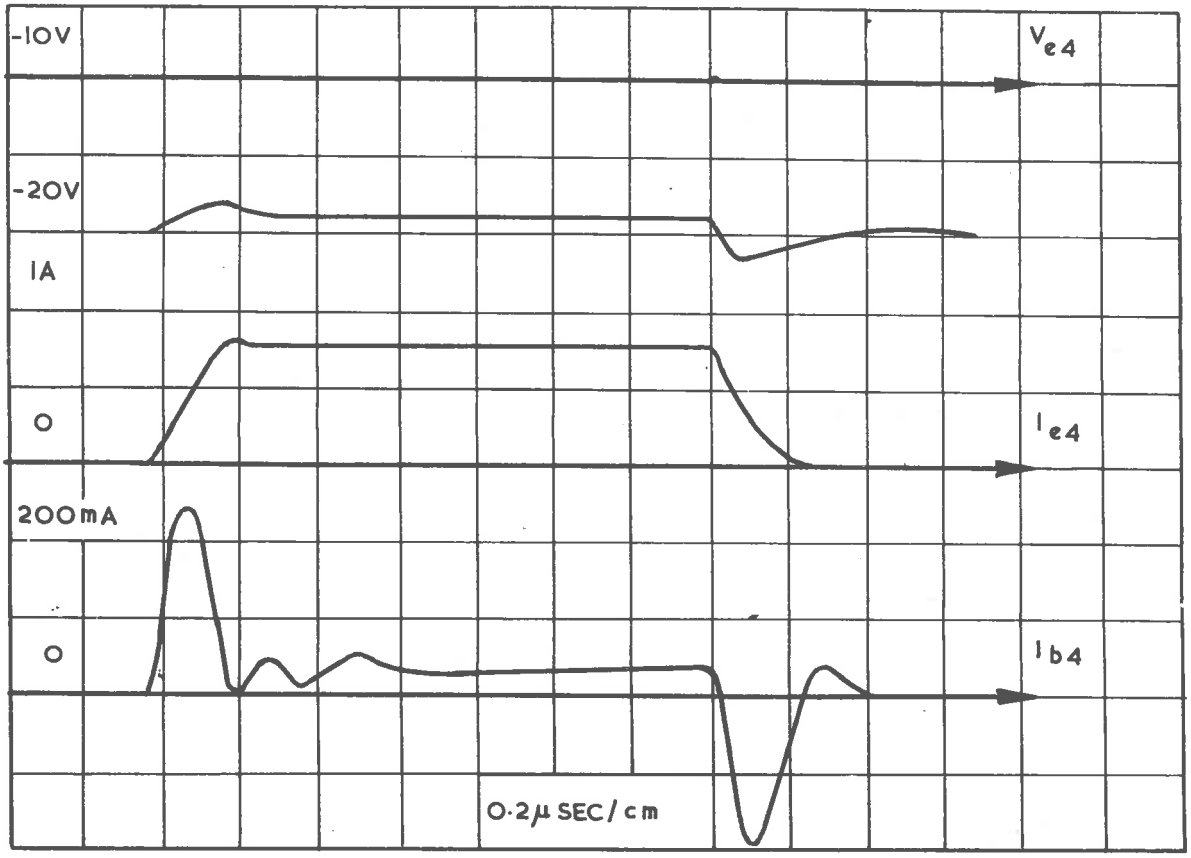


FIG. 28 CIRCUIT WAVEFORMS FOR SINK DRIVER

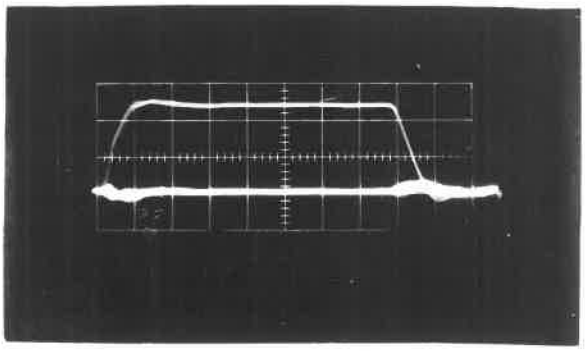


FIG. 29 SWITCH OUTPUT CURRENTS
100mA/cm 0·2μ SEC./cm

applied to the emitter. If the base circuit impedance is not very low, the output of the sink develops a positive going transient which is added to the plane voltage tending to drive the current switch into saturation. The saturated OC140 in the base circuit provided a sufficiently low impedance and being a symmetrical transistor could also handle the pulse of opposite polarity at the end of the drive pulse. The voltage applied to the current switch is rather greater than that due to the reflected drive voltage. Most of the increased voltage is due to the inductance of the non-selected transformers of the load-sharing switch or to variations in the transient response of the switch drivers.

The selected output has rise and fall times of approx. 150 n sec. and is delayed from the application of the R. clock by 200 nsec. The amplitude of the outputs varies by less than 5 mA from the nominal value. The spurious outputs occur almost entirely during the rise and fall of the drive currents and are due partly to mismatch in the transient response of the drivers and partly to coupling within the store and associated wiring. The maximum values observed were 25 mA "peak" and 5 mA "steady state". Neither is of sufficient magnitude to cause any trouble.

With the inductive load presented by the store, trouble was experienced with overshoot of the drive currents. This is apparently caused by base width modulation or the "Early Effect" in the current switches and is not apparent with a resistive load. Decreasing the damping resistor to control the overshoot increased the rise and fall times and gave a slight dip in the drive current due to the overshoot superimposed on the natural rise time of the waveform. With a short circuit across the switch output, the drive system is capable of generating pulses with rise and fall times of

40 nsec, limited by the response of the drivers. Each driver has to deliver a current of 140 mA, 130 mA to the switch and 10 mA to the damping resistor across the switch primaries. The switch losses, 30 mA can conveniently be classed as magnetising current. The sink driver must, therefore, handle a current of 780 mA.

The waveforms for the inhibit driver are very similar to those for the switch drivers except for the greater load. The waveforms are shown in Fig. 30. The action of the collector clamp diode can be seen during the rise of the current waveform. The diode regulates the rate of rise of the current through the inductance of the plane wiring so the transistor is kept out of saturation. The excess current is by-passed to the -9 V. supply. Without this diode the current through the inhibit winding has a 50 mA overshoot. The rise and fall of the inhibit current is approx. 350 nsec. with a delay of slightly more than 100 nsec. from the application of the inhibit clock. With the steering transistors placed as shown in Fig 24, a spurious current with a peak value of $\approx$ 80 mA is delivered to the capacity of the non-selected sections of the inhibit winding. Since this had no significant side effects, this current was allowed to remain.

During address selection a sink driver and the inhibit block switching are likely to be changed. The transient response of these circuits is shown in Fig 31. The long turn-off time of the sink driver is largely due to the time taken to bring the OC140 out of saturation, despite the drive conditions applied to this transistor, i.e. 10 mA turn-on and 20 mA turn-off. A similar effect is apparent in the inhibit steering, but in this case at least 3 µsec is available and speed is of little concern. The waveform for the inhibit steering is taken by observing the voltage on the output of

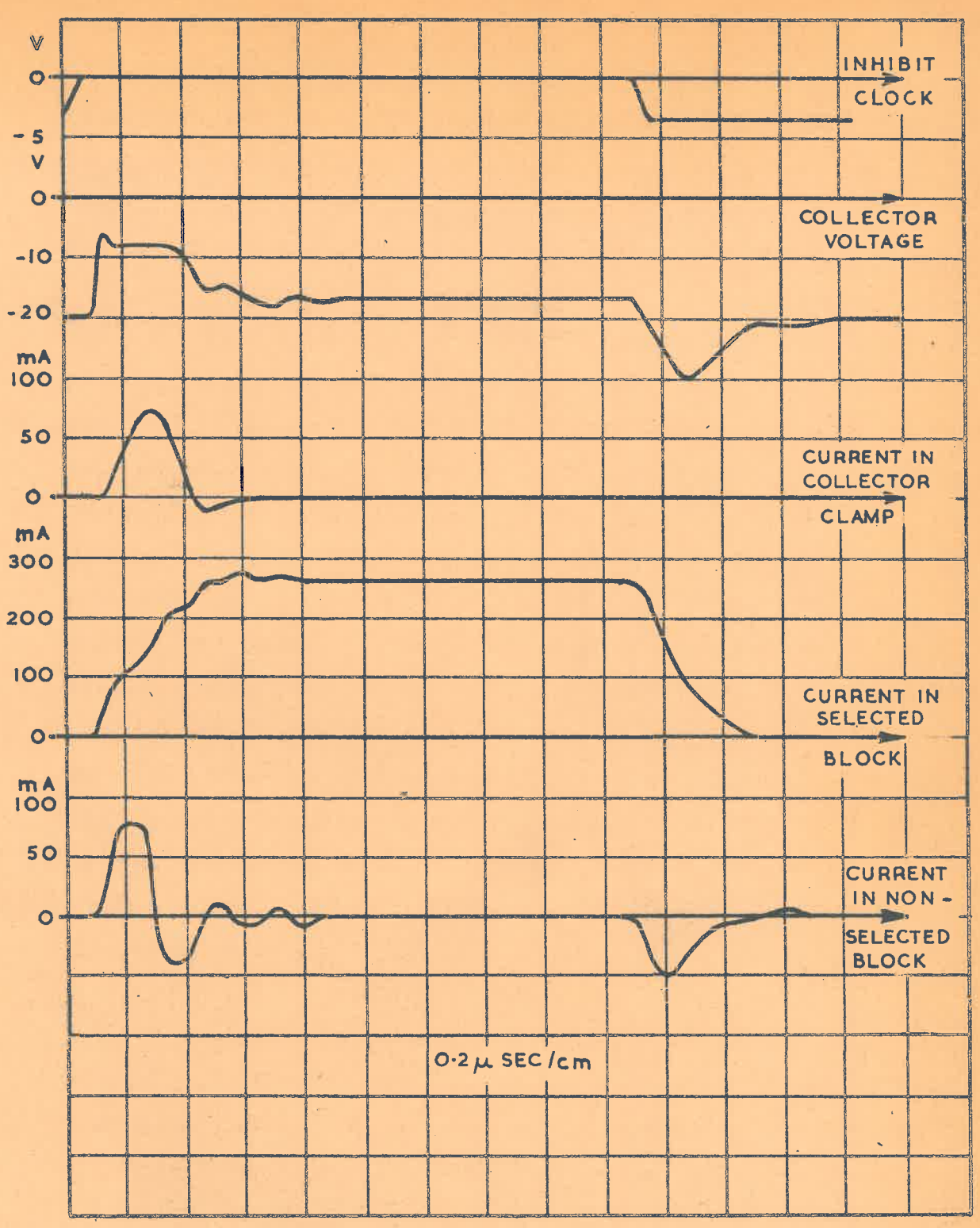


FIG. 30. CIRCUIT WAVEFORMS IN INHIBIT DRIVER

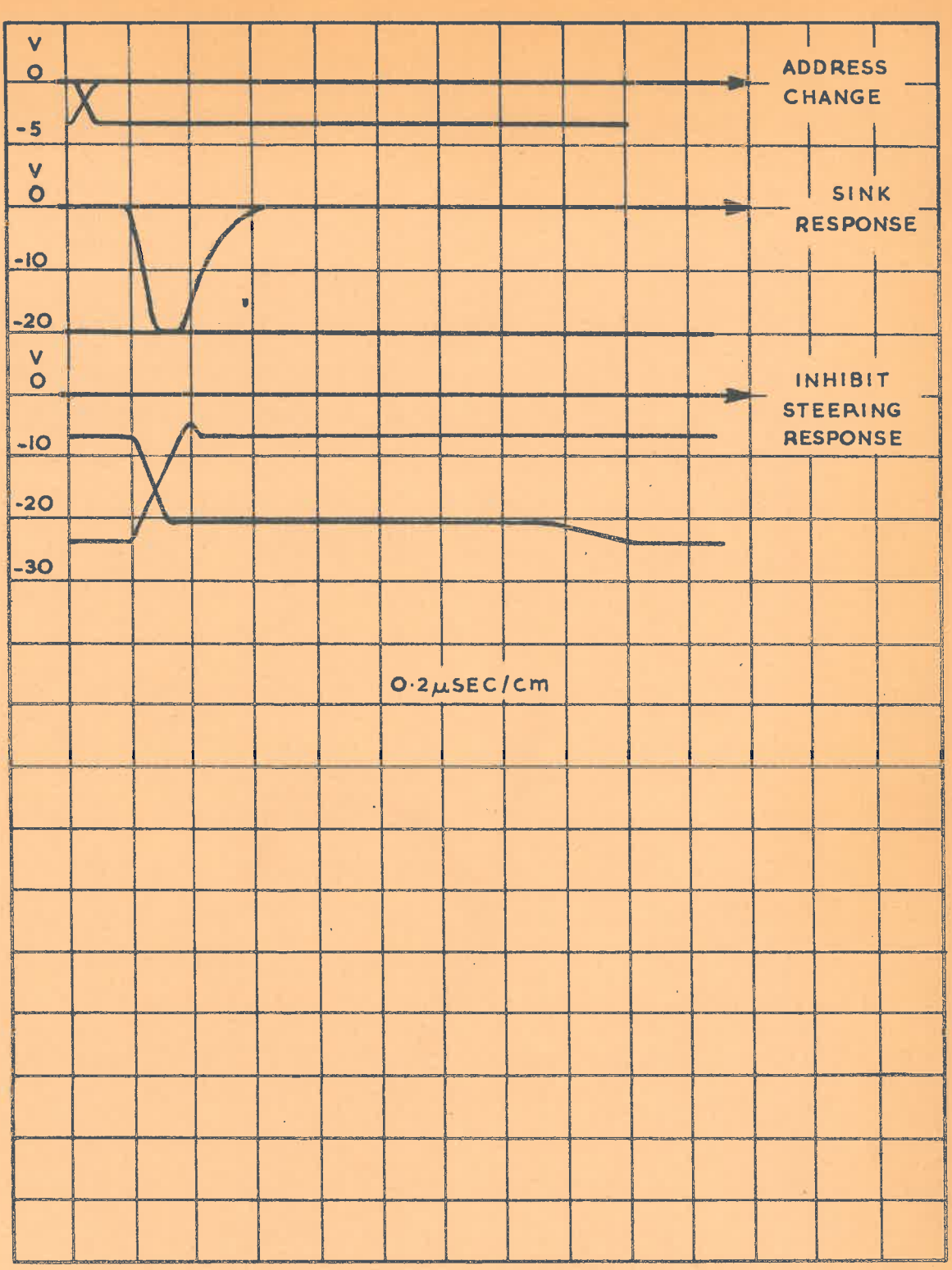


FIG. 31. TRANSIENT RESPONSE OF SINK AND INHIBIT STEERING CIRCUITS.

the BLK current switch. The response is therefore measured indirectly by noting the behaviour of the base-emitter diodes of the steering transistors.

(4.5) THE SENSE AMPLIFIER :

An inspection of the layout of the 4 blocks of store suggests that 2 sense amplifiers can handle the signals generated by the 4 sense windings by grouping into diagonal pairs. If the selected core is in block 0 (Fig 32), then the sense winding of block 3 produces no signal at all, so these two could share the same amplifier. Blocks 1 and 2 will generate a small signal during the rise and fall of the drive currents but should contribute no signal during the strobe interval. A similar result is obtained with the selected core in any position in the store.

The resulting sense amplifier is shown in Fig. 33. Each input is applied to a centre-tapped primary to eliminate the common-mode signals arising from capacitive coupling to the drive lines. The first stage uses the grounded base configuration largely for inpedance matching and amplifies the plane output to $\approx$ 2 V. The second stage provides the necessary power gain and some voltage gain to drive the rectifying network and threshold circuit on the base of T_3. The rectification is necessary to detect the bipolar output signal resulting from the diagonal sense winding of the planes. With the normal threshold setting, a switching core will produce a positive going signal of IV on the base of T_3, taking the output to -3·5V, the voltage level representing a '0'. The OA85 on the base of T_3 protects the transistor from the large signals generated by the inhibit current. A diode of high forward resistance is used to prevent excessive loading of T_2. The threshold level is

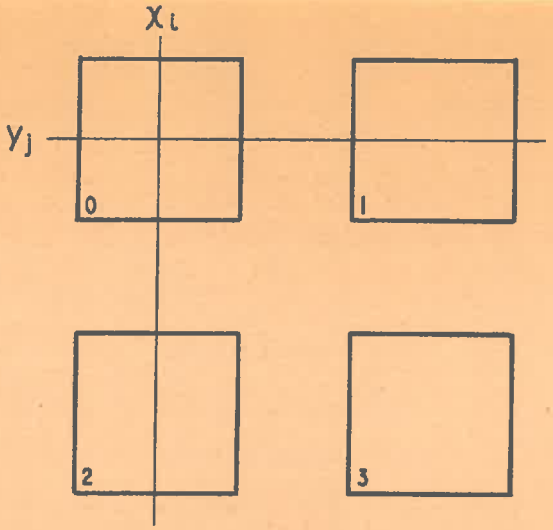


FIG. 32. ARRANGEMENT OF SENSE WINDINGS

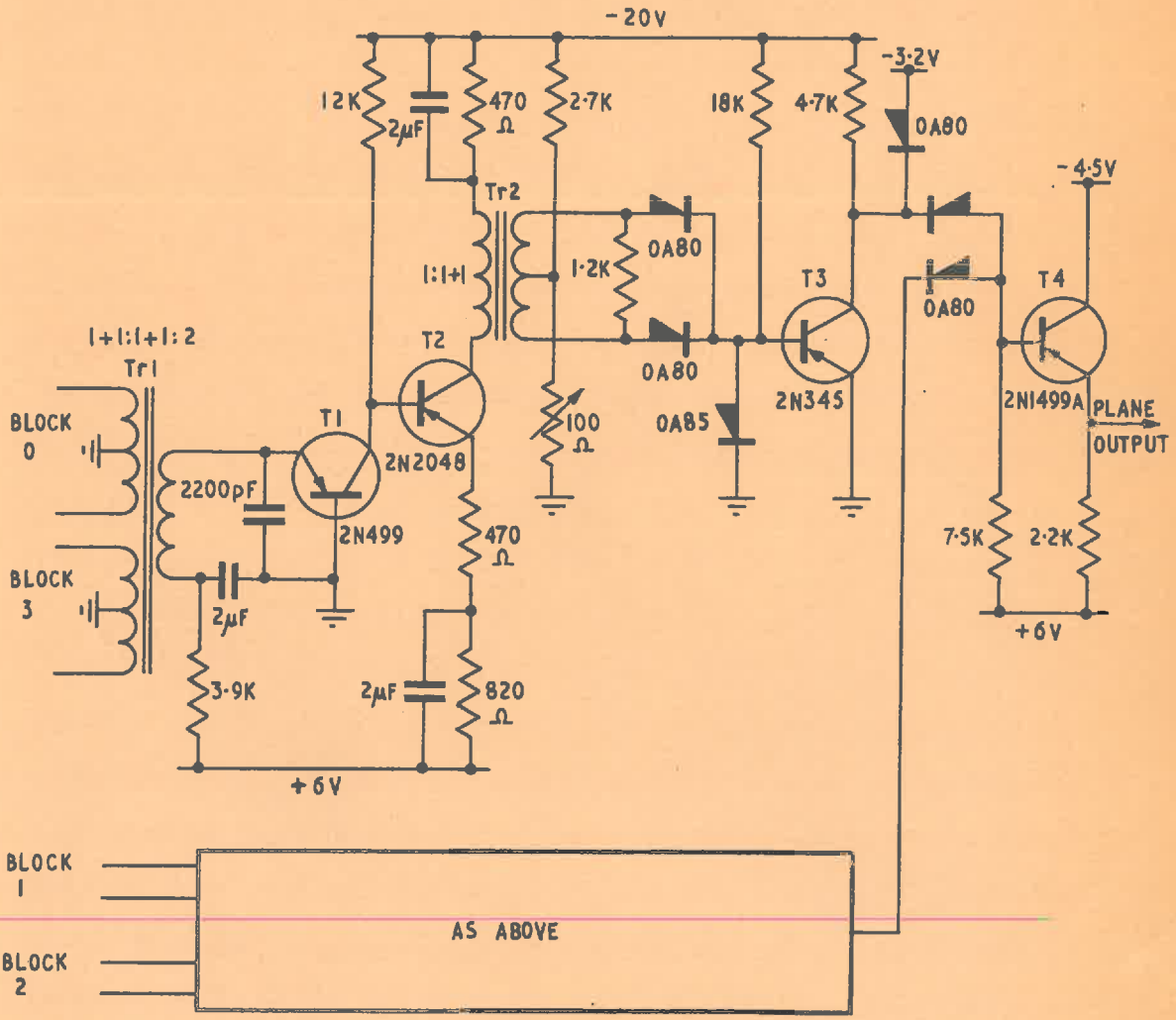


FIG. 33. SENSE AMPLIFIER

set by the 100Ω variable resistor which applies a reverse bias to the rectifying diodes. The gain can be adjusted over a sufficient range by choosing the appropriate value of load resistor on the secondary of Tr 2. The amplifier for blocks 1 and 2 is identical up to T_3. The outputs of the two amplifiers are then combined in a negative 'OR' gate to provide the plant output. The combination of grounded base and degenerate grounded emitter stages provides an amplifier with good high frequency response and a gain largely independent of transistor parameters. The 2N499 in the first stage was necessary to provide rapid recovery from the inhibit transient which can drive this stage into saturation.

No provision is made for strobing in the amplifier since this is achieved by sampling the amplifier output with the 0.15 μsec clock which inserts the information into the M register. The functional and circuit diagrams at one bit of this register, which is typical of all machine registers are shown in Fig. 34. The normal logical input is via the bidirectional gate. The appropriate input is selected by a signal from the control unit and the information is inserted in the flip-flop by applying a push-pull clock to the gate. The sense amplifier is one of the 4 inputs to the M register. A quiescent level of O V at the output of the sense amplifier is necessary to allow a bus connection system to be used for store extensions. The strobe circuit discussed below triggers the clock generator at the appropriate time, setting the state of the amplifier outputs into the M Register. This form of sensing does not make full use of the improved discrimination provided by the strobe technique since the reponse of the threshold transistor is too slow to faithfully follow the amplitude variations in the applied signal. However, the store output signals during the read period were clean

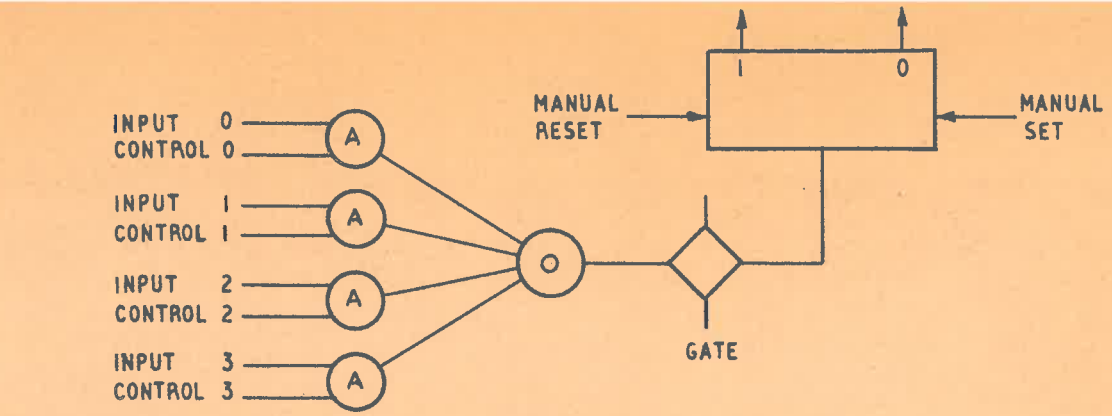


FIG. 34 (a) FUNCTIONAL CIRCUIT OF FLIP-FLOP

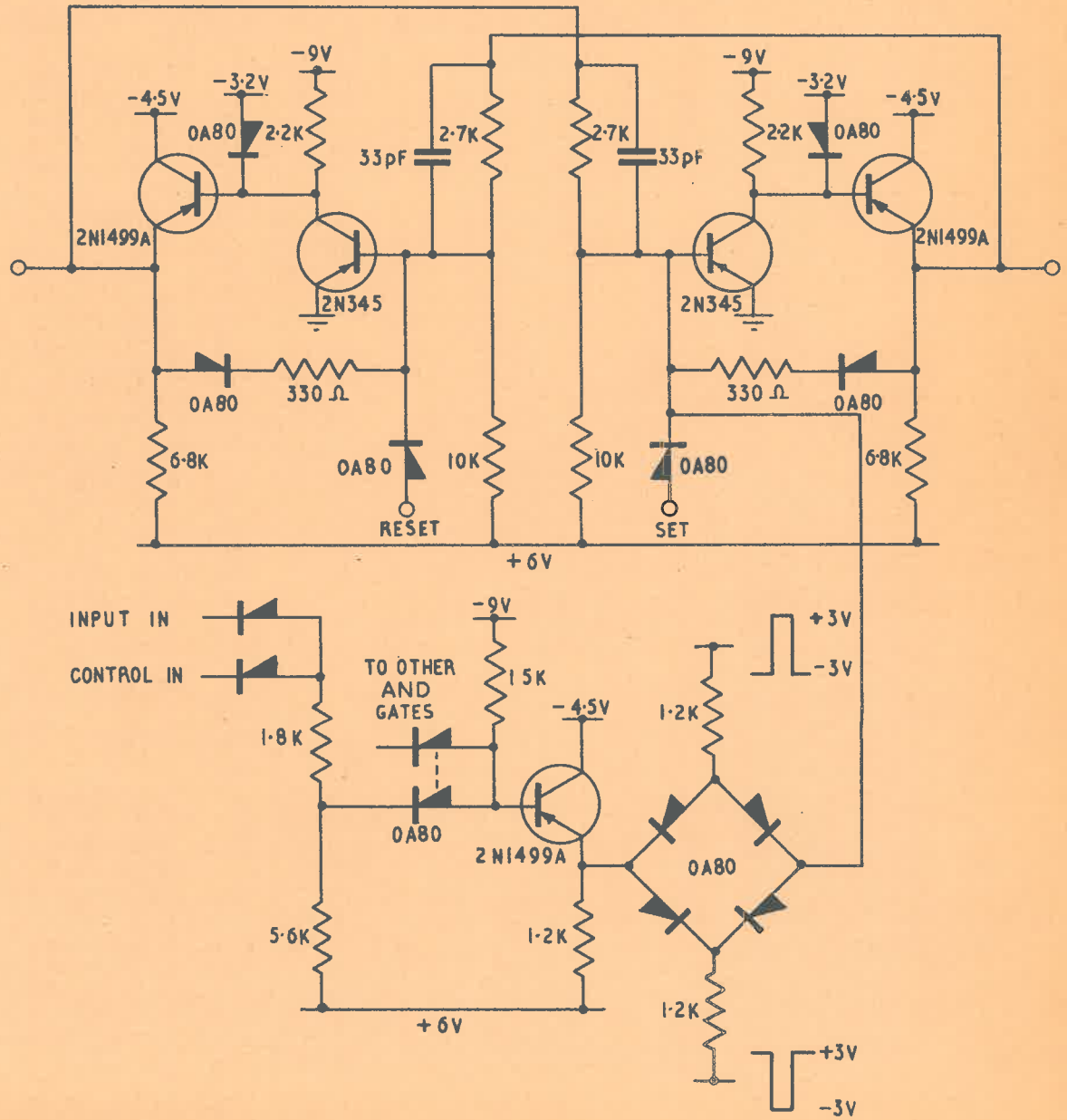


FIG. 34 (b) CIRCUIT OF FLIP-FLOP

enough to allow discrimination on the basis of signal amplitude and no trouble was experienced with this arrangement even with worst case signals. The circuit could be set to accept the signal from a faulty core, the output of which had half the amplitude and a much shorter duration than the normal signal.

With the method shown for coupling the two sections of sense winding to one amplifier, the load placed on the output of the sense winding is lower than the optimum, reducing the output signal and increasing the circuit time constant and consequently the duration of the noise coupled from the inhibit winding. The first effect can be overcome by increasing the amplifier gain and presented no difficulty. The second resulted in an undesirable increase in the amplifier recovery time although the required performance could still be achieved. The alternative series connection of the two sections was unsatisfactory since each section must be balanced to ground to achieve the required degree of common-mode noise rejection. The use of a separate pre-amplifier for each section would largely eliminate plane loading but since the circuit shown proved satisfactory, the extra hardware was not considered necessary.

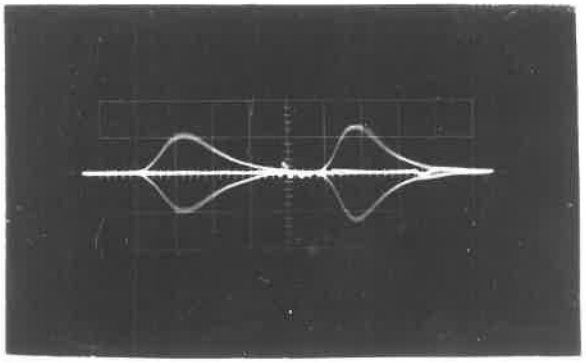
(4.6) THE PERFORMANCE OF THE SENSE AMPLIFIER :

Initially only blocks O and 1 of the store were installed. Each section of the sense amplifier therefore had only one input. To simulate the loading effects of the other plane the second input to the transformer was loaded by an equivalent impedance, a series combination of 12Ω & 15uH. All the results shown below were taken under these conditions and with the store cycled through all addresses in one block of store (4096 words).

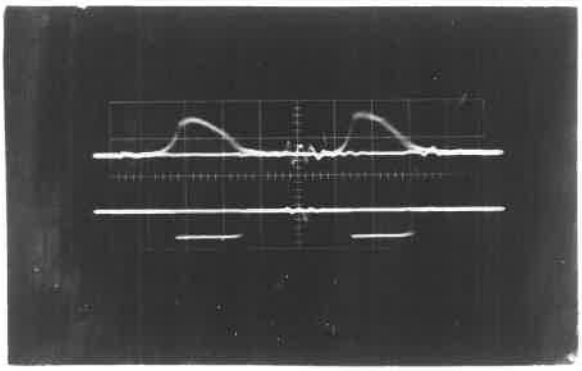
Typical waveforms through the sense amplifier for a '1' and '0' are shown in Fig. 35. The top trace is the collector voltage of the first transistor, showing the signals received from the store. The second trace is the voltage applied to the base of T_3. The O V Level coincides with the line crossing the waveform. The effective threshold is slightly negative since the base-emitter diode of T_3 does not have to be reverse biassed for the output to go to -3.5V. The voltage on the collector of T_3, the response of the threshold circuit and the amplifier output is shown in the bottom trace.

These waveforms were taken with patterns of all '1's and all '0's in the plane. Under these conditions, the inductive noise coupled from the drive windings to the read winding is minimised. The capacitively coupled noise has been virtually eliminated by the input circuit. A high frequency oscillation of $\approx$ 0.5 V. amplitude was present between one side of the balanced input and ground. This was largely rejected by the transformer and the remainder could be filtered by the condenser on the input to T_1 without significantly affecting the lower frequency core signal. The small oscillation due to the inhibit current could be ignored.

The worst noise occurs when every core linking the sense winding in a positive sense is in one state and every core linking in a negative sense is in the other. The wiring pattern of the sense winding was not known. However, the philosophy behind the pattern is that the sense wire threads equal numbers of cores on each X and Y line in a positive and negative sense. Similariy with the inhibit winding which is parallel to either the X or Y lines. A full select current applied to the sense winding should, therefore, set the cores into the states which corresponds to the worst case pattern. By setting the cores in this manner and reading the contents of the



(a) V_{c1} 2V/cm 0·5μSEC/cm



(b) V_{b3} 1V/cm 0·5μSEC./cm
(c) V_{c3} 5V/cm 0·5μSEC./cm

FIG. 35 WAVEFORMS THROUGH SENSE AMPLIFIER

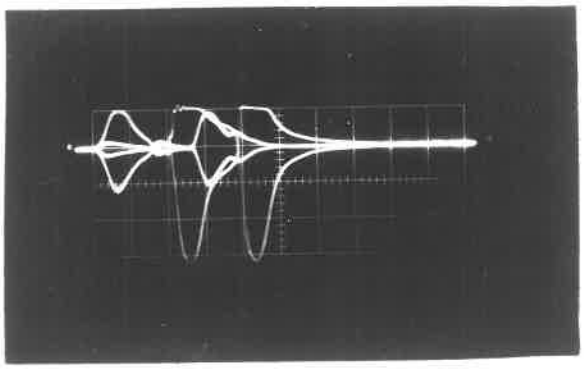
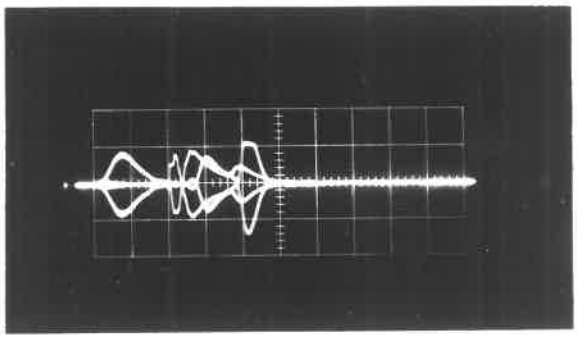
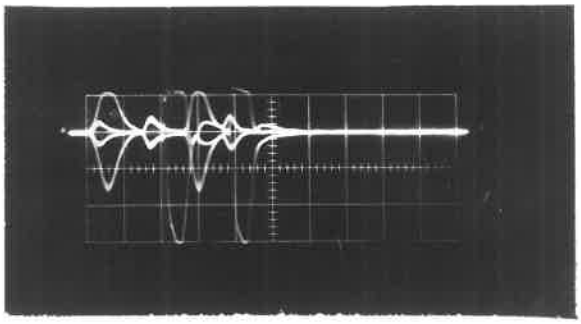


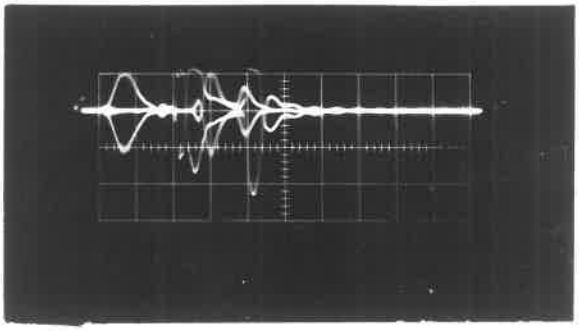
FIG. 36 PLANE OUTPUT UNDER WORST CASE CONDITIONS V_{c1} 2·5 V/cm 1μSEC/cm



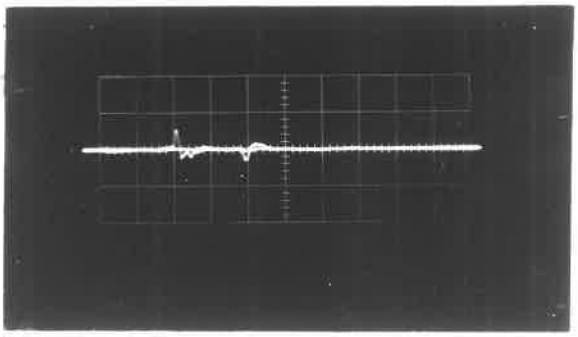
(a) UNEQUAL CURRENTS



(b) REDUCED PLANE LOADING EQUAL CURRENTS



(c) REDUCED PLANE LOADING UNEQUAL CURRENTS



(d) OUTPUT FROM NON-SELECTED BLOCK OF STORE

FIG. 37 WORST CASE NOISE VOLTAGES V_{C1} 2·5 V/cm
1 μ SEC/cm

store it was found that the worst case pattern could be derived from the address bits by the logical equation :

$$(A_6 A_7 + \overline{A_6}\,\overline{A_7})\,\overline{A_1} + (A_6\,\overline{A_7} + \overline{A_6}\,A_7)\,A_1.$$

where A_n = nth address bit.

This pattern was then written into the store as the address was cycled. The noise from this pattern is much greater, reducing the 1:0 discrimination and causing severe overloading in the amplifier. (Fig 36). The threshold could be increased to provide reliable sensing but due to the long time constant of the resulting inhibit transient, the recovery of the amplifier was too slow.

During marginal checking of the drive currents, it was noticed that the magnitude of the noise voltage was sensitive to variations in drive, in particular, to unbalance between the read and write currents. The optimum values determined experimentally were found to be :

Read current	-	490 mA
Write "	-	530 mA
Inhibit "	-	260 mA

To ensure that the core was fully reset by the reduced read current, the duration of the R clock was increased to 1.6 μsec. The noise under these conditions is greatly reduced (Fig 37(a)) giving improved discrimination and much faster amplifier recovery. The unbalance of drive current can conveniently be achieved by changing the -3.2V clamp voltage in the switch drivers. A flip-flop associated with the store in the control unit changes state at the appropriate times and provides the required voltage levels of-2.6 V and - 3.2 V. by means of two level shifting networks. With the drive currents adjusted in

this manner, the tolerance is slightly reduced but the performance proved to be quite satisfactory over a wide range of operating conditions. With the loading of the other plane removed and a 1 + 1 : 1 input transformer to reduce amplifier loading, the time constant of the sense winding is reduced and the inhibit noise is less troublesome. The resulting waveforms are shown in Figs. 37 (b) and (c) for equal and unbalanced drive currents respectively. In both cases the duration of the inhibit transient is significantly reduced and amplifier recovery occurs well within a 6 μsec cycle. The discrimination with unbalanced drive currents shows a marked improvement over that available with equal drive. It should be noted that noise conditions approaching those for the worst case pattern are unlikely to occur and typical random patterns of information produce signals similar to those shown in Fig. 35 for the ideal '1' and '0' case. In view of these waveforms the type of discrimination provided proved to be quite satisfactory.

The signal from a non-selected block of store is shown in Fig. 37 (d) for unequal drive currents with a worst case pattern established in the plane. This is due to the spurious current in the inhibit winding and has no effect on discrimination during read. The amplifier showed no significant drift of threshold due to repeated signals of the same polarity or any side effects from the inhibit noise even with equal drive currents. Experience with the store indicated that the post-write-disturb pulse could be eliminated allowing a further 0.5 μsec for amplifier recovery. This decision is subject to more complete testing so the small amount of hardware involved was retained.

(4.7) THE STROBE CIRCUIT :

The strobe signal is derived from the output of a 4 x 4

matrix inserted in the earthy end of the drive lines and operated by the drive currents. If the output due to the read currents is of sufficient amplitude, T_2 is switched and the blocking oscillator is triggered, generating an output of 0.4 μsec duration. This signal then triggers the clock on the M register, strobing the store outputs. The strobe output is included in the logical equations of the timing loop. The time of occurrence of the main store strobe is compared with that for the register store which is independently generated by the same technique. Insufficient overlap or failure of one or both strobes will cause the timing loop and hence the computer to stop immediately. The R clock is used as a gate on the output of the strobe plane to safeguard against possible spurious outputs. A small strobe matrix rather than a single core was necessary because of the poorly defined waveform of the common return current. This was due to cross-coupling within the store and external wiring and, to a lesser extent, spurious outputs from the driving switch. Splitting the drive lines into groups of 32 provided acceptable drive currents although the waveform was still poor, showing a considerable oscillation. Further subdivision gave little improvement unless a complete strobe plane was used, but this additional expense was not warranted.

The waveforms through the strobe circuit are shown in Fig. 39. The plane output is not particularly clean due to the drive current waveform but a satisfactory strobe can be generated.

(4.8) THE TIMING CIRCUITS :

For convenience of testing, each store has a separate set of timing generators. These receive two signals from the control unit of the computer, W_2 to initiate read and W_4 to initiate write. The block diagram and circuit details of the timing circuits

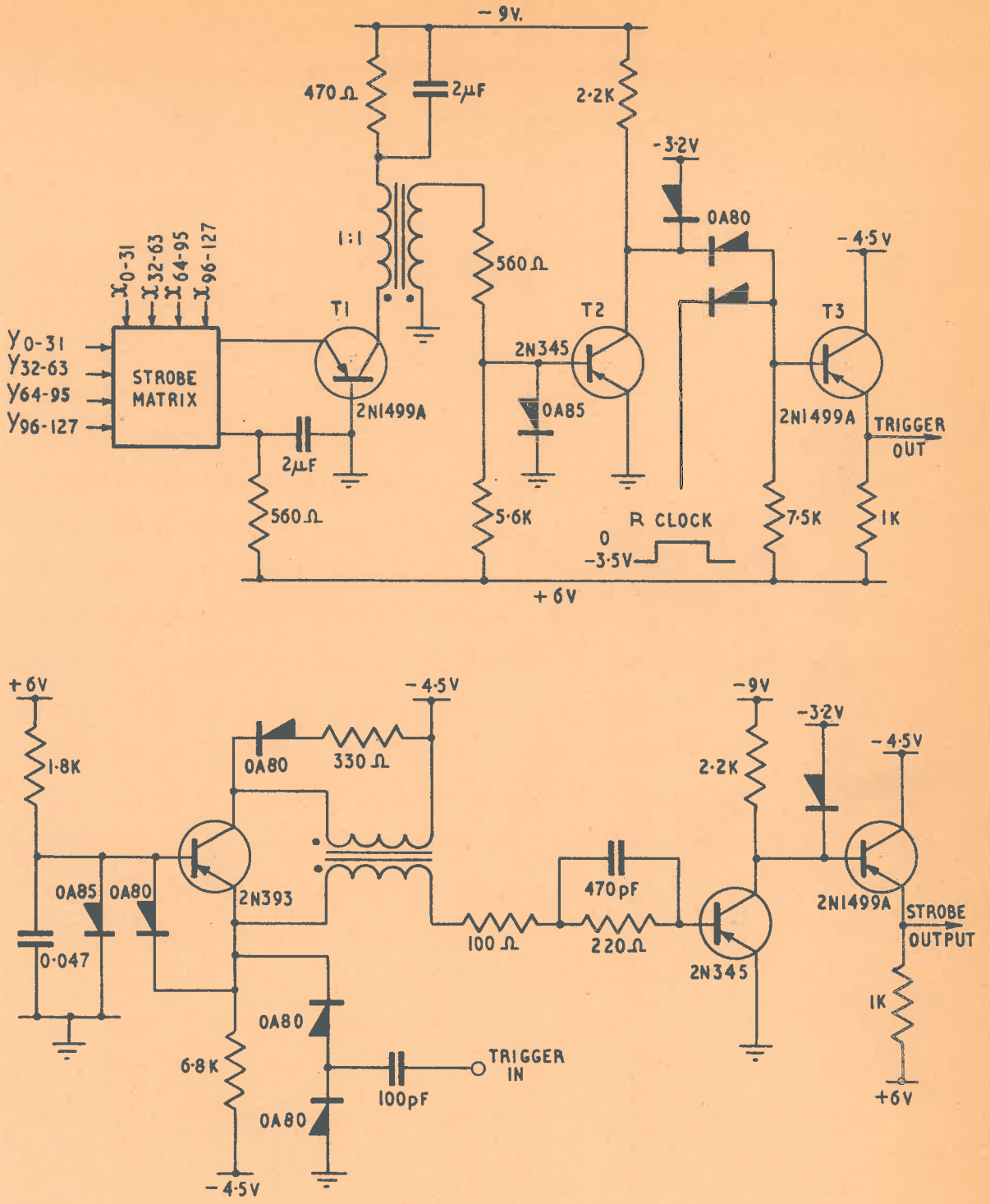


FIG. 38. THE STROBE CIRCUIT

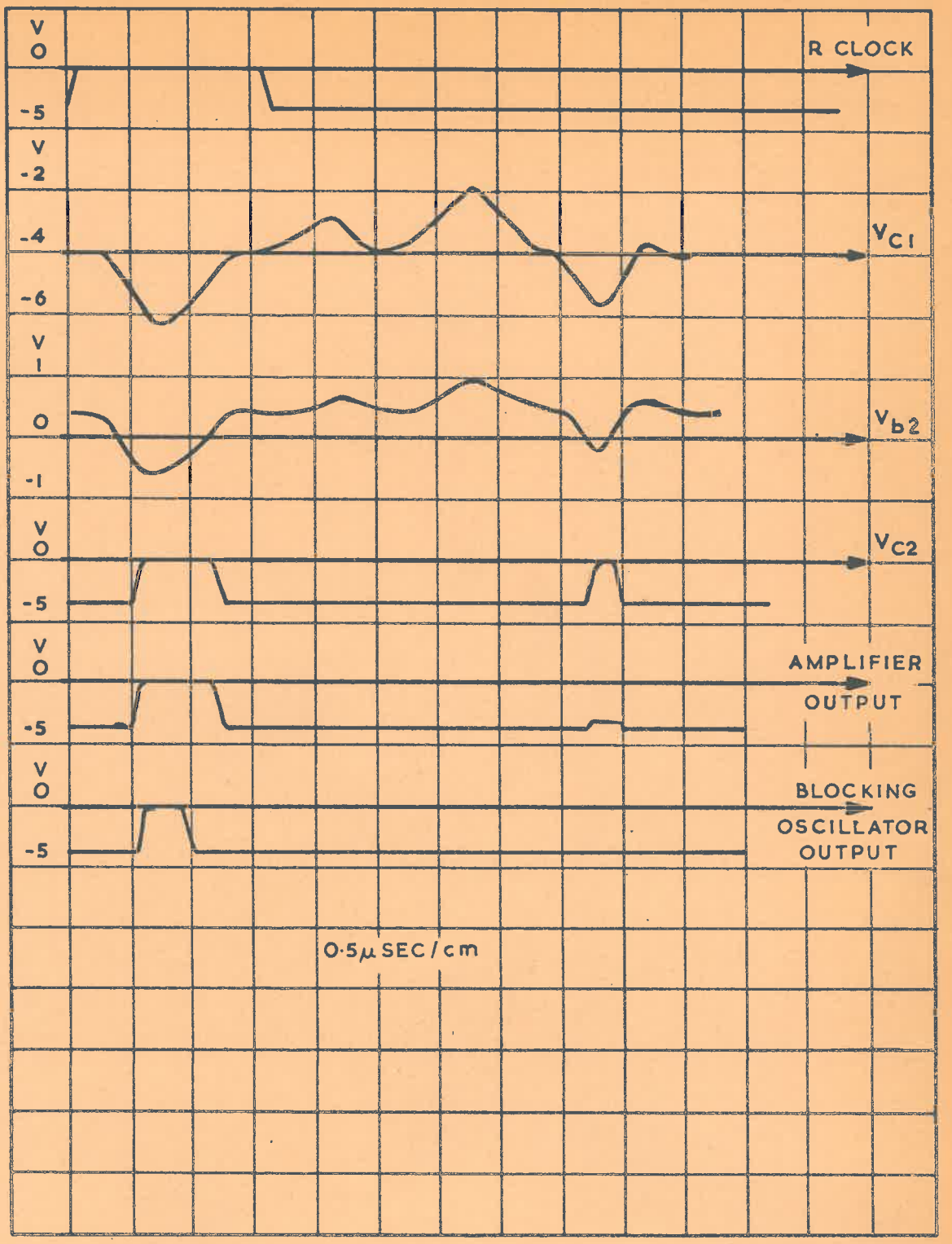


FIG. 39. WAVEFORMS THROUGH THE STROBE CIRCUIT

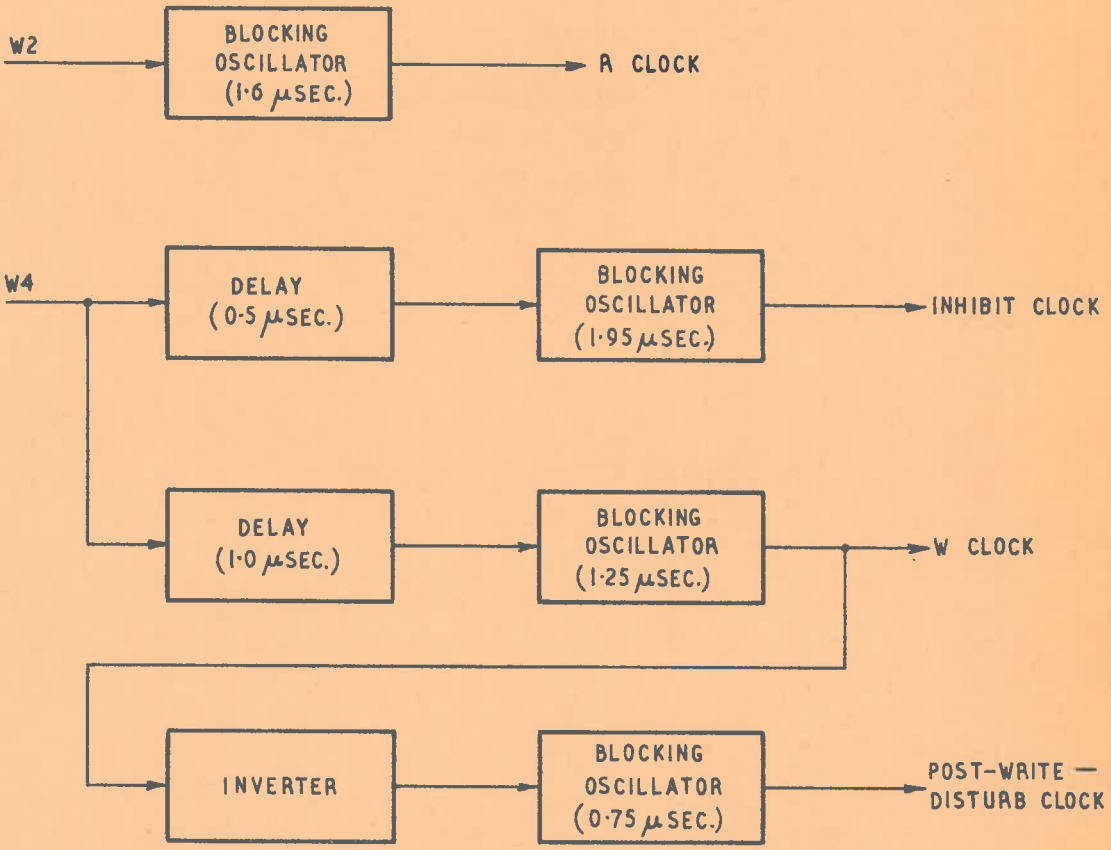
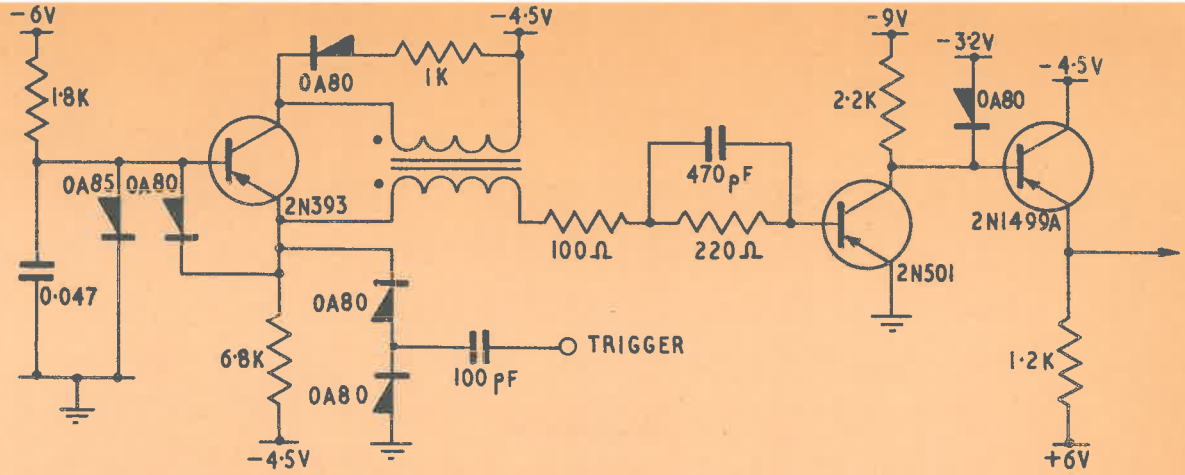
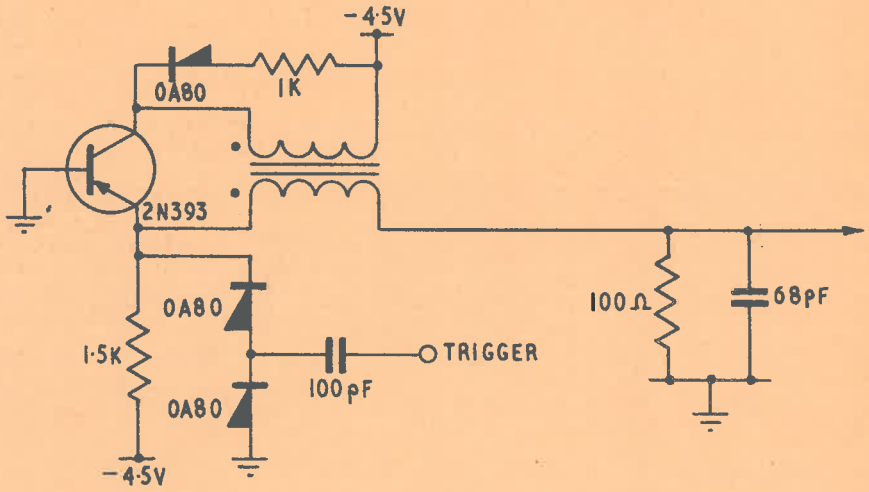


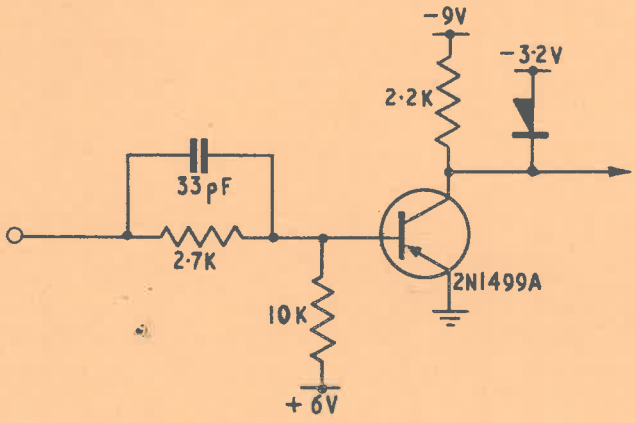
FIG. 40. BLOCK DIAGRAM OF TIMING CIRCUITS



(i) BLOCKING OSCILLATOR



(ii) DELAY



(iii) INVERTER

FIG. 41. CIRCUIT DETAILS OF TIMING CIRCUITS

are shown in Figs. 40 and 41.

(4.9) THE COMPLETE STORE:

The block diagram and timing for the complete store are shown in Figs. 42 and 43. Due to the structure of the computer, the input, output and address registers are part of the general hardware and are not therefore shown in the diagram.

Operating on the nominal cycle, all voltages and currents could be varied by at least 10% without a store failure. The most critical voltages are - 20 V. and - 25 V. due mainly to an increase in the turn off time of the sink driver if the difference between these two voltages becomes too small. To facilitate store checking the - 25 V. and + 6 V. supplies have switched marginal check positions giving the required 10% marginal voltages. The cycle time of 6 μsec is rather conservative for a core which switches in less than 1 μsec. This is due partly to the restrictions of general machine timing, and partly to the provision of substantial time margins within the store cycle. By using an improved sink circuit, separate pre-amplifiers for each section of the sense winding and less conservative timing margins, the store cycle could probably be reduced to 4.5 μsec without a significant reduction in reliability.

The store including regulators but not the static registers is contained in a frame ≈ 3' x 2' x 6" (Fig. 44) with space allowed for a possible extension to a 24 bit half word. All low level circuits are assembled in packages ≈ 5⅓" x 2¼" x 1" and the high power stages, the AUY10 current switches, are grouped together and mounted directly on sections of heat sink which are treated as a plug - in unit. Approximately 600 transistors, 500 gold bonded diodes (OA47), and 1200 point contact diodes (mainly OA80) are

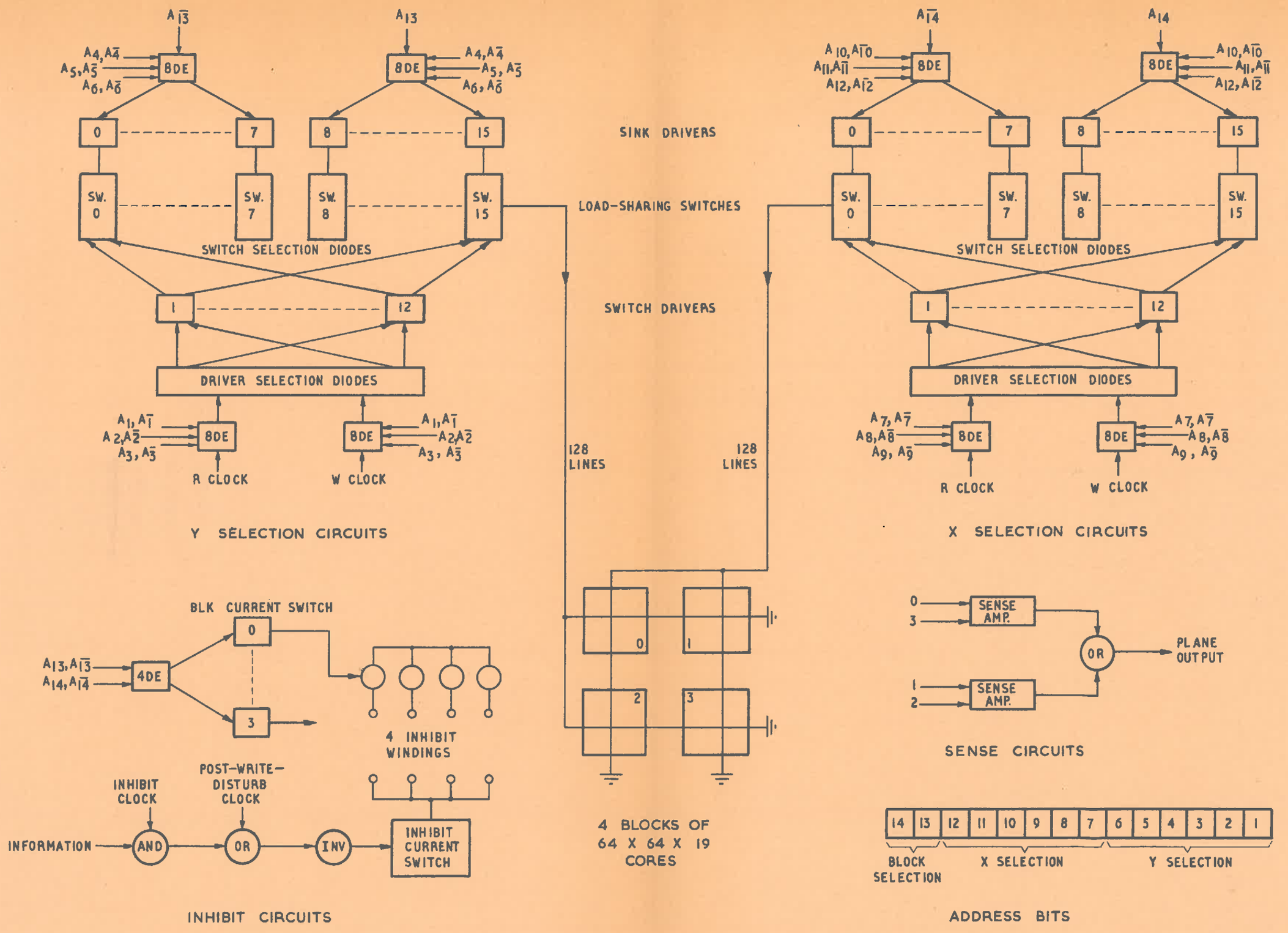


FIG. 42. BLOCK DIAGRAM OF THE MAIN CORE STORE

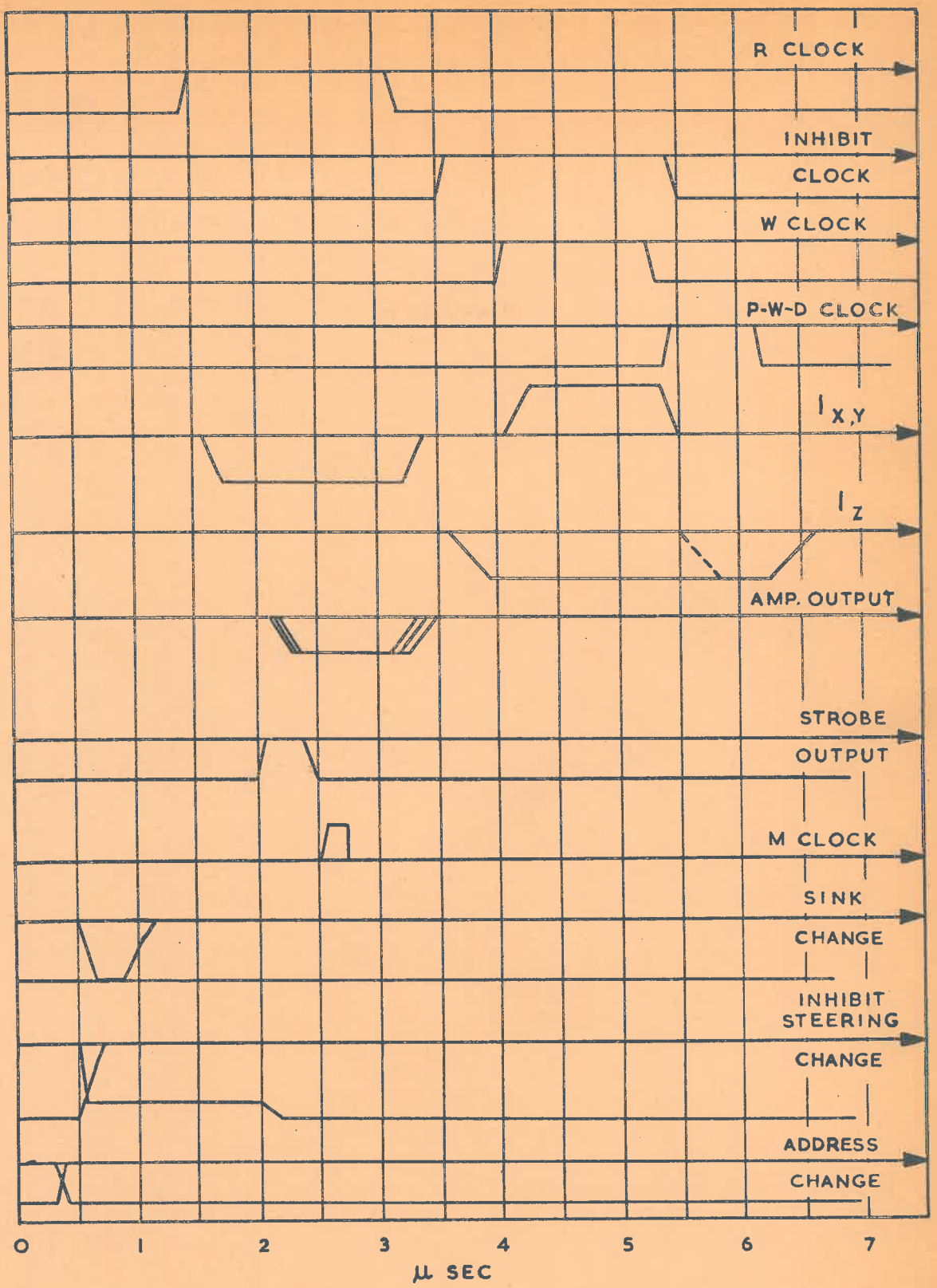
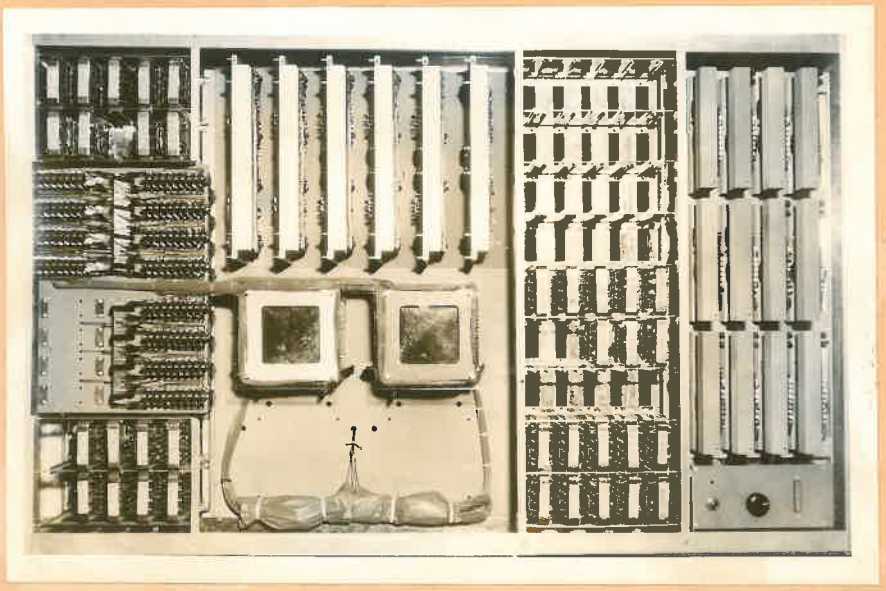


FIG. 43. TIMING OF STORE CYCLE



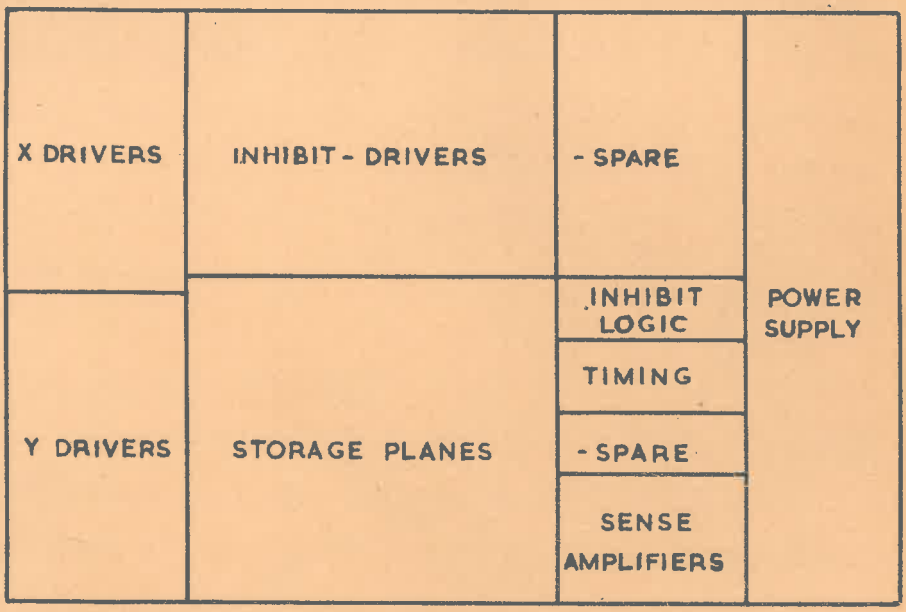


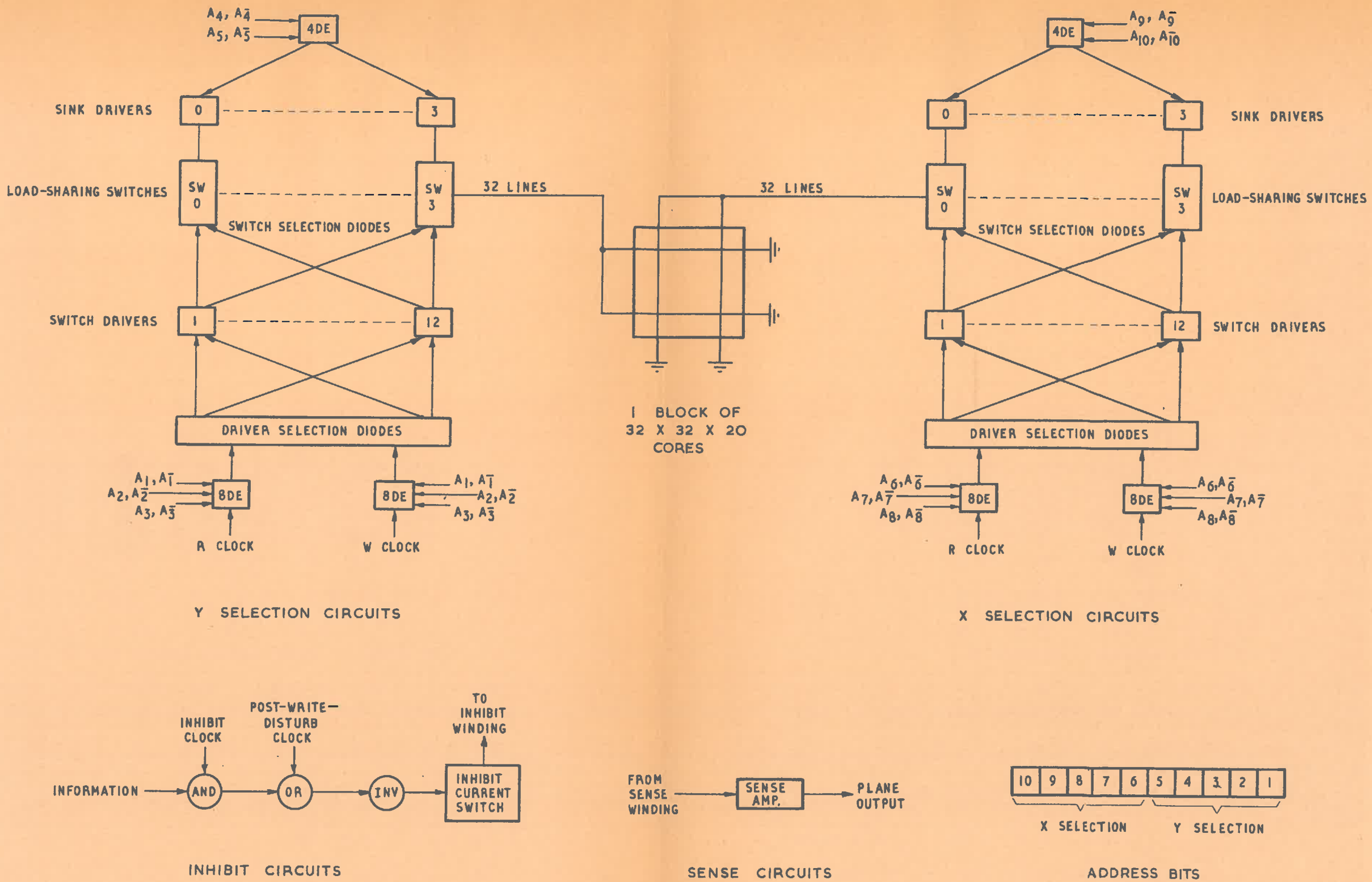
FIG. 44. MECHANICAL ASSEMBLY OF THE MAIN STORE

used. Only 80 transistors, the AUY10[S] have a dissipation in excess of 100 mW. The average dissipation in these transistors varies between 0.75 W and 1.5 W although the peak dissipation can be considerably higher. Sufficient heat sink is provided to limit temperature rise to a maximum of 20° C. above ambient under normal operating conditions. The total power consumption of the store is approx. 150 W. The packages shown in Fig. 3. are used in the core stores. These are a sense amplifier package (4 amplifiers) an address decoding package and an inhibit heat sink unit with 4 current switches.

The total cost of the packaged store hardware was ≈ £1500 including the cost of the switches. These were ≈ £10 each, about the same as a driver. By the completion of the project, the cost of the planes had fallen to £1200 for a 64 x 64 x 19 stack and £2,800 for a 128 x 128 x 19 stack. These figures emphasise the need for economy in circuit design since the associated electronics still account for a considerable fraction of the total cost of the storage system. If the cost of the static registers and the mechanical assembly of the store were included, the electronics would represent ≈ 45% of the total cost.

(5) THE REGISTER STORE :

The circuit techniques of this store are so similar to those of the main store that little comment is required. A block diagram of the store is shown in Fig 45. The driving circuits are identical except that the block selection on the inhibit drivers is not required. These circuits are, therefore, as shown for the basic inhibit driver of Fig 23. The sense amplifier also differs slightly since each plane has only one sense winding. The input transformer has only one centre-tapped primary and a 1 + 1 : 1 ratio is used. Due to the smaller plane size and the reduced loading on the sense winding, the inhibit noise did not prove to be sig-



Y SELECTION CIRCUITS

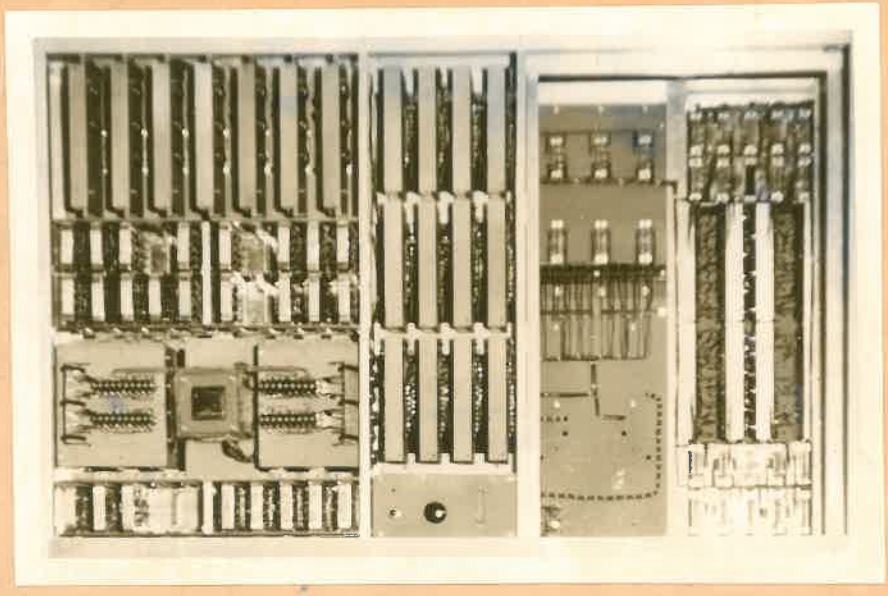
X SELECTION CIRCUITS

INHIBIT CIRCUITS

SENSE CIRCUITS

ADDRESS BITS

FIG. 45. BLOCK DIAGRAM OF REGISTER STORE



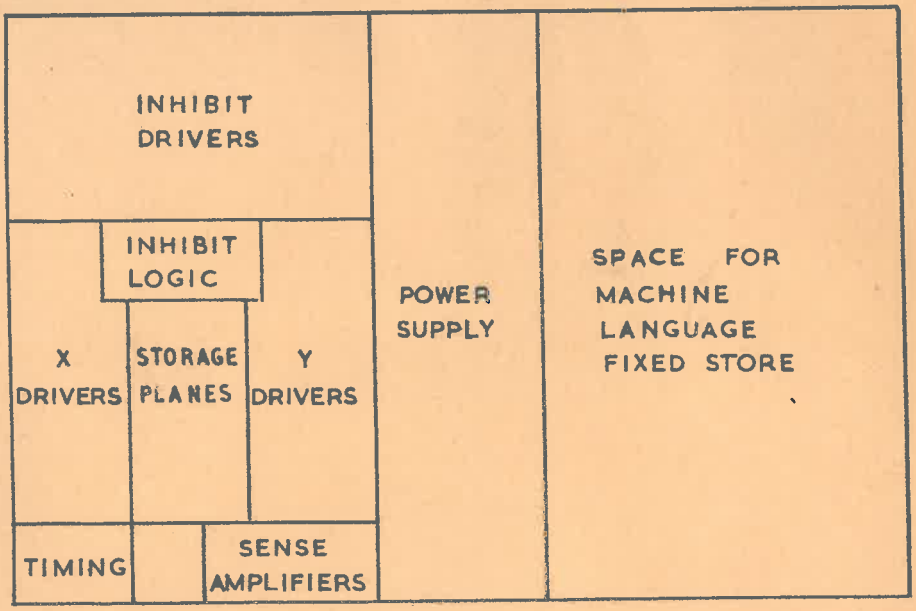


FIG. 46 MECHANICAL LAYOUT OF THE REGISTER STORE

nificant. Consequently, the unbalance of drive currents was not found to be necessary.

The register store is contained in a frame with the same dimension as that employed for the main store, but requires only 60% of the space. The remaining section of this frame will hold the machine language fixed store. The mechanical assembly of the store is shown in Fig 46. The register store used 300 transistors, 250 OA 47[8] and 750 OA80[8], i.e. slightly more than half the number required for the main store which had almost 16 times the capacity. This shows the relative inefficiency of small store capacities. The cost per bit is more than 4 times that of the main store.

SECTION C

THE FIXED STORAGE UNITS

(1) THE CHOICE OF A SUITABLE STORAGE MEDIUM.

The basic configuration of a fixed storage system as shown in Fig. 47 is very similar to that of a conventional store. The difference lies in the storage array. Instead of retaining information by the state of a bi-stable element such as a core, the information is contained as a pattern of coupling between the input or drive lines and the output i.e. the storage is based on the geometry of the system. The store is therefore non-volatile and allows non-destructive interrogation of the contents but the information can only be changed by mechanical means. The array is of necessity word-organised with a drive line for each word and an output line for each bit of the word. Coupling elements are placed between the two sets of lines in such a manner that when the appropriate drive conditions are applied to a drive line, either a '1' or '0' signal is generated in each output. A coupling element is usually required for each bit stored but in some cases a common coupling element at each bit position is sufficient.

Linear coupling is most commonly used, the information being stored by the presence or absence of the coupling element or by the position of the coupling element. Discrimination may be by the magnitude or polarity of the coupled signal, depending on the particular arrangement used. Non-linear coupling elements such as a square loop core can also be used, a '0' being stored by biassing the element to inhibit switching or by arranging the word lines so that these elements are not driven. This type of element provides greater noise immunity than linear coupling but is not capable of the same speed due to the need to reset the state of the elements after the store is driven and to the slower response of the elements. Drive currents are high in comparison with most stores using linear coupling. The various types of fixed stored are discussed further in a later section.

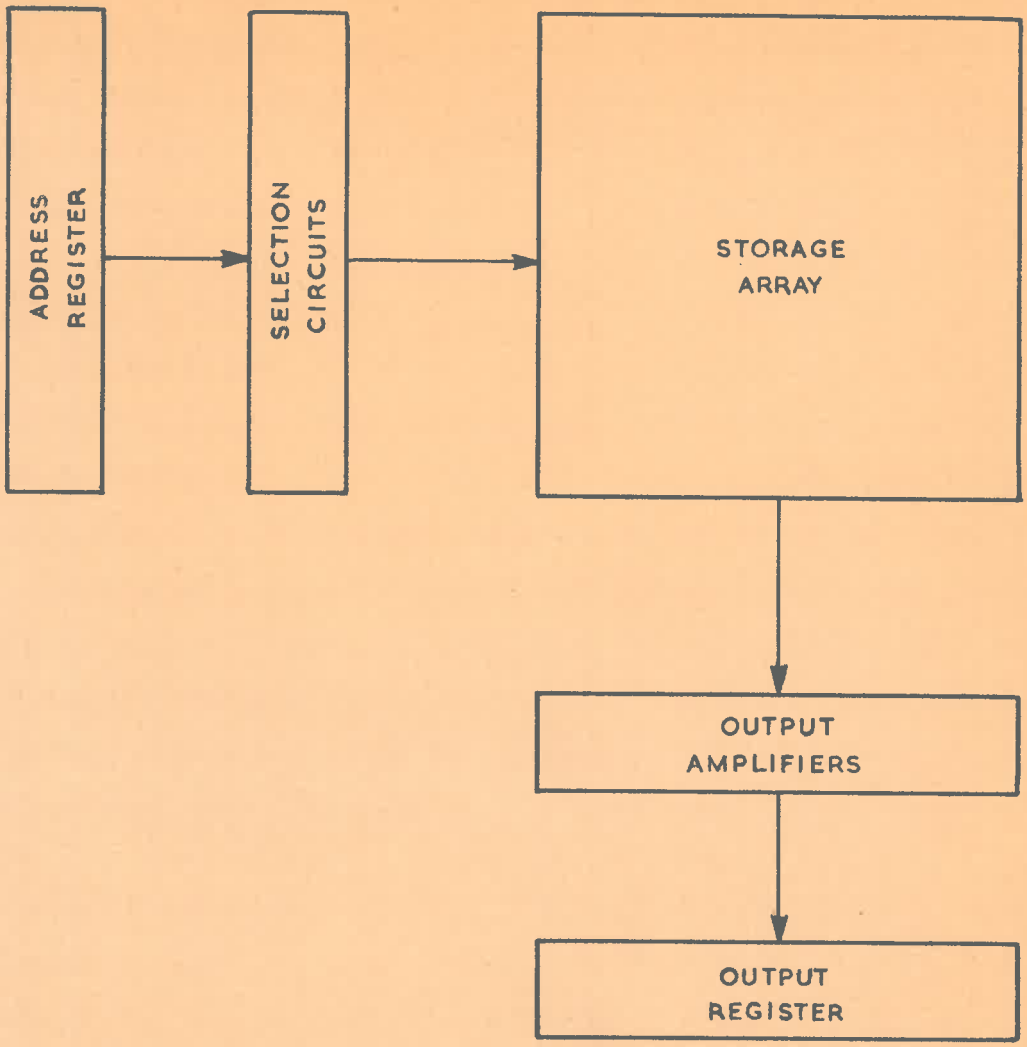


FIG. 47. CONFIGURATION OF A FIXED STORAGE SYSTEM

It would of course, be possible to provide the same functional behaviour with a conventional store which is regenerated after reading or to use some form of non-destructive sensing. Both these techniques are more expensive and do not provide the data security of a fixed store. The additional flexibility of these stores could however, make this form of storage more attractive in some applications.

The cost and convenience of a fixed storage system are strongly influenced by the type of coupling employed within the array and the mechanical construction of the array itself. Once these are chosen, the form in which the information is prepared and placed in the store and the terminal behaviour of the store, the drive conditions and the output signals, are largely determined. One of the major attractions of fixed storage is the potential low cost/bit of stored information which this form of storage can provide. If this is to be realised, some restrictions must be placed on the choice of the array. Since the store is word-organised a large selection and driving switch is required. The cost of this will be reduced if the drive voltage and current are kept within the ratings of the cheaper types of high frequency transistors and diodes. Because linear coupling is employed, the store outputs are sensitive to spurious outputs from the drive switch. Discrimination by the polarity of the output signal is more tolerant of poor signals than amplitude sensing and a store providing bi-polar output signals will be less sensitive to imperfect switch behaviour. A largek output signal allows the read amplifier to be simplified but this is less important than good discrimination between '1' and '0' signals if these two requirements should conflict. A simple mechanical construction and easy preparation and insertion of the information are also necessary if costs are to be kept low. If the information is subject to frequent alterations, the mechanical construction of the array must be chosen to allow this to be achieved quickly and easily.

The use of fixed storage in the design of CIRRUS assumed that a suitable form of storage could be provided at low cost. In both applications, in the control unit and as an extension of the core store, it was not anticipated that frequent alterations would be made to the stored information. A capacity of 4096 words of 38 bits with a cycle time of 1 - 1.5μsec was required.

The coupling between the drive and sense wiring can be achieved with either resistive, capacitive or inductive elements. Resistive, or diode, coupling was not considered suitable since this form of coupling is expensive and inflexible. Systems based on capacitive coupling have some attractive features. The mechanical construction of this type is well suited to printed circuit techniques and both the array and the coupling elements which represent the stored information can be prepared in this way. Electrically however, this form of storage is less attractive. Due to the small capacity/bit, the outputs tend to be low in amplitude and stray coupling can be troublesome. Discriminations between '1' and '0' by amplitude is most convenient but a satisfactory signal to noise ratio is not easily achieved. In addition the available printed circuit facilities were limited and relatively expensive. A fixed store based on inductive coupling appeared to be the most attractive and further investigation of fixed storage concentrated on this form.

(2) AN INDUCTIVELY COUPLED FIXED STORE.

The original concept involved the use of a row of toroids, one for each bit of the word. The toroids were placed edgewise down the row and an output winding wound around each toroid. A current in a wire passing through the toroid will induce either a positive or negative voltage in the output winding depending on the direction in which it passes through the toroid. Many words can be stored in the one row by weaving many wires through the toroids but only driving the appropriate wire. Although satisfactory electrically, the toroid introduced mechanical difficulties in mounting and threading the elements. Various other configurations were

considered with 1 or 2 toroids/bit and with both amplitude and polarity discrimination but none proved satisfactory mechanically. It was considered, however, that a store of this general configuration, in which a coupling element was provided for each bit position rather than for each bit of each word was well suited to the intended application and to the available workshop facilities. Other elements which would allow a more convenient mechanical construction were then investigated.

The element chosen was an E core with its matching I piece as shown in Fig. 48. The output winding is wound so that a drive current in a wire passing through one window will produce a positive or 'O' output signal and a current in a wire passing through the other window will produce a negative or 'I' output. A store can be formed from a row of these elements containing as many E cores as there are bits in the word. A word is inserted in the store by weaving a wire down the row or cores, passing through the appropriate window of each E core. Many wires can be passed through the same set of E cores and providing only one wire is driven, the voltage induced in the output winding of each element will produce the sequence of 'I' and 'O' signals representing the word wired into the store.

Ideally the output voltage wave form is the time derivative of the drive current.

$$e = N \frac{d\phi}{dt}$$

$$\therefore KA \mu N \frac{dI}{dt}.$$

In practice, however, the inductance of the output winding and the stray capacity form a low Q tuned circuit which is excited by an impulse from the driven wire. The output waveforms for various output windings and loading conditions are shown in Fig. 49. As the number of turns

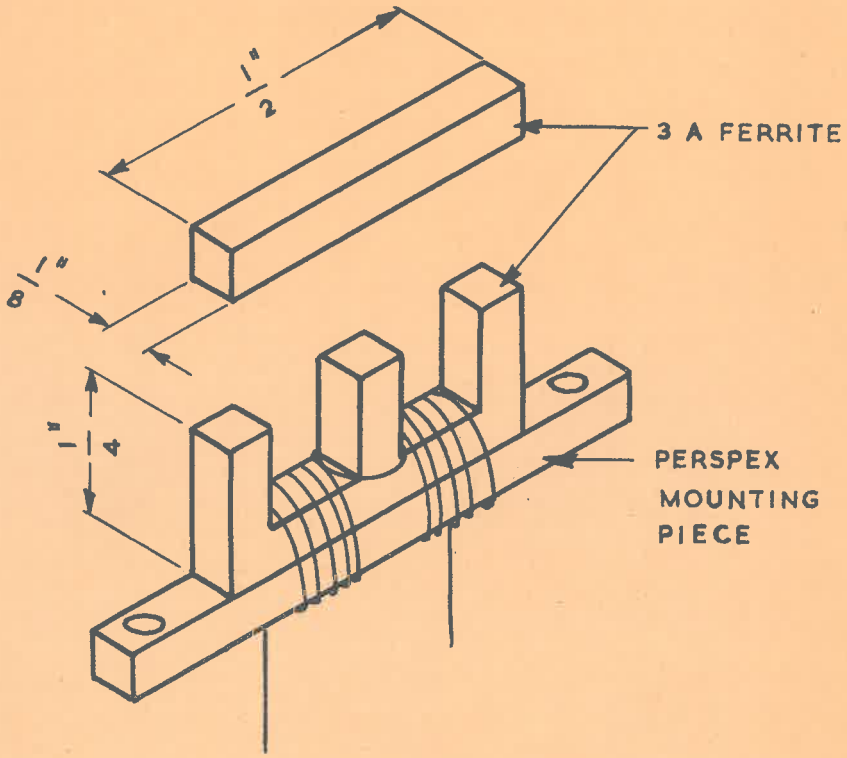


FIG. 48. BASIC ELEMENT OF FIXED STORE

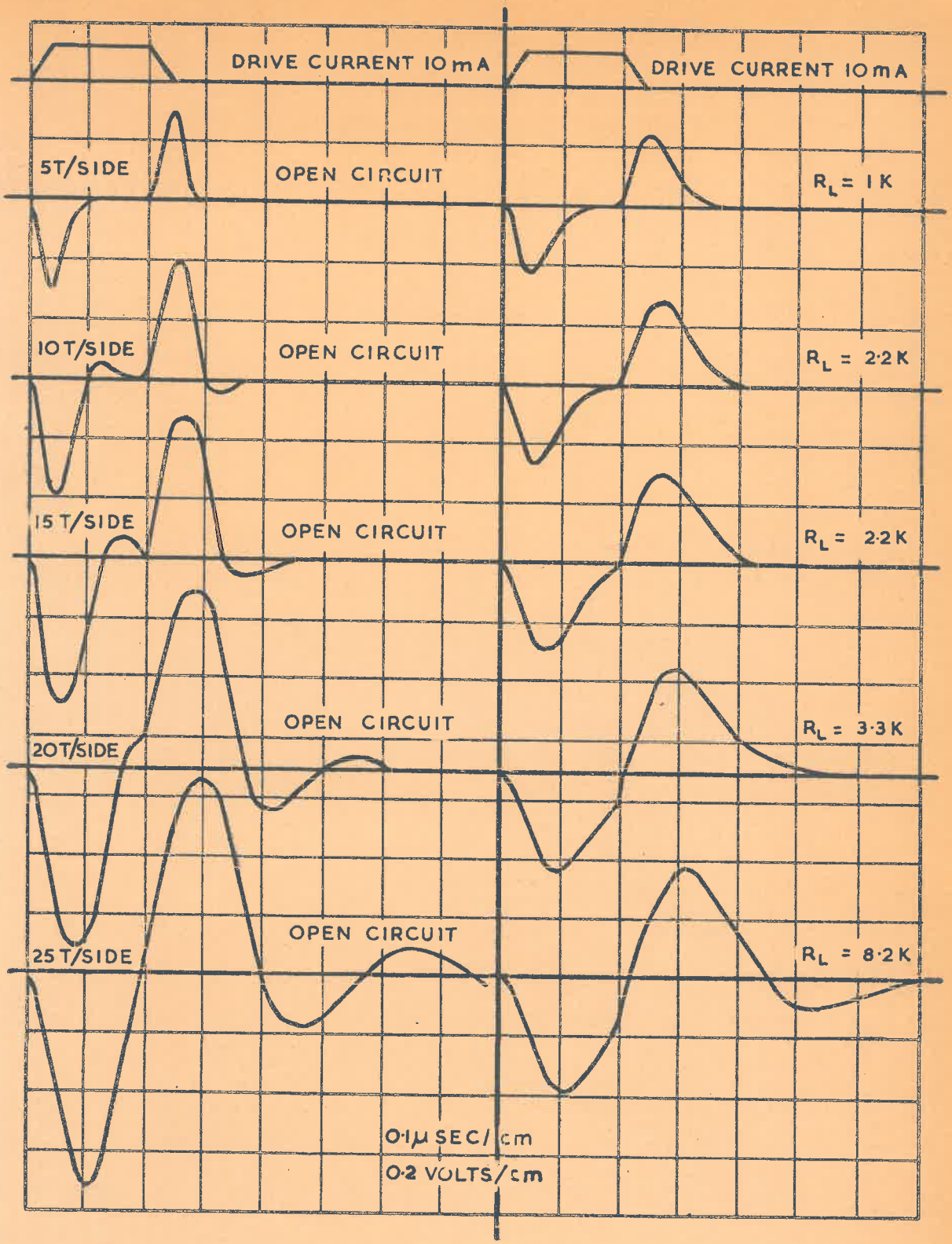


FIG. 49. RESPONSE OF COUPLING ELEMENT WITH VARIOUS OUTPUT WINDINGS.

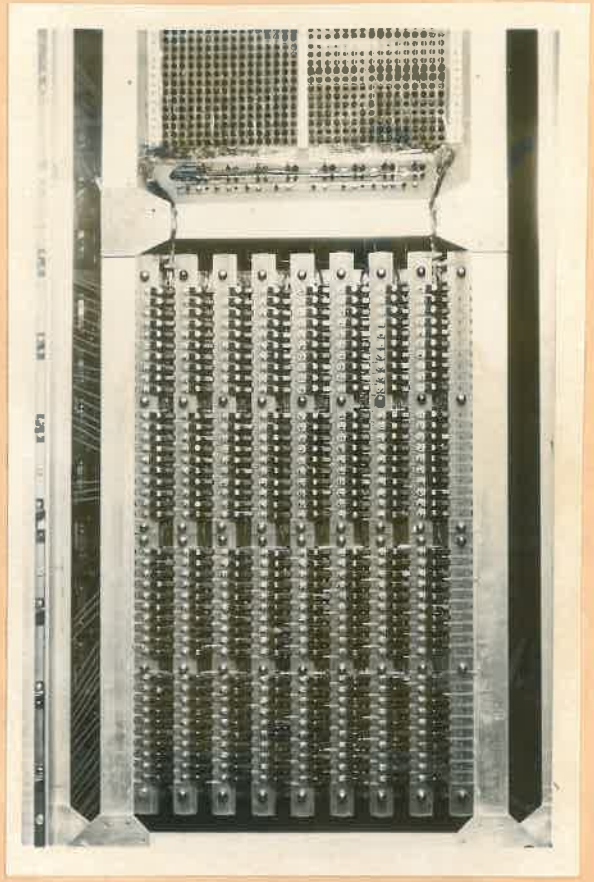
is increased, the output signal increases in magnitude and also in duration due to the lower resonant frequency of the winding. A corresponding increase in the Q of the tuned circuit produces a tendency towards a damped oscillation rather than a single impulse. The additional loading required to control this oscillation results in a relatively small increase in output voltage as the turns on the output winding are increased. A winding with 15 turns/side was chosen as representing a suitable compromise between signal amplitude and duration. The shorter duration of the signal from a smaller number of turns made sensing of the output more difficult and was not necessary with a cycle time of 1.5 μsec. If more turns were used, the tendency of the winding to oscillate proved troublesome. For all windings, the output voltage is proportional to the drive current and relatively insensitive to the rise time provided this is less than a ¼ period of the natural resonant frequency. The output signal from the element is a negative swing followed by a positive swing for a 'I' and vice versa for an 'O'. Discrimination is, therefore, achieved by strobing the first swing of the output wave form and sensing the polarity of the voltage.

Both the control fixed store and the machine language fixed store were to have a capacity of 4096 words. In most respects the single row store described above is not the most convenient arrangement. A diode switch is the most suitable form of selection switch for this type of store, since only unidirectional drive pulses are necessary. A switch of this size is both large and costly, requiring 4096 diodes and 128 drivers. To reduce switch leakage, the switch would have to be sub-divided, further increasing the number of drivers. A more convenient arrangement electrically is to use a multi-row store in which each wire threads all rows, the required word being selected by driving the appropriate wire and selecting the signal from the appropriate row. If N rows are used, the number of wires and the size of the switch

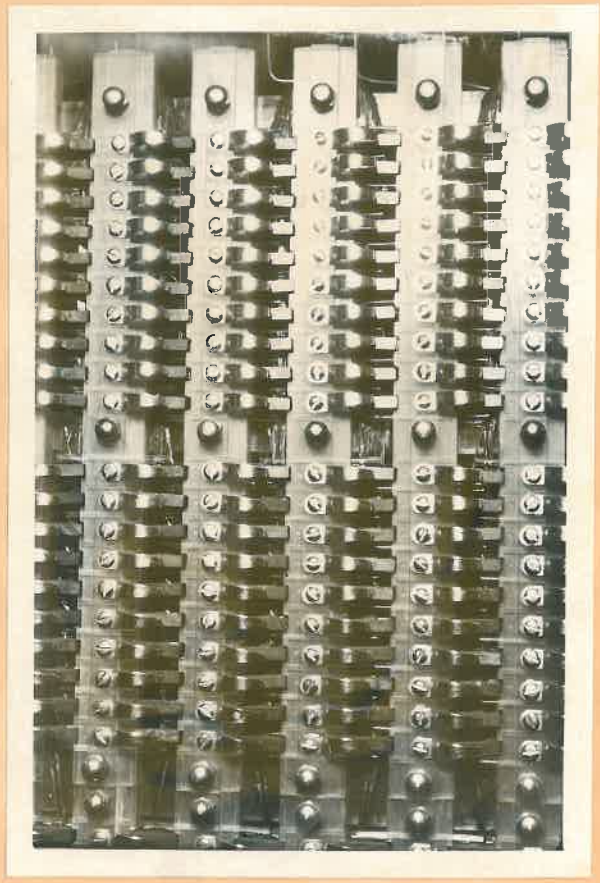
are both reduced by a factor of N but, with increasing N, the physical size and cost of the array increase and the drive voltage and propagation time through the store both increase N times. The cost of the row-selection circuits must also be weighed against the saving in wire selection circuits. For large N, the store becomes less convenient to use. If a word has to be changed, N words must be rethreaded and similarly an error in any of the N rows during threading will require that the whole wire be replaced. For convenience in addressing it is desirable that $N = 2^m$. Either 4, 8 or 16 rows would therefore appear to be the most likely choice.

For the CIRRUS stores, an 8 row arrangement was considered to be the most suitable balance between the above factors. Using 4 thou. wire, the minimum size which could be easily handled, the required 512 wires occupied less than 40% of the window of the E core if all passed through the same window. Each row contains 40 elements, giving a capacity of 4096 40 bit words. Only 38 bits are required, 36 information bits and 2 parity bits. The other 2 bits were intended to provide a self-derived strobe on the store output.

The mechanical assembly of the array is shown in Fig. 50. The elements are screwed to a perspex frame with 5/16" spacing down a row and 1" between rows. The array measures approx. 16" x 9" . For convenience in wiring, the diode switch and the array are mounted in the same sub-frame. The diodes on the back of the store and the circuits adjacent to the drive switch provide the row selection. To insert information the I pieces must be removed from the store. It was originally intended that all the I pieces would be flexibly mounted on a separate plate which could be quickly removed from the array. It was found, however, that the contact between the E and I pieces was not sufficiently reliable, giving poor output signals. It was, therefore,

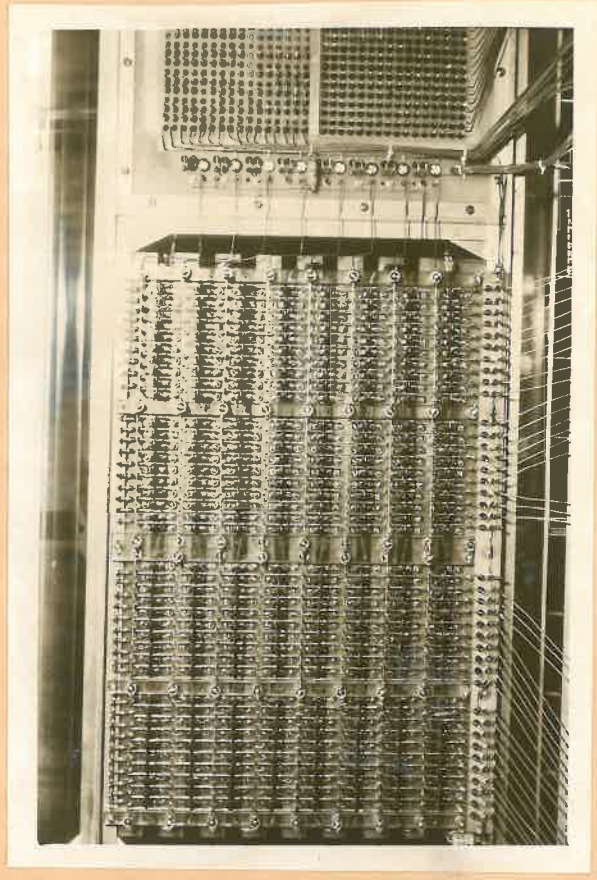


(a) FRONT VIEW



(b) DETAIL OF FRONT VIEW

FIG. 50 MECHANICAL ASSEMBLY OF FIXED STORE



(c) BACK VIEW

(d) DETAIL OF BACK VIEW

FIG. 50. MECHANICAL ASSEMBLY OF FIXED STORE

necessary to provide separate clips for each I piece.

(2.1) THE SELECTION CIRCUITS :

(2.1.1) WIRE SELECTION :

These circuits are required to select 1 of 512 wires and to provide the appropriate drive pulse to the selected wire. Since all drive wires pass through the common E core in each bit position, the selection ratio of the switch must be very high. The configuration of the store does not provide any protection against spurious currents, and the output signal from the E core will be the sum of signals due to the current in the selected wire and those due to the various spurious currents in other wires. The selection system used is based on the diode switch of Fig. 51. An array of diodes, one for each output is driven by 4 current sources (common emmitter circuits) and 4 current sinks (common collector circuits). A particular wire is selected by applying the appropriate potentials to the source and sink circuits attached to the coordinates of that position. The diodes will then steer the current from the active source through the selected wire to the active sink. The conditions shown in Fig. 51 are those required to select wire O. The full size switch uses 32 sinks and 16 sources to select 1 of 512 wires. This type of switch has been widely used for 1 of n selection, especially where a bi-directional current through the load is not required.

The nature of the load in this case, however, introduces several features not normally encountered in other applications. The wires attached to each output are not isolated from each other but due to the method of threading through the array have considerable mutual coupling. Fortunately the inductive coupling is always in such a direction that the voltage induced in the non-selected wires further reverse biasses the diodes attached to these wires. The magnitude of the coupling varies with the relative patterns of the wires, showing a

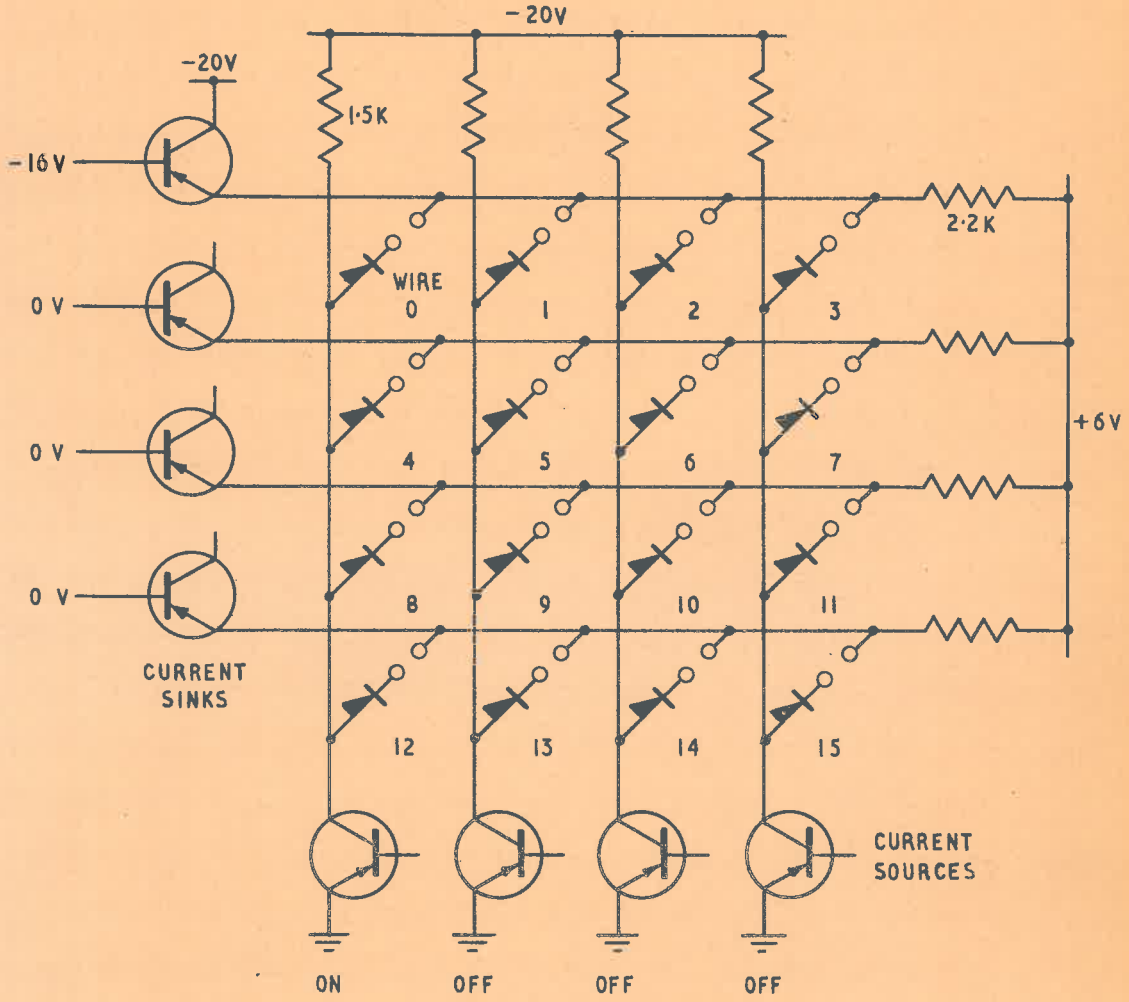


FIG. 51 DIODE SWITCH

3 : 1 variation between two identical patterns and two complementary patterns, but the flux linkage around the E core is such that no change of polarity is involved. There is, therefore, no possibility of the induced voltages destroying the steering action of the switch during the drive pulse.

Approximately 12-ft. of wire is required to thread through 8 rows of the store. The capacity between a wire and the bundle of other wires varies between 100 pf. and 200 pf. depending on the patterns woven into the store. In the switch of Fig 51. all wires are connected to a. c. earth at the sink end via the common collector circuits. There will, therefore, be a considerable spurious current generated by a capacitive coupling from the driven wire to the non-driven wires which can flow out at the sink end. (Fig. 52(a)). This coupling is sufficient to give unsatisfactory signals from those elements where the non-driven wires mostly pass through the opposite window to the driven wire. Most of this spurious current could be eliminated by using a diode at each end of the driven wires. The capacitive coupling between the wires is then isolated by a reverse biassed diode at each end of the wire and the capacitive current is greatly reduced. The decrease in capacitive loading on the selected wire also improved the propagation of the drive pulse and reduced the propogation time through the store from 0.2 μsec to 0.1 μsec.

The use of 2 diodes, however, introduced a sneak current through the switch at the source end of the drive wires attached to the selected source (Fig. 52 (b)). Both diodes are reverse biassed and the wires assume a potential somewhere between the O V level of the non-selected sinks and the -20 V. level of the sources. Since both diodes were of the same type, the majority of wires and their associated stray capacity

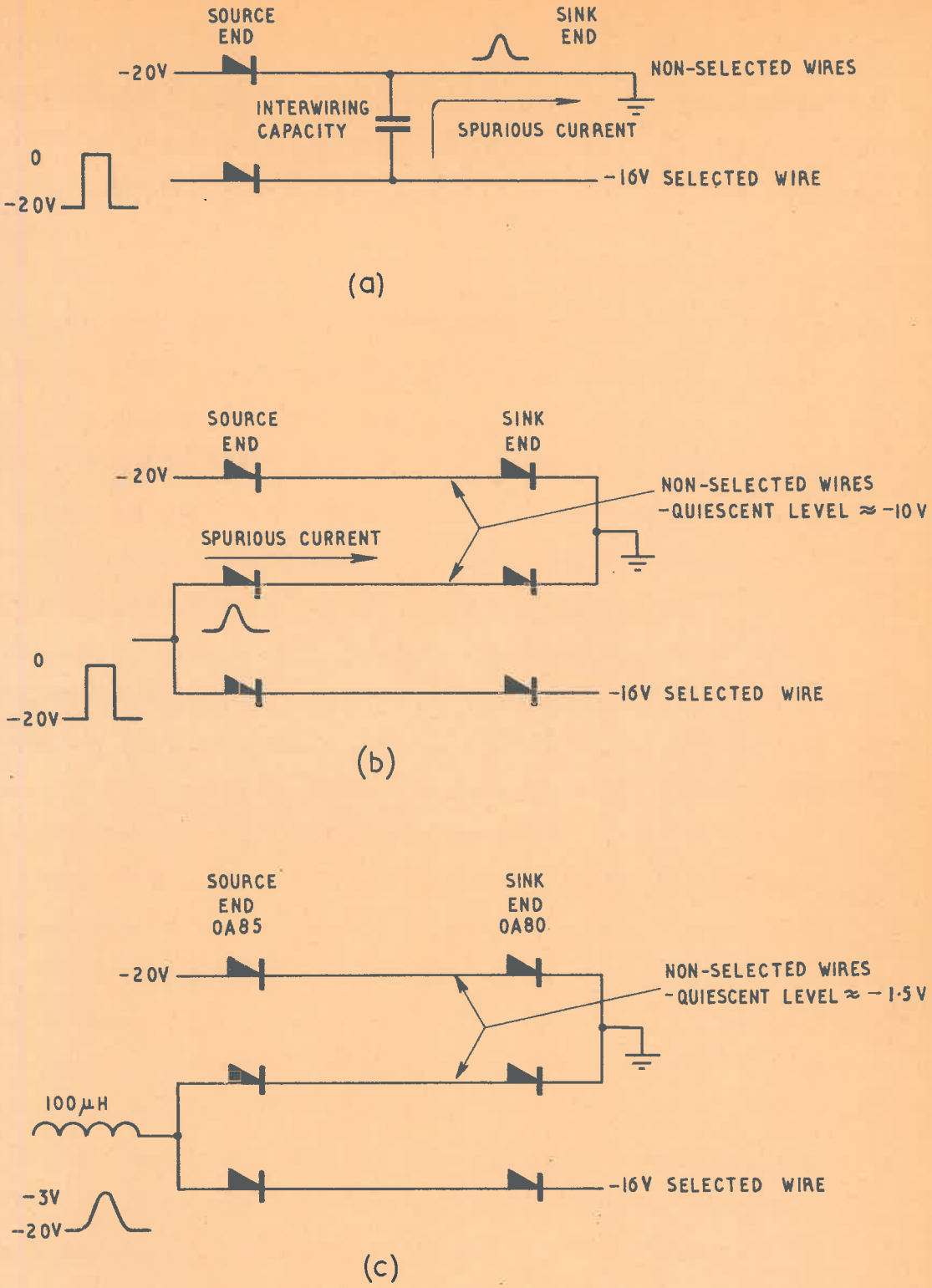


FIG. 52. SPURIOUS CURRENTS IN DIODE SWITCH

were 8 - 12 V below earth, the voltage being largely determined by the ratio of back resistances. When the selected source was energised, a current could pass through all diodes on the selected source into the capacity of the non-selected bundle. The current, apparent mainly during the rise of the drive current, was opposed by the inductive coupling from the selected wire but this occurred slightly later in time and had little effect on the spurious current. The result was poor signals from the E cores at the source end of the drive wire.

Two changes were made to reduce this spurious current (Fig 52. (c)). Firstly, diodes of different back resistance were used at each end of the drive wire. Those at the sink end were OA80[8] with a back resistance of 0.25 - 05 MΩ and those at the source end were OA85 with a back resistance of > 5 MΩ (both as measured by a multimeter). The static potential of these wires was then reduced to ≈ -1.5V. Secondly, an inductance of 100 μH was placed between the source driver and the switch. With a load of ≈ 200 uH due to the drive line plus the forward drop of the two diodes this meant that the input to the switch did not swing more positive than ≈-3 V. Ideally the nonselected diodes on the selected source could not be forward biassed. The inductance also increased the rise time of the voltage applied to the switch, such that the applied drive voltage was matched to the response of the output windings. The capacitive coupling between drive wires was then less apparent, due partly to the reduced direct coupling and partly to the fact that the inductive coupling became dominant with the slower waveform. Capacitive coupling between the drive wire and the output winding was also reduced giving cleaner output signals.

When the store was put into service, a further source of trouble became apparent. If during address changing, a sink change is involved, the static potential of wires attached to the sink which had been sel-

ected, and therefore applying - 16 V. to the switch, remain at a potential well below OV. These wires are isolated by reverse biassed diodes at each end of the wire and the potential of the wire drifts towards the correct level of -1.5V. with a long time constant. If the store is driven before the correct level is reached, a spurious current will flow into the store through nonselected diodes on the selected source. This current will only be present for the first pulse after the sink change since the resulting current flow will establish the correct static potentials in the store. The magnitude of the current was sufficient, however, to cause a store error. This behaviour had been anticipated when the source of switch leakage were investigated but the test rig being used was not suitable to adequately check a transient error such as this. It was more convenient to wait until the store was installed in the control unit where full checks could be easily set up. By the time this was done, it was apparent that another type of fixed store being developed was superior and would replace the store using E cores. Since this store, although similar in principle and using the same type of drive switch used only one diode per wire, this source of switch leakage would not occur. Consequently the problem was not pursued, the store was double pulsed and the first set of outputs ignored. This reduced the speed of the computer but did not otherwise affect the system performance.

With the above modifications, the performance of the drive switch was satisfactory, the total spurious currents being less than 10% of the selected wire drive current throughout the store. The output signals throughout the store were satisfactory apart from a progressive time delay through the store but this could be accommodated in the sense amplifier and presented no difficulty.

The source and sink driver used are shown in Figs. 53 and 54

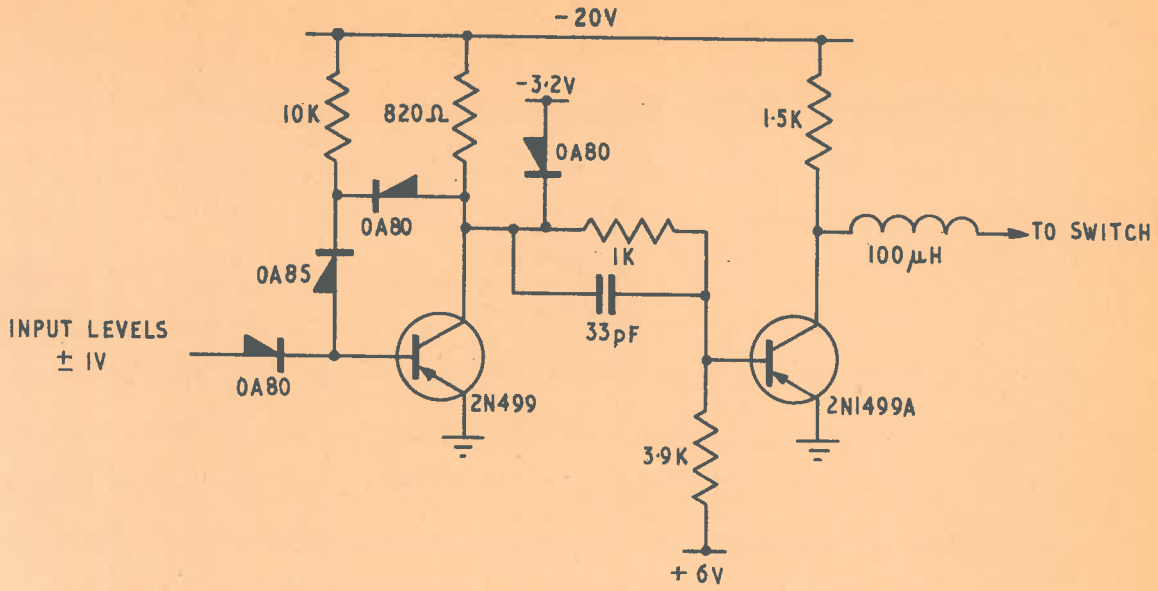


FIG. 53. SOURCE DRIVER

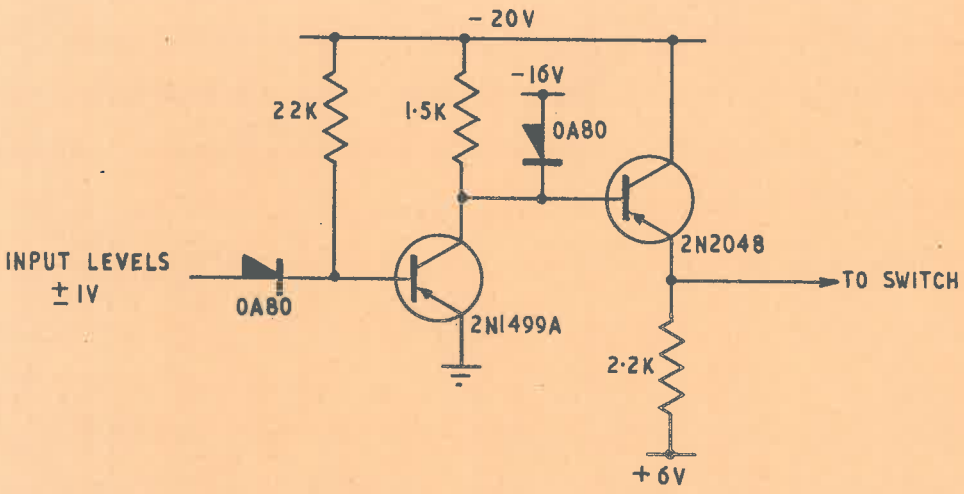


FIG. 54. SINK DRIVER

respectively. The input levels of $\pm$ IV are generated by the address decoding circuits discussed below. The current delivered by the source driver to the store is limited only by the inductance of the drive wire, rising to a peak value of approx. 18 mA at the end of the drive pulse. This behaviour is consistent because the method of wiring ensures that each drive wire has the same impedence, irrespective of the pattern of information inserted in the store.

This low drive current was a major factor in much of the trouble experienced with spurious capacitive currents. If the drive current were increased these would be relatively less significant and the driving problem would be eased considerably. This, however, would be accompanied by an undesirable increase in drive voltage. A better solution would be to reduce the drive impedence by using less magnetic material in each element, but the E cores used were the smallest available. Any further reduction in size would reduce the number of wires which can be passed through each element and would also make the elements too fragile mechanically. Another solution, to reduce the store to 4 rows, would increase the number of wires and size of the switch and could well introduce further mechanical and electrical trouble.

(2.1.2) ROW SELECTION:

The selection of the required 1 of 8 rows of the store is accomplished by the diode gating circuit of Fig. 55. A row is selected by taking the output of the appropriate row selection driver to -3.5 V, the non-selected row drivers being at O V. The diodes in each bit position of the selected row are then forward biassed, allowing the signals from this row to be passed through to the sense amplifier. An emitter follower on the output of the row selection gate is necessary to prevent loading of the store outputs. Excessive loading reduces the output voltage and causes an undesirable transient signal during row change resulting from the in-

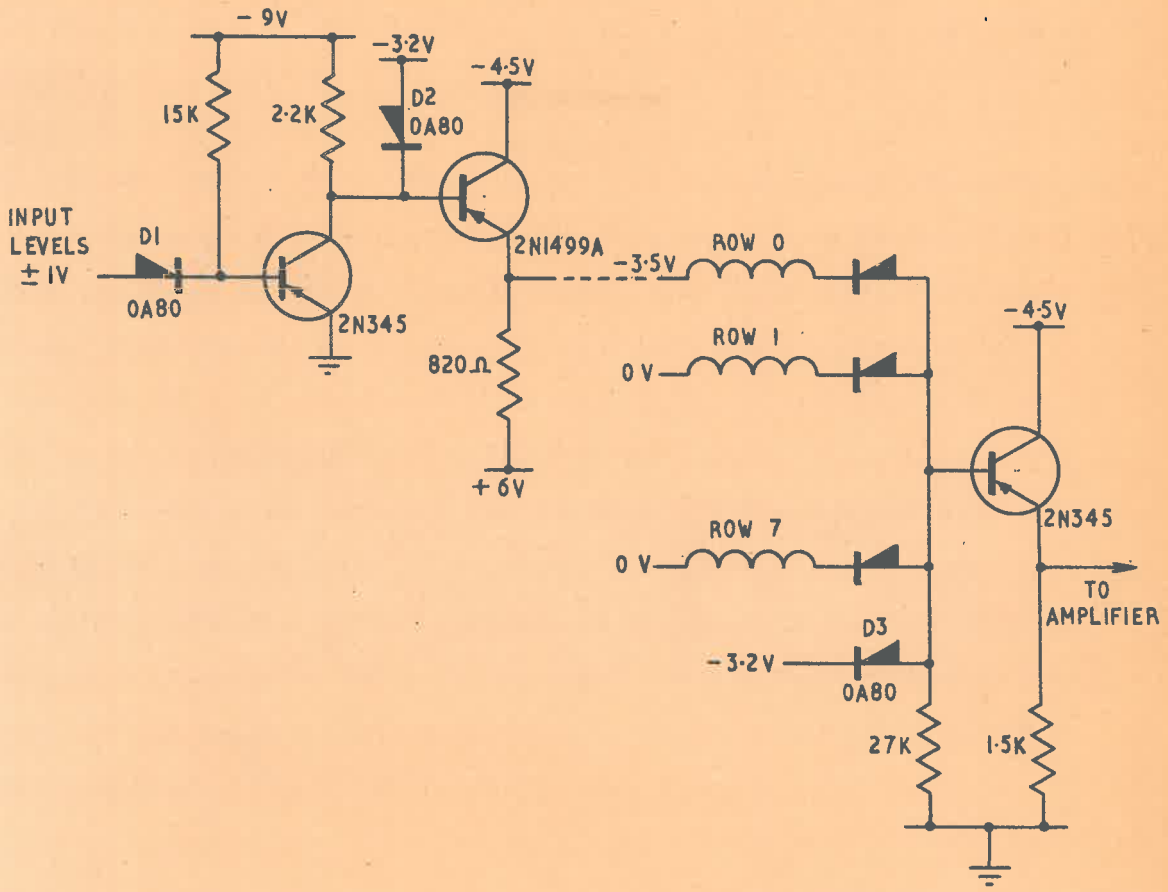


FIG. 55. ROW SELECTION CIRCUITS

ductance of the output winding. The emitter follower also reduced the capacitive loading on the output, minimising a tendency to ring after the drive pulse. The diode to -3.2 V. on the gating circuit, D_3, clips all positive going signals which have no significance in the sense amplifier. The -3.2 V clamp diodes of the row selection drivers, D_2, are selected for matched forward resistance to prevent a d.c. step being applied to the sense amplifier during row changes. An a.c. coupled amplifier is used and this transient applied shortly before the store is interrogated could cause faulty discrimination. The row selection gating diodes do not need to be matched since they do not show significant variation in forward voltage at the low current involved.

2.1.3) ADDRESS DECODING :

The address of the required word in the store is held in the 'S' register. To gain access to the word, one source, one sink and one row selection driver must be selected. The 12 bits of the 'S' register are decoded as shown in Fig. 56. The basic decoding package is the binary to octal conversion unit described above in connection with the core stores (Fig 18). For each address, one driver of each type receives a level of + I V and is selected. The drive pulse is timed by the clock waveform applied to the source drivers. Both the sink driver and the row selection driver are allowed to follow the state of the 'S' flip-flops since these must be selected before the drive pulse is applied to allow any resulting transients to decay. Due to the method of wiring, the row selection must use the 3 least significant address bits. The decoding of the other 9 bits is arbitrary providing the wires are terminated on the diode switch in accordance with the decoding.

(2.1.4.) THE PERFORMANCE OF THE DRIVE CIRCUITS :

The behaviour of the drive switch is shown in Fig. 57. At the source end of the wires a leakage current of approx. 1 mA, I_2, passes

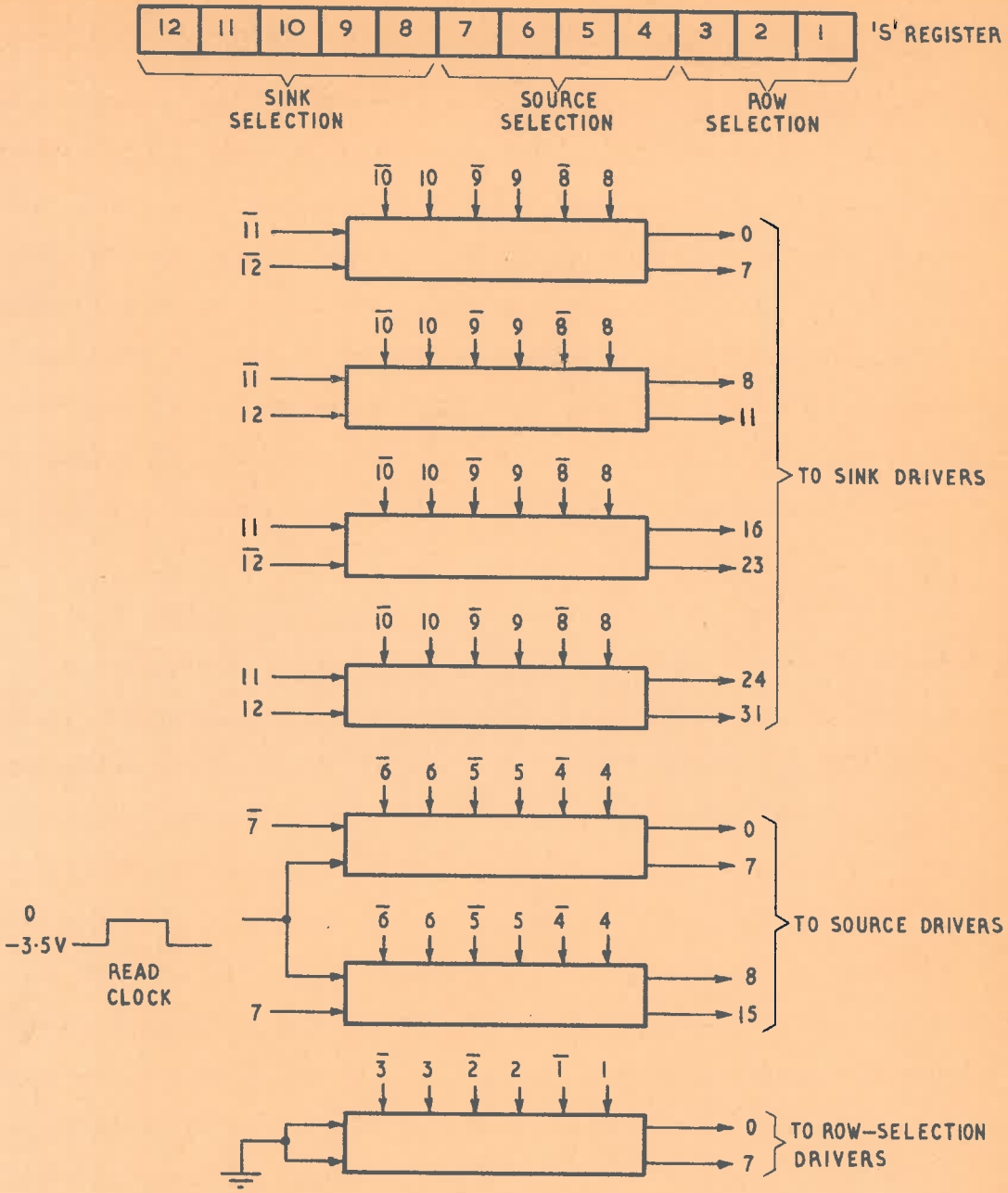


FIG. 56. ADDRESS DECODING FOR FIXED STORE

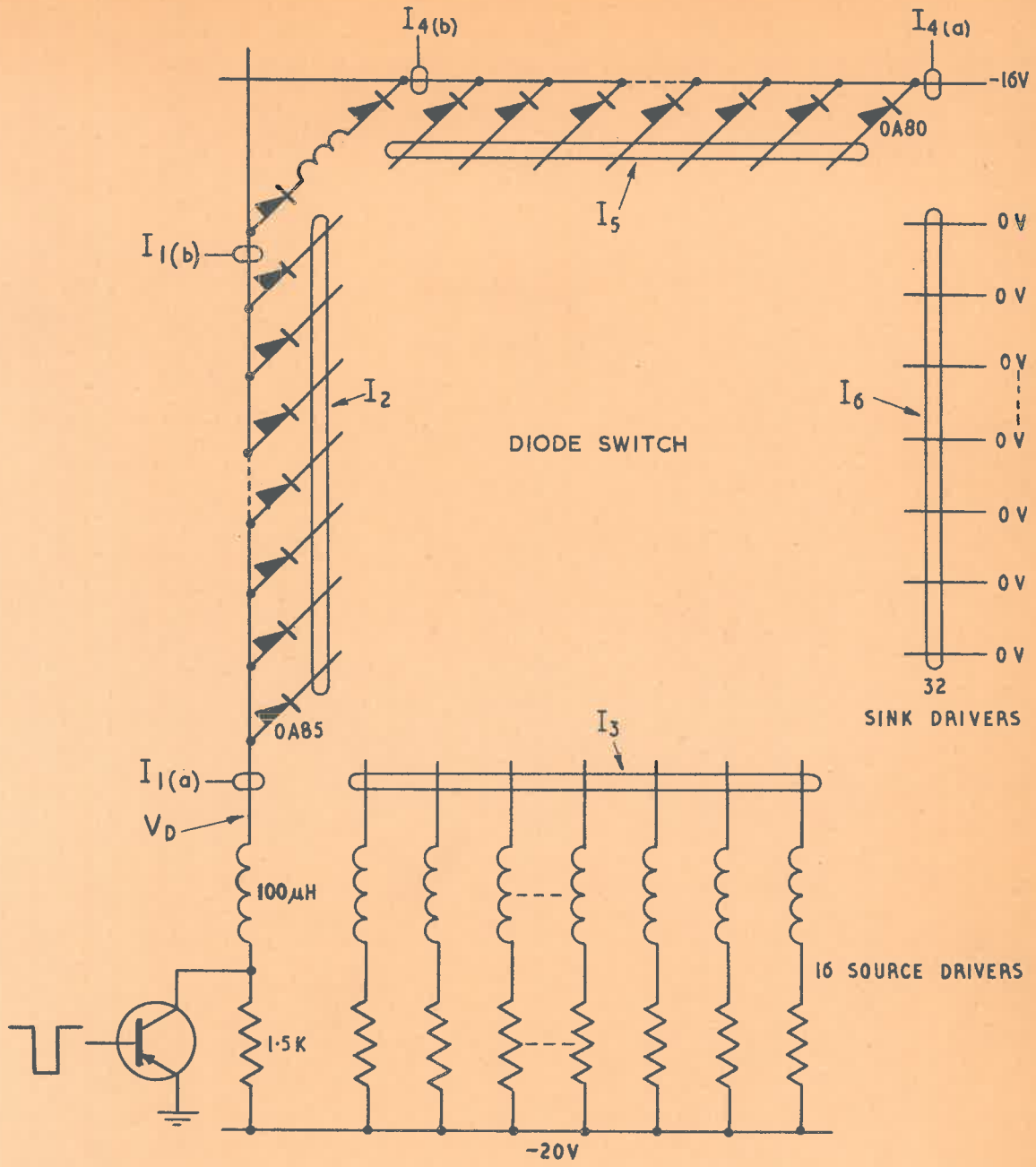


FIG. 57(a). SCHEMATIC OF DRIVE SWITCH SHOWING CURRENT MONITORING POINTS

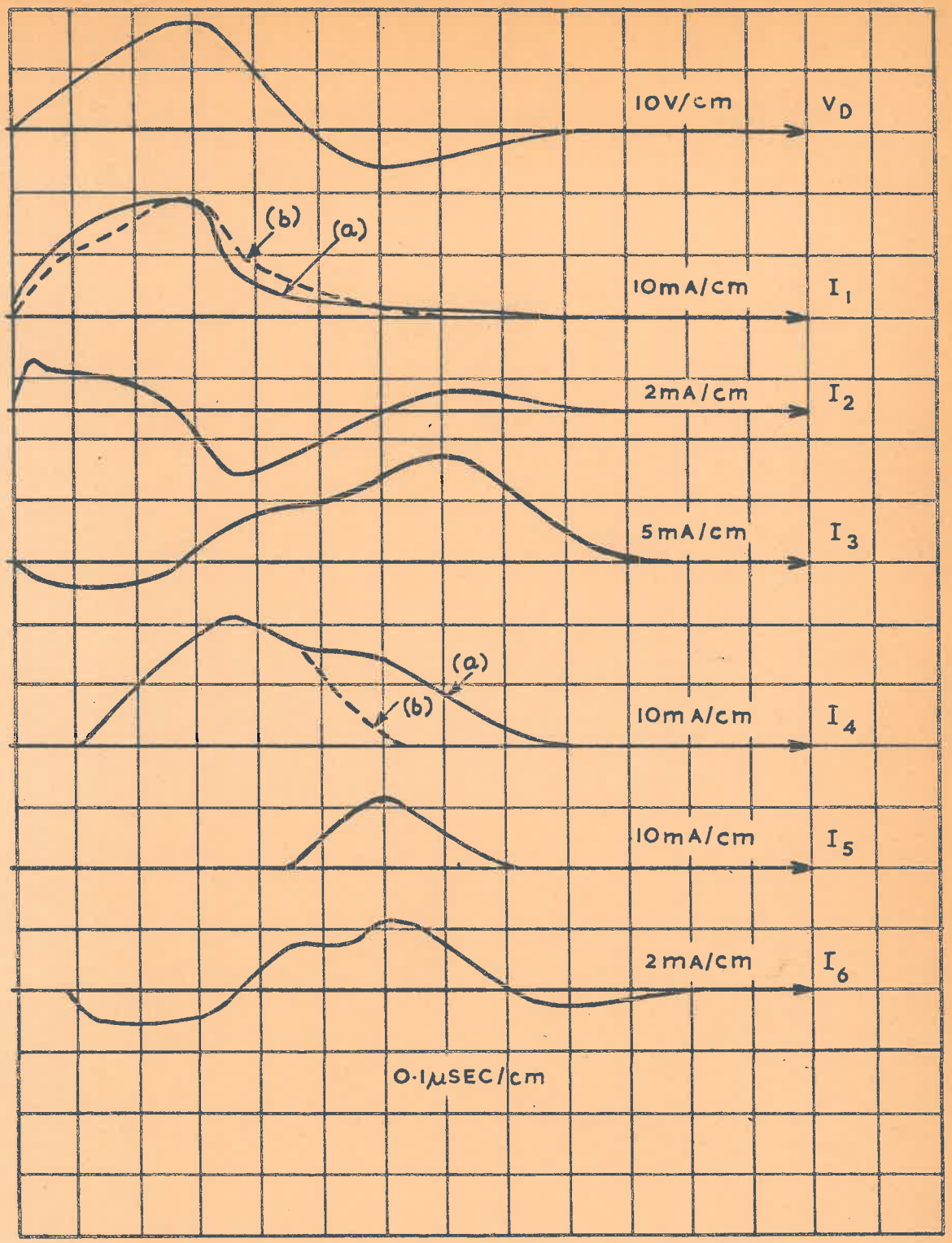


FIG. 57.(b) DRIVE SWITCH PERFORMANCE

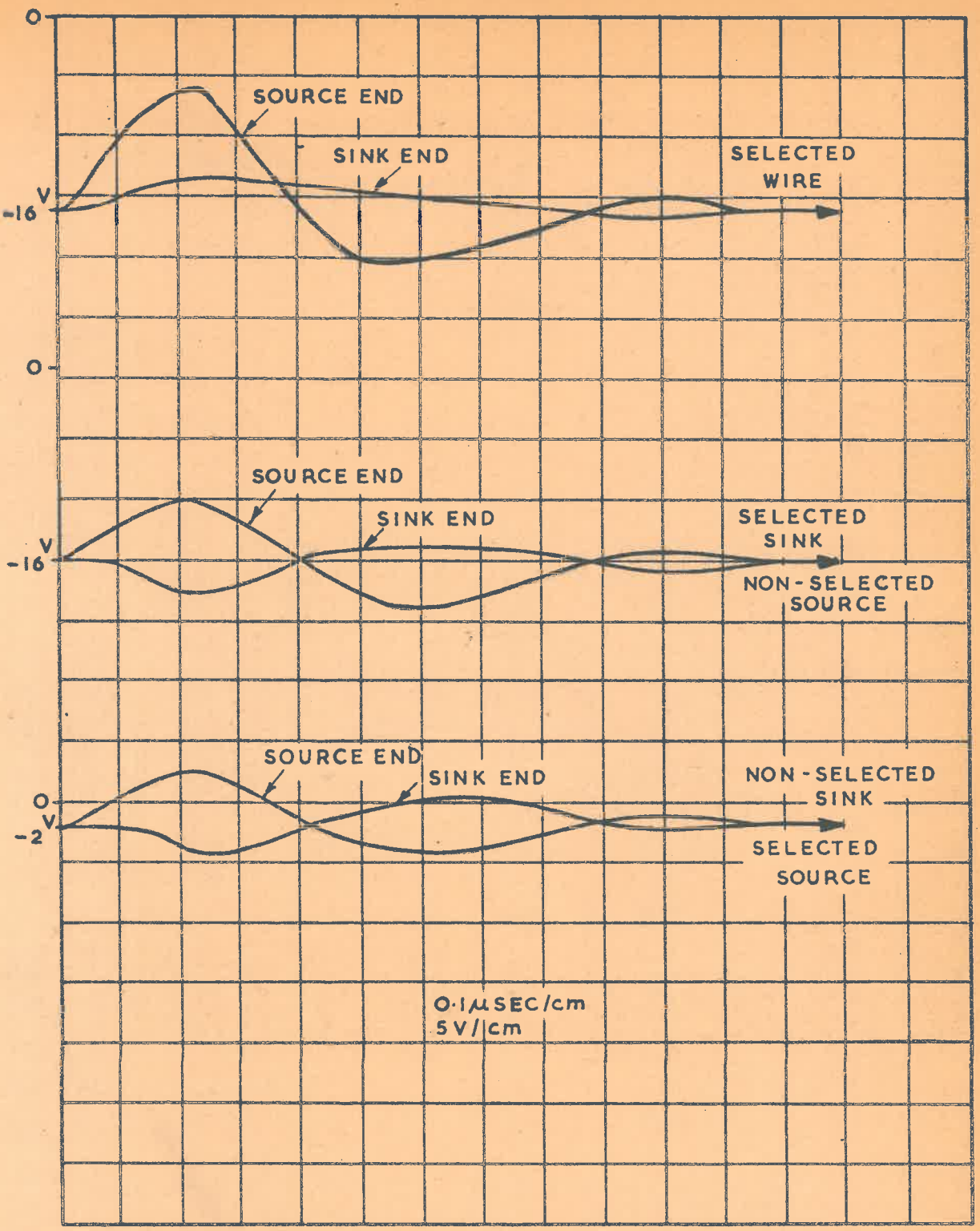


FIG. 58. VOLTAGES INDUCED WITHIN THE STORE

through the 31 non-selected diodes on the selected source. The corresponding spurious current at the sink end, I_5, is trivial. During the drive pulse, the voltages induced in the non-selected wires, Fig. 58. are in a direction to further reverse bias the diodes at each end of the wire, causing small leakage currents, I_3 and I_6, of opposite polarity to the drive currents to flow through the reverse impedance of these diodes. The waveforms of Fig. 58 were taken on the store side of the diodes at each end of the wire. At the end of the drive pulse, the voltage across all drive wires reverses, forward biassing all diodes on wires attached to the selected sink. The recovery of the array is then controlled by the 1.5 K resistors to the -20 V supply in the source drivers. During this period the switch becomes ineffective and the store outputs are meaningless. This behaviour can be seen in the waveforms for I_1, I_3, I_4 and I_5/ The time delay between the source and sink currents indicates a propagation delay through the store of 0.1 μsec. All these waveforms were taken without cycling addresses, but with the store being double-pulsed as discussed above, the waveforms do not differ significantly from those due to the second drive pulse.

(2.2) THE OUTPUT CIRCUITS :

A typical range of store output waveforms is shown in Fig. 61 (a). The variable signals are due to the propagation delay through the store, accentuated by the change in drive waveform and the variable response of the elements themselves. In addition, poor contact between the E and I pieces can result in signals of much lower amplitude and shorter duration than those shown. Reliable operation can only be achieved if the sense amplifier can accept these inferior signals without error. If possible the hardware should be capable of sensing any signal which can be distinguished by observing the output on an oscilloscope.

It was originally intended that the information would be sensed by strobing the first swing of the output waveform with a clock derived

from the output of a strobe position in each row, automatically compensating for the propagation through the store. This technique was not pursued for two reasons. Firstly, if sufficient amplifier gain were provided to allow reliable sensing of poor signals, the oscillation after the drive pulse and the transients due to address changing proved troublesome with the simple amplifier proposed. A more complex sense amplifier would have overcome this problem but with 38 amplifiers involved it was desirable that the circuit be kept as simple as possible in the interests of economy. Secondly, the outputs from the strobe positions were not sufficiently uniform to provide a suitably timed strobe, although these could probably have been adjusted if required. Rather than attempting to strobe the output, a wider gating waveform was applied which would sense any negative or '1' signal appearing during the time when a unambiguous output could be obtained. The positive going signals are therefore clipped off by the row selection circuit to keep irrelevent signals out of the amplifier. This form of sensing proved to be much more tolerant of poor signals than a strobing technique.

The circuit of the sense amplifier is shown in Fig. 59. A negative going '1' signal on the input presents a negative going voltage to the gate. If this signal coincides with the period when the read gate waveform is at - 3V, then it will pass through the gate and, if of sufficient amplitude, will turn on T_2. The output is then taken to + 1 V, and the C flip-flop set to the '1' state. Any positive signal or a negative signal in the absence of the gating waveform will produce no output. The amplifier output is applied to the manual set input of the C flip-flop. This is identical to that used in the M register the circuit of which is shown in Fig. 34 (b). All C flip-flops are reset to the '0' state prior to driving the fixed store.

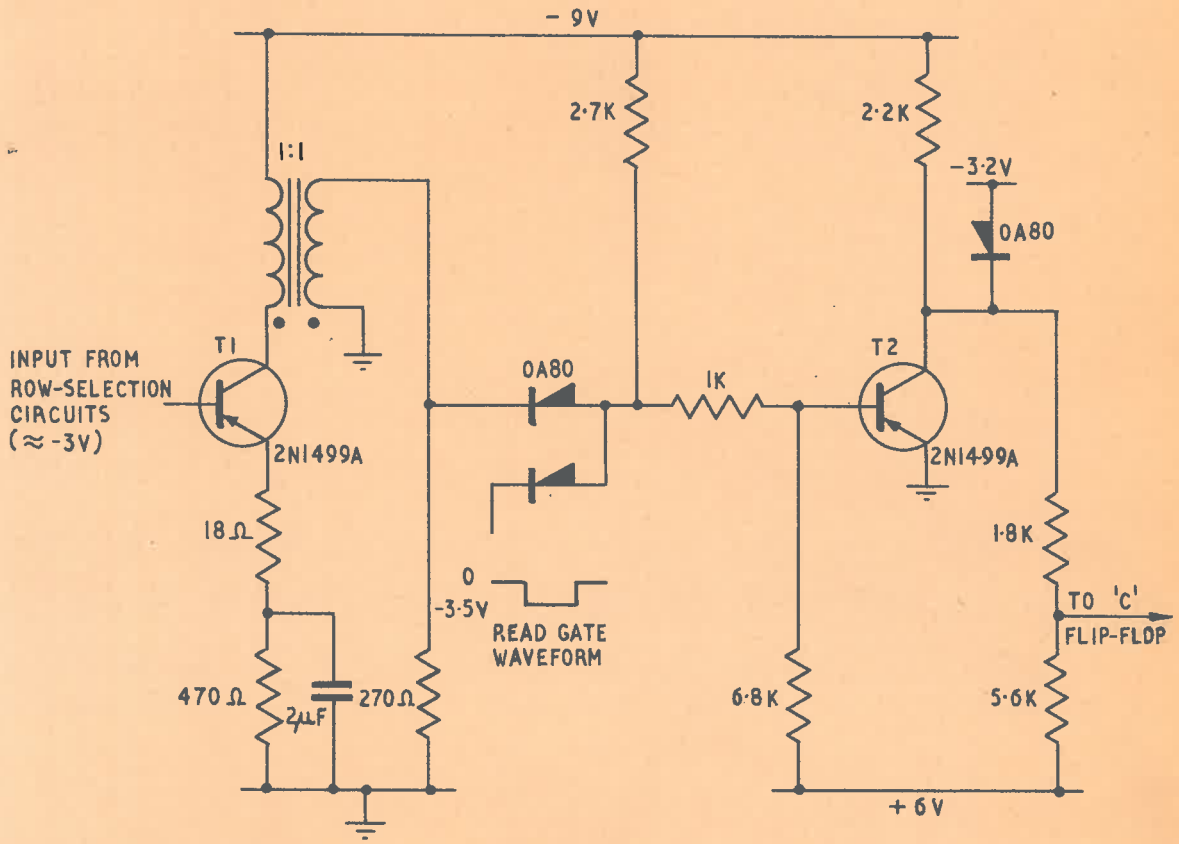


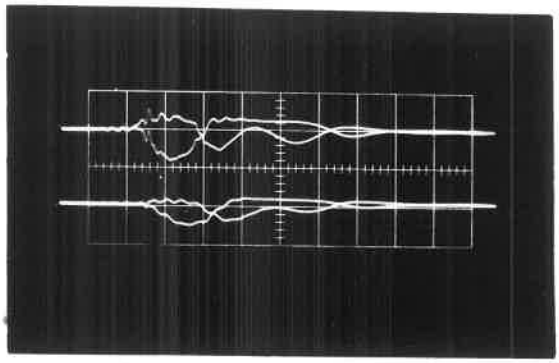
FIG. 59. SENSE AMPLIFIER FOR FIXED STORE

The waveforms through the amplifier for a '1' and '0' signal are shown in Fig. 60. A repetitive scan of 8 wires gave the set of 64 input and output signals of Fig. 61. The disturbance following the store outputs is the rowchange transient. The inductance of the output winding on the E core is sufficient to cause a small signal as the gate current is transferred. The sink change transient could not be included in a scan of this nature since insufficient consecutive wires were threaded to provide a meaninfgul set of wave forms. This transient is caused by a current flow into the selected sink from the stray capacity of the drive wires as the sink voltage changes from O V to 16 V. The amplitude of the transient is pattern sensitive and varies with the selected row, being most significant at the sink end of the store, i.e. rows 6 & 7. Typically the disturbance is slightly greater than that due to a row change.

This amplifier and method of discrimination was capable of accepting any reasonable output from the store. The bipolar store output was a significant factor in achieving this performance.

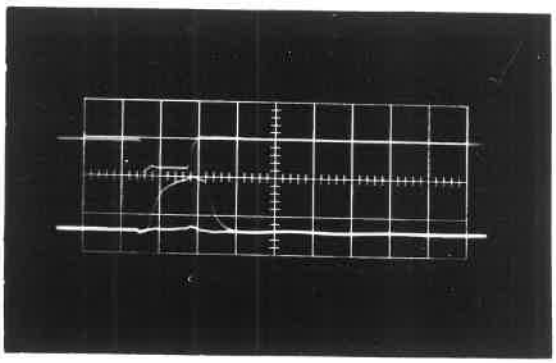
(2.3) THE COMPLETE STORE.

The block diagram and timing of the control fixed store are shown in Figs. 62 and 63 respectively. The store proved to be very tolerant to variations in voltages and currents. All voltages could be varied by at least 10% and the drive current could be reduced to less than 10 ma before failure occurred. The access time of the store as used was approx. 0.4 μsec but this did not include address selection since the new address is set up during the previous cycle. Total access time would be increased to approx. 1 μsec if address selection were included since time must be allowed for the resulting transients to decay. The cycle time of 1.5 μsec is determined mainly by the timing of the control unit. Successful operation has been demonstrated on a 1 μsec cycle but margins were considerably



(a)

TOP TRACE: INPUT SIGNALS 0·5 V/cm
BOTTOM TRACE: GATE INPUT 5 V/cm

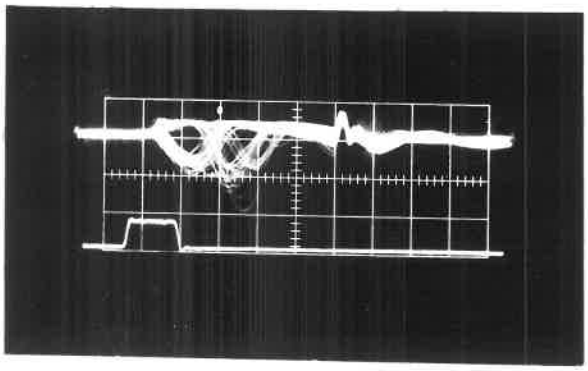


(b)

TOP TRACE: GATE WAVEFORM 5V/cm
BOTTOM TRACE: AMPLIFIER OUTPUT 2 V/cm

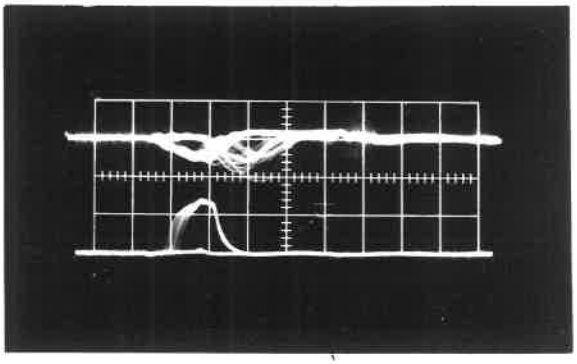
TIME SCALE: 0·2 μ SEC. / cm

FIG. 60 WAVEFORMS THROUGH SENSE AMPLIFIER FOR '1' & '0'



(a)

TOP TRACE: INPUT SIGNALS 0·5 V/cm
BOTTOM TRACE: READ CLOCK 5 V/cm



(b)

TOP TRACE: GATE INPUT 5 V/cm
BOTTOM TRACE: AMPLIFIER OUTPUT 2 V/cm

TIME SCALE: 0·2 μ SEC./cm

FIG. 61 WAVEFORMS THROUGH SENSE AMPLIFIER FOR SCAN OF 64 WORDS

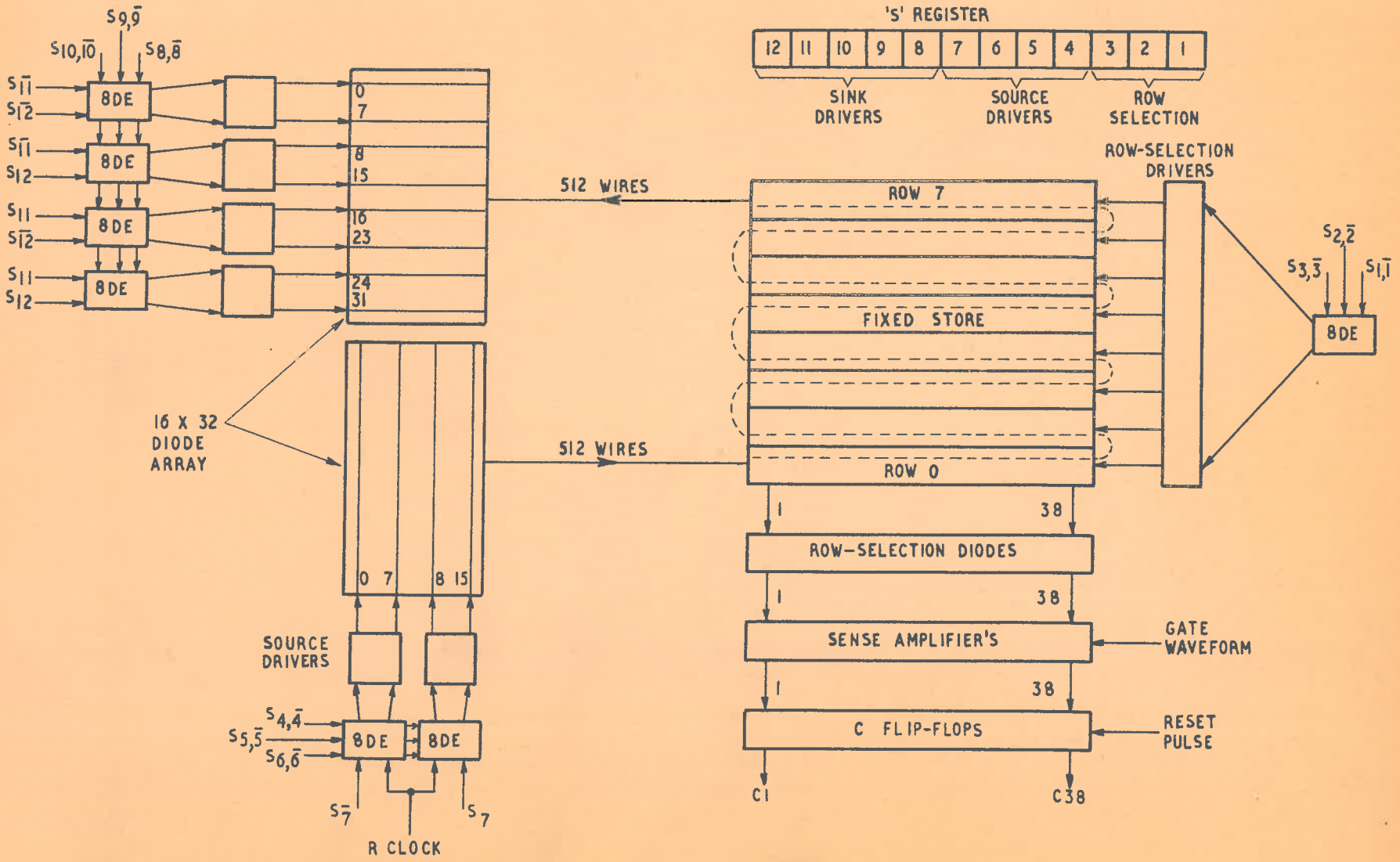


FIG. 62. BLOCK DIAGRAM OF THE CONTROL FIXED STORE

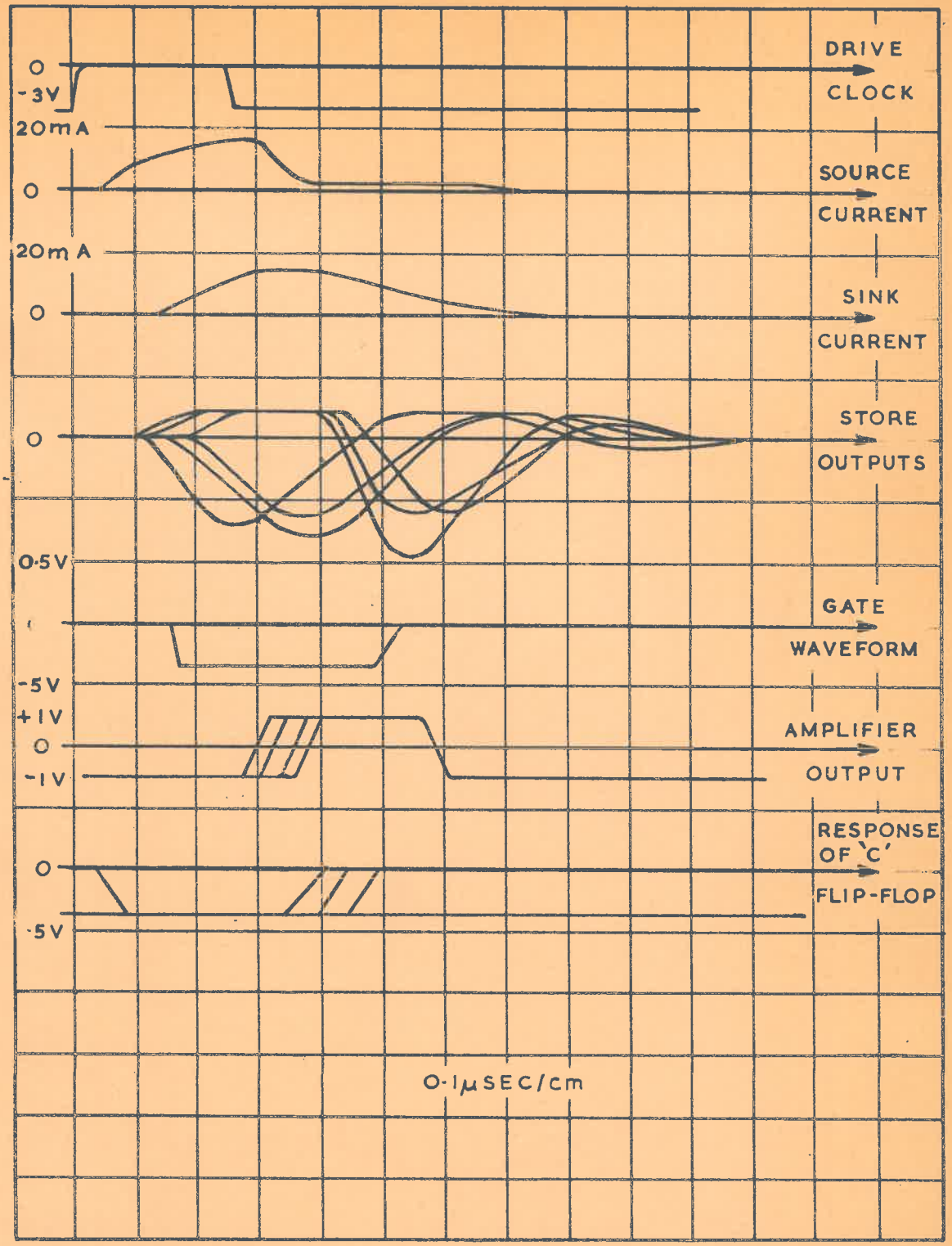


FIG. 63. TIMING OF FIXED STORE

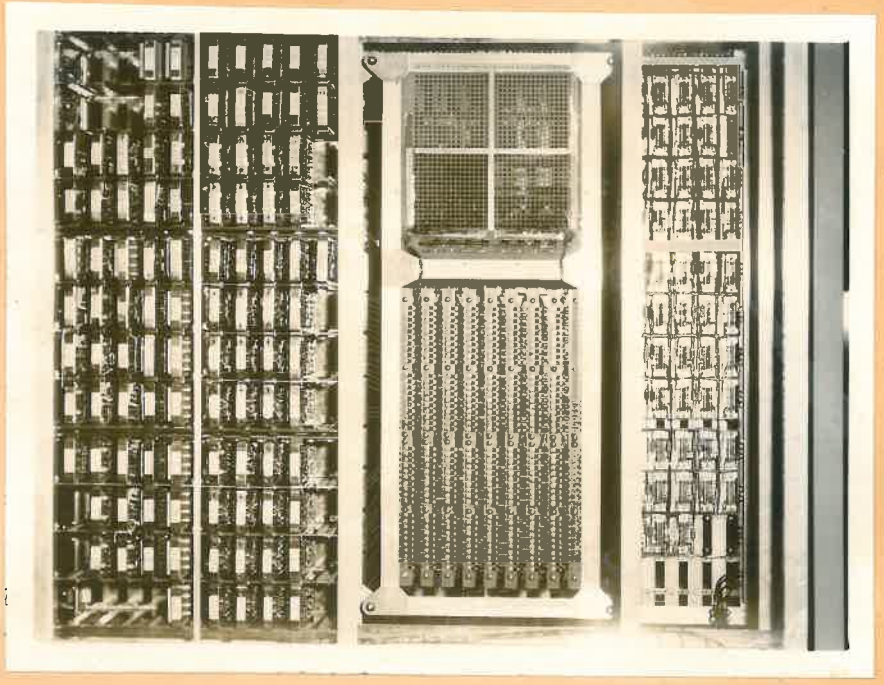
reduced. The limit is imposed by the recovery of the array from drive currents and address changing transients.

The word read from store contains two parity bits. The states of the C flip-flops are continually monitored by two parity check packages which cause an immediate stop if an incorrect parity is detected. To assist in the checking of the wired information, one parity bit is determined by all odd bits and the other by all even bits. The most likely source of error in both wiring and checking the information is to interchange or skip one bit in a sequence. With the parity arranged as above, this error will be detected by the parity check as well as a normal failure due to an incorrect read. The information is also treated as a series of octal numbers both to facilitate reading and to minimise errors.

The mechanical assembly of the control fixed store is shown in Fig. 64. The circuits are contained in packages similar to those employed for the core stores. The decoding, driving and output circuits require 300 transistors and 2000 diodes. The total cost of the store was approx. £1,000 - £500 for components and materials and £500 for labour. Wiring speed was better than 1000 bits/hr. giving a total cost of £150 to wire the complete store, a relatively small factor in store cost.

(3) SOME DISADVANTAGES OF THIS TYPE OF FIXED STORE :

The concept of this store was originally tested with a 12 x 4 model with the I pieces mounted on a separate plate. In this size the store was quite successful, but when the full size store was built the method of construction proved to be unsatisfactory. Unreliable contact between the E and I pieces required that the top plate be replaced by a set of separate spring clips, allowing each I piece to be individually



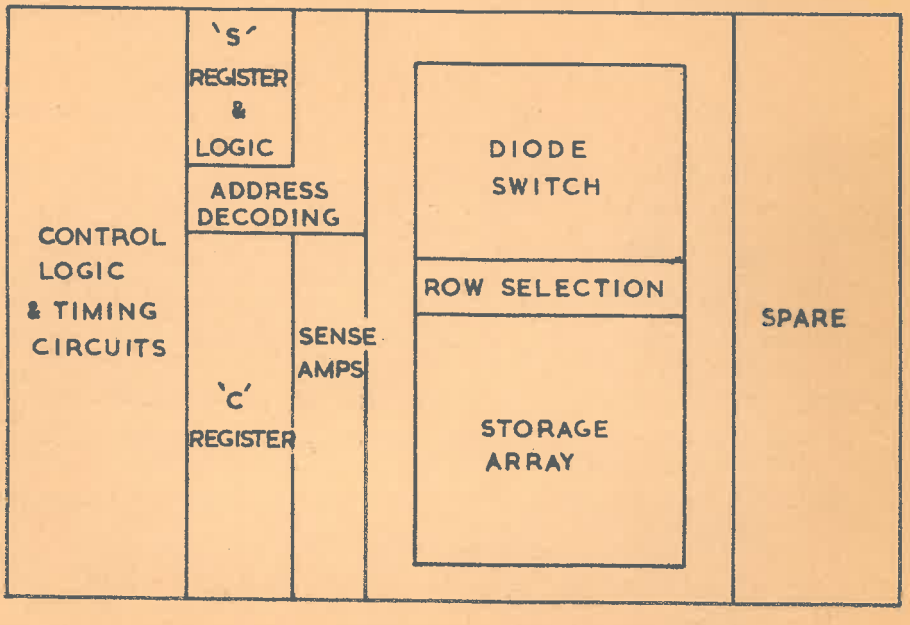


FIG. 64. MECHANICAL ASSEMBLY OF CONTROL FIXED STORE

adjusted for good contact. The removal of 320 clips and I pieces and the subsequent adjustment when replaced made additions or modifications to the store a tedious process. Fortunately, the store did not prove to be unduly sensitive to poor contact when in service, due largely to the ability of the sense amplifier to detect the resulting poor signals. The checking facilities on the store also allowed any marginal behaviour to be quickly corrected. When initial test patterns were threaded into the store it was found that the sharp edges of the ferrite cut through the insulation of the wire. Since the ferrite used was of relatively low resistivity, low impedence paths were established between wires and from drive wires to the output winding, giving poor output signals. Each E core was therefore coated with a suitable epoxy resin to protect the insulation of the wire.

During threading the wire passes through a 6" length of glass tube, the end of which is drawn down to a fine point. This tool allows the wires to be placed neatly into the E cores, but care must be taken to ensure that wires do not jump over the centre leg of the E core and that the wires do not build up around the centre leg or between the cores. Nylon "fingers" placed between the cores allowed the wires to be threaded loosely and minimised these effects, but were inconvenient during wiring. The wires were also held in place with wax every 10 bits as a further precaution. Nevertheless, the above considerations would probably limit store capacity to 256 wires or 2048 words. This would not place any serious restriction on the computer in either application but the additional capacity could certainly be used if available.

Similarly, the inconvenience of using separate clips for the I pieces instead of a single plate is not very serious since with either method the computer would be out of service for a considerable period while alterations or additions were made to the store contents due to the

time required to insert a wire. After an initial testing phase of both the computer and the programs, the contents would not need to be changed very frequently. However, if a quick change were possible, this could on occasions be used to advantage, since by changing the contents of the control fixed store either completely or in part, the order code and behaviour of the computer can be changed. Such a facility could on occasions be very useful and in the later stages of machine design, a greater emphasis was placed on the ability to make rapid changes of the stored information.

Most of the above restrictions were apparent in the early stages of testing the full scale store. It was felt, however, that this store could be made to work reliably and to ensure that the development of the computer would not be held up by lack of a control unit, the store was completed although not wired with the full order code. Development was also commenced on a second version which it was thought would provide a better and more flexible fixed store. This configuration had been tested earlier but at the time was rejected in favour of that using E cores. In the subsequent discussion, the two types of store will be called MkI. and Mk. II. for each of reference.

(4) AN IMPROVED FORM OF FIXED STORAGE - Mk. II :

(4.1) THE PRINCIPLE OF OPERATION :

The concept of the two stores is very similar in that each uses a multi-row inductively coupled array. The difference lies mainly in the method of achieving coupling between the input and output wires and a corresponding change in the mechanical construction (Fig. 65 and 69). The coupling element in each bit position consists of a rod of 3 B. ferrite 76 mm. long and 1.6 mm. diameter, wrapped with an output winding of 200 turns and enclosed in a glass tube for mechanical support. These elements are then inserted in the base plate to form the array.

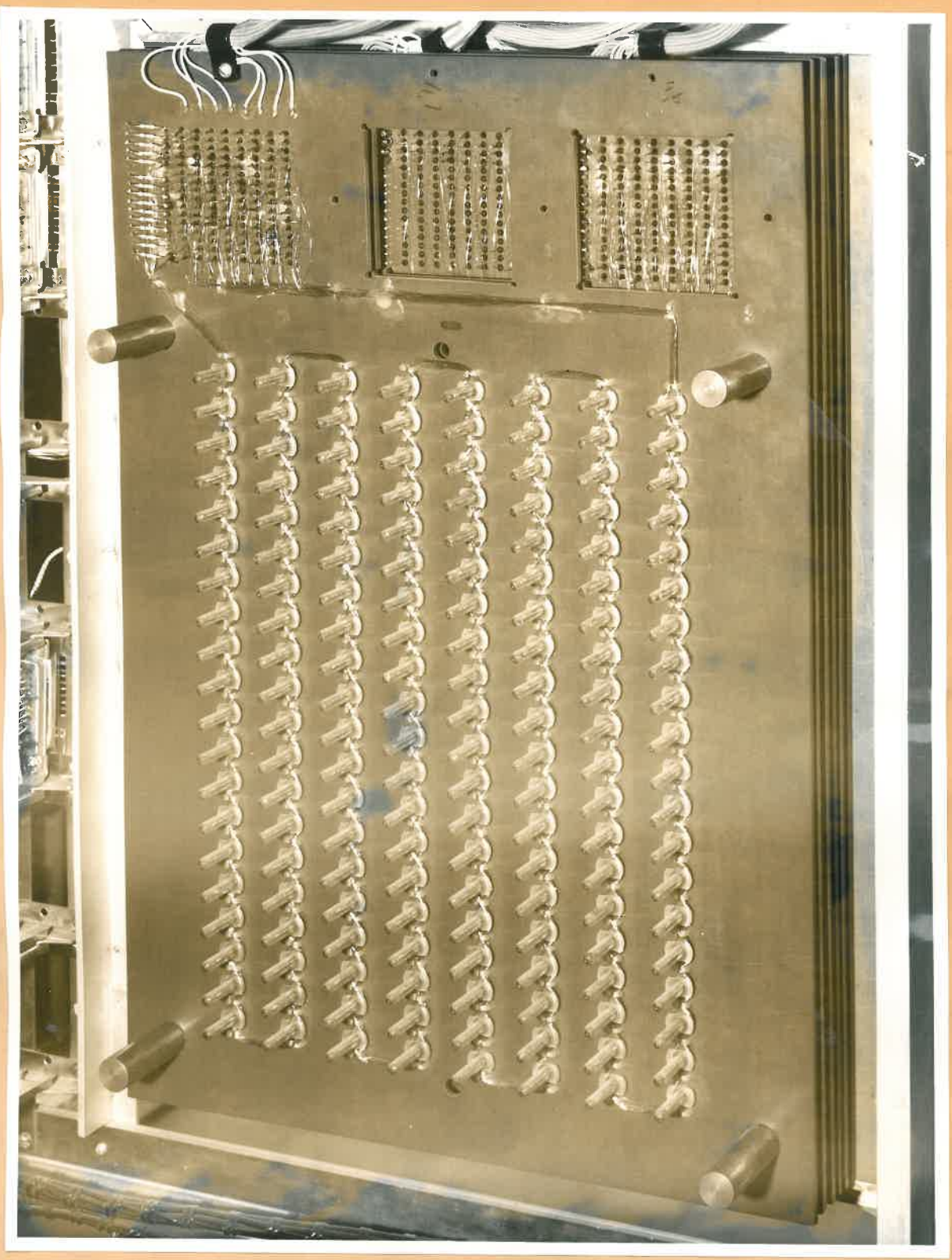


FIG.65. MECHANICAL CONSTRUCTION OF MK. II FIXED STORE

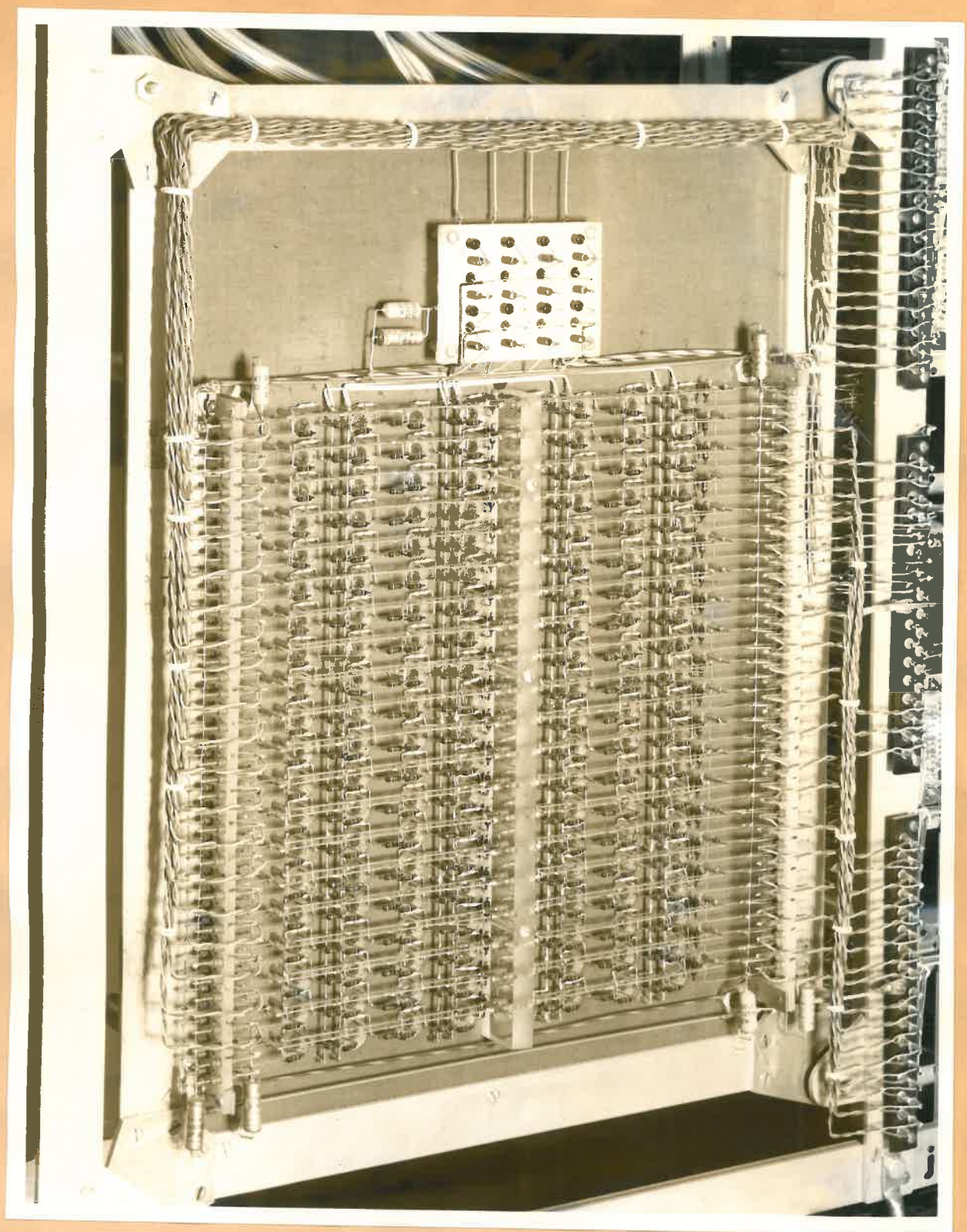


FIG. 65 MECHANICAL CONSTRUCTION OF MK. II FIXED STORE

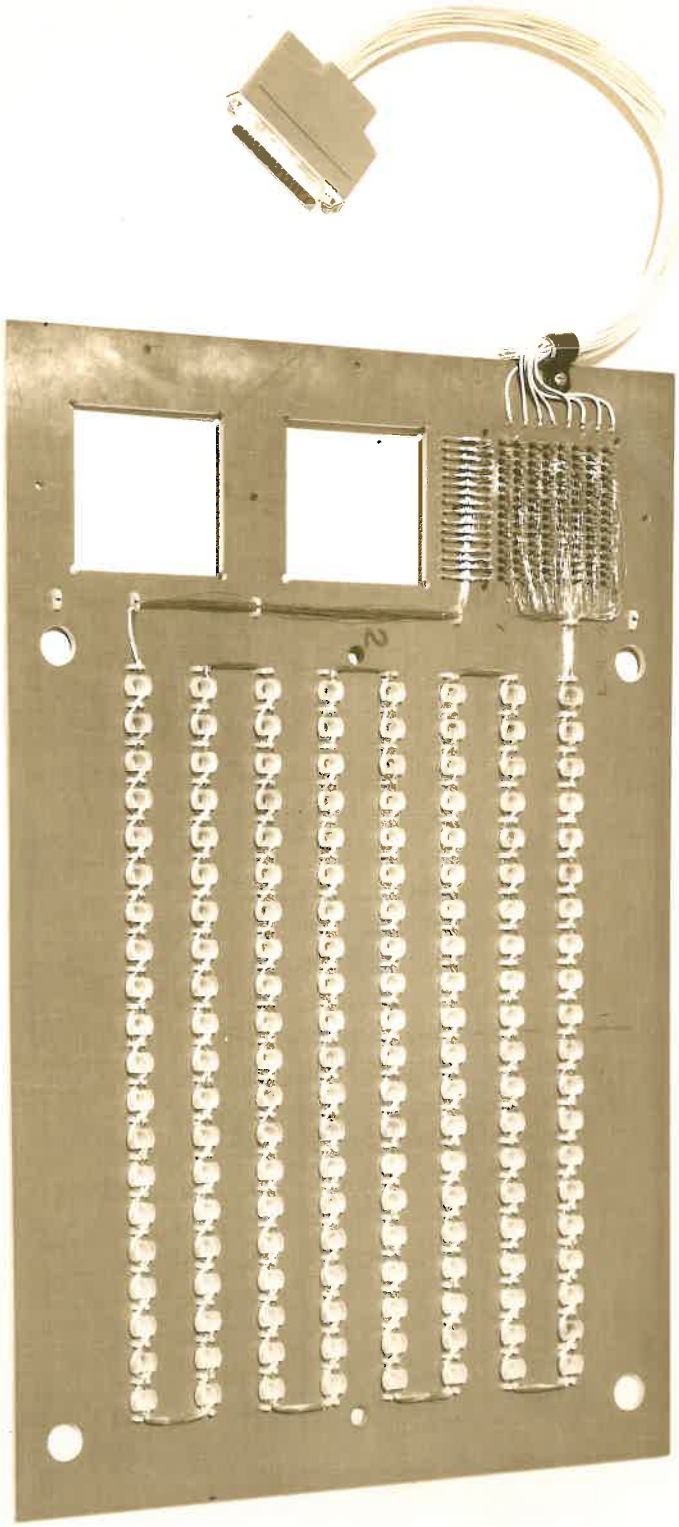


FIG. 65. MECHANICAL CONSTRUCTION OF MK. II FIXED STORE

The input wires are woven around guides on the plate which is then placed over the array of rods. Up to 8 plates each with 128 wires can be accommodated. When a wire is driven, a positive or negative signal is induced in the output winding, depending on which side of the rod the wire passes.

The response of these elements to a drive pulse is very similar to that of the E core element. The output winding is an over-damped resonant circuit excited by energy transferred from the drive winding. The magnitude and polarity of the output signal are determined by the magnetic field intensity experienced by the rod as a result of the current in the driver wire.

For the conditions shown in Fig. 66 (a), the H at point P due to I is

$$dHp = \frac{I \sin \theta_2 \, dl}{4 \pi r^2}$$

If the current flows in a circular path of radius R around P, then

$$Hp = \frac{I}{2R}$$

The path of a drive wire around a rod (Fig. 66 (b)) can be approximated by a segment of a circle, giving

$$Hy = K . \theta . \frac{I.}{d}$$

where K = constant

and θ = angle subtended by sector.

The flux in the rod at this point is therefore

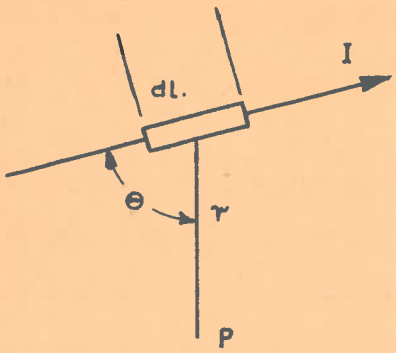
$$\phi_y = \mu H_y A$$

and a voltage

$$e_y = n \frac{d\phi}{dt}$$

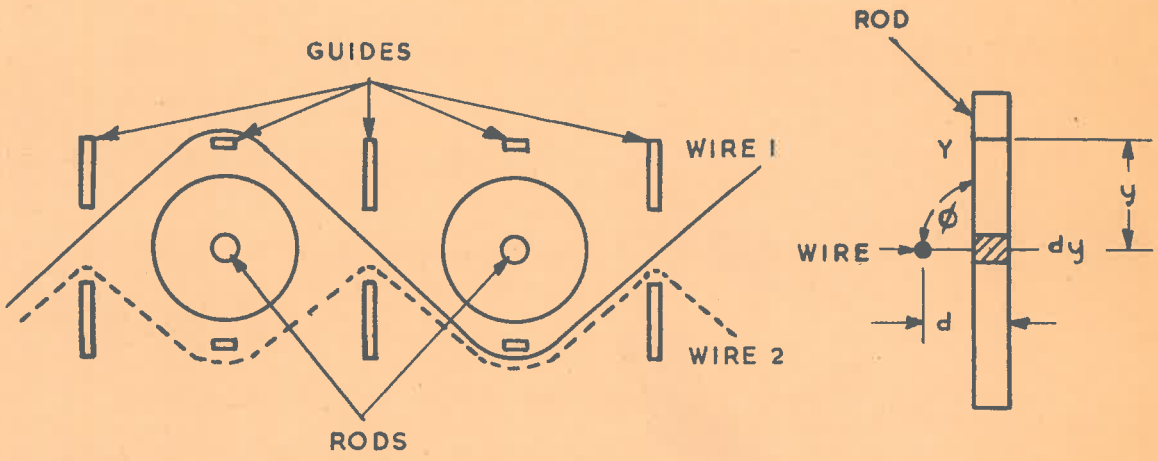
$$= \frac{Kn \, \theta \, \mu . A}{d} \cdot \frac{dI}{dt}$$

is induced in the section, dy, of the output winding.



$$dHp = \frac{I \sin \phi}{4 \pi r^2} \, dl.$$

(a)



(b)

FIG. 66 WIRE PATH IN FIXED STORE

The other sections of the output winding will also contribute to the output voltage. At Y, a distance y along the rod, the H acting along the rod is

$$H_Y = H_y \cdot \frac{d^2}{d^2 + y^2} \cdot \cos \phi$$

$$= H_y \frac{d^3}{(y^2 + d^2)^{\frac{3}{2}}} \frac{3}{2}$$

For $y = 2d$,

$$H_Y < 0.1 \, H_y$$

indicating that only the section of rod adjacent to the wire contributes significantly to the output.

The total induced voltage can then be approximated by

$$e = \frac{C.N.\Theta.u.A}{d} \cdot \frac{dI}{dt}$$

where C = constant

N = turns per unit length of the output winding

Θ = angle subtended by the segment of the drive wire adjacent to the rod.

u = permeability of the rod material.

A = area of cross-section of the rod

d = distance of wire from rod.

This voltage represents an impulse applied to the resonant output winding which will then respond in a manner which depends on the circuit Q. To provide rapid recovery from the drive pulses and any transient due to address changing, without any undesirable ringing, the output winding is slightly over-damped with a shunt resistance.

This analysis is simplified in several respects. Only the section of the drive wire adjacent to the rod is considered but other sections of the drive wire will also contribute to the total H at each rod position. Since $H \propto \frac{1}{r^2}$, the effect of these sections is small

and in any case would only change the scaling factor C. Due to the open magnetic path of the rods, some cross-talk between elements can also be expected if these are closely spaced.

The analysis does show the significant factors which determine the output voltage, i.e. the distance of the wire from the rod, the permeability of the material, the area of cross-section of the rod, the winding pitch and hence number of putput turns, and of course, the drive current, but the system was determined largely by the practical considerations of how the store could be built, the physical size and capacity required and the materials available. These factors led to the construction shown in Fig 65.

The output signals from the store for various output windings are shown in Fig. 67. using the preamplifier shown. These signals are for the worst case conditions as discussed below. The output voltage does not increase significantly with increasing turns due to the greater damping required to prevent oscillations in the output. The output from this store is lower than that available from Mk I, the worst case signal being approx. 100 mV. In comparison with other types of store this is quite satisfactory but the lower signal level required more sophisticated row selection circuits than those used for Mk I. These are discussed in a later section. A balanced sensing system required for other reasons also eliminated the capacitive coupling apparent in these waveforms.

The magnitude of the cross talk between elements is shown in Fig. 68. These results were taken by measuring the output of the centre element of a group of 3 for both aiding and opposing crosstalk. To minimise the effect of a different θ for the two patterns, 5 turn

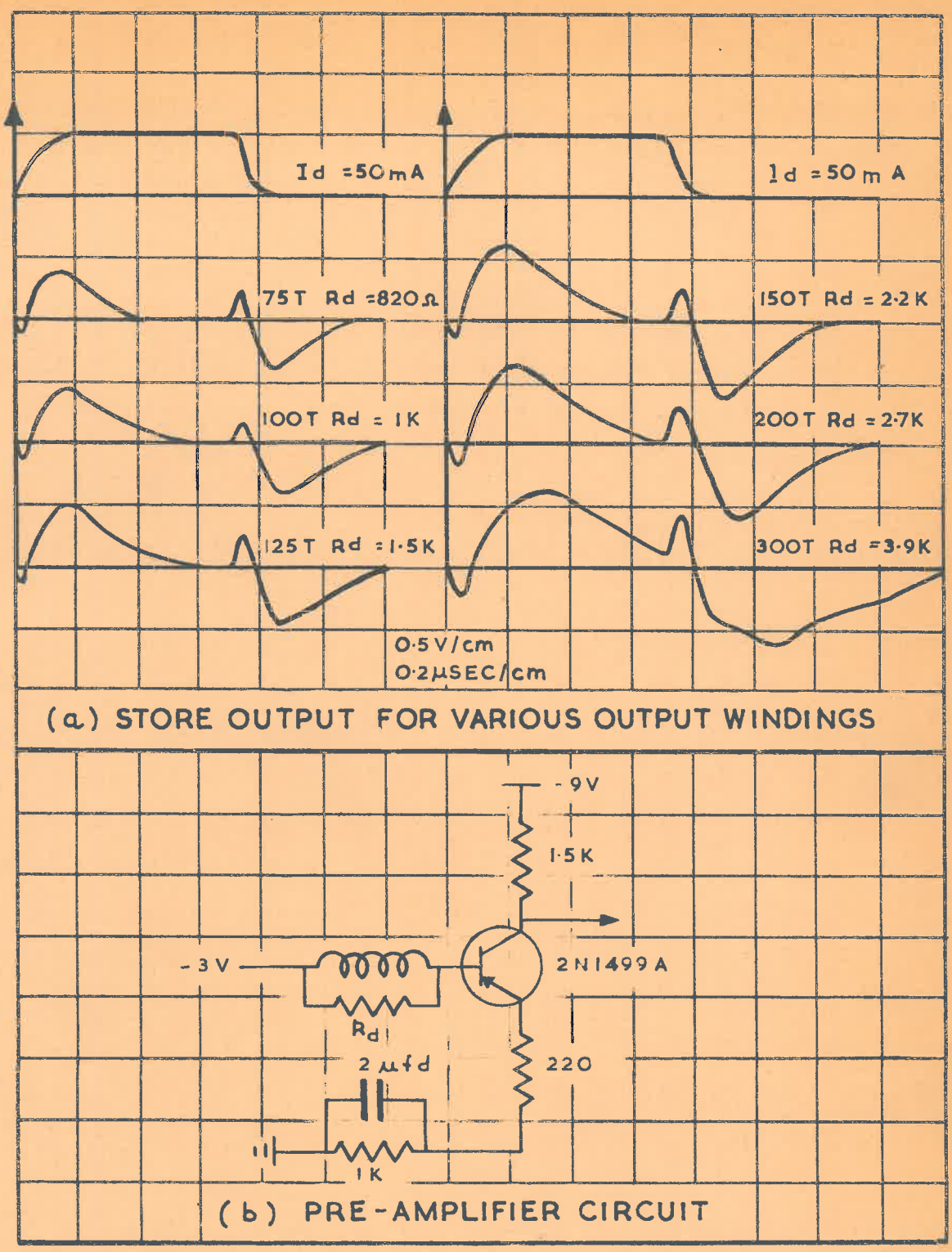


FIG. 67. RESPONSE OF COUPLING ELEMENT

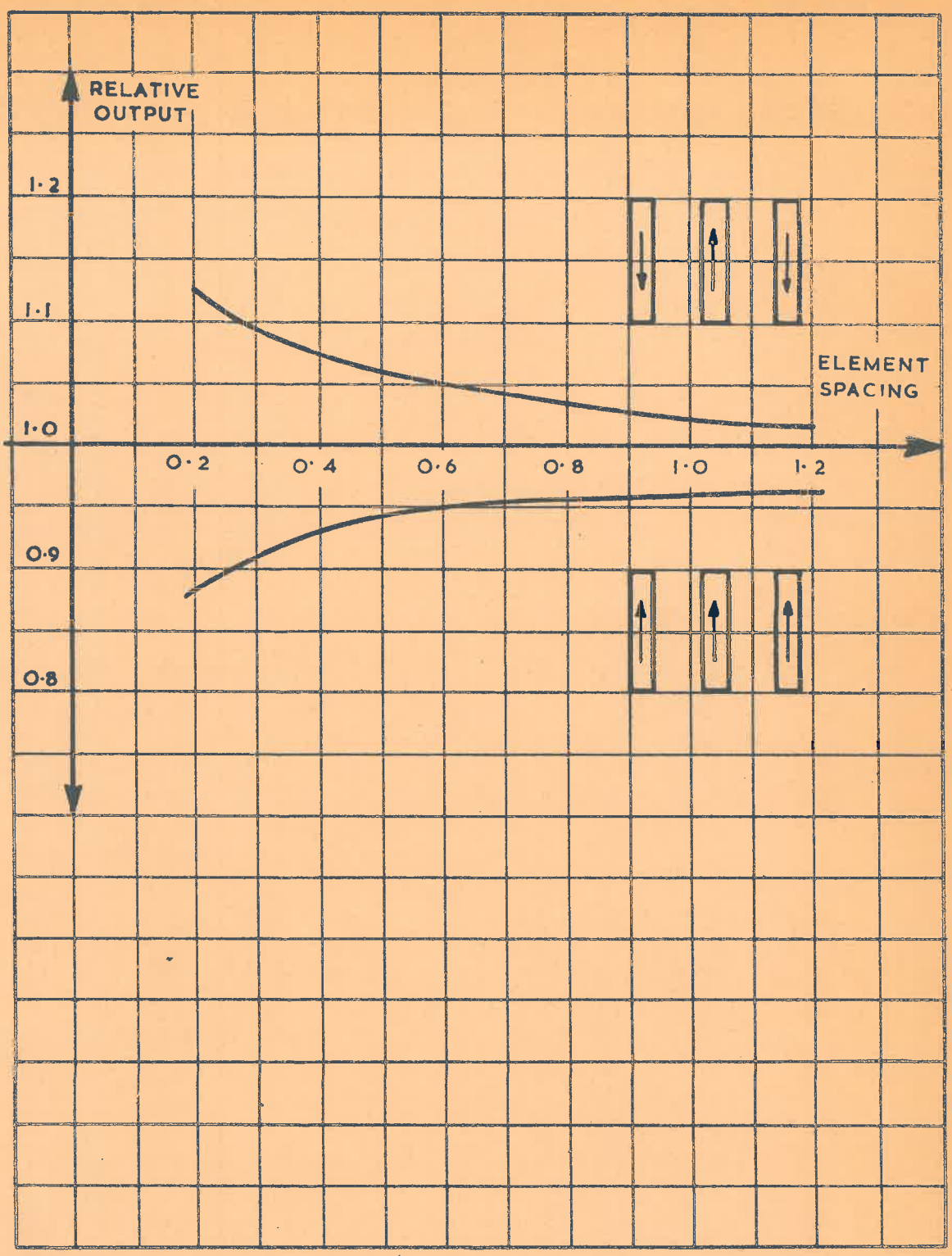


FIG.68. OUTPUT AMPLITUDE RELATIVE TO AN ISOLATED ELEMENT FOR VARIOUS ELEMENT SPACINGS.

windings were used around each element. As expected the crosstalk increases as the element spacing is reduced. The crosstalk in a larger array is only slightly greater than in this simple system and at the spacing employed, ½" between elements in a row and 1" between rows is less than $\pm$ 10%.

Pattern sensitivity due to the wiring configuration is much more significant. If consecutive '1's or '0's are wired into the store, the amount of wrap around the element is considerably less than if alternate '1's and '0's are wired. Since the output signal is approximately proportional to the amount of wrap, the output signal for these two cases can differ considerably. The above effects are additive, i.e. the pattern giving minimum wrap also gives opposing crosstalk and the ratio of maximum to minimum signal from the store can be as high as 3 : 1. This is not a serious objection with polarity discrimination. Dummy rods inserted between the elements had little effect on either the output or crosstalk. In any case they would have been avoided if possible for the sake of mechanical simplicity.

The output signal also varied with the position of the wire along the rod, nominally falling to half value at the end of the element. To prevent this affecting the store output, the rod was selected to be 1" longer than the stack of plates, allowing ½" spare at each end of the rod. Since each of the 8 plates was ¼" high, a total rod length of 3" was necessary. A non-linear distribution of the output winding was also employed, with the winding pitch reduced at the ends of the element. The output was then virtually independent of the wire position.

(4.2) MECHANICAL CONSTRUCTION :

The range of suitable ferrite shapes and materials available was rather limited. Only two shapes, a rod of 1.6 mm diameter and a tube

of 4 mm OD and 2 mm ID were potentially useful. Both could be obtained in a range of ferrites but the maximum standard lengths were well short of the required 3". However, by arrangement with the local manufacturer, the rod could be produced to this length from 3 B ferrite, so this shape and material were chosen for the elements.

The dimensions of the rod made some form of mechanical support essential. This was provided by enclosing the rod with its output winding inside a non-metallic tube (see Fig. 69). To maintain a high output signal, the distance between the rod and the wire should be kept as small as possible. Three dimensions are involved, the wall thicknesses of the tube and wiring bobbin and the clearance between the tube and bobbin. The tube material must be strong and rigid to provide sufficient support with a small wall thickness and any tendency to warp will reduce the clearance with the bobbin. Although rather brittle, glass proved to be the most suitable material for the application. A convenient size was available and the tube was selected to have an OD of 175 thou. $^{+0}_{-5}$ thou. and an ID of 90 thou. $^{+5}_{-0}$ thou. The wiring bobbins on the plates had an internal diameter of 200 thou. and a wall thickness of 25 thou. The minimum clearance between tube and bobbin was therefore 12.5 thou.

A number of factors influence the minimum practical clearance, the accuracy to which the plates and base can be drilled, the accuracy to which the elements can be mounted perpendicular to the base and the stability of the base and plate materials. The first is ensured by making an accurate jig for drilling both the base and the plates. Only a 20 x 4 jig was required, the other half being drilled with the jig reversed. The plates were then a mirror image about the longitudinal centre line and could be placed either way over the rods. The second proved to be rather difficult. The glass tube varied in

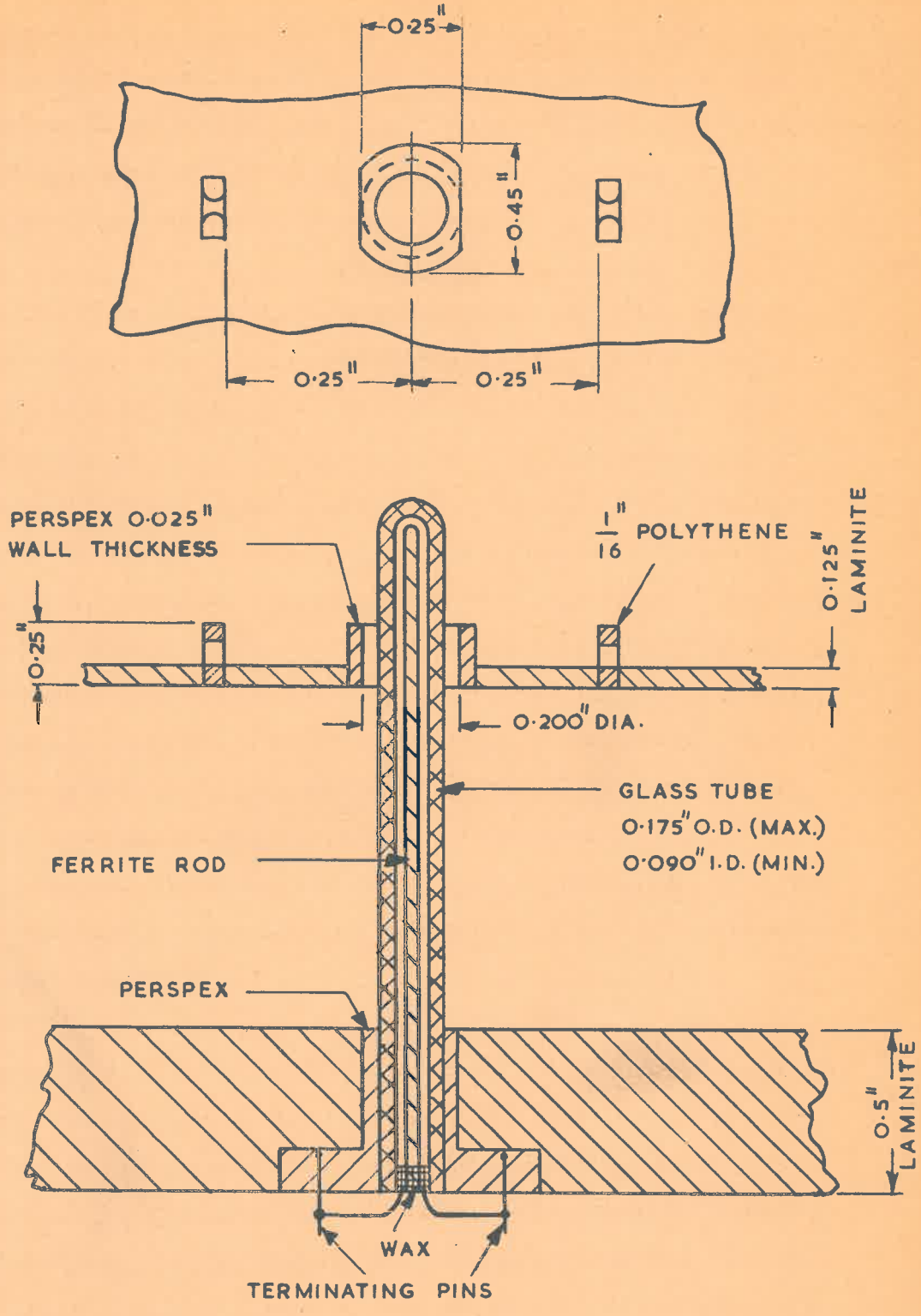


FIG. 69. DETAIL OF MECHANICAL CONSTRUCTION OF MK II FIXED STORE.

diameter and was often several thou. out of round. The tube had to be mounted vertically with an eccentricity of less than 5 thou. at the end of the tube. Approx. 2. 3/4" of tube projected from the base plate. The first ½" of the rod, allowed to provide uniform signals over the rod was contained within the base plate. The plates could then be stacked directly on the base plate and the unsupported length of the tube was minimised. The method used to provide the required mounting accuracy is shown in Fig. 69. A bush turned roughly to size was cemented on to the tube and then turned to the correct size with the tube held in a collet, ensuring concentricity of the tube and bush. The holes in the base plate were lightly reamed to provide accurate and vertical holes. The bushes are a firm fit in the base plate so the assembly can be easily removed if broken. This method involved much accurate and tedious machining but the results achieved were quite satisfactory. Both the base and plates are extensively machined and subject to stress due to the firm fit of the bushes and wiring bobbins resp. Any tendency to warp or creep under these conditions was minimised by making these from a high grade, cloth-based bakelite board, ½" thickness for the base and 1/8" for the plates. The clearance around the four corner pillars is much less than that around the rods, so that when placed on the store it should not be possible for the plates to touch the rods. The clearance shown in Fig. 69 proved to be sufficient although careful construction was essential.

In view of the small clearances and the need for rigidity, it was thought safer to build a 20 x 8 array rather than the 40 x 8 array of Mk. 1. The overall dimensions of the array are 16" x 11" with the array of rods requiring an area of 9½" x 7", Each word occupies two rows, requiring a slight change to the row selection circuits for the control fixed store but well suited to the machine language fixed store

which stores half words as in the core stores. As with Mk.I fixed store the 40 bit word length contains 36 information bits, 2 parity bits and 2 strobe bits. The strobe bits were provided in case a self-derived strobe was required, but a fixed strobe proved quite satisfactory and these bits were not used.

Both fixed stores can use the same plate. These are prepared by drilling the holes for the bobbins and corner posts with the jig used for the base. The slots for the wiring guides are punched using these holes as a reference. The bobbins and guides are then pressed into the plate. The total height of each plate is ¼". A diode switch provides the wire selection with the appropriate section of diode matrix mounted on the plate making each plate a self-contained unit requiring only 24 connections to the drivers. The diodes are mounted perpendicular to the plate requiring a total height of approx. ½". Clearance for the switch diodes when the plates are stacked is provided by mounting the diodes in one of three areas on the plates. The other two areas are cut out, allowing the diodes to project through adjacent plates. Some restrictions are therefore placed on the stacking order of the plates, but the position occupied by a plate is irrelevant provided the appropriate drivers are connected to the plate.

The wiring of the plates is a relatively simple process. The wires are firmly held by the bobbins and wiring guides which determine the path of the wire and are held at each end by wax. The wire is threaded on to the plate with a tool similar to that used for wiring Mk.1. store. Wire of 3.5 thou. diameter with a double covering of self-fluxing enamel is used. The 128 wires can be comfortably accommodated, allowing space for corrections or alterations to the store contents.

The row selection circuits employed are similar to those used on Mk.1 store. The row selection driver and the diode gates are mounted directly on the base of the store with buffer emitter followers to ensure that the wiring between the store and the sense amplifier is relatively insensitive to stray pick-up and capacative loading.

(4.3) THE DRIVING CIRCUITS :

The driving behaviour of this store differs considerably from that of Mk.1. The most significant factor is the reduced drive impedance due to the smaller amount of magnetic material present. The inductance of the drive wire is, in fact, due almost entirely to the self inductance of the drive wire, increasing by less than 10% when the plate is placed over the rods. The impedance of the wire is approx. 10 Ω and 3 μ H, neglecting the diode in the selection switch. A much higher drive current can therefore be used without introducing excessive drive voltages.

The same type of selection circuit, i.e. diode switch, was employed, but in this case a 1 of 1024 selection had to be made. For convenience in decoding and to reduce the switch leakage, the switch was arranged as a 16 x 64 matrix with 16 sink drivers and 64 source drivers. The switch was divided into 8 sections of 16 x 8 one of which was mounted on each plate. The 16 sink drivers are shared by all plates but each has a separate set of 8 source drivers and is in effect driven independently of the other plates. It was found that a satisfactory switch performance could be achieved with only one diode per wire, avoiding much of the trouble experienced with Mk.1 store.

A number of factors contributed to this improved performance. The second diode was introduced in Mk.1 to isolate the capacitive coupling between the driven wire and the bundle of non-driven wires,

reducing the capacitively coupled spurious currents and improving the propagation of the drive pulse through the store. In Mk. 11, each drive line was shorter, the drive voltage was lower, being only an inductive spike during the rise of the drive current and the magnitude of drive current was much greater, 75 mA c.f. 20 mA. The drive wires and diode switch were also effectively subdivided into sections of 128 wires so that only the coupling within a plate was significant. The capacitive current which remained was present only during the rise of the drive current and although of considerable magnitude was too short in duration to cause significant trouble. Spurious currents in the nonselected wires on the selected sink were trivial. Only 7 wires were involved and the voltage swing of the source driver was such that these diodes were always reverse biassed. Inductive coupling between the drive wires was much less than in Mk. 1 and was not a significant factor in switch behaviour.

The address decoding and switch driver circuits differ considerably from those used for Mk. 1. A block diagram of the address decoding is shown in Fig. 70. Plate selection and source selection are shown as separate functions but the two are in practice used concurrently to select 1 of 64 sources, i.e. 1 of 8 sources on 1 of the 8 plates. The 8 DE and 4 DE packages used for sink and row selection respectively are identical to those described earlier, providing a 1 of 8 or 1 of 4 decoding with output levels of + I V for the selected output and - I V for the non-selected outputs. The 8 DI package, Fig 71. uses the same logic as the 8 DE but has an inverting output stage to provide a level of - 1 V on the selected output and + I V on the non-selected outputs.

The source and sink drivers are shown in Fig. 72. The sink driver applies a potential of -20 V. to the switch when selected or O V if non-selected. A complementary emitter follower is necessary to

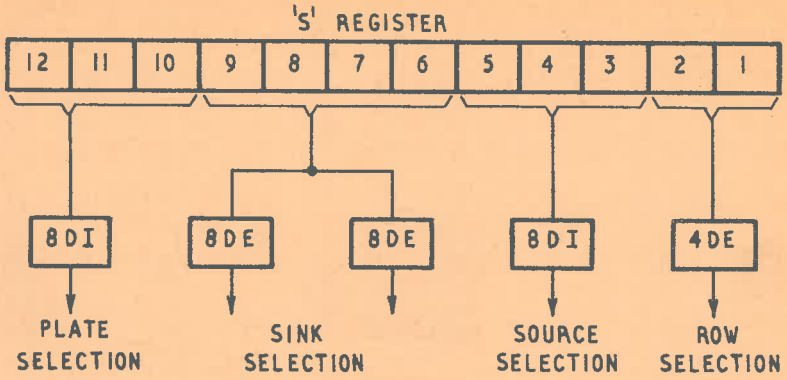


FIG. 70. ADDRESS DECODING FOR FIXED STORE

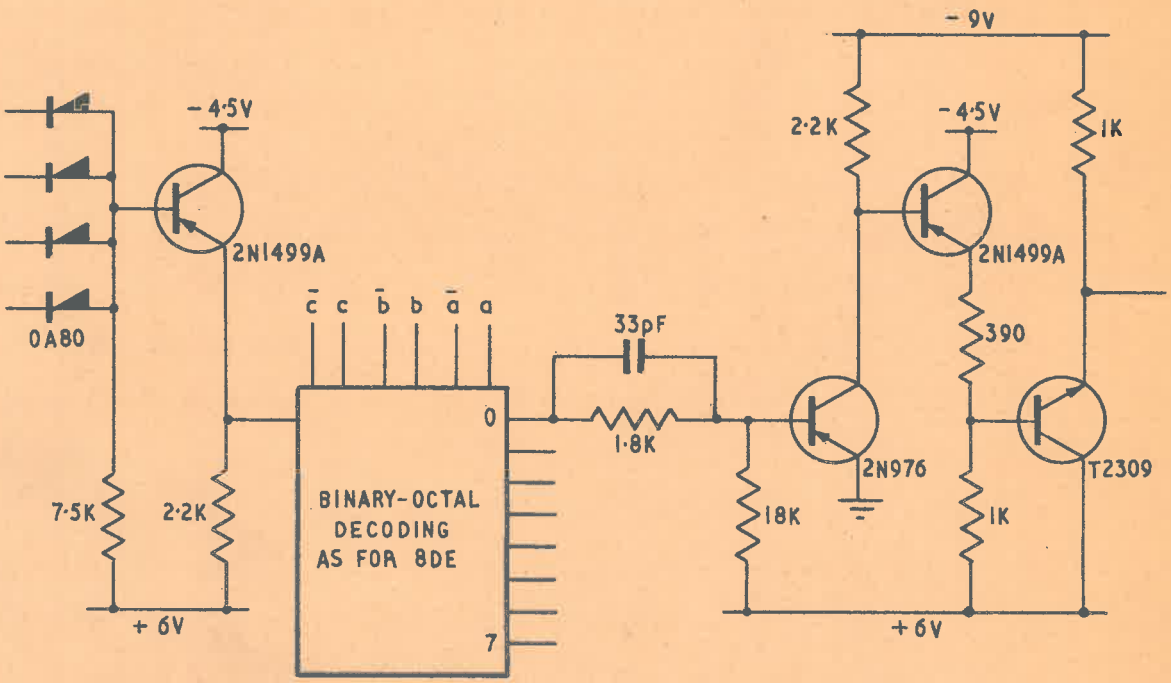
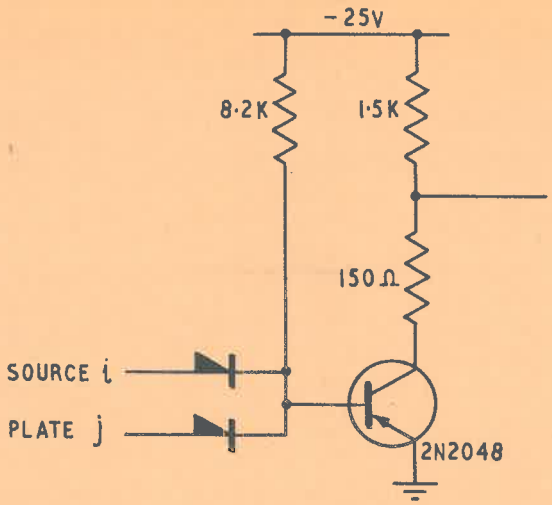
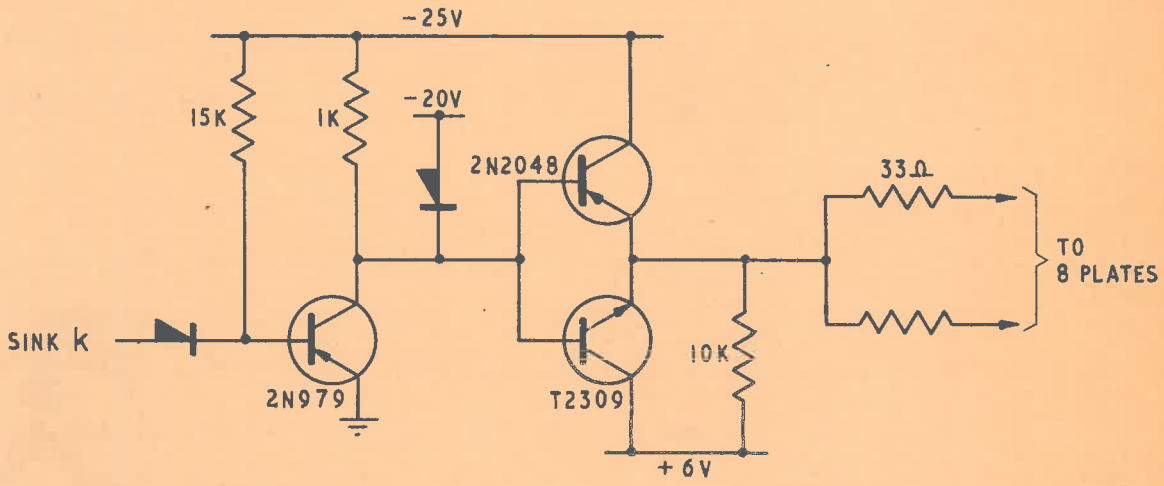


FIG. 71. 8DI PACKAGE



(a) SOURCE DRIVER



(b) SINK DRIVER

FIG. 72. SWITCH DRIVERS

to drive the capacity of the plate wiring during address changes. The selected wire is then driven by selecting 1 of the 64 source drivers. This is selected if both the plate and source inputs are at - 1 V. The driver delivers a 70 mA 0.4 μsec pulse to the selected wire. The current is determined by the series resistance in both the source and sink drivers and the forward voltage of the switch diode (OA91). The resistance is split as shown to prevent an oscillatory sneak current into the non-selected sinks by capacitive coupling from the selected wire. The 33 Ω resistor damped the oscillation, leaving a pulse of spurious current during the rise of the drive current but this was not of sufficient magnitude or duration to significantly affect the store outputs. A separate resistor is provided for the sink connection of each plate to minimise the effect of the resistance on the charging current during address changes. The 150 Ω resistor in the source driver also limits the positive swing of the source driver to approx. -6 V. ensuring that none of the diodes on non-selected wires can be forward biassed.

Despite an increase in the size of the switch from 512 to 1024 outputs, and an increase in both the speed and power of the outputs, these circuits require no more semi-conductor elements than those for Mk. 1 store. Both require approx. 180 transistors and 1200 diodes. This is achieved by decoding at a higher power level for Mk. 11 and by the need for only one diode per wire. All diodes and transistors are relatively inexpensive types.

(4.3.1) THE PERFORMANCE OF THE DRIVE SWITCH :

The significant waveforms through the drive system are shown in Fig. 73. A delay of 80 nsec. occurs between the application of the read clock and the rise of the drive current. Most of this delay is due to the response of the 2N2048 in the source driver. The duration

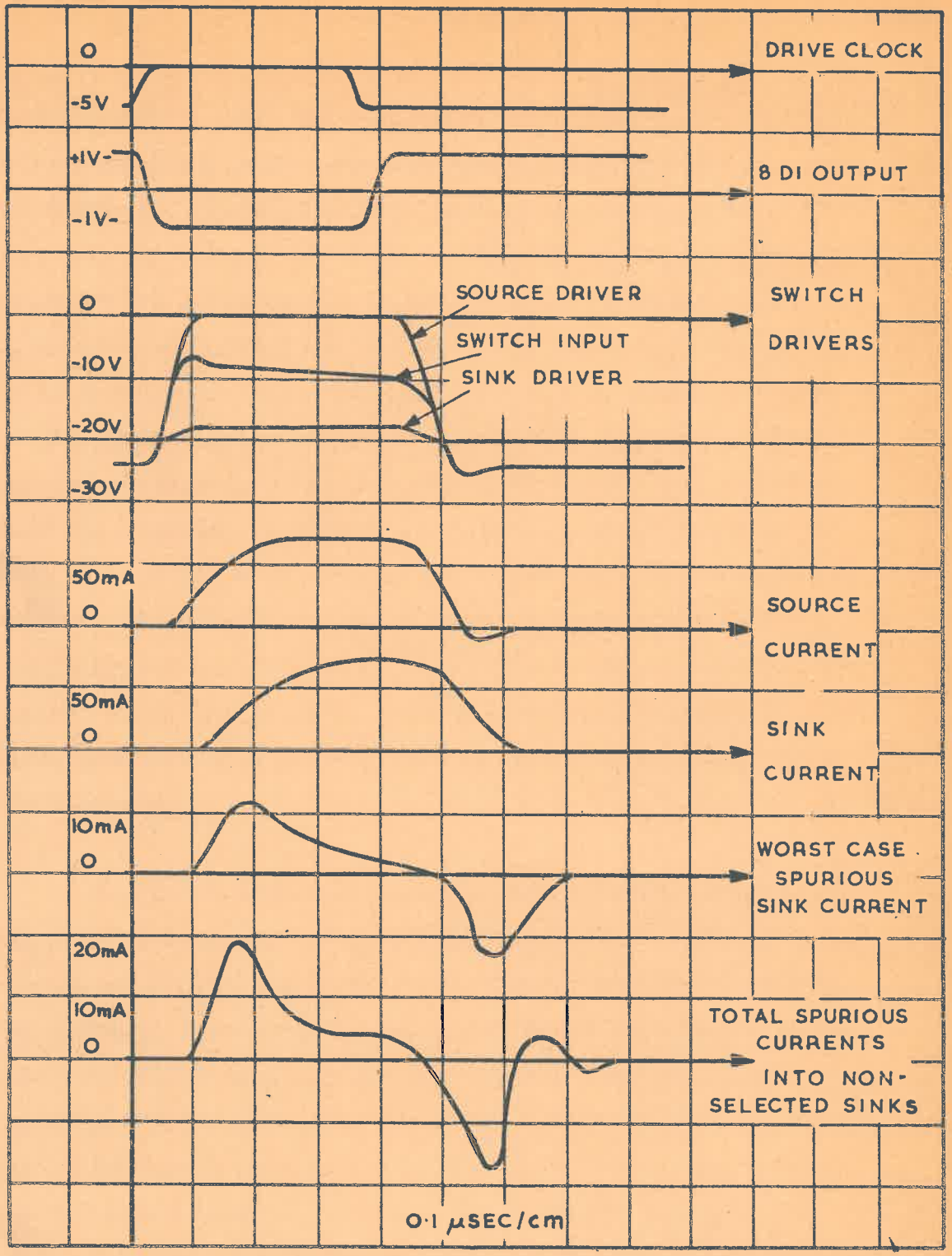


FIG. 73. DRIVE SYSTEM WAVEFORMS

of the drive current varies between 400 and 500 nsec. due to variations in the storage time of the 2N 2048. This has little bearing on the store behaviour so no attempt was made to achieve a more consistent performance. A delay of approx. 30 nsec. is apparent between the current at the source and sink ends of the store. The driving impedance of the store is dominated by the switch diode. These diodes require a forward bias of 7 V. to pass the 75 mA drive current while the rise time of the drive pulse is determined by the forward transient of the diode rather than the impedance of the drive wire. A spurious current of approx. 20 mA peak value is transferred to the non-selected wires by capacitive coupling from the driven wire, passing out of the store via the non-selected sinks. As discussed above, the duration of this current is too short to significantly affect store outputs. The other possible spurious currents could enter the store via the diodes at the source end of the stove. Both of these currents, via the diodes on non-selected sources and via the non-selected diodes on the selected source are trivial.

The performance of the drive switch on Mk. 11 store is far superior to that of Mk. 1. The improvement is due largely to the lower impedance of the drive wires and reduced coupling between wires. The spurious currents due to capacitive coupling and to a lesser extent inductive coupling were confined to a pulse of current during the rise of the drive current. The short duration of these currents and the smaller value relative to the current in the selected wire allowed acceptable performance to be achieved with one diode per wire, avoiding most of the trouble experienced with Mk. 1 store. The subdivision of the switch and associated store wiring into 8 sections was also a significant factor in the improved switch performance.

(4.4) THE OUTPUT CIRCUITS :

The outputs from Mk. 1 store showed considerable variation

in waveform, amplitude and timing and did not allow direct clocking of the output waveform as originally intended. The type of discrimination used proved to be very effective in dealing with the poor waveforms but required set-reset operation of the C flip-flops. The resulting transients on the control lines of the machine were not troublesome but should be eliminated if possible. The outputs from Mk. 11 were much more uniform and allowed the use of a direct clock similar to the method employed for staticising the output of the core stores. (Fig. 34). This is due to a substantial reduction in the progation time through the store and to the more consistent behaviour of the heavily damped output winding. It was, therefore, possible to apply the output of the sense amplifiers to the normal logical input of the C flip-flops, using the clock on the bidirectional gate to sample and insert the information into the C register.

Row selection circuits similar to those used in Mk. 1 store were initially proposed but did not prove to be suitable, the minimum signal level of the outputs, 100 mV, being less than the diode gating noise of the row selection circuits. Most of this noise was due to variations in the levels of the row selection drivers driving the gating diodes. Even if the clamp diodes defining these levels were closely matched, the gate noise could not be reduced sufficiently to allow the required margins with a d.c. coupled amplifier. An a.c. coupled amplifier was tried with only moderate success. If the coupling time constants were adjusted for satisfactory attenuation of the store output signals, the recovery time from the various address change transients was excessive.

A d.c. coupled amplifier is preferable if a suitable circuit configuration can be found. Three possible circuits were investigated :

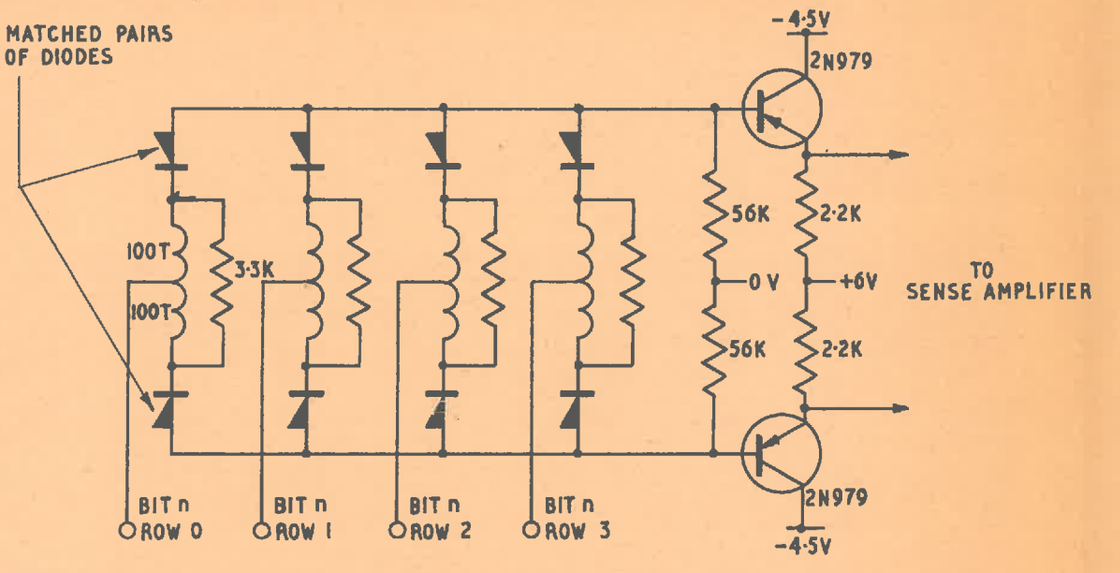
(a) matched row selection diodes,

(b) a balanced sense amplifier with matched pair of diodes,

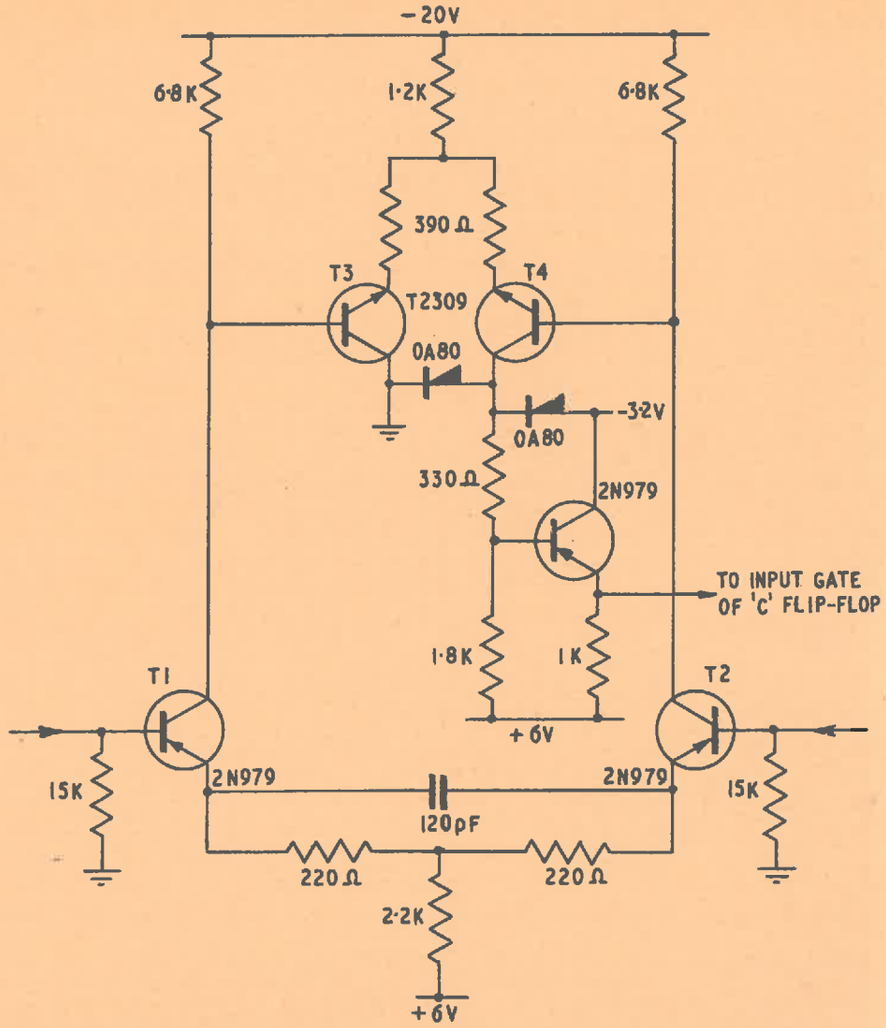
(c) separate preamplifiers on each element with row selection at a higher signal level.

Method (a) is not particularly attractive, the output levels of the row selection drivers would have to be closely matched and to ensure interchangeability of the sense amplifiers all gating diodes would also have to be matched. The d.c. level through the row selection circuits would have to be held to within 25 mV of the nominal value. The output level would also be sensitive to variations in the supply voltages. A balanced system using a centre-tapped sense winding and matched gating diodes, (b), would largely eliminate the sensitivity to both input level and supply voltages although requiring rather more hardware. Method (c) is the best solution. A single stage amplifier with a gain of 20 could raise the signals to a minimum amplitude of 2 V about a d.c. level of -1.5 V, allowing the row selection to be achieved with the standard AND - OR gating used on the input of the other machine registers. Row selection transients as encountered in the other selection circuits would not exist. Of the three methods investigated, (b) was the most suitable. With the present method of construction, (c) could not be conveniently accomodated on the store base and required buffer emitter-followers if packaged away from the store, making this approach unnecessarily expensive. If a faster cycle was required, however, this type of row selection would be preferred.

The output circuits developed are shown in Fig. 74. The $\overline{\text{row}}$ selection driver has an output level of -3.5 V if selected, otherwise O V. The diodes on one of the four sets of sense windings are, therefore, forward biassed and the outputs gated through to a d.c. coupled differential sense amplifier. The quiescent level of the amplifier is set to O V by adjusting the value of the 1.2 K resistor and is driven to



(a) ROW SELECTION CIRCUITS



(b) SENSE AMPLIFIER

FIG. 74 OUTPUT CIRCUITS

$\pm$ 2 V. by the output signal. The amplifier outputs are applied to the inputs of the C flip-flops and set into the C register by an appropriately timed clock. The amplifier is relatively insensitive to variations in the input level but to obtain the maximum margins, the clamp diodes in the row selection drivers are matched.

(4.4.1) THE PERFORMANCE OF THE OUTPUT CIRCUITS :

The significant waveforms in the sense amplifier are shown in Fig. 75 (a) and (b), taken after the first stage of amplification and at the amplifier output respectively. After the first stage the minimum signal is raised to 2 V amplitude allowing ample overdrive of the output. To limit the signal swings applied to the input of the flip-flop, the collector of T_4 is clamped by diodes to O V and -3.2V. The drive pulse width, nominally 0.4 μsec, and the sense winding of 200 T were chosen to allow a suitable margin for the strobe without introducing trouble due to the recovery of the sense winding and amplifier.

The spurious signals due to address change transients are shown in Fig. 75 (f) (g) (i) and (j). During sink changes a large current flow through the store results from the capacity between the sinks. The current flow is consistent with a capacity of $\approx$ 500 pf., a value which was verified by direct measurement. The resulting transient in the store output is relatively minor due to the short duration of the current. The row change transient due to gating current in the sense winding is more significant but still well below the minimum store signal. With a centre-tapped sense winding, this transient should ideally be balanced out but in practice was not significantly less than for an unbalanced system. Due to the high amplifier gain these signals appear to be more significent than they proved to be in practice. The maximum spurious signal was less than 25% of the minimum store output, although occurring at different times within the cycle. The store outputs re-

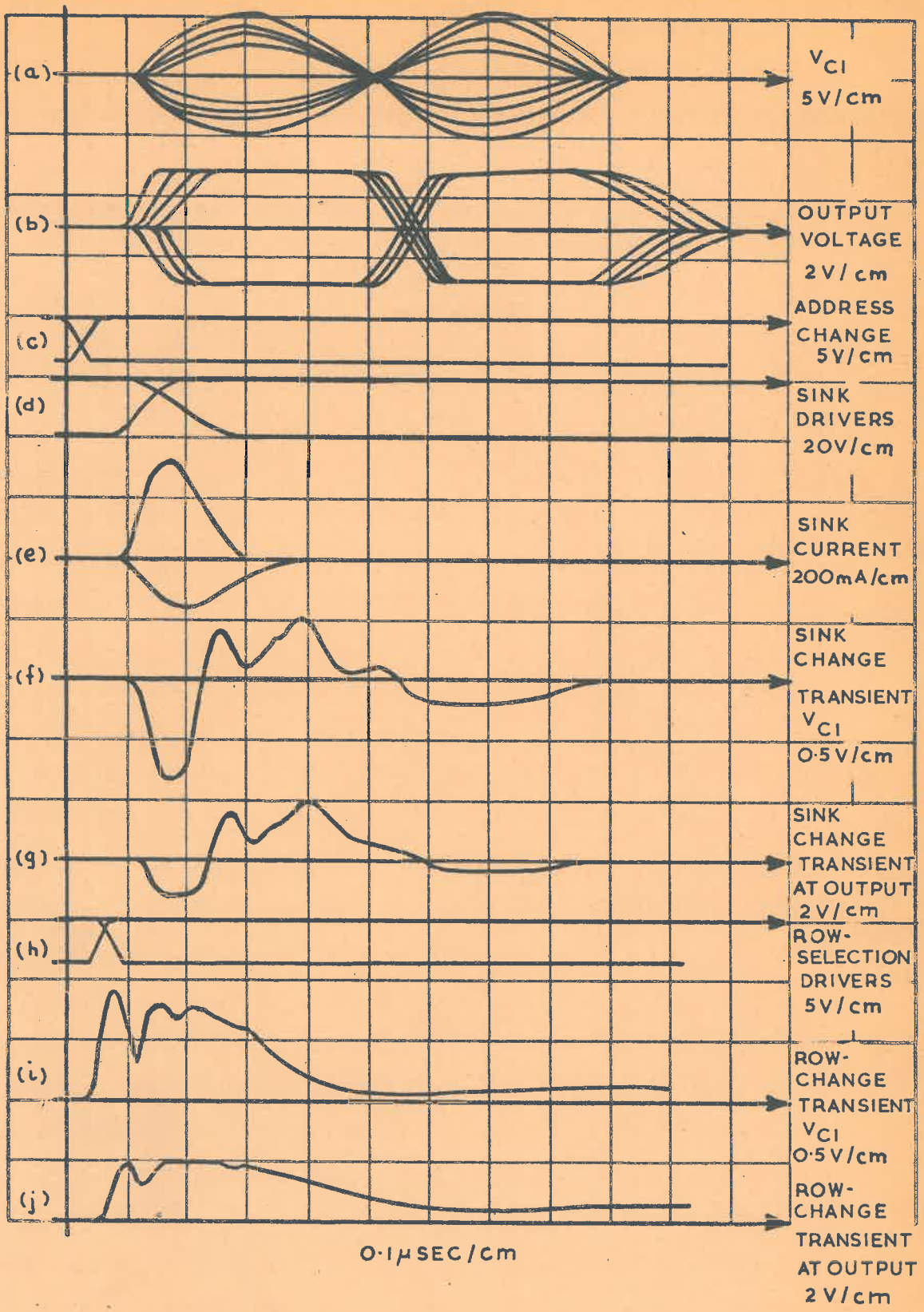


FIG. 75. WAVEFORMS THROUGH THE OUTPUT CIRCUITS

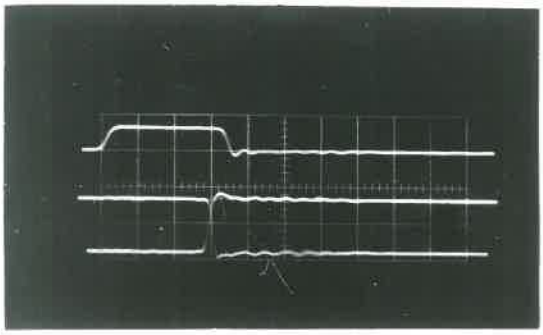
sulting from an attempt to interrogate a word which has not been wired are also trivial illustrating the high selection ratio of the drive switch.

(5) THE OVERALL PERFORMANCE OF THE FIXED STORE :

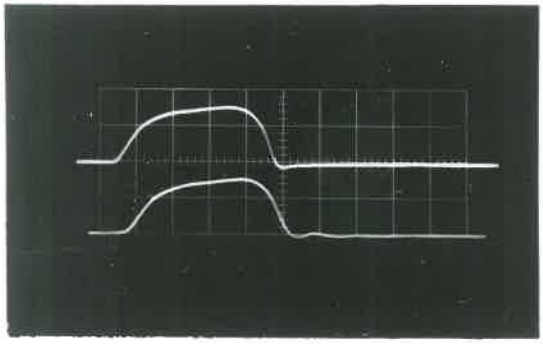
The performance of the store is summarised in the waveforms of Fig. 76 taken with the store cycling through 64 addresses. One wire of the group was not required and these four words do not produce an output. The store operates easily on a 1.5 μsec cycle with an access time of 0.3 μsec. The access time does not include the time required to set up the address which in the intended applications is set up at least 0.75 μsec before the store is driven. Fig. 77 shows the store outputs resulting from a scan of two plates or 1024 words, the waveforms being taken directly on the output emitter followers.

The waveforms for the complete cycle, Fig. 78 (a) show the transients due to row and sink changes. The high gain of the sense amplifier accentuates the magnitude of the resulting transients. The store can be driven 0.1 μsec after an address change without these transients significantly affecting the store outputs, Using an earlier clock than shown in these waveforms, the total access time could be reliably reduced to less than 0.4 μsec.

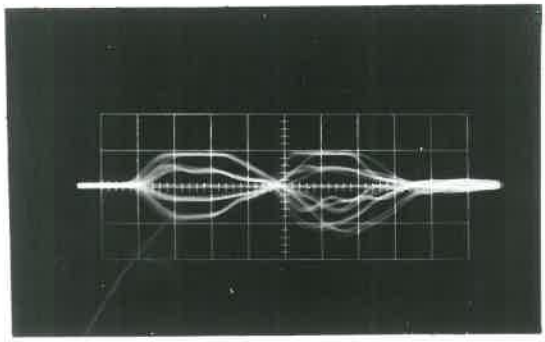
The maximum cycle speed of the store is governed by the recovery of the sense winding and/or the sense amplifier from the drive pulse and the address change transients. As the number of turns on the sense winding is reduced, the duration of the output pulse decreased, but without a proportional loss of amplitude, due to the increase in the self-resonant frequency of the winding. The minimum turns would be determined by the ability of the sense amplifier to discriminate between the '1' and '0' signals. The transients due to address change also decrease with reduced sense turns, the sink change transient in proportion to the output amplitude but the row



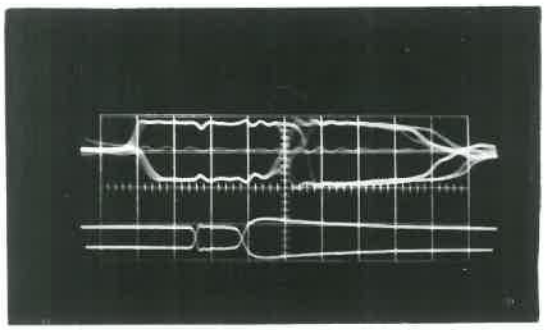
(a) DRIVE CLOCK 5 V/cm
(b) FLIP-FLOP RESPONSE 2V/cm



(c) DRIVE CURRENT-SOURCE END 50 mA/cm
(d) DRIVE CURRENT-SINK END 50 mA/cm



(e) STORE OUTPUTS - V_{C1} 5 V/cm



(f) AMPLIFIER OUTPUTS 2 V/cm
(g) REGISTER CLOCK 10 V/cm

FIG. 76 STORE WAVEFORMS - CYCLED THROUGH 64 WORDS
0·1 μ SEC./cm

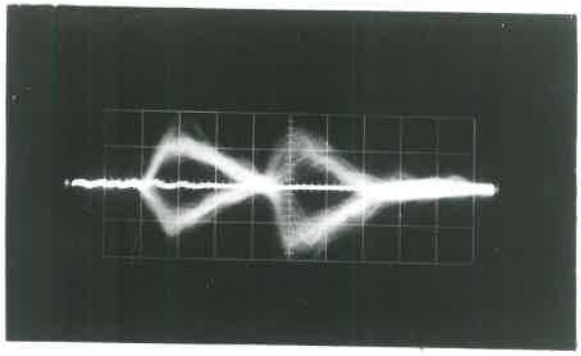
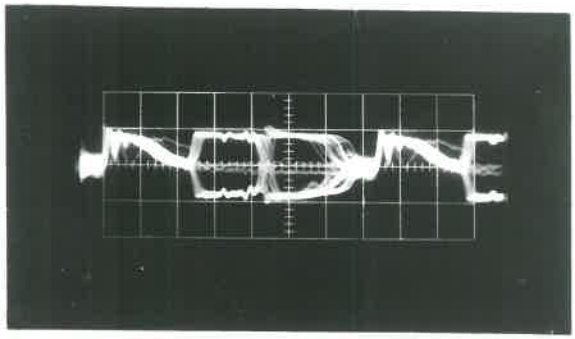
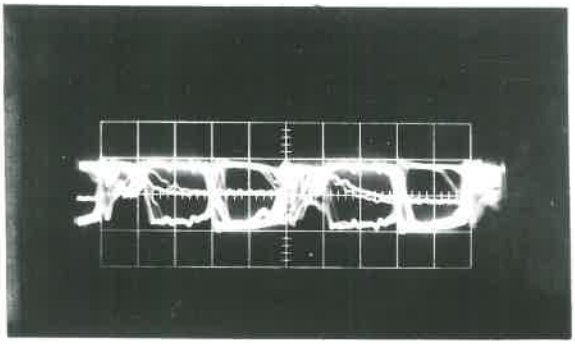


FIG.77 OUTPUT VOLTAGES FROM SCAN OF TWO PLATES
250 mV/cm 0·1 μ SEC./cm



(a) 1·5 μ SEC. CYCLE



(b) 1 μ SEC. CYCLE
2 V/cm 0·2 μ SEC./cm

FIG.78 AMPLIFIER OUTPUT FOR 1 & 1·5 μ SEC. CYCLES

change transient which is the more troublesome in the present store is a function of the inductance of the winding and will, therefore, decrease more rapidly. However, if the maximum possible speed was required, it would probably be desirable to use a separate pre-amplifier for each element as discussed above, eliminating the row change transient altogether. If trouble were encountered with the sink change transient, this could probably be reduced by transformer coupling between the switch and the drivers with the drive system arranged to minimise the voltage swings on the drive wires, especially during address changes. With less sense turns, the effect of the spurious capacitive current would be more noticeable and the store outputs may degenerate.

With a 200 T sense winding, the cycle could be reduced to 1 μsec, the limit of the test rig, without significant degradation of the store output during the strobe period. The waveforms are shown in Fig. 78 (b). The store would probably be capable of an 0.75 μsec cycle with less turns on the sense winding and with modified row selection circuits a cycle time of 0.5 μsec should be possible.

The store is very tolerant to variation in the supply voltages. The circuits will function correctly with at least a 10% variation in supplies, individually or simultaneously. The only effect on the drive circuits is a change in the magnitude of the drive pulse and hence output signal. The store will in fact, operate without error with the drive currents reduced to 25 mA. The differential sense amplifier provides considerable protection against variations in both the d.c. level of the input and the supplies while the high gain of the amplifier allows a considerable margin for weak signals. The bidirectional gate on the flip flops in the remainder of the machine has nominal input levels of $\pm$ 1 V and will function reliably with the signal reduced

to $\pm$ 0.5 V. With nominal inputs of $\pm$ 2 V. for the C flip-flops, even for worst case signals, this provides ample tolerance for variations in the d.c. level of the sense amplifier output and/or low signals from the store.

(6) THE CONTROL FIXED STORE :

The fixed store described above is the configuration required for the control fixed store. The selection, driving and output circuits require approx. 450 transistors and 1600 diodes, all low cost types, contributing significantly to the overall economy of the store. The total store cost including plate wiring was approx. £A1,100 giving a total cost of $\approx$ 1.5d/bit. The static registers for input and output represent a further cost of $\approx$ £500. Initially only 6 of the 8 plates will be required.

Fig. 79 shows the store installed in the frame. The selection and driving circuits are now placed above the store allowing space adjacent to the control and timing logic for future modifications or extensions.

(7) THE MACHINE-LANGUAGE FIXED STORE :

This store is very similar to that used for the control unit. The mechanical construction and the selection and driving circuits are in fact identical. Since this unit is used as an extension of the main core store, the information is only read in half words of 19 bits, so the row selection circuits are slightly modified to provide a 1 of 8 selection. The two forms of storage are addressed as a single unit, both operating on a 6 μsec cycle. Within this framework the appropriate timing sequence is generated by the control unit after examination of the two most significant address bits, assuming both forms of storage are provided in blocks of 4096 words. When interrogated the output of the fixed store is set into the M Register.

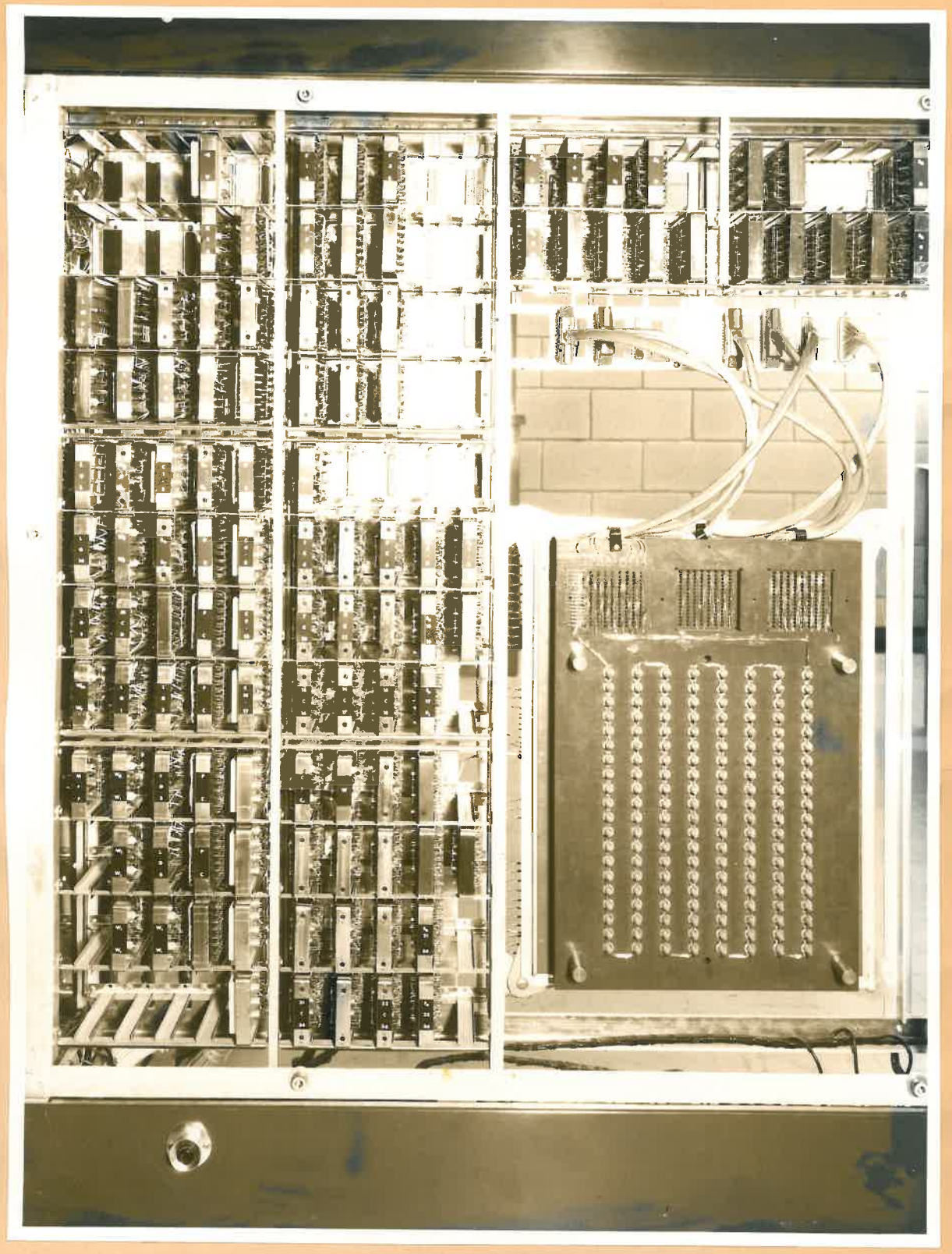


FIG.79 THE CONTROL UNIT USING MK.II FIXED STORE

Access is provided via the sense amplifier of the core store and then into the input logic of the M register. Each sense amplifier is in practice two amplifiers, the outputs of which are combined by a negative OR gate to provide the plane output (Fig 33). This final gate has a third input to accept the output of the fixed store amplifier. The amplifier used for the control fixed store must, therefore, be modified to give nominal output levels of 0 & -3.$\frac{5}{8}$ V with a quiescent level of OV to be compatible. The amplifier is, therefore, modified as shown in Fig. 80. The quiescent level of T_4 is -2V to allow full use of the positive and negative signals from the store. However, when the fixed store outputs are not required the output level of the amplifier is held at a slightly positive value by a control signal acting via the gate. The necessary control levels are derived from an inverter clamped to - 4.5V. instead of -3.2V.

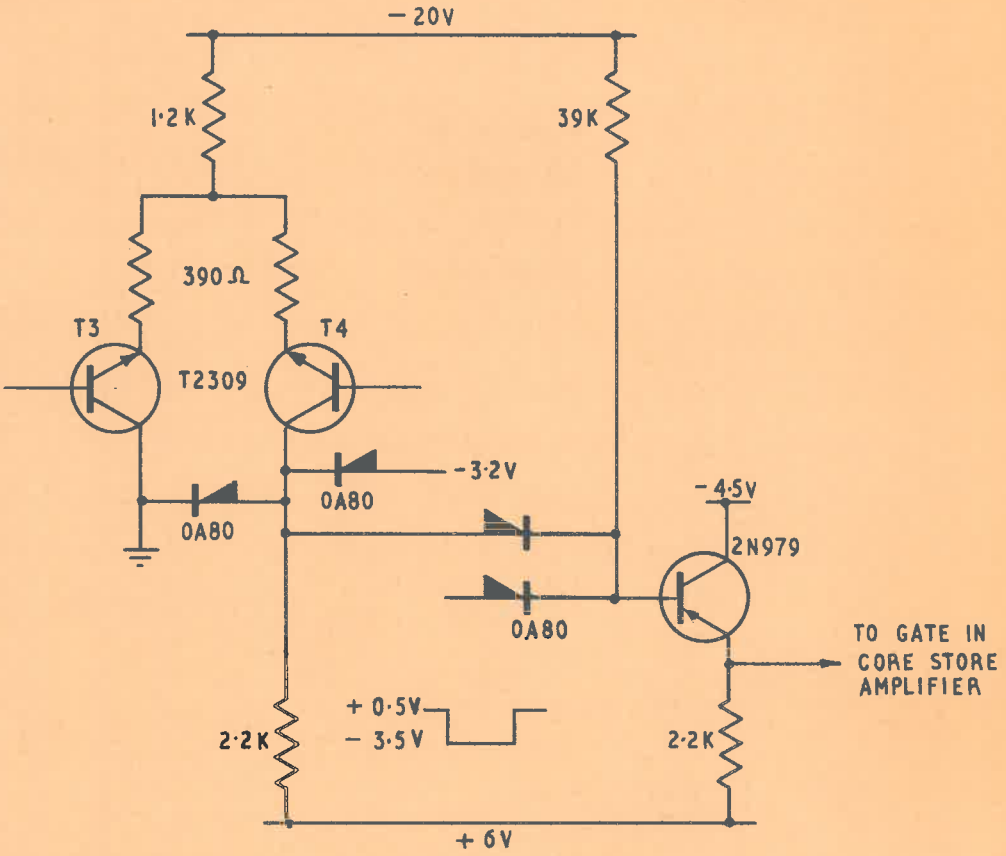


FIG. 80. MODIFICATIONS TO SENSE AMPLIFIER TO SUIT MACHINE-LANGUAGE FIXED STORE

SECTION D

OTHER FORMS OF FIXED STORAGE

(1) INTRODUCTION

When development work was commenced on the CIRRUS fixed stores, late 1959, this type of storage had received little attention. Wired arrays of square loop cores (K1, A2) were the only types which had been applied to computers (N 1) although the concept had been employed in telephony for many years (K19). The majority of stores developed for the latter were slow speed devices, although the flying spot store (K14) was capable of quite high speed, being used in a prototype electronic exchange. A number of other types have subsequently been developed. Some of these, the electro-luminescent store (K6) the magnetically biassed twistor array (K2-K5) and arrays of biassed square loop toroids (K16, K17, L7) use non-linear coupling but emphasis has been placed on linear coupling arrays using either capacitive (K12-K14) or inductive (K7-K11) coupling. The salient features of these stores are briefly discussed below.

(2) STORES USING NONLINEAR COUPLING

(2.1) STORES USING SQUARE LOOP CORES

The configuration most commonly employed is shown in Fig.81. A core is provided for each bit of the word and a number of wires pass through or around the cores to represent a '1' or '0' resp. When a wire is driven, those cores linked by the wire will switch, producing an output to indicate a stored '1'. The cores must of course be reset after the store is interrogated. The core size is a compromise between drive current and the number of wires which can be passed through the cores. To avoid a tangle of wires around the cores, it is more convenient to use several rows of cores, OR-ed together by the output wires. Alternative arrangements, which have the advantage of constant drive impedance and opposite output polarities for '1' and '0', are to thread the word wires through the cores in

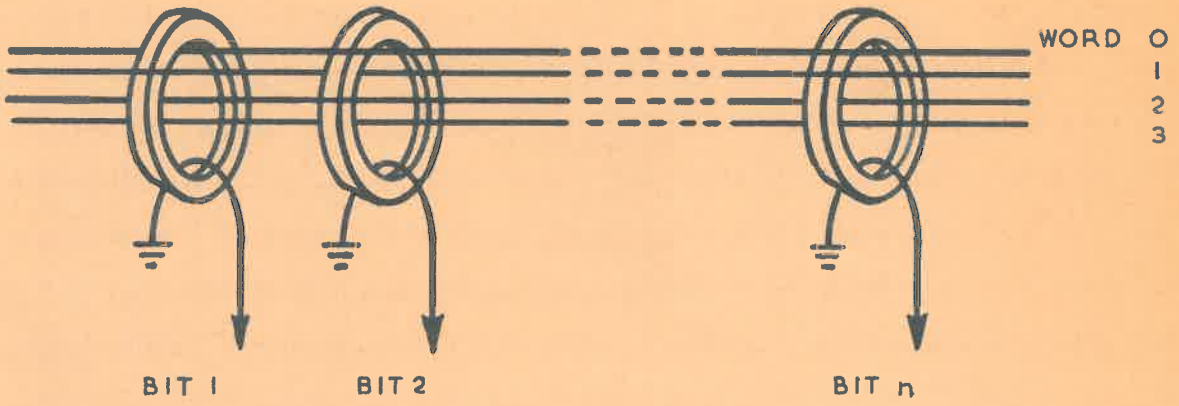


FIG. 81. ONE-CORE-PER-BIT STORAGE

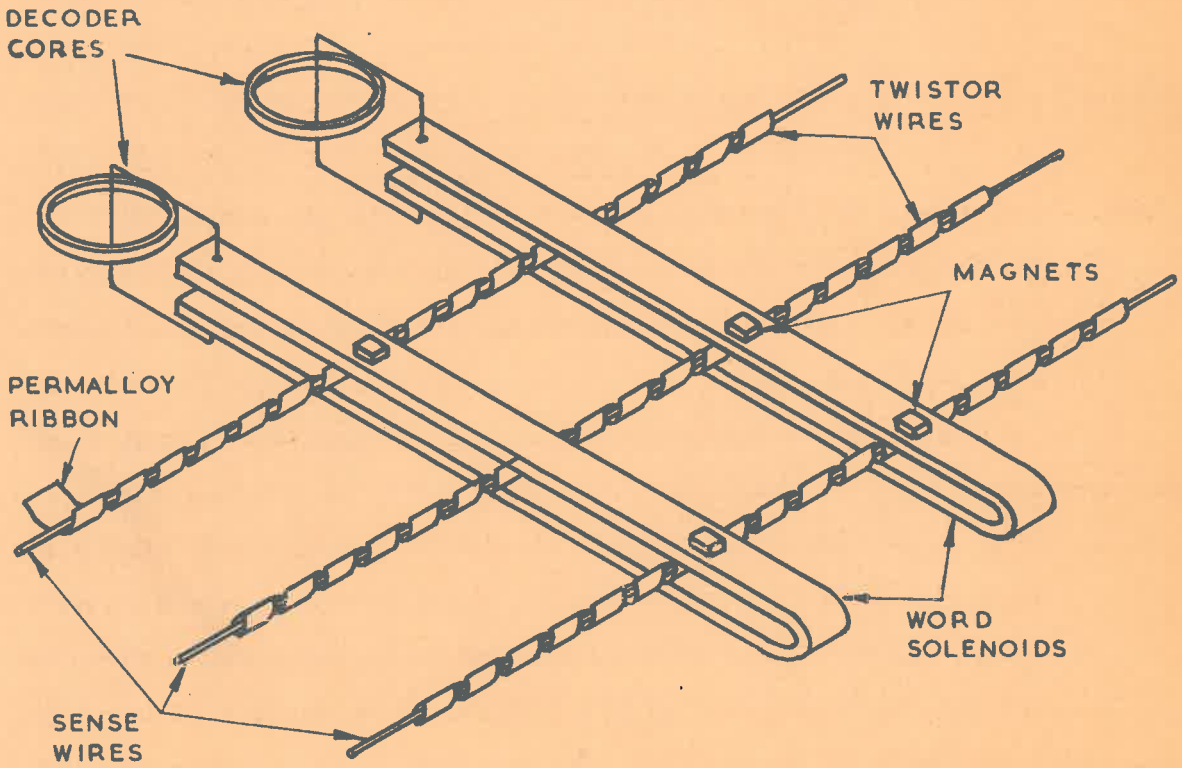


FIG. 82. THE PERMANENT-MAGNET-TWISTOR STORE

opposite directions for '1' and '0' or to use two cores in each bit position, threading the wire through one or the other core for '1' and '0'.

Another possible configuration is the dual of that shown in Fig. 81 i.e. a core is provided for each word and the bit or sense wires threaded through the cores to produce either a '1' or '0' output as required. The cores provided for each word can also be organised as a magnetic selection switch to provide the word selection. Since each wire passes through each core, changes in the contents of the store can be difficult and may involve complete rethreading.

No direct functional advantage is achieved by using square loop material in the majority of these configurations, the stores could be built using linear cores with the advantages of lower drive currents and higher outputs. A selection switch with lower spurious outputs would however be necessary to achieve a satisfactory store performance. The CIRRUS fixed stores both belong to this general class of store, a common feature being that one coupling element is shared by the same bit position in many words. All stores described below used a separate coupling element for each bit stored.

(2.2) THE PERMANANT - MAGNET - TWISTOR STORE

The principle of the store is shown in Fig. 82. Each twistor is formed by wrapping a permalloy tape around an insulated copper wire which also acts as the sense wire. The tape has a square hysteresis loop and a preferred direction of magnetisation along the tape. A twistor wire is required for each bit of the word, and a single turn solenoid wrapped around the twistors for each word. Each section of twistor within a solenoid provides storage for one bit. The tape is normally reset to saturation by passing a current

through the sense wire. A magnet is placed adjacent to the solenoid in the bit positions storing a '0' biassing the twistor further into saturation. When a current is applied to a word solenoid, the twistor wire within the solenoid will switch unless inhibited by the presence of a magnet. The discrimination between '1' and '0' is therefore by the magnitude of the output signal. The twistor is reset by a current in the reverse direction through the solenoid. A typical solenoid current is 1A for a 1 μsec switching time and an output of 4mV.A d.c. biassed coincident current drive switch (C3) is most commonly employed, giving automatic resetting of the twistor at the end of the drive pulse. The magnet array is made by bonding a sheet of Vicalloy to an aluminium sheet and etching out the required pattern of magnets. The twistor is folded to provide a more compact assembly and the cards containing the information are inserted into the store to register with the word solenoids. A similar configuration using square loop cores has also been developed (K17).

(2.3) STORES USING PHOTOGRAPHIC TECHNIQUES

The photographic plate is potentially capable of cheap, high density storage. Access to the information is by scanning the plate with a light beam and sensing the magnitude of the transmitted light. As the information density increases, the resulting accuracy of beam deflection requires the use of digital techniques.

Two approaches to this problem have been described. The first (K15) uses a C.R.T. to provide the scanning of the plates. The principle is shown in Fig. 83. A spot of light is produced on the C.R.T. screen and focused by an array of lenses so that it falls simultaneously on to the corresponding position in each storage area. A storage area is required for each bit of the word with two additional areas provided to code the position of the spot. The latter are used

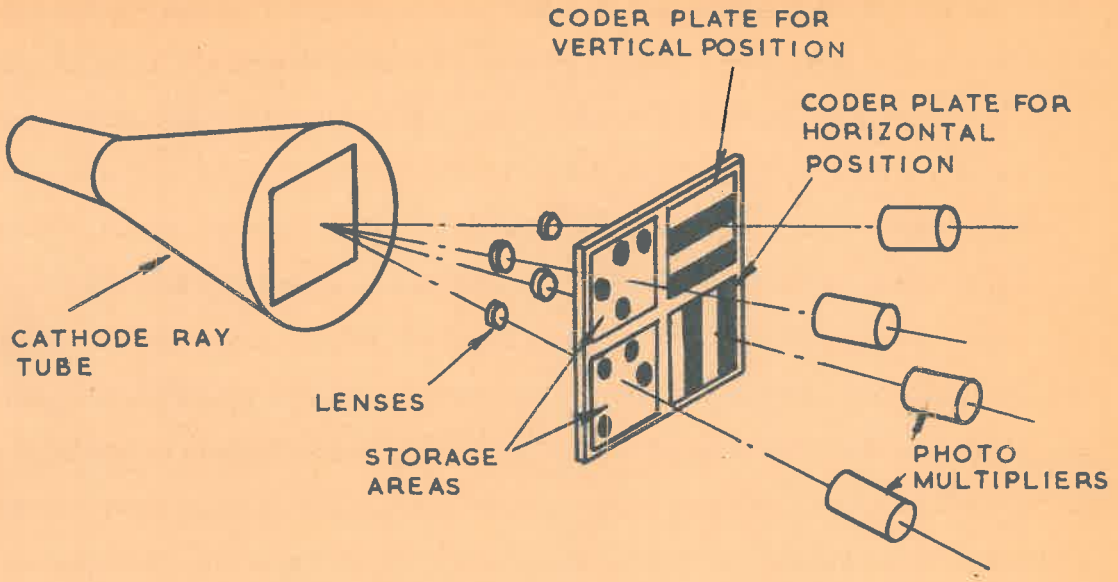


FIG. 83. THE FLYING SPOT STORE

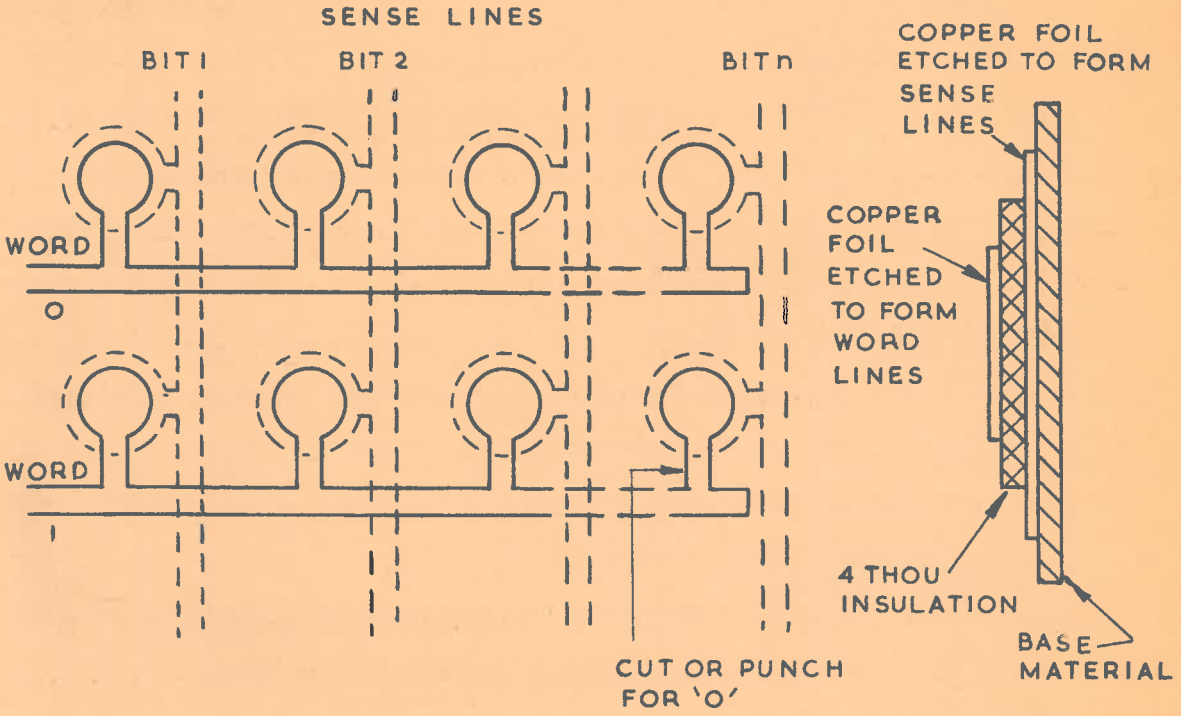


FIG. 84 CAPACITIVELY COUPLED FIXED STORE

in a closed loop servo, providing accurate, drift free control of the spot deflection. The transmitted light is detected by photomultipliers focussed onto the appropriate section of the plate. The photographic plates can be exposed with the same basic hardware used to scan the plates.

The second store (K.6) generates the light spot with an electro-luminescent matrix. This is constructed by sandwiching an electroluminescent phosphor between X and Y co-ordinate conductors. The matrix is deposited on a glass substrate with the conductors adjacent to the glass being thin enough to be transparent. A photographic mask containing the information is placed adjacent to the glass. Crosstalk between adjacent locations is prevented by using a very thin substrate. Total internal reflection of the emitted light will then occur before light from one cell can pass through the mask in adjacent locations. If an X conductor is excited with a frequency of f_1 and a Y conductor with a frequency f_2, the light emitted by the cell at the intersection will be amplitude modulated at the cross-modulation frequencies ($f_1 - f_2$), (f_1 and f_2), etc., uniquely defining this cell in the presence of spurious outputs from the half excited cells.

A photomultiplier followed by an amplifier tuned to say $f_1 - f_2$ detects the presence or absence of the transmitted light. If parallel access to a word is required, an electro-luminescent matrix must be provided for each bit.

(3) STORES USING LINEAR COUPLING

(3.1) CAPACITIVELY COUPLED STORES

Three basic configurations of fixed storage using capacitive coupling have been developed. The principle of the first (K13) is

shown in Fig. 84. A printed circuit board is etched to form the sense lines and the associated capacitor plates. A sheet of 2 thou. Mylar with 1 thou. of adhesive on each side is placed over this pattern and another sheet of copper bonded to the assembly. This sheet is then etched to form the word lines and the other capacitor plates. The conductors are 15 thou. wide and the capacitor plates 1/8" dia., giving a bit capacity of 5 pf. All bit positions are fabricated on the assumption that a '1' is to be stored. A '0' is stored by removing the connection between the word line and the top capacitor plate. A 20 V pulse on a word line couples a 10 mV signal to the output with a '1' to '0' ratio of 4:1.

In another store (K14) the word and sense conductors are arranged in the same plane (fig. 85). Each crosspoint consists of a triangular row electrode and column electrode, connected together to form word and sense lines resp. Coupling is provided by placing an insulated coding strip adjacent to the array of cross-points. If a '1' is to be stored in a particular bit position, the coding strip has a segment of conducting material placed to provide coupling between the word and sense electrodes. The coupling capacity (approx. 4 pf) is therefore a series connection of two separate capacitors and the information is stored by the magnitude of the coupling. The matrix is prepared in sub-assemblies of 20 10 bit words, the required capacity and word length being built up by the appropriate interconnection of these units. A 330 Kc/s sine wave drive is used and a '1' output of 0.5 mV is obtained.

The third store of this type (K12) was developed to allow the sensing of information prepared on a modified punched card. The card is made by sandwiching a layer of foil between two layers of

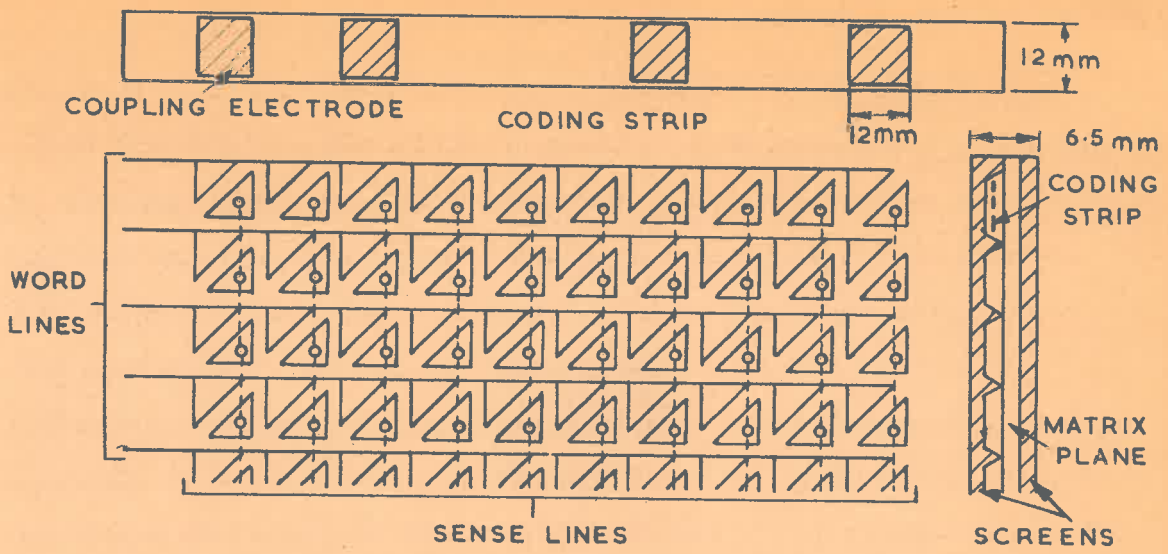


FIG. 85 CAPACITIVELY COUPLED FIXED STORE

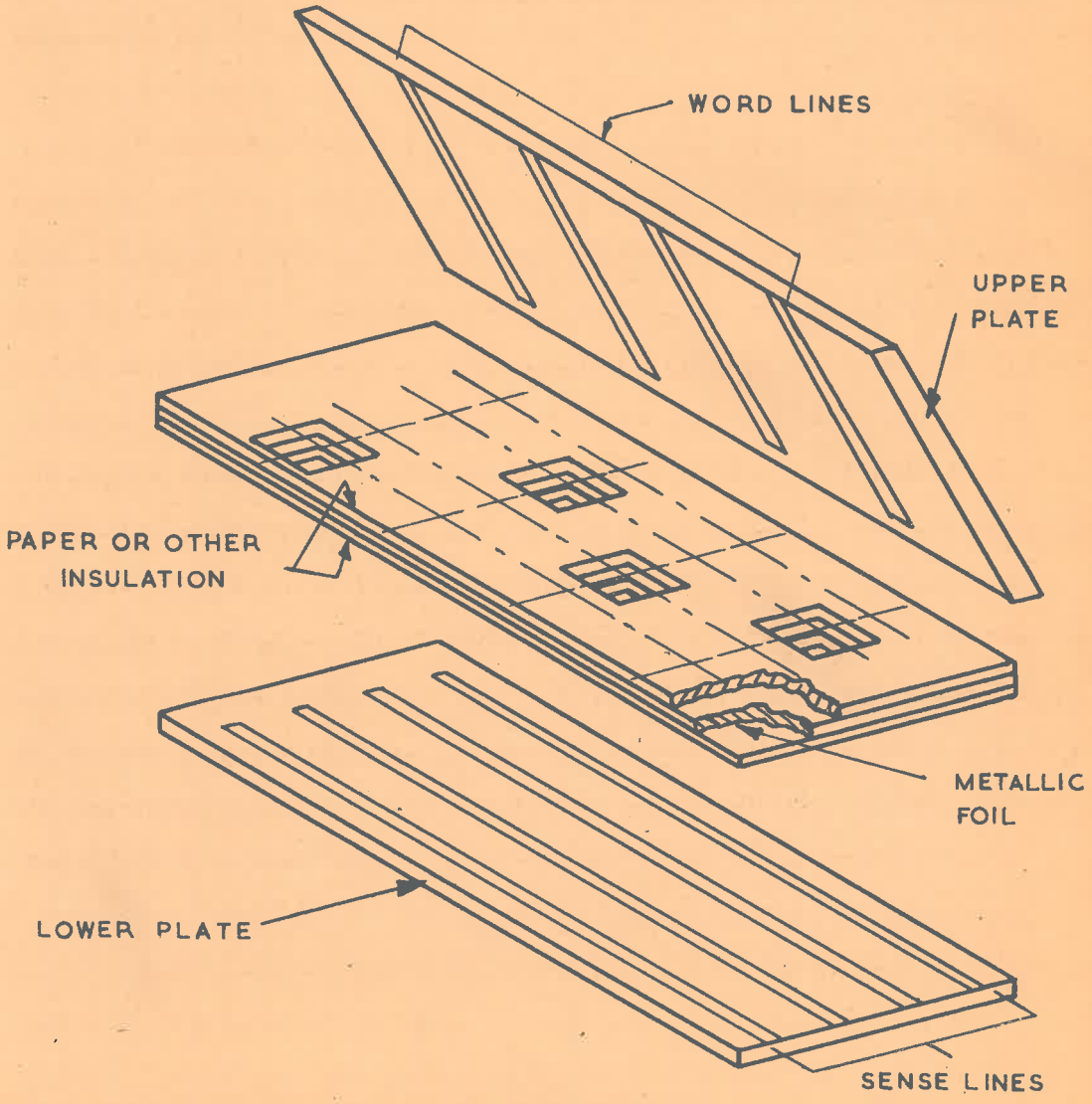


FIG. 86. THE CARD CAPACITOR STORE

insulation. The assembly is the same size as a standard punched card and the information can be prepared by punching out sections of the card on conventional punched card equipment. The punched card is inserted between two printed circuit boards etched to form the word and sense lines (Fig. 86). The crosspoints of these orthogonal sets of lines register with the position of the punched holes in the card. The layer of foil in the card is earthed. If a card has no hole at a particular crosspoint or storage cell, the word and sense lines are shielded but a hole punched to represent a '1' introduces a capacity of $\simeq 0.15$ pf. A voltage pulse applied to a word line will therefore read the information punched on one column of the card. Due to the small coupling capacity, the output signals are small, 1 mV for 100 V drive pulse.

(3.2) INDUCTIVELY COUPLED STORES

The first described and probably best known inductively coupled store is the peg store developed for the Atlas computer (K7). This is formed from a woven mesh of insulated wires (Fig. 87). Adjacent pairs of wires of the warp are used for the drive lines and adjacent pairs of the weft for the sense lines. The intersections of these pairs of wires are the storage cells of the matrix. If a '1' is required in a bit position, a ferrite peg 1 mm dia and 6 mm long is inserted into the mesh, being held in position by a plasticine backing. If a current pulse is applied to a drive wire, the signal coupled to the sense wires is much larger in those positions containing a peg than in those where the peg is absent. To prevent cross talk between storage cells, keeper pegs are inserted into the mesh between the cells. The drive current is a 50 m A pulse for a '1' output of 2 mV.

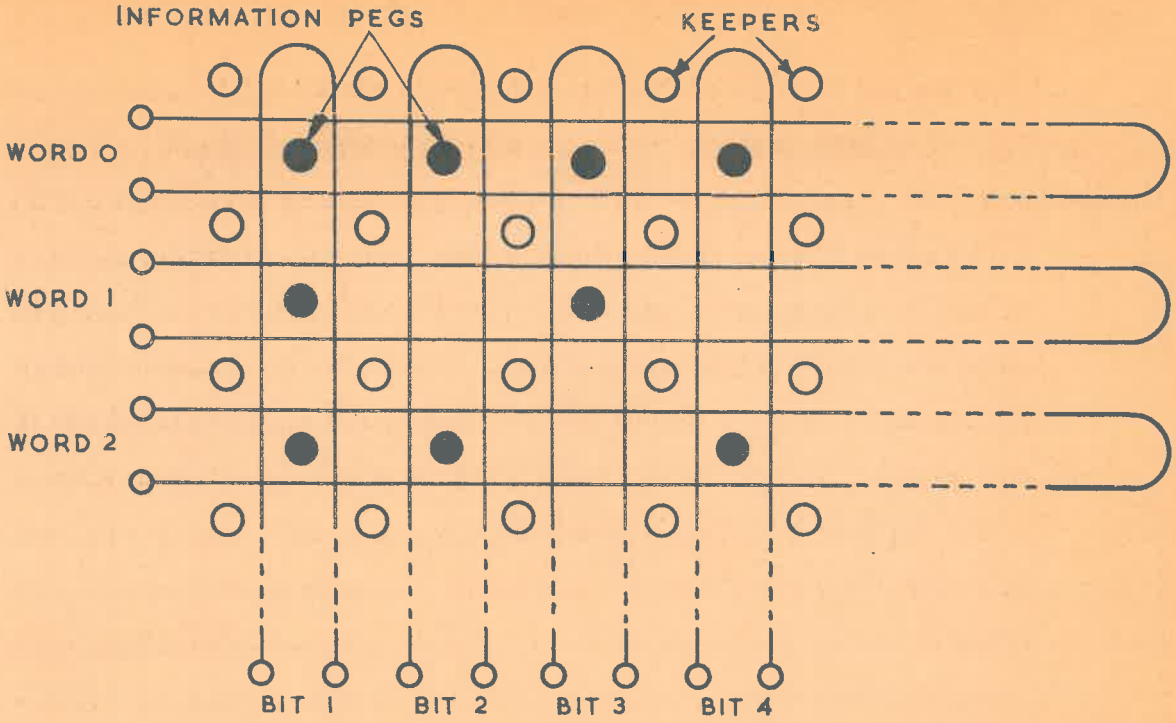


FIG. 87 THE FERRITE PEG STORE

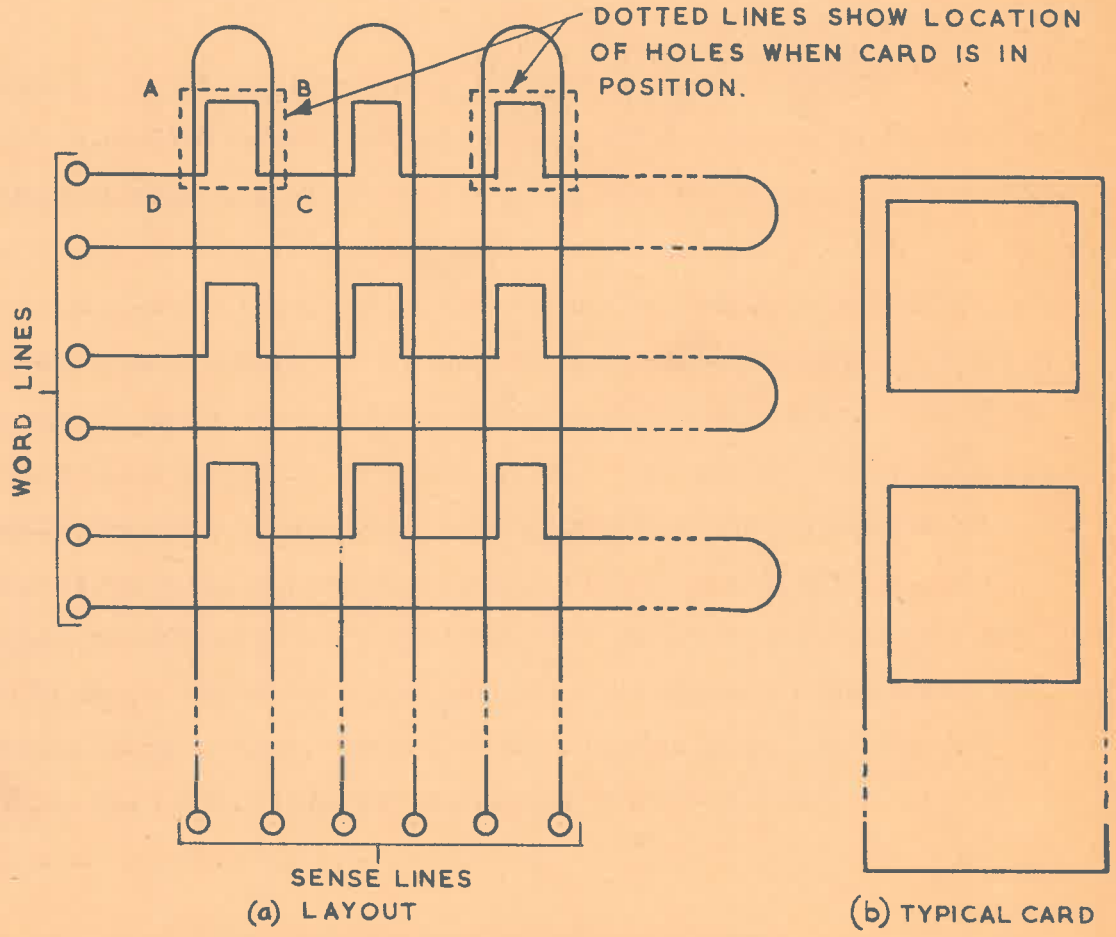


FIG. 88 METAL CARD STORE

In many respects, the eddycard store (K9) is a printed circuit equivalent of the peg store. Two sets of coupling loops are prepared by printed circuit techniques and bonded together to form an array of storage cells similar to that of the peg store. To minimise the spacing between the loops, the sense lines are prepared on a 5 thou. board. In the absence of any other conductors, the coupling between the two sets of loops is very small, but if a square section of conductor is placed over a storage cell, the eddy currents due to a pulse in the drive loop will couple to the sense loop giving a larger output signal. The information is therefore prepared as an array of copper squares on a printed circuit board which is placed on top of the drive and sense loops. If a '0' is to be stored, a section of the corresponding copper slug is punched out, blocking the path of the eddy currents. A 300 mA drive pulse induces a '1' signal of 1 mV in the sense wires. A similar principle is also employed in the unifluxor store (K8) using a slightly different mechanical arrangement.

Another inductively coupled store also making extensive use of printed circuit techniques is the metal card store (K10). Word and sense loops are etched on separate boards and each covered with a 0.1 mm layer of insulation. The boards are mounted face to face, spaced 0.7 mm apart with the conductors registering as shown in Fig. 88. Duralumin cards containing the stored information in the form of punched holes are inserted between the two boards. A hole at a storage cell, introduces a small mutual inductance between the drive and sense coils, otherwise the card acts as an effective shield. A 1.6 mc/s drive gives a '1' output of 2 mV. A similar store (K11) uses a 500 mA drive pulse for a 25 mV output signal.

TABLE 1

PERFORMANCE DETAILS OF VARIOUS FIXED STORES

Type of Store	Drive Conditions	1 Output	1:0 Discrimination Ratio	Cycle Time	Flexibility of Contents	Basic Unit of Information
1. Wired) Biassed) core stores	0.5-1A pulse	50mV-10V	10:1	1-5 μsec	Poor	Word
2. Peg Store (K7)	50mA pulse	2.5mV	15:1	0.4 μsec	Excellent	Bit
3. Unifluxor (K8)	500mA pulse	10mV	15:1	0.4 μsec	Moderate	Card
4. Eddycard (K9)	300mA pulse	1 mV	3:1	0.1 μsec	Moderate	Card
5. Metal Card Store (K11)	500mA pulse	25mV	3:1	0.5 μsec	Good	Word
6. Metal Card Store (K10)	200mA 15V 1.6 Mc/s Sine wave	2mV	20:1	67 μsec	Good	Word
7. Capacitive Coupling (K13)	20V pulse	10mV	4:1	3 μsec	Moderate	Card
8. Capacitive Coupling	5V 330 Kc/s Sine wave	0.5mV	30:1	20 μsec	Good	Word
9. P-M-Twistor Store (K4)	1A	4mV	5:1	5 μsec	Moderate	Card
10. Flying Spot Store (K15)	-	-	10:1	25 μsec	Moderate	Card

(4) A DISCUSSION OF THE VARIOUS FORMS OF FIXED STORAGE

The performance details of the fixed stores described on the previous pagesare summarised in Table 1. With the exception of some forms of wired core storage, all these stores are word organised with the information stored by the presence or absence of coupling between the input and output lines. Discrimination is therefore by the magnitude of the output signal.

In comparing the various forms of fixed storage, three factors are considered relevant: the cost of the store, the cycle time and the ease with which the stored information can be changed. The physical size of the store may also in some applications be relevant, but, in general, this is not an important consideration in the selection of a storage medium.

The total cost of the storage system is determined by the individual costs of generating and distributing the drive pulses, preparing the storage array and the stored information, and sensing the output from the store. The majority of the stores make extensive use of printed circuit techniques to reduce the fabrication costs but in some cases, notably 3, 4 and 5, the resulting drive currents would probably cancel any benefit gained by the cheaper construction. Since the stores are word organised a large selection switch is required and the linear coupling employed within the array requires a very high selection ratio in the switch if satisfactory output signals are to be obtained. If high output power is added to these requirements, the cost of the selection circuits could be excessive. Stores using capacitive coupling place an additional restriction on the drive circuits in that the non-selected drive lines must be terminated in a low impedance to prevent spurious coupling through the array via non-selected words. A notable feature of most of these stores is

the low output signal and/or relatively poor discrimination ratio, requiring expensive sensing amplifiers. Inductively coupled stores use balanced sensing circuits to minimise the capacitively coupled signals. Sine wave drive has the advantage that tuned sense amplifiers can be used, allowing more reliable discrimination of low output signals but these amplifiers normally have a poor transient response and are not suitable if a fast cycle is required. The flying spot store shows to best advantage in stores of large capacity. The access circuits are expensive but the cost does not increase as rapidly with the store capacity as with the other forms of storage. No attempt is made to directly compare the cost of the various types of store.

The cost of a storage medium must be considered in conjunction with the cycle time. The speeds of the various stores are shown in Table 1. In some of the faster stores the speed claimed is perhaps a little optimistic, while the principle of the slower types can often be applied to much faster stores. Not all types are designed for high speed, low cost, large capacity or flexibility of contents being more important in the intended applications. This is reflected in the range of speeds shown. Those with a very fast cycle, 2-5 were developed for computer usage with speed as the major objective, while the slow stores 6, 8 and 9, were intended to provide a cheap semi-permanent store of large capacity for electronic telephone exchanges.

The various stores differ widely in the method by which the information is prepared and the ease with which it can be changed. Those using arrays of coupling elements on cards allow large scale changes of information to be effected quickly and easily, but the

alteration of a few bits of information may require the preparation of a complete new card. The metal card stores and Van Goethem's capacitive store all use one information strip/word while the peg store allows direct alteration of each bit stored. With these stores, frequent minor alterations to store contents would be more conveniently achieved. An alternative form of the peg store was developed in which the contents could be changed at 1500 bits/sec. allowing rapid large scale changes of information. The various types of wired core stores do not allow the contents to be changed conveniently and should be considered as permanent rather than semi-permanent storage.

The CIRRUS MK II store compares favourably with the stores described above. The total cost is quite low, despite the larger amount of manual labour involved in constructing and threading the store. Drive current is moderate and the output signal in comparison with most of the other stores is large, both factors contributing toward economical circuitry. The fast cycle gives a good speed/cost ratio. Large scale changes of information involve only a plate change, although detail changes are not as convenient, requiring alterations to the plate wiring.

Most of the fixed store configurations have their attractive features but none is markedly superior as a general purpose fixed store. In any particular application the most suitable form of storage is strongly influenced by the required speed and capacity, the frequency and extent of changes to the contents, and in many cases the cost of the store.

SECTION E

THE FIXED STORE AS A SOLUTION TO COMPLEX SWITCHING CIRCUITS

(1) THE FIXED STORE AS A LOGICAL NETWORK.

The main application of fixed storage and the main incentive for development has been to provide a cheap form of storage for digital information which is not subject to frequent changes. In addition to the low cost, fixed storage has some inherent advantages over other types of store, such as immunity from accidental loss of information and non-destructive sensing of the contents, which can also be important. The various forms of fixed store discussed in the previous section have been described as fixed stores, permanent or semipermanent memories, read-only memories, translators, coders, etc. the varying terminology often being influenced by the particular application. In a more general sense however, the fixed store can always be considered as a translator having the terminal properties of Fig. 89, with inputs $x=(x_1, x_2 \ldots . X_m)$, and outputs $Y = (y_1, y_2, \ldots . y_n)$ Each value of x is associated with a particular value of y as defined by the translation within the store.

A combinational switching network can also be represented by an identical functional block and it can be simply shown that a fixed store is logically equivalent to an n - input, m - output combinational network in which the transmission function for each of the m outputs is a canonical sum-of-products expression. The n bit input code provides the address for the store, the decoding circuits on the input deriving 2^n addresses $a_0, a_1 \ldots a_{2^n-1}$, equivalent to the 2^n possible product terms of n variables. These terms are then logically added within the store, a term a_i being included in the expression for m_j if the required coupling is provided within the store between the input line representing a_i and the output line representing m_j. The coupling array is therefore equivalent to a set of OR gates and the address decoding to a common set of AND gates.

FIG. 89 TERMINAL BEHAVIOUR OF FIXED STORE OR COMBINATIONAL NETWORK

A fixed store and associated addressing circuits are consequently capable of providing the outputs corresponding to any desired transmission function and can be considered as a universal gating network.

The question immediately arises as to the relative merits of fixed storage and conventional techniques in realising logical networks. The most important factors in the present context are that fixed storage is more flexible and under some conditions cheaper.

To provide a basis for comparison, some assumptions must be made about the configuration and specific hardware form of the network. It will therefore be assumed that diode-transistor logic will be used and that the logical functions will be achieved with AND-OR cascades. Three possible configurations will be considered, each with 12 input variables and 40 output variables as for the CIRRUS fixed store . The logical expressions in canonical sum-of-products form could therefore have a total of up to 40 x 4096 = 163,860 terms.

The logic could be realised using the same sum-of-products expressions as the fixed store with each output separately derived. A 12 input AND gate is required for each term of each expression and a corresponding OR diode i.e. 13 diodes/term. For a large number of terms it is more economical to separate the AND and OR functions as in the fixed store. A 1 of 4096 decoding can be realised as a dual tree with $\approx$ 8500 diodes, representing close to the minimum. Each term will then only require a single OR diode. Neither of these configurations makes any significant attempt at minimisation which would certainly reduce the number of diodes required. The actual reduction would depend on which terms were used and how many levels of logic were permitted. A figure of 5 diodes/term will be assumed to represent

a reasonable lower limit. In a practical situation, allowances must also be made for packaging and driving the logic circuits and for possible regeneration of the outputs. Assuming £0.1/diode and a 50% loading for packaging etc., the cost of the three forms varies with the number of terms involved as shown in Fig. 90. By comparison the fixed store would cost $\approx$ £1100, irrespective of the number of terms required. The fixed store makes available within the array very large OR gates at very low cost so that once the array has been constructed, the addition of terms involves only the appropriate wiring of the store.

The assumptions made could easily introduce considerable errors, but would not significantly alter the overall picture which emerges. As could be expected, the conventional techniques are cheaper for a small number of terms and the fixed store for a large number. Allowing for the inaccuracy, a break-even point of 2000 terms could be taken, or $\approx$ 1% of the maximum possible number. This allows only 50 terms per output bit. If a parity bit were provided on the output of the network, a desirable feature in the network of this size, then this alone could require the 2000 terms.

It is quite possible that a minimised form of the equations could be obtained which would reduce the cost below that shown, especially if more levels of logic were permitted. A minimised network, however, loses the flexibility of the other forms, an inconvenience in many applications. The addition of terms to the transmission functions may require a considerable re-organisation of the logic circuits especially if these have already been packaged and wired. The fixed store is particularly attractive in this regard since modifications to the logical expressions require only a change in the coupling within

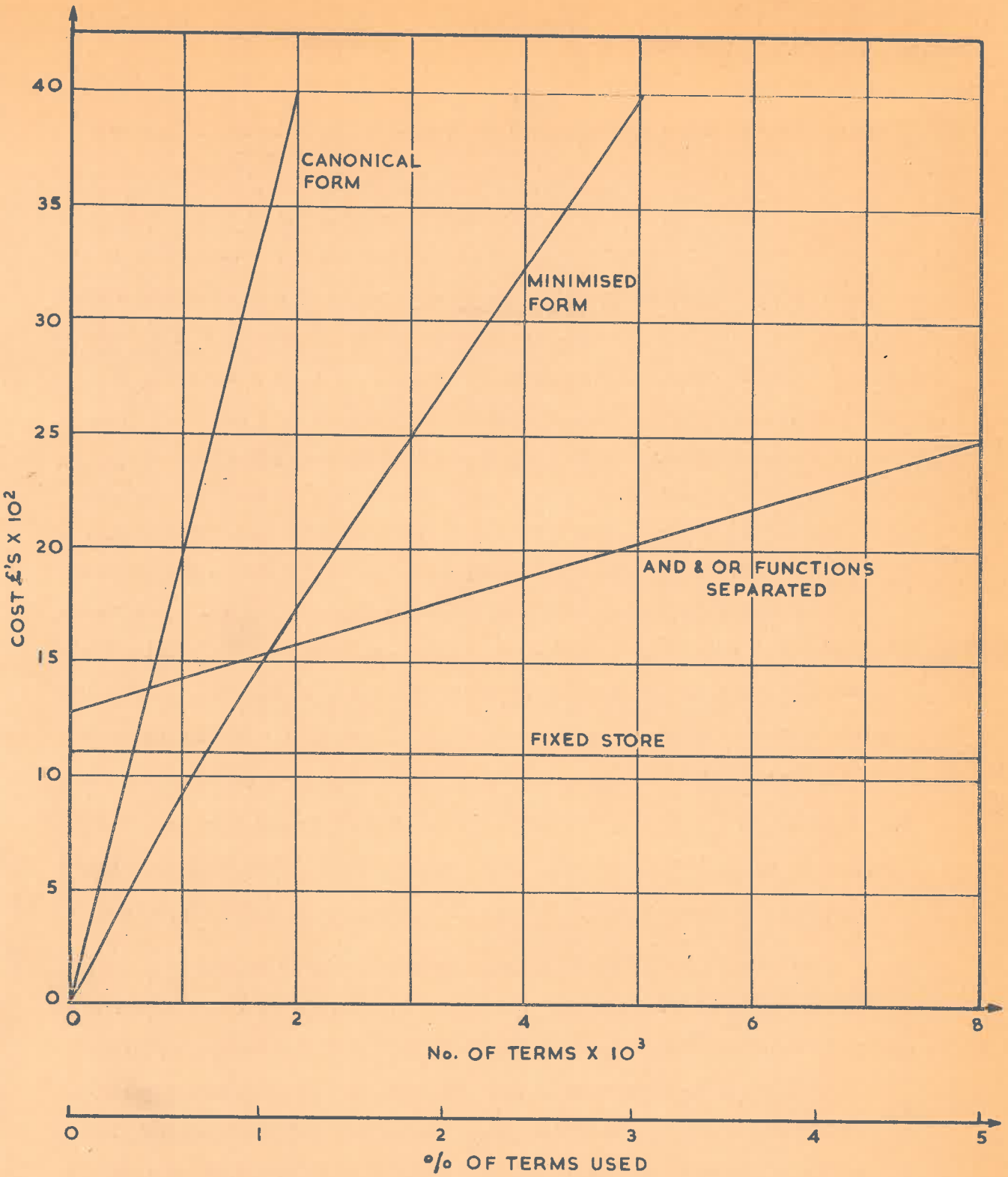


FIG. 90 COMPARATIVE COSTS OF VARIOUS TYPES OF COMBINATIONAL CIRCUIT.

the array. Many fixed stores have been designed to allow rapid changes of the contents and modifications from a few terms up to a completely new set of transmission functions can be readily accomplished. This facility can be of great assistance during the design of equipment. The construction of the store requires only a knowledge of the word length and capacity required. The internal coupling representing the required transmission functions can then be inserted when these have been finalised.

The relative speeds of the two types of network is biased in favour of the conventional techniques. With a two level logical structure, a response time of 0.1 - 0.2 μsec is not difficult to achieve even with low cost components. Very large networks and those in which more levels of logic are used could, however, exceed this figure. The equivalent time for the fixed store technique is the access time of the store, the time taken to convert the input information or address to the appropriate output signals. Some of the faster forms of fixed store can have an access time of < 0.1 μsec, but these would be more expensive than the type used in CIRRUS. It is likely, however, that these would still be cheaper than the alternative conventional network in many applications while retaining the advantage of greater flexibility.

The required cycle time of the fixed store need not be directly related to the access time. Every switching circuit has, in effect, a cycle of behaviour, the interval between successive values of the input. This interval will vary with the particular application but could easily be long compared with the time allowed to convert to the required output, even in a high speed machine. A short access time to the store may in many cases be more important than a fast cycle.

In the above discussion it was shown that a fixed store has a structure equivalent to that of a conventional multiple-input, multiple-output combinational network, but the equivalence of structure is not necessary. Given a particular set of inputs there is no reason why a store should not be consulted to determine the required outputs. The external behaviour of both is identical, a functional block which will generate an m bit output for each n bit input in accordance with a predetermined set of transmission functions. This is only a translation process which can be realised in any form which satisfies the boundary conditions of speed, cost and ease of modification. Flexibility and cost favour the fixed store translation but conventional techniques are capable of higher speed. The fixed store approach is best suited to large networks or those whose transmission functions contain many terms. Practical considerations of address decoding would probably limit the input word length to 14 bits, a store capacity of 16,384 words, but the output word can be of any reasonable length. The fixed store would allow parity checking of the output at very low incremental cost, a facility which although desirable would be too expensive to provide with conventional techniques. Small size and reduced power consumption are other potential advantages of fixed storage.

(2) THE APPLICATION OF THIS TECHNIQUE TO THE DESIGN OF DIGITAL EQUIPMENT.

The logical design of a computer or any other device to handle digital information involves two inter-related processes, the selection of a suitable set of registers, stores and logical networks to allow the basic data manipulation and the design of sequences of data transfers within this hardware to implement the desired machine functions. The latter are then converted to hardware form in the design of the control unit. This is a sequential switching circuit having as outputs the control signals necessary to enforce these transfers within the machine hardware, and to

control its own behaviour in generating the required sequences of transfers. At this stage of design, the specification for the control unit will contain many equivalent states, i.e. the same outputs from the control unit and consequently the same set of transfers may be common to a number of different phases of machine operation. The conventional design procedure then involves the elimination of this redundancy by merging the equivalent states and deriving logical equations to control the transfers between these states. The control unit will then proceed from state to state in a predetermined manner executing each of the required machine functions. Each machine function is consequently realised by a defined sequence of data transfers within the machine hardware just as a program is developed from sequences of order.

In minimising the system as a whole to obtain the most economical configuration, both the manipulation section and the control unit must be simultaneously minimised. In performing this process, a balance must be found between the hardware and resulting cost of each section, since efforts to minimise the hardware in one section is normally associated with a complication of the other.

In a simple machine, the most economical configuration can generally be achieved with a minimal and integrated set of efficiently used hardware in the data manipulation section without creating a particularly difficult design problem in the control unit (N2), but with the trend towards more complex machine behaviour and more powerful order codes, this approach gives a very complex control unit and minimisation of the control presents a formidable task. Computer programs have been written to handle various aspects of this problem but those developed to date are still somewhat restricted in their application and efficiency. (N3 - N7) Even if suitable methods were developed the resulting control unit is likely to be costly and, due to

minimisation of the control logic, inflexible if realised by conventional techniques. The problem is more commonly met by sub-dividing the machine into smaller and more convenient functional units each with a separate control operating under the supervision of the central control unit. This does not minimise the system and requires the provision of a considerable quantity of special purpose hardware used much less efficiently. Such a design approach may, however, lead to faster operating speeds due to the possibility of parallel operations in the different sections of the machine. The cost of the machine has consequently risen rapidly as the complexity of the machine functions has increased.

This tendency is acceptable if the operating speeds rise sufficiently to offset the increased cost, but if it is desired to design these advanced facilities into a low cost machine, neither of these approaches is satisfactory using conventional hardware techniques. However, the availability of a cheap and fast form of fixed storage and the suitability of this device to the design of large scale switching circuits significantly alters the balance between the two sections of the machine. The complex control functions resulting from the first approach can now be realised in an economic and flexible manner.

The control unit of a digital machine considered as a sequential switching circuit can be represented in the general case as in Fig 91. i.e. a conventional combinational switching network with the addition of feedback paths from the output to the input. The P feedback paths cause the response of the circuit to be a function not only of the present inputs to the network but also of the previous sequence of inputs as represented by the P present state inputs. The next state information, derived from both the present inputs and the present state inputs is introduced into the combinational network with a delay to provide immunity from race conditions. The combinational network represents the major portion of the control hardware and if extreme speed is not required, can be realised with a fixed store as discussed previously.

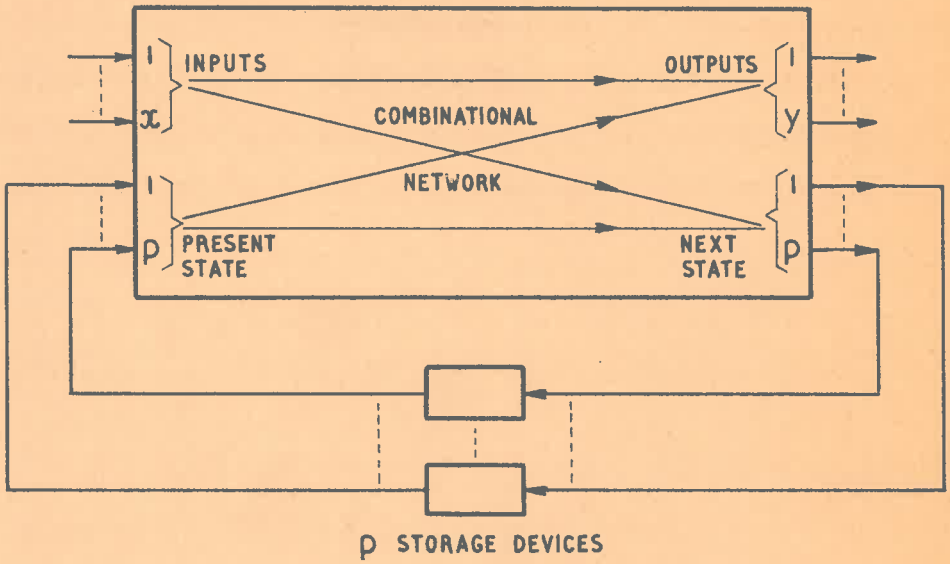


FIG. 91. THE GENERALISED SEQUENTIAL CIRCUIT

A decision to base the control unit on fixed storage carries certain implications into the general approach to machine design, implications which if fully pursued result in a control unit design which would be quite impractical to realise by conventional techniques. In this respect, a direct comparison between the two forms of switching circuit is somewhat unrealistic for the particular case of the control unit.

The different approach to machine design is a result of the non-linear relationship between store cost and store capacity, i.e. the cost/bit decreases for large capacity stores whether extended by increasing the number of words or by increasing the word length. The designer need not, therefore, be unduly concerned about a design approach which requires a large capacity in the control store. The machine functions can then be developed from sequences of relatively simple transfers with much less hardware in the data manipulation section. This hardware can be chosen to realise these transfers in the most efficient manner with little thought for the resulting control problem. It may in fact be desirable to deliberately add complexity to the control functions in achieving this objective. If the basic set of transfers are well chosen, any desired machine function can be realised with a suitable sequence of transfers and incorporated in the control store. A comprehensive order code and complex system behaviour can then be achieved at low cost since the internal design complexities are reflected in the control store capacity rather than the machine hardware.

A control unit designed in this manner also avoids the difficult and tedious process of minimisation, associated with more conventional types of sequential switching circuit. The circuit behaviour can be realised more simply and more economically by providing the store capacity necessary for a completely non-minimised switching circuit i.e. the sequence of transfers defining each machine function is placed directly into the store in consecutive addresses without any attempt at merging, avoiding the logical decisions which would then be involved. Within the restrictions imposed by the allowed transfers, this particular form of

control gives a simple and completely flexible design approach particularly suitable with existing hardware for medium speed, low cost machines.

The CIRRUS computer discussed in the following section provides a convenient example of such an application of fixed storage. The discussion is restricted largely to the principles involved to avoid unnecessary detail.

(3) THE CIRRUS COMPUTER :

(3.1) The System Structure :

The general structure of the machine shown schematically in Fig 92. has been discussed in broad outline in Section A and familiarity with this will be assumed. The machine can be considered to contain 4 subsystems :

(a) an information processing unit comprising the arithmetic/logical network, the 4 main registers M, R, N, Z and 2 smaller registers A and E and miscellaneous small buffers and logical networks.

(b) an input/output channel associated with the M register and providing for information transfers from the main store and the slow speed peripherals including the operating consoles.

(c) an input/output channel associated with the R register, providing for information transfers from the register store, and, via this unit, the high speed peripherals and real time interruptions.

(c) the control unit comprising the S and C registers, the control fixed store and the timing circuits.

The basic units of hardware in the information processing unit can be interconnected in a flexible manner to provide a wide range of arithmetic and logical functions. Information is transferred from the

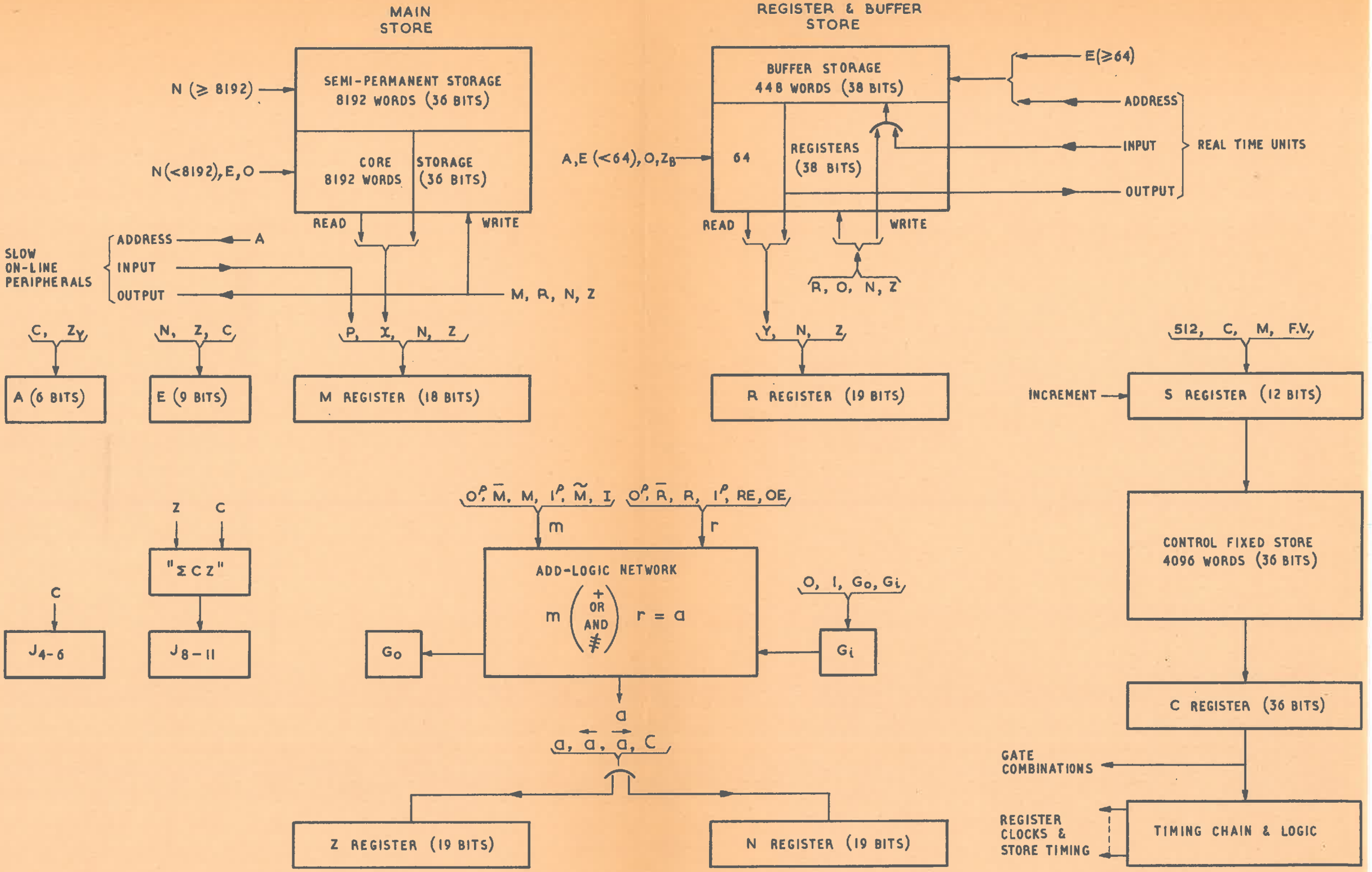


FIG. 92. CIRRUS STRUCTURE

M, R and E registers to the N or Z registers through the arithmetic/logical network with, if required, a single place shift to left or right. All or part of the contents of the N or Z registers may be transferred to the M, R, A or E registers directly. Any of these registers may also be set directly or indirectly with information from the C register. The arithmetic/logical network is basically a half-word parallel adder, which, with slight modifications, can also perform the logical operations of AND, OR and NOT EQUIVALENT. Each input to the network may come from 1 of 6 sources, $\tilde{M}$ from O, $\overline{M}$, M, I, $\tilde{M}$ or I and r from O, $\overline{R}$, R, I, RE or OE. The M, $\overline{M}$, R. and $\overline{R}$, inputs are the contents or complements of the M. and R. registers respectively, $\tilde{M}$ a slightly modified M and O and I are half words of all '0's and all '1's. RE and OE are R or O with E replacing the bits at the least significant end. I is a set of 18 indicator circuits, the states of which are determined by the availability of the peripherals. G_i is a single bit buffer used when subtracting or to insert the carry buffered in G_o when continuing carry propagation over a full word. The two inputs can be added, subtracted or, by suitable choice of input form and network function, can be combined in any of the 16 possible logical operations.

This section provides a general purpose arithmetic/logical facility intended to process information on a purely transient basis. The function performed by each register varies during the different phases of the machine behaviour. Any information which must be retained for an extended period is returned to one of the core stores and brought down to the information processing section when required. Consequently, the functions of accumulator, index register, sequence counter etc., for each program are provided by storage locations rather than hardware. The computation associated with these functions is performed in the arithmetic unit.

An information channel to and from the arithmetic unit is associated with the M register. This consists basically of three bus

systems, x_o for output from the arithmetic unit, x_i for input to the arithmetic unit and X_D to specify the source or destination of the information. The x_i inputs are inserted directly into the M register but both x_o and X_D may come from 1 of 4 sources, x_o from the 4 main registers M, R, N or Z and X_D from N, E, A or zero.

During peripheral transfers, X_D, derived from A, defines the unit involved, and one character of information is transferred from a buffer in the peripheral to M or from one of the machine registers to the buffer. If information is to be transferred to or from the main store, X_D, derived from N, E or zero, represents the required address within the store.

The outputs of the sense amplifiers, 18 bits + parity are clocked directly into M or ignored while the input to the store is taken from the x_o bus system. The store is therefore considered as a peripheral unit of the arithmetic section during information transfers with the functions of address register, input register and output register provided by borrowing the hardware of the arithmetic unit via the three bus systems. Similarly the peripheral transfers are controlled by the hardware of the arithmetic unit, without buffering other than the single character buffer necessary in these units.

The information channel associated with the R register differs in that information can only pass through the register store. The information in the 64 program accessible registers is addressed by A, E, Z_b or zero. The store output is clocked into R or ignored and the store input is either zero or may be obtained from R, N, or Z. Information transferred on the real time bus is inserted directly into the buffer section of the register store. During such a transfer, the state of the arithmetic unit is frozen by suppressing all register clocks. The drive circuits and read and write amplifiers of the register store are then borrowed by the real time address, output and input bus systems to effect the transfer between the register store and the peripheral buffer. The information is

placed in or removed from the buffer store in the same way as access is gained to the 64 registers although this section is normally inaccessible to the programmer.

This hardware provides a data manipulation section in which the units can be inter-connected in a flexible manner by gating circuits to perform the necessary information transfers and manipulations. The particular interconnection required is specified by the C register in the control unit, the transfer being enforced by a sequence of appropriately timed clock pulses applied to the registers and stores. The gating logic and method of register clocking were shown in Fig 34. The control unit with which this section is primarily concerned is discussed in greater detail below.

(3.2) THE CONTROL UNIT :

In section A, the control unit was referred to as a sub-computer and the sequences of transfers defining the machine behaviour as sub-programs. Superficially, the analogy is satisfactory and provides a convenient way of describing and discussing the control unit. If carried too far, however, the analogy falls down and will not be pursued in the subsequent discussion.

The control unit of the machine contains four basic elements, the control fixed store, an address register S, an output register C and the timing circuits and logic. The first three of these constitute a sequential switching circuit which is a special case of the general switching circuit of Fig 91. No direct inputs to the network are used, the inputs from S being equivalent to the present state inputs P. Some of the bits set into C represent the y output bits and control the timing circuits and the information flow within the data manipulation section. Others directly or indirectly define the next state of the network or the next value to be set into S. In generating the sequences of transfers corresponding to the various machine functions, the S register is normally incremented by

one between successive interrogations of the store but gating connections and machine transfers are provided which allow S to be set unconditionally or as a result of tests on the state of a specified section of the data manipulation hardware. The next "effective" value of S may consequently be derived by a sequence of one or more dummy settings which define and control the testing of the data manipulation hardware.

The information set into the C register may be interpreted in 1 of 8 ways as determined by the first three bits of C. Five of these eight sets of transfers define arithmetic and/or logical operations and the remainder provide for testing and setting registers. The structure of each set is shown in Fig. 93.

The 5 F and A type transfers are all of similar form with the C bits used as follows :-

C_{1-3}	-	type of transfer used by the timing circuits.
$C_{14, 15}$	-	control overlapping of timing circuits as discussed below.
$C_{4, 5}$	-	address source for main store or in more general case the M information channel.
$C_{6,}$	-	upper or lower half word in the main store.
$C_{7, 8}$	-	source of information for output to the main store or M information channel.
$C_{9, 10}$	-	address source for register store.
$C_{11,}$	-	upper or lower half word in register store.
$C_{12, 13}$	-	source of information for output to the register store.
$C_{16,}$	-	next value of S.
$C_{17,}$	-	source of information to be set into A register
$C_{18, 19}$	-	" E "
$C_{20, 21}$	-	" M "
$C_{22, 23}$	-	" R "
C_{24-27}	-	set up arithmetic/logical network to required function.

TYPE OF TRANSER		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36
AXY	ARITHMETIC (BOTH STORES)	0	1	0	NE − 0 → X_D		U → X_H L	MRNZ → x_0		AE0 → Y_D Z_B		U → Y_H L	R0N → Y Z		0̀ Lap	1 2 0̀ Laps	S+1 → S 512	HOLD → A Z_Y	HOLD N Z → E −		HOLD x_i N Z → M		HOLD Y_R N Z → R		0 I G_0 → G_i G_i		L	≠	0 M M I$^{\rho}$ Ṁ I → m			0 R R I$^{\rho}$ RE OE → r			N Z HOLD I	N.S. L.S. R.S. I N,Z I	
AY	ARITHMETIC REGISTER (STORE ONLY)	0	1	1	0	0	0	0	0	"		"	"		"	"	"	"	"		HOLD − N Z → M		"		"		"	"	"			"			"		
AX	ARITHMETIC (MAIN STORE ONLY)	1	1	0	NE − 0 → X_D		U → X_H L	MRNZ → x_0		0	0	0	0	0	"	"	"	"	"		HOLD x_i N Z → M		HOLD − N Z → R		"		"	"	"			"			"		
FA	ARITHMETIC (NEITHER STORE)	0	0	1	COPY AX, AY, AXY CODING IF OVER-LAPPING OTHERWISE ZEROS										0	0	"	"	"		HOLD − N Z → M		"		"		"	"	"			"			"		
FM	MULTIPLY STEP	0	0	0	"										"	"	"	"	"		"		"		"		"	"	"			"			"		
P	INPUT	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	"	0	0	0	0	0	0	0	"		"	"	"			"			"		
	OUTPUT	1	1	0	1	0	0	MRNZ → X_0		0	0	0	0	0	0	0	"	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
SR	SET N OR Z —OR— SET A OR E	1	0	1	0	0	0	0	0	0	N_1	N_2	N_3	N_4	0	0	0	0	0	0	N_5	N_6	N_7	N_8	N_9	N_{10}	N_{11}	N_{12}	N_{13}	N_{14}	N_{15}	N_{16}	N_{17}	N_{18}	N	1	1
										Z_0	Z_1	Z_2	Z_3	Z_4	0	0	0	0	0	0	Z_5	Z_6	Z_7	Z_8	Z_9	Z_{10}	Z_{11}	Z_{12}	Z_{13}	Z_{14}	Z_{15}	Z_{16}	Z_{17}	Z_{18}	Z		
					COPY AX, AY, AXY CODING IF OVER-LAPPING OTHERWISE ZEROS										0	0	C(6) C (1)	C → A HOLD	1	1	C → E HOLD	0	0	0	0	0 E_1	0 E_2	0 E_3	A_2 E_4	A_3 E_5	A_4 E_6	A_5 E_7	A_6 E_8	A_7 E_9	A_P E_P	0	0
SJ	SET J_{8-11} TO ΣCZ	1	0	0	0	0	0	0	0	Z_0	Z_1	Z_2	Z_3	Z_4	0	0	0	0	0	0	Z_5	Z_6	Z_7	Z_8	Z_9	Z_{10}	Z_{11}	Z_{12}	Z_{13}	Z_{14}	Z_{15}	Z_{16}	Z_{17}	Z_{18}	0	ΣCZ → J_8 J_9 J_{10} J_{11}	
JP	SET S CONDITIONAL ON J_{0-15} SET J_{4-6}	1	1	1	COPY AX, AY, AXY CODING IF OVER-LAPPING OTHERWISE ZEROS										512 C M F.V. → S		HOLD J_{4-6} → C	J_4	J_5	J_6	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_P	BINARY ADDRESS J_{0-15}		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36

FIG. 93. INTERPRETATION OF 'C' BITS

$C_{28 - 33}$ - sources of information for the arithmetic/logical network.

$C_{35, 36}$ - source of information to be set into N or Z register.

$C_{34,}$ - set information into N or Z register.

The hold register facility is provided by inhibiting the register clock or in the case of the E register by setting the register to itself.

Not all of these bits are necessary for all transfers. The A_x and A_y transfers make use of only one store, the main store and the register store respectively. The C bits associated with the other store are arbitrarily set to zero but are ignored. The F transfers do not use either store and bits $C_{4 - 13}$ are ignored unless overlapping as discussed below. Information transfers on the M information channel constitute a special case of the A_x order. On input to the machine, $C_{4, 5}$ specify A to X_D and the information is transferred to the M register and then to N or Z if required. On output the information in M, R, N or Z register is transferred to the output bus and hence to the required peripheral. C_{21} determines whether the transfer is input or output.

The S_R transfers contain 2 sub-sets, both concerned with transferring part of the C word to a register. In setting the N or Z register, $C_{35, 36}$ sets the gating circuits and C_{34} specifies which register is involved. The information is contained in bits 9 - 13 and 20 - 33. This information can be subsequently transferred to M or R if required with an F transfer. In a C to A or E transfer, $\overline{C}_{16}\ \overline{C}_{17}$ transfers $C_{28 - 34}$ to A $C_{16}\ \overline{C}_{17}$ transfers C_{33} to A and $C_{18}\ C_{19}\ \overline{C}_{20}$ transfers C_{25-34} to E.

The Sj transfers specify a test word to perform the Σ CZ operation and buffer the result into one of the jump buffers J_{8-11} as directed by $C_{35, 36}$. The bits C_{9-13} and C_{20-33} provide a mask which allows any sub-set of Z to be tested for zero.

A J_p transfer allows the setting of S to be conditional on 1 of the

sixteen jump buffers J_{0-15}. The source of S information is specified by $C_{14,15}$ and for a C to S transfer, the S bits are contained in C_{20-32}. J_{4-6} may also be set to bits C_{17-19} at the same time. The jump buffers J_{1-3}, J_7, and J_{12-15} are derived from various bits of the machine registers and $J_0 = 1$ to provide an unconditional jump. An unsuccessful jump results in S being incremented.

The timing pulses required to carry out these transfers are generated from a basic chain of blocking oscillators linked together with logic circuits. The particular interconnection required is specified by C_{1-3}. The A transfers use a 6 μsec loop while the F, S and J transfers which do not involve store access have a 1.5 μsec cycle. The initial section of both interrogates the control fixed store, setting up the gating and logic throughout the machine and defining the type of transfer and timing to follow. The continuity of the timing chain is conditional on parity checks on the information transfers and in the event of a parity failure the machine will freeze with the faulty information displayed in the registers. One or two 1.5 μsec timing cycles may also be overlapped with the latter portion of the 6 μsec A cycle, allowing F, S or J transfers within the hardware not involved in writing into the stores. Under these conditions the settings of C_{4-13} and some registers must be retained to avoid interference with the A transfers. Logic circuits based mainly on the appropriate bits of the C register gate the basic timing pulses to provide the register clocks and to control store behaviour.

The normal machine user will not be concerned with the detail of the control function, a machine order providing direct contact only with the main store, part of the register store and the peripheral units. The structure of the machine order as held within the machine is shown in Fig 94 (a). B and Y specify the register in the register store to be used for index register and accumulator respectively, while X generally refers to a location in the main store. The B and Y addresses are relative to the first location of register storage allocated to the particular program but

1	2 3 4 5 6	7	8 9 10 11 12	13 14 15 16 17 18	1 2 3	4	5 6 7 8 9 10 11 12 13 14 15 16 17 18
T	B	P	Y	F	V	r	X
(1)	(5)	(1)	(5)	(6)	(3)	(1)	(14)

FIG. 94 a. THE CIRRUS INSTRUCTION

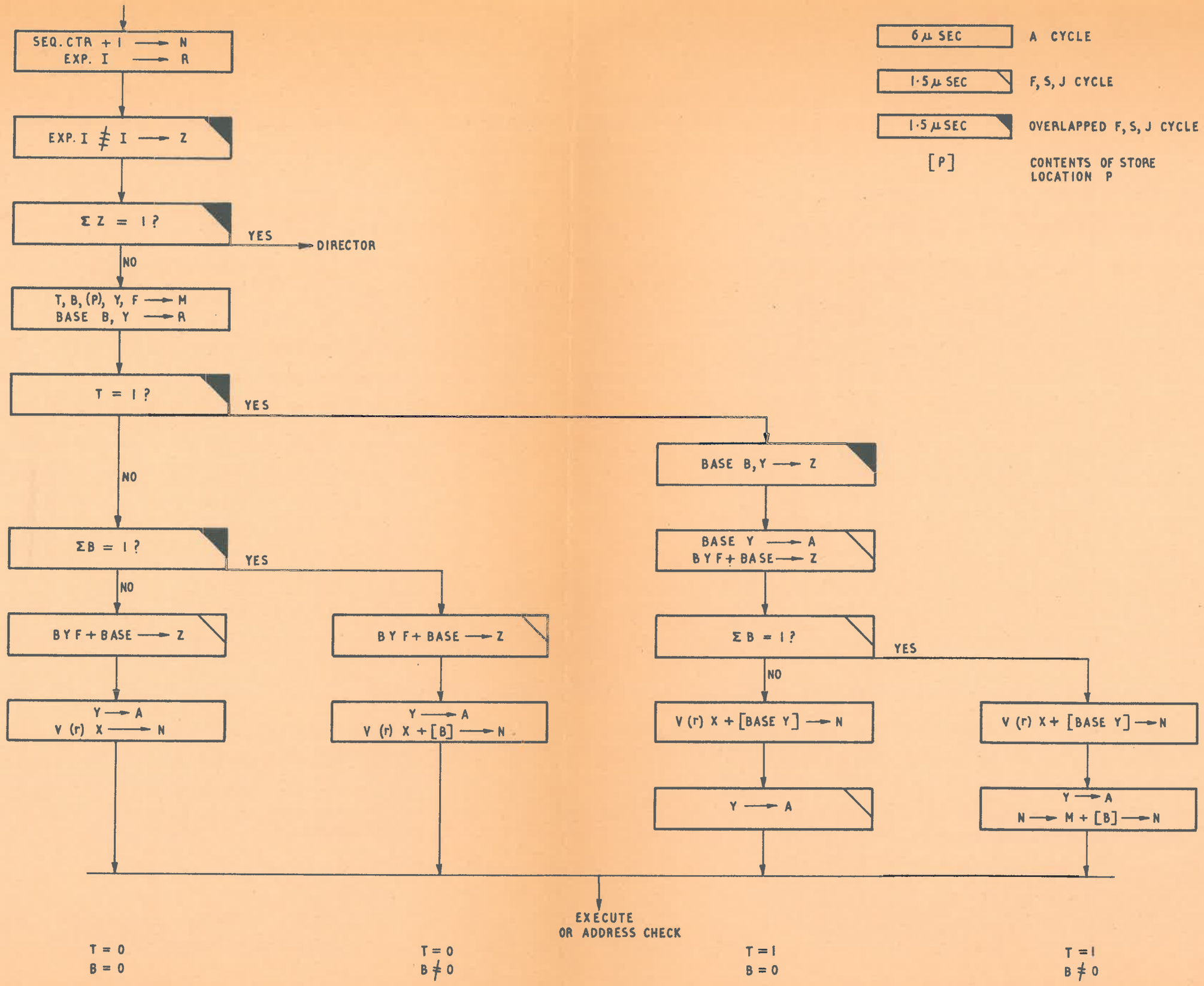


FIG. 94 b. THE ROUTINE PHASE OF ORDER EXECUTION

X as generated by the assembler or compiler is an absolute address within the main store. F and V together define 1 of 512 possible orders as an order type or function, F, and a variant, V, which may specify half word, full word, floating etc. The T bit allows a second address modification independent of that provided by the index register by adding the contents of register O (relative) to the X address. The p and r bits are generated during compilation and will be ignored in the present discussion.

The execution of a machine order takes place in two phases, a routine phase common to all orders which sets up the order ready for execution, and the execution phase specific to each order which performs the required data manipulation. Both phases are controlled by sequences of transfers held in the control fixed store. The transfers of the routine phase, shown as a flow diagram in Fig 94 (b), suitably illustrate how the basic transfers are combined to provide the required machine behaviour and how the hardware of the data manipulation section may be time-shared.

Entry to the routine phase is obtained by setting the S register to 512, the address in the control fixed store of the first of these transfers. In the first cycle, both stores are interrogated, the main store being addressed from E and the register store to the lower half of location O. The E register contains the address in the main store of the sequence counter for the machine program currently being executed. This is the only information held in the machine registers between machine orders and if E is used for any other purpose during the execution of a machine order, the contents of E must be stored and returned to E before re-entering the routine phase. The contents of the sequence counter are brought down, incremented and returned to the store with the value retained in N. Location O in the register store contains the expected state of the indicators associated with the peripheral units. The first overlap cycle compares the expected and actual states of the indicators using the $\not\equiv$ function of the arithmetic unit and stores the result in Z. A second overlap cycle then tests the value of Z with a J_p transfer ($\Sigma Z = Z_1 + Z_2 + - - + Z_{18} = J_{15}$). If $\Sigma Z = 1$, S is

set to enter the director, a set of transfers controlling the multiprogramming facility which will determine the subsequent machine behaviour.

Assuming Z = O, the stores are again interrogated, the main store from N and the register store to the upper half of location O. The quantities, T, B, Y and F are set into M and the base address of B and Y into R. The T bit, M_1, is tested with an overlapping J_p transfer ($M_1 = J_7$) If T = O another overlapping transfer tests the B address ($\Sigma B = M_2 + M_3 - - + M_6 = J_2$). For B = O, denoting no address modification, M and R are added and the upper half of the order with B and Y converted to absolute addresses is set into Z. In the third store cycle, the main store, addressed by N is interrogated and the lower half of the order is transferred to N. Simultaneously the Y address is transferred from Z to A. If $\Sigma B = 1$, the register store addressed by the B bits of Z is interrogated in synchronism with the main store and the contents of the index register added to the lower half of the order as it is transferred to N.

If the test on T indicated that T modification was required, three fast cycles follow the test cycle. The first sets Z to R and the second transfers the base address of Y (= Register O relative) to A and subsequently sets the modified upper half of the order to Z. The B bits of M are then tested in the third cycle. The main store, addressed by N and the register store addressed by A are then interrogated and the modified lower half of the order is set into N. If ΣB test showed B = O, a fast cycle transfers the Y address from Z to A but if $\Sigma B = 1$, the contents of the index register are extracted from the register store and added to N in a fourth store interrogation.

At this stage all branches have resulted in the order being set up in the Z and N registers with all addresses modified and with the address of the register providing the accumulator function held in A. If the program is operating in "checking mode", the X address is now checked to ensure that it is within the limits allocated to the program. This pre-

caution will not normally be necessary with tested programs. The final step of the routine phase is to transfer the F and V bits of the order to S, entering the execution phase. The first 512 locations in the control fixed store are called the directory. Approximately half of the machine orders, which can be accomplished with 1 or 2 words in the control fixed store, are executed directly. In all other cases, the word addressed by the F and V bits causes a jump out of the directory to another section of the control fixed store which contains the necessary sequence of transfers to execute the order. The final step of each execution phase contains a 512 to S transfer causing re-entry to the routine phase.

The overall system behaviour is thus defined by two sequences of transfers held in the control fixed store, the routine phase of order execution and the director. The latter is concerned with the multiprogramming behaviour while the former controls the detail of program execution, initiating a transfer to the director when necessary.

The above discussion developed from a consideration of the control unit of a digital machine as a sequential switching circuit. The resulting form of control does not in itself represent an innovation, since the concept of holding the set of transfers describing each machine function within a control store was originally described by Wilkes nearly ten years ago (N1). The availability of a cheap high speed store of large capacity has allowed this technique, commonly known as microprogramming, to be highly developed in the design of CIRRUS. This particular application consequently provides a convenient illustration of the use of fixed store to realise complex switching circuits and shows the influence which this can have on the design of digital equipment. No fundamental difference in structure exists between a microprogrammed machine and a more conventional structure. The advantages of this approach, economy and flexibility, are derived almost entirely from the particular hardware form of the control.

Two associated forms of control have also been described, both intended to provide even greater flexibility in the control functions but also illustrating other approaches to sequential circuit design based on the use of storage. In the first, the fixed store is replaced by a variable store, typically using cores. This has the advantage that the transfer functions of the combinational network can be more easily changed or, what is perhaps more significant, can be changed electrically and if required by the machine whose control functions are based on this store. This provides an additional degree of freedom in the design of both the control unit and the machine which could be exploited to advantage in some applications. This facility has been provided in a rather different manner in the second variation (N8) by the use of two stores, one fixed and the other variable. Each word in the fixed store represents a unique state, the fixed store providing the decoding from the input or address to the required control outputs. The contents of the variable store directly or indirectly specify sequences of addresses for the fixed store, defining the sequence of states necessary to execute the various machine functions. This configuration effectively separates the combinational and sequential aspects of the control. A change in the behaviour of the machine will normally require only a change in the contents of the variable store.

Both of these types of control would be slower and more expensive than that using only a fixed store, while the additional flexibility of an electrically changeable store could only be used in a few special purpose applications. In the majority of cases, some form of semi-permanent storage would be more suitable.

SECTION F

CONCLUDING REMARKS

The core stores described in section B were designed as part of a larger project and consequently the development was directed towards the needs of this project rather than to extending the state of the art. The objective was to design a reliable and economical store compatible in speed and cost with the rest of the machine and using components conveniently available through local sources. Within these restrictions, the core stores represent the best compromise possible at the time the development work was carried out, although faster stores could have been designed, at greater cost, using either linear selection or coincident current selection. Improved cores and semiconductors now available would however allow the speed of both the stores and the logic circuits to be doubled without increasing the cost of the machine. The faster switching speed of more recent coincident current cores is largely achieved by an increase in the coercive force of the ferrite and a corresponding decrease in core size. These two factors tend to compensate so that the drive current and drive voltage are similar to those for the slower cores.

To make best use of the current components, a number of changes would be made to the store circuits although the same basic approach would still be used. The non-saturating drivers used to generate the switch and inhibit currents proved to be the simplest and cheapest circuit configuration at the time, but the AUYIO is relatively expensive and satisfactory performance could now be achieved more cheaply with saturated drivers. The sink driver would also be modified by replacing the OC140, AUYIO combination with a saturated NPN transistor, reducing both the cost of this circuit and the time required for address selection. Similarly the OC140 steering transistors in the

inhibit drivers would be replaced with more suitable transistors.

The changes to be made to the sense amplifier are not as well defined, being dependent on the magnitude of the noise in the plane output, but two modifications can be anticipated. The first, concerning the input stage, could well be made to the existing amplifier. As mentioned in section B, although the present configuration is satisfactory, the method used to couple the two sections of these winding to a single amplifier results in an undesirable loading of the sense winding and accentuates the disturbance due to the inhibit current. This would be prevented by using two preamplifier transistors each with a separate input transformer allowing a more suitable plane loading to be chosen. The two inputs could be OR-ed into the subsequent amplifying stages by using a common collector load. If the store outputs have sufficient signal to noise ratio during the read phase, the present method of discrimination may be satisfactory with a faster threshold transistor, but it may be necessary to use a different approach to both output discrimination and the clocking of the M register to ensure reliable operation. Problems of amplifier recovery at the faster cycle may also require a different approach to the design of the sense amplifier.

The time allowed for recovery of the sense amplifier from the inhibit transient represents a delay in the store cycle which for most cycles is unnecessary. The overall speed of the store could be increased appreciably by making the re-drive of the store conditional on the recovery of the amplifiers from the previous write disturbances. The amplifier outputs OR-ed together would provide the appropriate control signal. The time

allowed for amplifier recovery would then be adjusted to the required figure rather than to a fixed worst case maximum. Such a procedure would allow the stores in their present form to operate on a 5 μsec (ave) cycle without any reduction in operating margins if the machine timing were adjusted accordingly, and would simplify amplifier design for a higher speed store. The required modifications to the timing circuits are relatively simple.

The self-derived strobe used in the core stores did not prove to have any significant advantages over a fixed strobe and for simplicity has been discarded in favour of the latter. This is largely due to the poorly defined currents applied to the strobe plane and the resulting compromises in the design of the strobe circuit. This technique is potentially capable of yielding considerable information about the store operation. The peak value of the output voltage is an indication of the magnitude of the drive currents and could be monitored to adjust for drift in the power supplies or drive circuits and to compensate for variations in the ambient temperature. The time of occurrence of the peak would allow the position of the strobe to be adjusted to sense the store outputs when the discrimination ratio is a maximum while a failure in the drive circuits would be indicated by the absence of a suitably timed strobe. A complete strobe plane would have been necessary to obtain signals clean enough to give the full benefit of this technique. A spare plane was not available, but it is doubtful if the added expense and complexity would be warranted. With the poor signals from the small strobe plane, the self-derived strobe was effectively fixed in time, showing little variation with the magnitude of the drive current. The

only advantage gained by the use of this circuit was that for low drive currents, strobe failure occurred before the output discrimination deteriorated but this did not contribute significantly to store operation, or to the diagnosis of store faults. In any case the parity bit provided sufficient check on the store performance, detecting marginal behaviour or by using even parity on 19 bits, a failure of the drive circuits with the resulting all '1' output.

The fixed stores were also intended to be an integral part of a system and development work was of necessity confined to those forms which provided the required characteristics and which could be constructed with the available facilities. In particular, any store using printed circuit construction or specialised production techniques could not be considered. The emphasis again was on achieving the desired performance at low cost. The MK I store was an attempt to overcome the functional and mechanical disadvantages of wired core arrays. This form was not particularly successful but the experience gained with MK I proved to be most useful in the design of MK II. Although the various parameters of MK II were chosen to suit the particular applications, the store is capable of much higher speed than the 1.5 μsec cycle required in the control unit. Unfortunately circumstances did not permit the full potential of this store to be investigated. Some modifications necessary for operation at higher speeds were discussed in section C when this store was described.

The machine language fixed store has not yet been constructed and may not in fact be used although it has always been assumed

that portion of the main store, probably 4096 words would be fixed storage holding the assembler, compiler and important sub-routines. The uncertainty is due to the limited address capacity of the CIRRUS instruction, 14 bits or 16,384 words, and to the cost structure of core storage. Being a multi-program machine, it is desirable that the maximum possible core storage be provided, and it is almost certain that the full address capacity will ultimately be used. The application of fixed storage here does not convey any direct benefit other than a potential saving in cost, although the storage of the important system programs within the machine does provide considerable operating advantages and a reduction in the total storage requirements for multi-program operation. The non-volatile nature of fixed storage is a convenience, but is not essential and this section of the main store could be conventional core storage if this were more convenient.

Only two blocks of core storage, 4,096 words, are currently installed in the machine although the store was designed electrically and mechanically for 8,192 words. The addition of the other two blocks of store and 4,096 words of fixed storage would fill the available space within the machine frame. The other 4,096 words whether fixed storage or core storage would have to be accommodated externally in a separate frame. Two factors, the availability of faster cores and of larger planes with a much lower cost/core, suggest that this may not be the best avenue of development.

Planes of 64 x 64 cores cost £63 in comparison with £140 for 128 x 128 planes, with in both cases a 10% increase for 6F2

cores which for a full drive of 600 mA will switch in 0.4 μsec. The cost of various units of storage is then approximately as follows:-

(i)	Complete present core store	£2,500
(ii)	Separate store of 4,096 words using 10 128 x 128 planes driven as 20 128 x 64 planes	£3,000
(iii)	Separate store of 8,192 words using 19 128 x 128 planes	£4,500
(iv)	Separate store of 12,288 words (effectively (ii) & (iii) driven as single unit) 6 μsec cycle	£6,000
	3.5 μsec cycle	£6,500
(v)	Separate store of 16,384 words using 38 128 x 128 planes with arrangements to handle half words 6 μsec cycle	£7,500
	3.5 μsec cycle	£8,000
(vi)	4,096 words of fixed storage	£1,000

Units (i) - (iii) would have to have a 6 usec store cycle for compatibility with the present store and would have to be placed in a separate frame external to the machine. Units (iv) and (v) could be accommodated in a frame of the same size as the existing store and using the faster cores could provide a store cycle of not more than 3.5 μsec. If the faster cores were used, the present store would be discarded and the rest of the machine hardware would have to be modified to make use of the greater speed. The register store cores would have to be replaced with the faster type and some transistors in the logic circuits would also have to be replaced. The existing hardware in the register store would probably be satisfactory for the faster cores. These circuits were designed around the larger main store and have

considerable reserve capacity with the smaller unit. These modifications would cost £1000-£1500. It would also be desirable to decrease the cycle of the control fixed store to say 1 μsec. This would involve at most the substitution of the present 200T output winding with 150T elements, a relatively simple process. There would also of course be consequential changes to machine timing but these involve only magnitudes and not the timing logic.

The cost of the various alternative methods of extension are therefore:

A	Complete present store	2500
	add 4096 words of core store	3000
	& 4096 words of fixed store	1000
		£6500
B	Add separate unit of 8192 words of store	4500
	& 4096 words of fixed store	1000
		£5500
C	Add separate unit of 12,288 words of store	£6000
D	Discard present store and construct 12,288 words of	6600
	faster store and 4096 words	1000
	of fixed store. Modify rest of machine to suit	1500
		£9000
E	Discard present store and construct a 16,384 word store using faster cores	8000
	modify rest of machine	1500
		£9500

These figures reveal three significant facts: the designed method of extension is not the most economical, fixed storage allows a cost reduction of only £500 and the use of the faster cores enables the machine speed to be almost doubled for an expenditure of approximately £3500 or 10% of the total machine cost at this stage of development. Financial considerations would suggest that B or C would be the most likely method of extension, but factors other than cost could well influence the final choice.

APPENDIX 1

SELECTION SWITCHES BASED ON BINARY CODES

(1) SOME BACKGROUND THEORY

The majority of magnetic selection switches use a 2-dimensional array of square-loop switch cores with a driver connected to each of the co-ordinate drive lines of the array. The required 1-of-n selection is achieved with a relatively simple addition of M.M.F.$^{\Delta}$ in the switch cores against either a fixed bias or a variable bias generated by a sub-set of the drivers. The selection process generally makes use of both the flat saturation characteristic and the switching threshold of the core material, and in most cases, only one driver effectively contributes to the switch output. There exists, however, another class of switch which makes use of the relationship between the codes of error-correcting code groups and which has a number of advantages over the more conventional type of switch.

Consider the set of M linear transformers shown in Fig. 95. The primary of each transformer is connected to a driver capable of delivering to the transformer a voltage of +1 or -1 units. Each transformer has N identical secondaries ($N \leqslant 2^M$) interconnected in the manner shown. The characteristics of this arrangement can be expressed by (1) where each element A_{nm} can take values of +1 or -1 and represents the polarity of connection of the transformer secondaries. V_m and V_n are driving and output voltages resp.

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \\ v_N \end{bmatrix} = \begin{bmatrix} A_{1,1}, & A_{1,2}, & \cdots & A_{1,m}, & \cdots & A_{1,M} \\ A_{2,1} & A_{2,2}, & \cdots & A_{2,m}, & \cdots & A_{2,M} \\ & & & & & \\ A_{n,1}, & A_{n,2}, & \cdots & A_{n,m}, & \cdots & A_{n,M} \\ A_{N,1}, & A_{N,2} & \cdots & A_{N,m}, & \cdots & AN,M \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_m \\ V_M \end{bmatrix} \quad \text{- (1)}$$

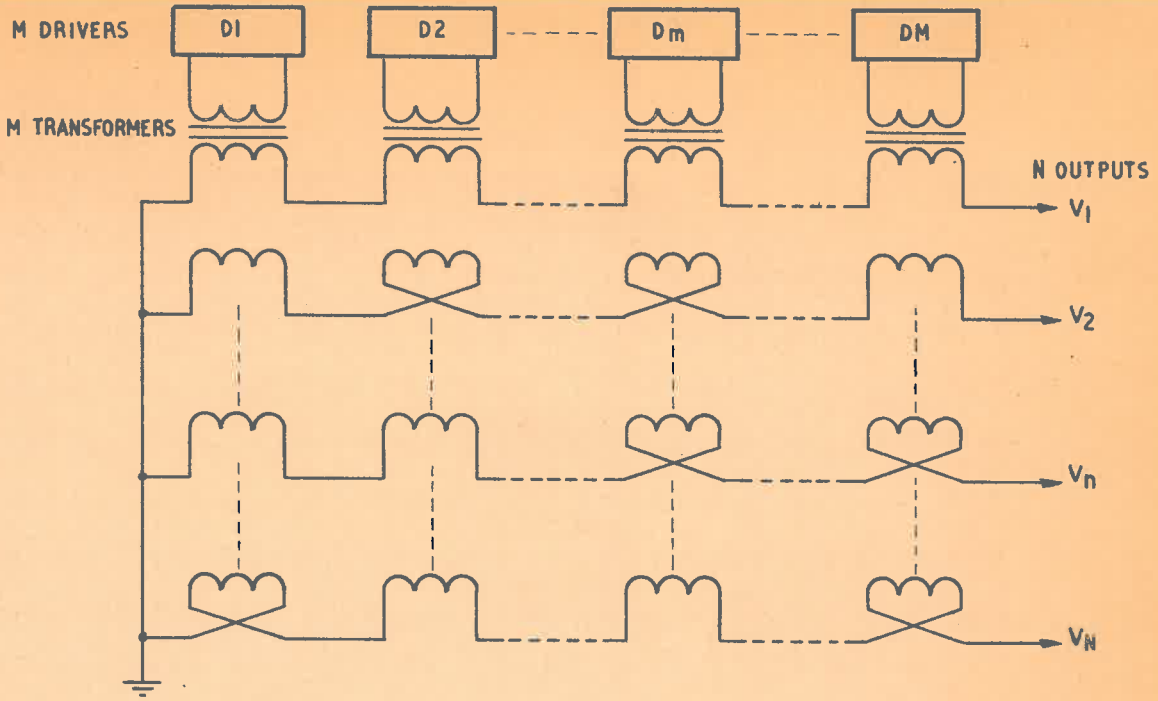


FIG. 95. VOLTAGE-DRIVEN SWITCH

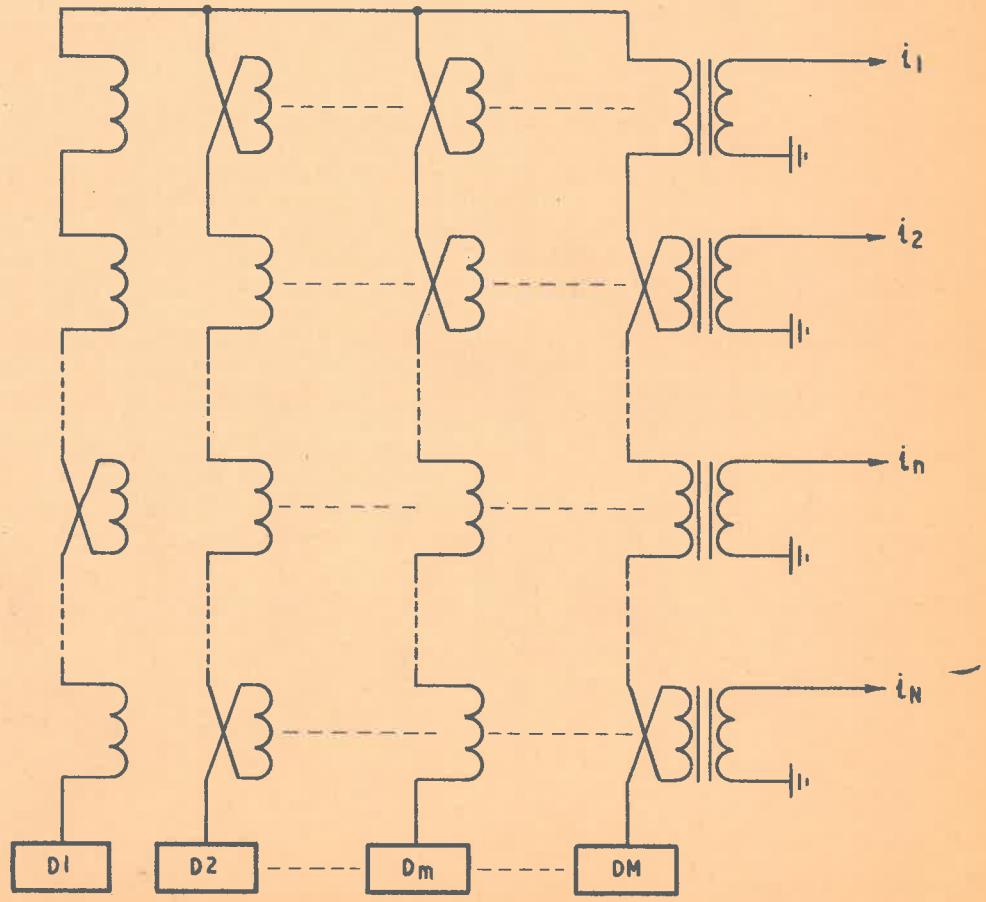


FIG. 96. CURRENT-DRIVEN SWITCH

If we now introduce the vectors.

$$\bar{A}_n = (A_{n,1}, \quad A_{n,2}, \quad \cdots \quad A_{n,m} \quad \cdots \quad A_{n,M})$$
$$\bar{V} = (V_1, \quad V_2, \quad \cdots \quad V_m, \quad \cdots \quad V_M) \qquad - (2)$$

then (1) can be written:

$$v_n = \bar{A}_n \bar{V} = \sum_m A_{n,m} V_m \qquad (3)$$

If a driving signal represented by the vector $\bar{V} = \bar{A}_n$ is applied to the network, the selected output v_n has the value.

$$v_n = \bar{A}_n \cdot \bar{A}_n = M. \qquad (4)$$

since all input signals reinforce to produce v_n

The value of v_n for $n' \neq n$ is

$$v'_n = \bar{A}_n \cdot \bar{A}'_n = \sum_m A_{n'm} A_{n.} \qquad (5)$$

$$= s - d$$

$$= M - 2d$$

where s = the number of elements $A_{n',m}$ of $\bar{A}_{n'}$ which agree with elements A_{nm} of $\bar{A}_n$.

& D = the number of elements $A_{n',m}$ of $\bar{A}_{n'}$ which disagree with elements A_{nm} of $\bar{A}_n$.

i.e. $s+d = M$.

Consequently the discrimmination ratio, k, of selected to non-selected outputs is

$$k = \frac{M}{M - 2d} \qquad (6)$$

Note that if $d = \frac{M}{2}$ then $k = \frac{M}{0}$ and only the selected output, n, is energised.

This voltage driven switch requires standardised input voltages and provides a set of output voltages defined by (4) and (5). However in many cases it may be more convenient or more appropriate for the switch to be current driven i.e. defined currents are applied to the primaries and delivered to the secondaries. In this case, the A matrix defining the wiring and interconnection of the transformers is used in a different manner, the matrix describing the polarity of coupling relative to the secondary of a set of interconnected primaries, the $M.M.F^s$ developed by the drive currents being added algebraically in the transformer core. The matrix is used in the same sense, describing an array of M inputs and N outputs, but the interconnection is now done column-wise instead of row-wise, with N transformers each with M windings instead of M transformers with N windings (Fig 96). This is just the dual of the voltage driven case.

If each of the binary sequences represented by the vectors A_n are considered to be members of an M-bit binary code group containing N codes, the d of (5) is equivalent to the distance between the two members $\bar{A}_n$ and $\bar{A}_{n'}$. To obtain a sufficiently high value of k, then d, or d_{min} if d is not constant, must be relatively large. Consequently the vectors $\bar{A}_n$ constitute an error-correcting code and a number of switches of this type are based directly on these codes. For any chosen values of N and k it is possible to develop a suitable code, but M increases with k and a compromise must be reached between the discrimination ratio and the number of drivers required. For the desirable case where $d = M/2$ it has been shown that M>N (M5). This class of switches, commonly known as the load-sharing switch, is discussed later.

For the class of switch with a finite value of k, it is necessary to associate a threshold element with each output or to have a

threshold in the load to ensure that only one output is affectively energised. The threshold may be either polar or non-polar. A polar element is one which responds to signals algebraically greater than a certain threshold, e.g. a diode in a voltage driven switch. A non-polar element is sensitive to signals greater than the threshold in magnitude, irrespective of polarity. A square-loop core in a current driven switch may be included in this category. A non-polar threshold places an additional restriction on the system in that a maximum distance is also specified between any two codes. The value of d must be between d and $M - d_{min}$ to ensure that the magnitude of the non-selected outputs is always less than $M - 2d_{min}$. It can be simply shown that this restriction implies that for a given M and d_{min}, N cannot be greater than half the value possible for a switch with polar threshold elements.

The major advantage of this type of selection switch is that each of the M drivers contributes to the switch outp ut, allowing each driver to be more lightly loaded. The properties of the core material have only a second order effect on switch behaviour and the square loop material used in the more conventional switches can be replaced by linear material with a corresponding reduction in switch losses. An important feature of these switches, associated with the addition of power from a number of sources, is the protection provided against driver failure. If one driver fails, the discrimination ratio of theswitch will be reduced to $k = \frac{M - 1}{M - 2d + 1}$. In the event of a double failure, or an error, i.e. a driving signal of +1 instead of -1, the discrimination ratio is reduced to $k = \frac{M - 2}{M - 2d + 2}$. The system could be designed so that these reduced values of k would still give satisfactory performance.

These switches may also require less drivers than more conventional switches, but the actual saving is difficult to estimate unless a particular application is considered. The type of threshold element and the nature of the load can be very significant factors. For instance a polar element restricts the output to one polarity and may require duplication if a bi-polar output is required. Again, if a core store is driven with this type of switch and the cores themselves used as the threshold element, the many spurious outputs from the switch may generate sufficient response in the store to reduce the signal to noise ratio below a satisfactory level. It is also likely that the cost of separate threshold elements for each output would negate any saving in the cost of the switch drivers.

A detailed discussion of the generation of the codes for these switches is beyond the scope of the present discussion, but some typical examples are shown below.

(2) SOME SWITCHES WITH $d \neq \frac{M}{2}$

Any code group with a suitable value of d can be used for these switches but those which provide the increased distance by simple parity checks are the most convenient since the selection of the appropriate drivers is much simpler. Three examples are shown below and others can be found in Ref M1.

(a) $N = 16,\ M = 6,\ d_{min} = 2.$

$D_1 = 0$

$D_2 = 1$

$D_3 = 2$

$D_4 = 3$

$D_5 = 4$

$D_6 = 0.1.2.3.4.$

D_1 is a digit representing a constant 1 signal and restricts d_{max}

to $M - d_{min}$ by ensuring that no code is present in its complemented form.

$D_2 - D_5$ are the independent address digits specifying the 16 addresses. D_6 is derived by taking even parity on digits 0, 1, 2, 3 and 4 or 1, 2, 3, and 4 since 0 is a constant signal and only introduces an inversion in the parity.

The first 8 of these codes are:

1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0

etc.

For this code $2 \leq d \leq 4$ with corresponding outputs of +6, ± 2 and 0, or -6, ± 2 and 0.

To select output N, the driver M_i delivers an output of +1 if $A_i = 1$ or -1 if $A_i = 0$.

Complementing this procedure will reverse the polarity of the output.

(b) $N = 1024$ $M = 16$, $d_{min} = 4$

$D_1 = 0$) - constant 1

$D_2 = 1$)
)
$D_3 = 2$)
)
$D_4 = 3$)
)
$D_5 = 4$)
)
$D_6 = 5$)
)
$D_7 = 6$)

$D_8 = 7$)
$D_9 = 8$) In dependent address bits specifying
$D_{10} = 9$) $2^{10} = 1024$ outputs
$D_{11} = 10$)

$D_{12} = 0.1.2.3.4.6.8.10.$)
$D_{13} = 0.2.3.5.6.9.10.$)
$D_{14} = 1.2.3.7.8.9.10.$) Parity checks
$D_{15} = 4.5.6.7.8.9.10.$)
$D_{16} = 0.1.2.4.5.7.10.$)

This code is derived from Hamming's single error correcting code with the minimum distance increased from 3 to 4 by the addition of overall parity to the normal internal parities of this code.

The distance varies between 4 and 12 giving outputs of 16, $\pm$ 8, $\pm$ 6, $\pm$ 4, $\pm$ 2 and 0.

(c) $N = 2048 \quad M = 16 \quad d_{min} = 4$

If in the above case the constant digit represented by D_1 is replaced by another independent address digit, N is increased to 2048 but d_{max} is now 16 and the code is suitable only for use with polar threshold elements. The outputs are

$\pm$ 16, $\pm$ 8, $\pm$ 6, $\pm$ 4, $\pm$ 2 and 0.

(d) Some advantages can be obtained by using a different number of turns on the transformers for positive and negative excitation such that for a positive output from the selected transformer, the non-selected outputs are zero or negative. (M9)

Referring to equation (5), the condition for zero excitation is:

$N(+).\ (M-d) = N(-).\ d.$

i.e. $\frac{N(+)}{M(-)} = \frac{d.}{M-d}$

Consider the current driven switch with

$N = 16,\ M = 5\ \ d_{min} = 2$

i.e. $N(+) = 2$ and $N(-) = 3$

$D_1 = 1$)
$D_2 = 2$) Independent address bits.
$D_3 = 3$)
$D_4 = 4$)
$D_5 = 1.2.3.4$ - Odd Parity

Each driver still emits outputs of +1 or -1 units but the wiring is separated for the positive and negative inputs to the switch with a slight modification to the A wiring matrix and to the transformer wiring to allow for the unequal turns.

Transformer	Code A B C D P	Wiring Matrix A($\bar{A}$)	B($\bar{B}$)	(C) $\bar{C}$	(D)$\bar{D}$	(P)$\bar{P}$	Nett Excitation
0	0 0 0 0 1	-3+2	-3+2	-3+2	-3+2	+2-3	0
1	0 0 0 1 0	-3+2	-3+2	-3+2	+2-3	-3+2	0
2	0 0 1 0 0	-3+2	-3+2	+2-3	-3+2	-3+2	0
(3)	0 0 1 1 1	-3+2	-3+2	+2-3	+2-3	+2-3	+10
4	0 1 0 0 0	-3+2	+2-3	-3+2	-3+2	-3+2	-10
5	0 1 0 1 1	-3+2	+2-3	-3+2	+2-3	+2-3	0
			etc.				

Where the digit of the code is in agreement with the driver concerned the linkage is +2 units, otherwise -3 units. This arrangement is to be compared with a bi-directional driver and +1 or -1 units of linkage with a single wire for the case with equal turns.

For any selected output, the nett excitations will be $\pm$ 10 and 0. If the switch cores are made of square loop material, the negative excitation will only drive the core further into saturation and the output will be small. The selected core cannot be reset by the complementary set of drivers since some cores will receive a positive excitation and will be set giving a large spurious output. Resetting can be most conveniently accomplished with a resetting bias of say - 5 units.

This modification complicates the switch wiring but removes the need for separate threshold elements and allows bi-directional outputs from the switch.

(3) THE LOAD-SHARING SWITCH

As noted above, this is only a special case of the type of switch described above in which all codes have $d = \frac{M}{2}$, resulting in no nett excitation for the non-selected transformers.

The codes can be generated by any suitable method, but a relationship has been observed between orthogonal matrices and error-correcting codes (M2, M3), and this is probably the easiest method of generation. Paley (M4) studied square matrices of order n x n where the elements are binary variables. The orthogonality condition requires that if any two rows are compared, the number of similarities equals the number of dissimilarities. Each row can therefore be considered as an n-bit binary code with a distance $n/2$ from every other code, i.e. an orthogonal matrix is a group of codes with $d = \frac{M}{2}$. One of the necessary conditions for a matrix

to be orthogonal is for n to be divisible by 4, and Plotkin (M5) in his work on error-correcting codes showed that there are at most N orthogonal sequences of N bits. Thus an orthogonal matrix generates the full complement of codes for each value of N. These have been derived for all relevant values of N between 4 and 128 except N = 92 and 116 (M3, M4.).

The load-sharing switch places another minor restriction on these codes i.e. each code must contain an equal number of +1's and -1's. There is always one code which does not satisfy this condition. Thus for any number of outputs, the minimum number of drivers is achieved by going to the next multiple of 4 for which an orthogonal matrix is possible. The original switch by Constantine (M6) overcame this difficulty by adding the complemented code set to create a 2n x n matrix requiring approx. twice the number of drivers (2.2^n instead of $2^n + 4$ to select 1 of 2^n outputs).

For a matrix with M inputs and N outputs, the selected output is M/2 units since each code contains $M/2 + 1^s$ and $M/2 - 1^s$. By appropriate selection of drivers, the selected output can be positive or negative, but the non-selected outputs are always zero.

A detailed account of the generation of these codes is covered in M2 - M4 and M6, but the codes for N = 4, 8 and 16, the most commonly used switches for computers are shown in Fig. 97. These switches differ in two respects from those of section (2). First the drivers are only required to deliver a uni-directional output pulse defined as +1 units. The codes shown therefore represent the polarity of coupling of the inter-connected windings relative to the input winding for a voltage driven switch or to the output winding

+	−	+	−	+	−	+	−
+	+	−	−	+	+	−	−
+	−	−	+	+	−	−	+
+	+	+	+	−	−	−	−

(a). 8 INPUT-4 OUTPUT SWITCH

+	−	+	−	+	+	+	−	−	−	+	−
+	−	−	+	−	+	+	+	−	−	−	+
+	+	−	−	+	−	+	+	+	−	−	−
+	−	+	−	−	+	−	+	+	+	−	−
+	−	−	+	−	−	+	−	+	+	+	−
+	−	−	−	+	−	−	+	−	+	+	+
+	+	−	−	−	+	−	−	+	−	+	+
+	+	+	−	−	−	+	−	−	+	−	+

(b). 12 INPUT-8 OUTPUT SWITCH

+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	−
−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	+	−
+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	+	−
+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−	−
−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−	−
−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−	−
−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−	−
−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−	+	−
+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	+	−
−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	+	−
+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−	−
−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	+	−
+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	+	−
+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	+	−
+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	+	−
+	+	+	+	−	+	−	+	−	−	−	−	+	+	−	+	+	−	−	−

(C). 20 INPUT - 16 OUTPUT SWITCH

FIG. 97. LOAD-SHARING SWITCH CODES

for a current driven switch. Secondly the codes bear no direct relationship with the b independent address bits defining the 2^b outputs as with the previous type of switch. This makes driver selection more difficult but for switches of the size considered practical this is of little consequence.

A modification to these switches, described by Vogl (M8) uses both primary and secondary summation although the switch is basically current diriven. It has the advantage of fewer windings on each transformer, a significant factor where very high operating speeds are required.

By applying the concepts of block designs to the logical design of load-sharing switches another class of switch has been developed (M10-M12) which allows greater design freedom and permits the construction of larger switches than those based on orthogonal matrices. These switches are still subject however to the restriction that $M \geq N$. One example of this type is the switch of Fig. 98. By using unequal turns on the windings a zero noise 17 input - 16 output switch has been developed. The excitation of the selected output is +12 or -12 depending on the choice of drivers.

Normally the aim is to produce a switch with the minimum number of inputs as has been assumed above. However if this requires excessive power from each driver or if it is a design condition that the switch will still operate satisfactorily with a limited number of driver failures, then the number of drivers may

-1	2	-1	-1	-1	-1	-1	2	-1	2	2	-1	2	-1	-1	2	-2
-1	-1	-1	-1	2	2	-1	-1	2	2	-1	-1	2	-1	2	-1	-2
-1	-1	-1	2	-1	-1	2	-1	-1	2	2	2	-1	-1	2	-1	-2
2	-1	2	-1	-1	-1	-1	-1	-1	-1	2	-1	2	2	2	-1	-2
-1	-1	-1	2	-1	-1	-1	2	2	-1	-1	-1	-1	2	2	2	-2
-1	2	-1	2	2	2	-1	-1	-1	-1	2	-1	-1	2	-1	-1	-2
-1	2	-1	-1	-1	-1	2	-1	2	-1	-1	2	2	2	-1	-1	-2
2	2	2	2	-1	-1	-1	-1	2	2	-1	-1	-1	-1	-1	-1	-2
-1	2	2	-1	2	-1	2	-1	-1	-1	-1	-1	-1	-1	2	2	-2
-1	-1	2	-1	-1	2	2	2	2	-1	2	-1	-1	-1	-1	-1	-2
-1	-1	2	2	2	-1	-1	2	-1	-1	-1	2	2	-1	-1	-1	-2
2	-1	-1	-1	2	-1	2	2	-1	2	-1	-1	-1	2	-1	-1	-2
2	2	-1	-1	-1	2	-1	2	-1	-1	-1	2	-1	-1	2	-1	-2
2	-1	-1	-1	2	-1	-1	-1	2	-1	2	2	-1	-1	-1	2	-2
2	-1	-1	2	-1	2	2	-1	-1	-1	-1	-1	2	-1	-1	2	-2
-1	-1	2	-1	-1	2	-1	-1	-1	2	-1	2	-1	2	-1	2	-2

FIG.98. 17 INPUT-16 OUTPUT SWITCH

have to be increased. This is achieved by using an abridged form of a larger switch e.g. the M = 20, N = 16 switch of Fig. 97 could function as an M = 20 N = 8 switch by using only the first 8 rows of the matrix. The other properties of this non-minimum switch are the same as for the complete switch.

APPENDIX 2

A DRIVE SYSTEM USING A NEW TYPE OF DRIVE SWITCH

(1) INTRODUCTION

The drive system described below was designed during early development work against a very different background to that of the system finally adopted. The capacity required in both stores was lower, 4096, 19 bit words in the main store and 128 20 bit words in the register store. Only 80 thou. cores were available at the time, the core used, F X 1508, requiring 400 mA 1.75 μsec drive pulses for coincident current selection. The transistors available at the time had very limited ratings and had to be used as saturated switches to minimise dissipation. The use of the load-sharing switch was almost essential. The transistor ratings were marginal for direct drive and inadequate for most other forms of magnetic switch due to switch losses and the fact that only one driver actively contributed to the switch output.

In this case the load-sharing switch is used as a set of voltage rather than current transformers although primary summation is used. The output current is defined by resistors in the output windings of the switch. If linear magnetic material is used for this mode of operation trouble is experienced with the fall time of the drive pulses. During the pulse the operating point of the transformer core is driven up the hysteresis loop and will return to zero at the end of the pulse, generating a current in the reverse direction, the magnitude and duration of which are determined by the circuit time constant. The use of square loop material can prevent this undesirable effect, since the flux state does not reset at the end of the drive pulse.

The operating path of the core is shown in Fig. 99. The cores normally rest at A. During the read pulse, the selected switch core

is driven from A to B generating a pulse on the selected output. When the drivers are switched off, the core falls to C, terminating the read pulse. The drive for the write period is in the opposite direction and the core is driven along the path CDEF, generating a write pulse of opposite polarity in the selected output. At the end of the write pulse the core returns to A. The irreversible flux available for the write pulse is less than that available for the read pulse and with equal read and write drives, F is sufficiently far into saturation to ensure that A is a stable initial state.

During the pulse the drive windings are fed from a low impedance constant voltage source and produce a constant output voltage. To provide an effective constant current source, and to minimise the time constant of the load, the secondary resistance is chosen to be much greater than the inductive reactance of the drive lines. The current taken from the switch drivers is determined by the magnetising current of the transformer and the reflected load current. For a given output pulse duration, the percentage of flux switched and the magnetising current required are determined by the applied voltage and the choice of both core and turns. The non-selected cores of the load-sharing switch receive no magnetising current and appear as a small impedance in series with the switch drivers.

A load-sharing switch of sufficient size to provide the 1 of 64 selection required by the main store was neither practical nor economical so a combination of load-sharing switch and magnetic switch was employed. Conventional magnetic switches were deliberately designed for undirectional drive pulses and are not suited to the bidirectional output of the load-sharing switch. The switch of Fig. 100 was developed for this purpose. Each of the 8 outputs of the load-sharing switch is connected

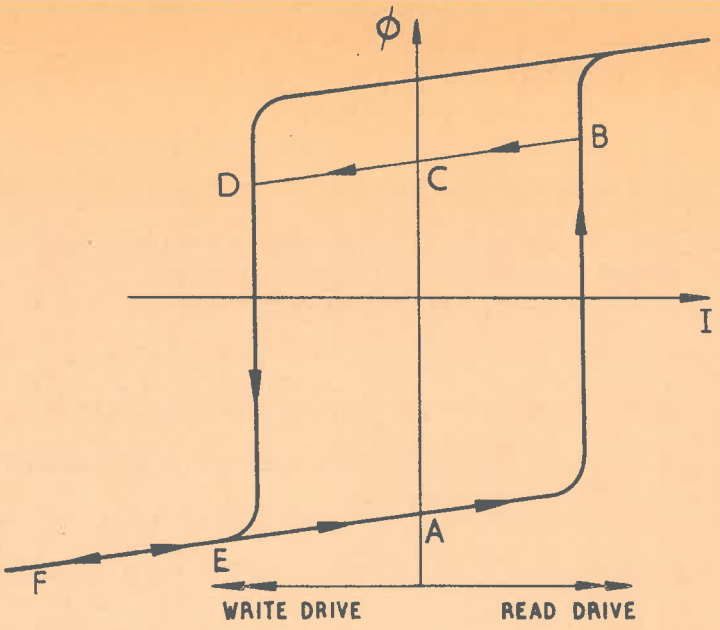


FIG. 99. OPERATING PATH OF SWITCH CORE

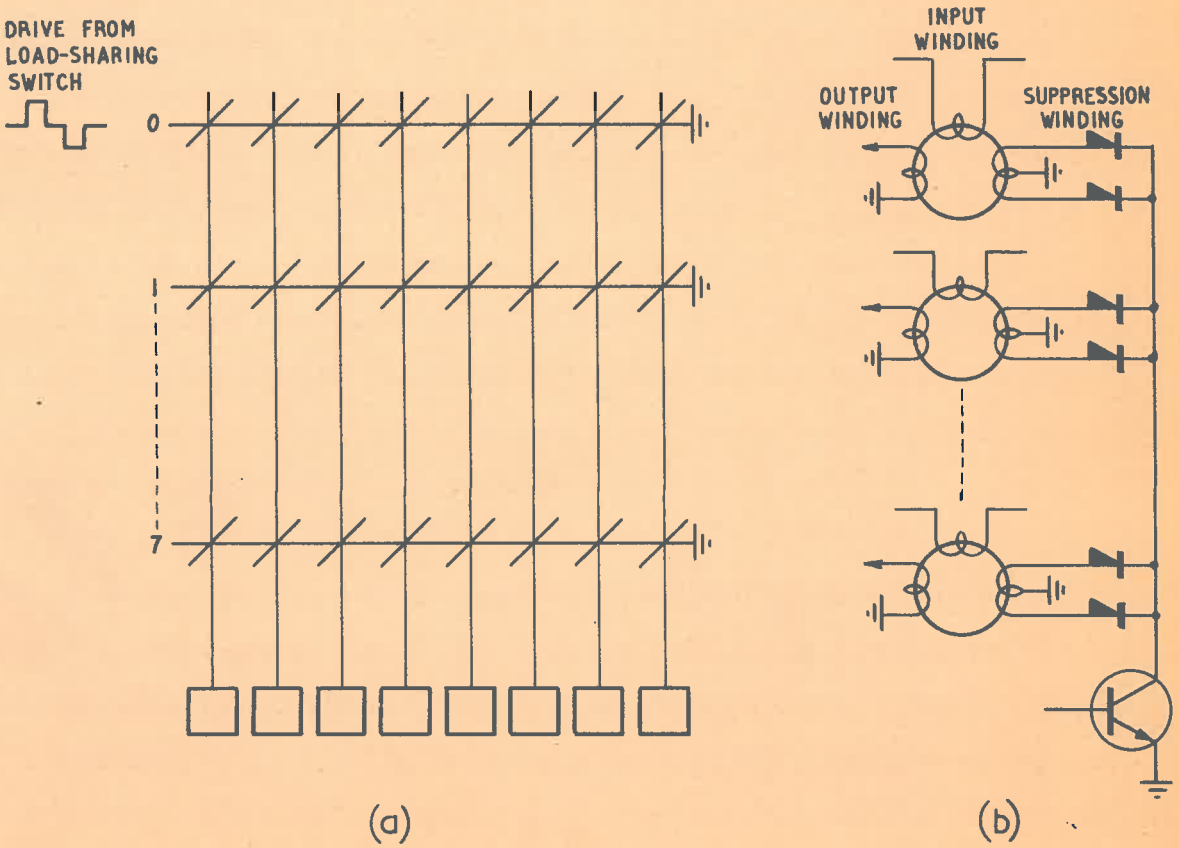


FIG. 100. SCHEMATIC DIAGRAM OF SUPPRESSED SWITCH

to a row of 8 cores each of which has 3 windings, an input winding, an output winding and a suppression winding. By applying a short circuit across the suppression winding of the non-selected cores in the driven row, only the selected core will switch freely and produce an output, thus driving the selected drive line. The short circuit is applied by means of a saturated transistor as shown in Fig. 100 (b). Only one transistor is required for each column since only one row is active at any time and the diodes necessary to cope with both positive and negative drive pulses also isolate the cores in a column preventing interaction. The suppression transistors need not have a high power rating since they only dissipate power when in the saturated state. By having many turns on the suppression windings the voltage across the input and output windings can be made very low. The limit is imposed by the voltage applied to the suppression transistor in the off state by the selected core. The impedance of the non-selected cores is mainly resistive and had less effect on the output waveform than a similar switch in which the non-selected cores were biassed into saturation.

A 32 output switch of this type was constructed using an 8 input - 4 output load-sharing switch and 4 rows of 8 cores in the drive switch. This was to drive the register store, each plane of which used a 32 x 4 array of cores. A 4 output load-sharing switch was to drive the other set of drive lines. The switch was also intended to establish whether this technique was suitable for driving the main store. Two drive switches each using a 16 input - 8 output load-sharing switch and 8 rows of 8 suppressed cores was proposed for X and Y selection. The additional drive power required by the larger store would be provided by the increased input power to the load-sharing switch. The other circuits required to make the register store an operational unit, the address decoding circuits, inhibit drivers, and sense amplifiers and strobe

generator were also developed but are not discussed.

(2) A 32-OUTPUT SUPPRESSED SWITCH

The general configuration of the driving system is shown in Fig. 101. The 8 load-sharing diriver are emitter coupled blocking oscillators similar to those described earlier (Fig. 41). Each is designed to deliver a 250 mA 1.75 μsec pulse to the load-sharing switch. The 2N601 has a 30V rating but the maximum collector voltage which can be applied is limited to slightly more than half this figure due to the voltages coupled through the switch to the inactive drivers. The R-C network in the collector circuit provides a short term voltage overdrive to compensate for the inductance of the switch and load during the rise of the drive currents. Some difficulty was experienced in finding a suitable transistor for the suppression circuit due to the voltage generated in the suppression winding. The OC140, selected for a Vcer>50v was chosen subject to a better transistor being found. A gold-bonded diode, 0A5, was used for the diodes in the suppression circuit to keep the resistance as low as possible.

In a circuit of this type, the current delivered by the drivers is limited only by the impedance reflected through the transformers. A circuit failure, incorrect timing or an accidental short circuit can result in the destruction of the driving transistors. To prevent this happening the - 16$\frac{1}{2}$V supply was delivered by a special regulator which monitored the current drawn by the switch and turned off if this was excessive. The circuit is shown in Fig. 102. T_1 and T_2 form a binary in which both transistors are normally off. T_3, T_4, and T_5 are a conventional regulator. If the pulse current drawn by the switch exceeds a value set by R_1, the voltage induced in the secondary of

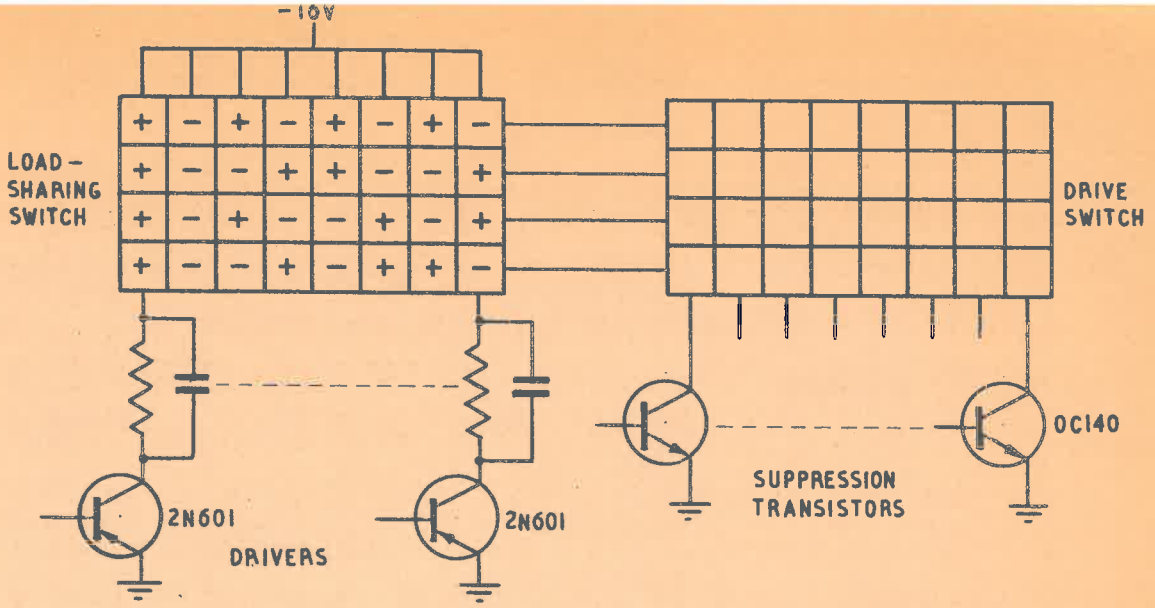


FIG. 101. BASIC CONFIGURATION OF DRIVE SYSTEM

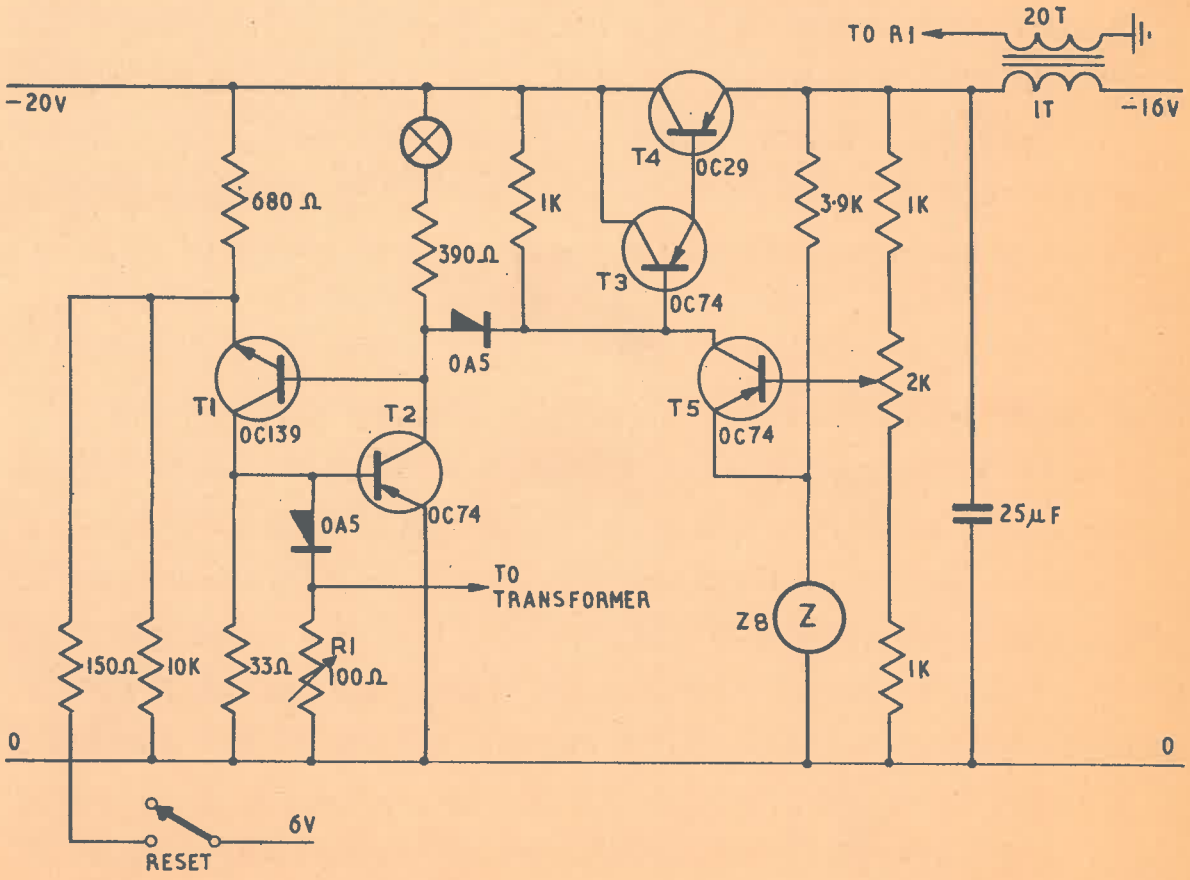


FIG. 102. PROTECTED POWER SUPPLY

the transformer is sufficient to trigger the binary. T_2 then clamps the output of the comparitor to O V via D_1, and the output falls to O V. The protection provided is such that a short circuit could be placed across the output of the drive switch or the load-sharing switch without destroying the drive transistors or the regulator.

(3) SWITCH DESIGN

The core used in both switches was F X 1396, 8 mm o.d., 6 mm i.d., & 2 mm high. The design data for this core is shown in Fig. 103. For a switching time of 2 μsec., the core requires a switching m.m.f. of 2.5 AT and generates 0.42 volts/turn assuming a rectangular output waveform. Assuming a value of 0.4 volts/turn will therefore allow for a sufficient tolerance on core properties without fully switching the core. Fig. 104 is the approximate equivalent current of the driving system. This neglects inductive effects and only applies during "steady state" conditions i.e. during the pulse.

The lead-sharing switch was chosen to have a turns ratio of 1:1 for ease of wiring. Since the total input current of the 4 drivers was ≈1A, the output current from the switch was chosen to be 1A. Allowing for a 4 V drop in the series resistors in the drivers, 12 V are applied to the input of the load-sharing switch.

Assuming $R_i = 0$, $n_1 = n_2 = 30T$

The resulting d.c. resistance of the input windings is 0.3 Ω .

∴ the effective source resistance $R_1 = 0.3 \times 4 \times \frac{1}{4} = 0.3$ Ω .

The output winding uses 2 wires in parallel

∴ $R_g = 0.15$ Ω .

The magnetising current of the load-sharing switch cores is

$$I_{mag.} = \frac{2.5}{30} \text{ A} = 80 \text{ mA.}$$

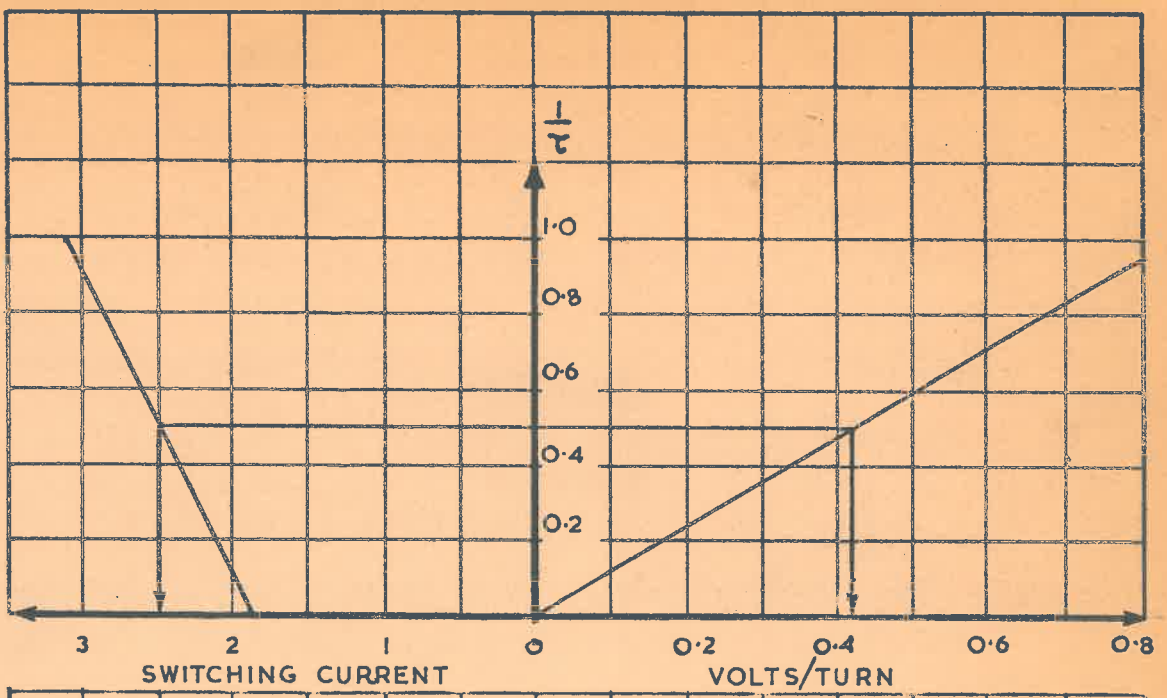
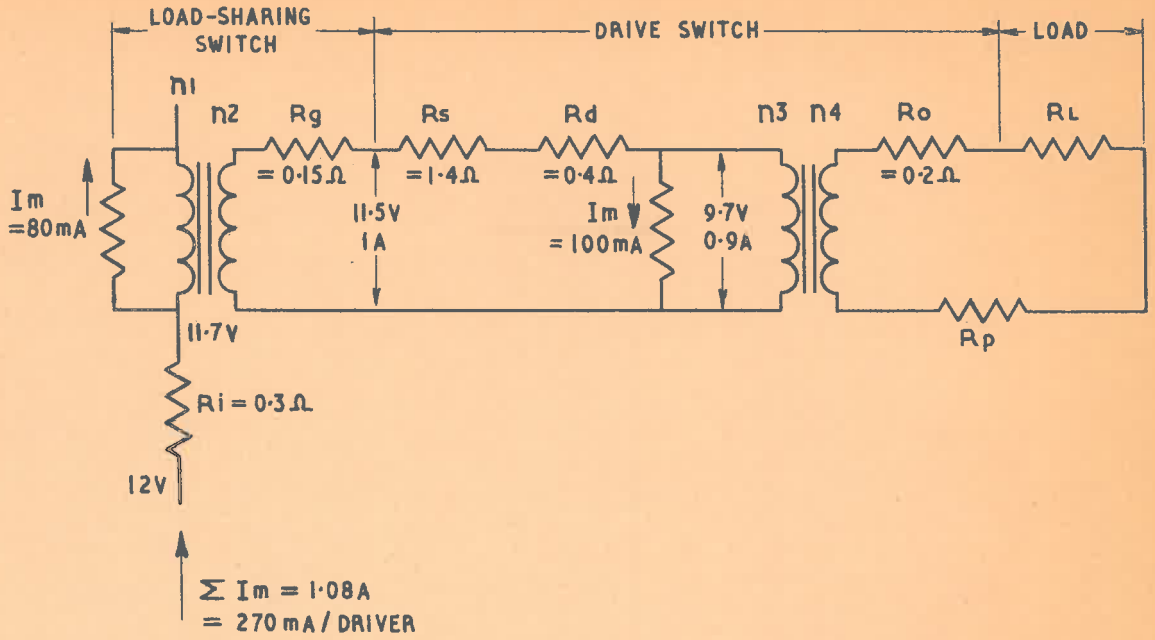


FIG. 103. DESIGN DATA FOR FX1396



Ri = EQUIVALENT SOURCE IMPEDANCE OF DRIVERS.

Rg = OUTPUT RESISTANCE OF THE LOAD SHARING SWITCH.

Rs = REFLECTED RESISTANCE OF THE SUPPRESSION CIRCUITS OF 7 NON SELECTED CORES.

Rd = D.C. RESISTANCE OF THE DRIVE WINDINGS OF 8 CORES.

Ro = OUTPUT RESISTANCE OF DRIVE SWITCH.

RL = RESISTANCE IN SERIES WITH THE DRIVE LINE.

Rp = RESISTANCE OF THE DRIVE LINE.

FIG. 104. EQUIVALENT CIRCUIT OF DRIVE SYSTEM

The output of the load-sharing switch is 11.5V, 1A.

Assuming $R_s = 1\Omega$ and $R_d = 0.5\Omega$, 10 V is applied to the selected switch core.

$\therefore N_3 = 25$ T.

A suppression winding of 120T + 120T will then generate the maximum safe voltage of 48 V on the suppression transistors.

The resistance across the suppression winding is 5Ω (1Vm, 200 mA.).

$\therefore R_s = 7 \times 5 \times (\frac{25}{120})^2 = 1.4\Omega$

and $R_d = 0.4\Omega$

The original estimate of 1.5Ω is therefore low but leaving $N_3 = 25T$ is on the conservative side.

$\therefore$ I'mag. $= \frac{2.5}{25}$ A $= 100$ mA.

The input to the switch core is therefore 9.7V, 0.9A.

For 400 mA output current.

$n_4 = 57$ T

and $R_L = 56\Omega$

For 1V across the suppression winding, the spurious current from the 7 non-selected outputs is

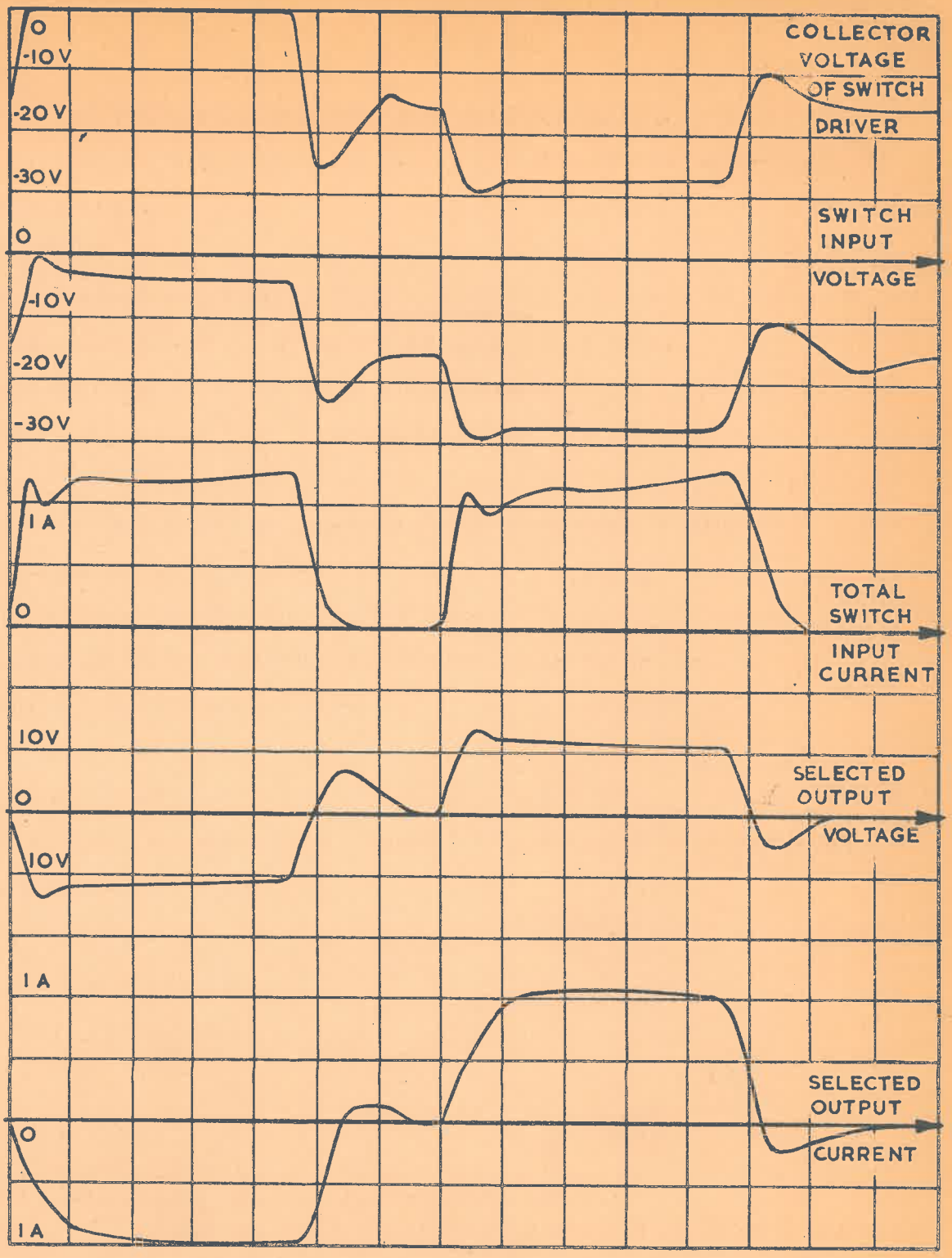
$$1 \times \frac{57}{120} \times \frac{1}{56} \text{ A} = 9 \text{ mA}$$

The switch efficiency is

$$\frac{(0.4)^2 \times 56}{12 \times 1.08} \approx 70\%$$

(4) PERFORMANCE OF SUPPRESSED SWITCH

The significant voltage and current waveforms through the drive system are shown in Figs. 105 and 106. These are in fair agreement with the calculated values. To compensate for the inductance of the suppressed switch and the load during the rise of the drive currents, a series R-C network of 5Ω and 0.02 mfd. was placed across each



0·5 μ SEC/cm

FIG.105. WAVEFORMS FOR LOAD - SHARING SWITCH

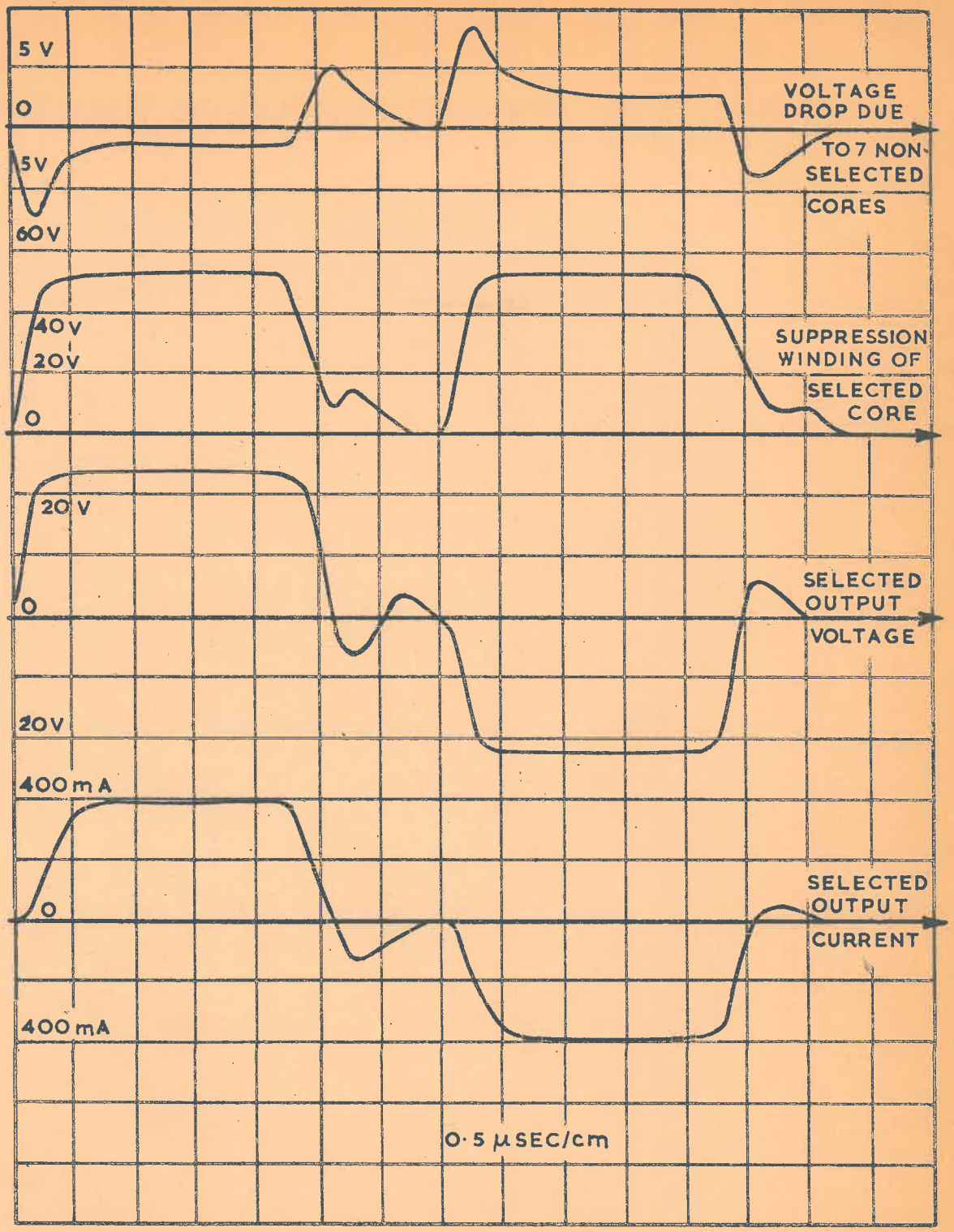
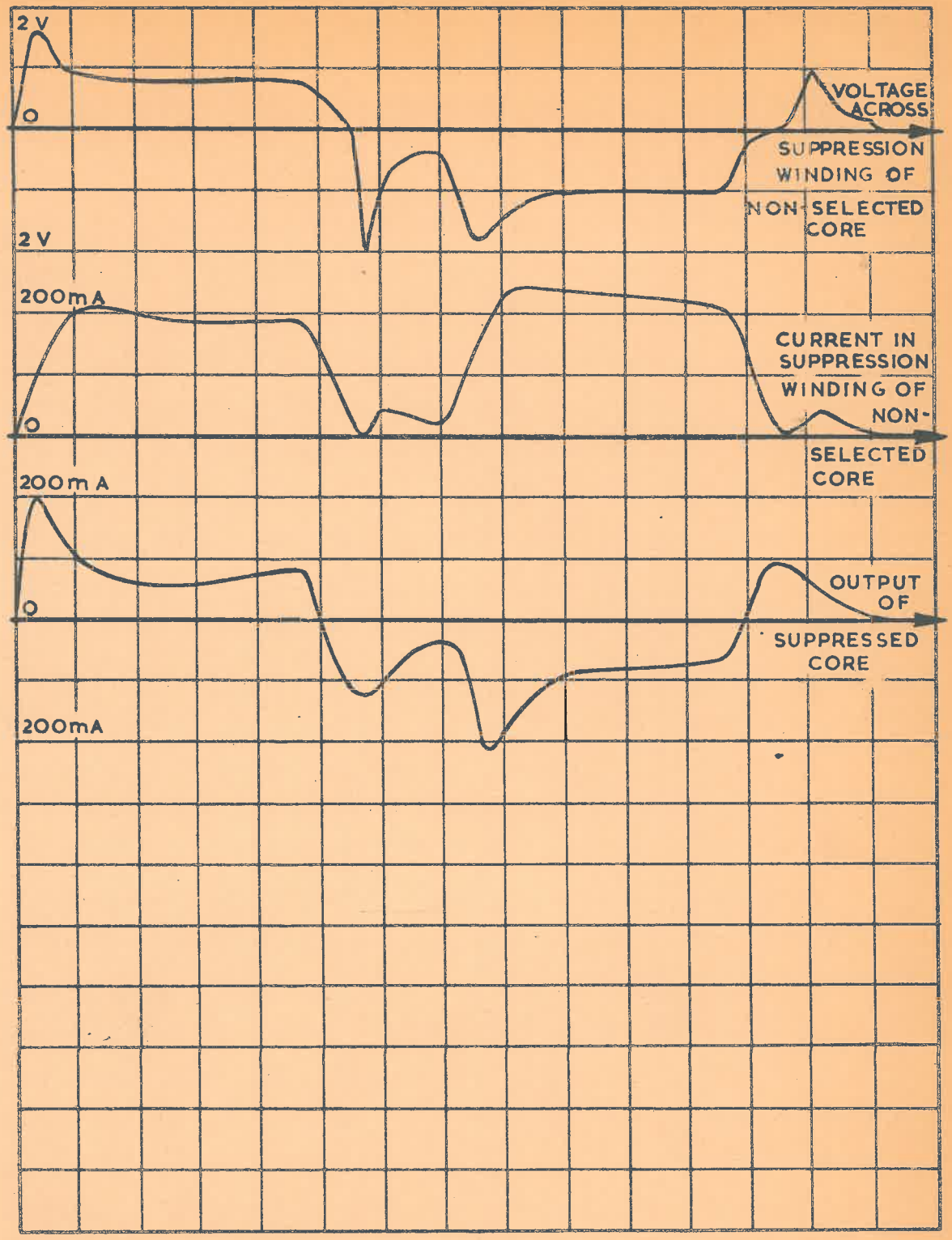


FIG. 106(a) WAVEFORMS FOR SUPPRESSED SWITCH



0·5 μSEC/cm

FIG. 106.(b) WAVEFORMS FOR SUPPRESSED SWITCH

output of the load-sharing switch. This gave the desired improvement in rise time but resulted in an increased fall time and accentuated the overshoot on the trailing edge of the drive currents. Due partly to flux leakage, between the drive and suppression windings and partly to the forward transient of the 0A5, the non-selected output showed a considerable initial peak. Since this occurs mainly during the rise of the drive currents, there is little danger of destroying the information in half-selected cores and no trouble of this nature was experienced. The outputs from the cores in the non-selected rows were trivial. The switch drivers were well matched and any unbalance between drivers had to exceed thresholds in both the load-sharing switch and the drive switch to produce a spurious output to the store. The selected outputs showed a variation of < 15 mA about the nominal 400 mA.

The switch performance was, in general, satisfactory in this application, although the greater load of the main store would have presented additional difficulties particularly with the rise time of the resulting output current. Investigation of this type of switch was dropped when better transistors became available. These favoured current driven switches for which this technique is not suited. In any case a better switch performance could have been obtained with the same hardware by using an arrangement such as that shown in Fig. 107 in place of the suppressed cores. The output of the load-sharing switch is applied to the row of cores, the required 1 of 8 outputs being selected by turning on the appropriate steering transistor. As with the suppressed switch each of the 8 steering transistors could be common to a column of the switch since the other rows ideally

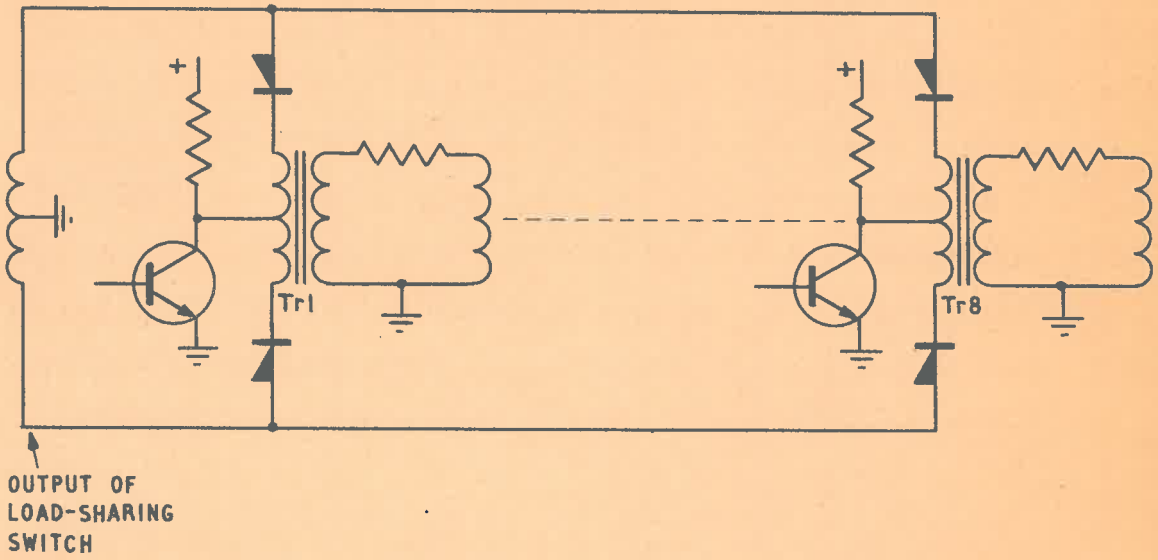


FIG. 107 AN ALTERNATIVE TO THE SUPPRESSED SWITCH

receive no drive from the load-sharing switch. If a 1:5 ratio is used for the load-sharing switch the ratings on the drives and transistors are almost identical and one less winding is required on the switch core. A higher switch efficiency and a better output rise time could also be expected since the series impedance of the non-selected cores has been removed. The suppressed switch therefore represents an interesting development which in this application did not have any advantages over more conventional techniques.

APPENDIX 3

A SURVEY OF HIGH SPEED

RANDOM ACCESS STORAGE

TECHNIQUES

(1) INTRODUCTION

The provision of adequate storage is a fundamental requirement of the modern high speed digital computer and is often a limiting factor on the performance of the system. The storage involved can generally be classified into three types, temporary storage of intermediate results or control information, working store for data and program and a backing store of large capacity for bulk data and 'library' information. Ideally all these facilities would be available in a single level high speed store of very large capacity but the restrictions imposed by cost and technology have forced the development of a number of different types, each designed for a specific section of the field.

The storage of large quantities of information can only be achieved economically by means of electro-mechanical devices such as magnetic tapes, drums and discs. These are available in capacities up to 100 M. bits with an access time ranging from msecs. to 10's of seconds due to the sequential access required. High speed random access storage of up to 10^6 bits with an access time of 0.5-2 μsec. is generally achieved with ferrite cores and associated devices. Thin films, tunnel diodes and special cores have been employed for storage units an order of 10 faster but to date the capacity has been limited to approximately 10^3 bits. Specialised forms of storage for information which is essentially permanent or semi-permanent in nature have also been developed and can provide random access of a fraction of a microsecond to stores with capacities in excess of 10^5 bits.

The following discussion is restricted to those devices providing random access storage. This also is a natural dividing line for other reasons. The majority of random access

stores use a discrete storage element for each bit stored, e.g., a core, a tunnel diode or a spot of film, and interrogate destructively, requiring a two phase read-write cycle of operation. The slower large capacity stores use a technique of surface recording on a magnetic layer with non-destructive sensing of the stored information.

(2) CORE STORAGE

Storage systems based on magnetic cores were first announced over 10 years ago (C1, C2) and due to their high speed and excellent reliability quickly became the preferred form of high speed random access storage. The core is normally prepared from a special ferrite with a square hysteresis loop and is typically a toroid of 30-80 thou. outside diameter. Binary information can be stored by setting the core to saturation in either a clockwise or anti-clockwise direction around the central aperture. The required magnetising force around the core is applied by currents in wires passing through the central aperture. The cores are normally assembled as a 2-dimensional array or plane with from 2 to 6 wires passing through each core. A number of planes are then interconnected to form a store of the required capacity. These stores can be operated in both a word-organised or linear selection mode (C31) and a bit-organised or coincident current mode (E2). Both organisations have their respective merits and both are widely used. The salient features of the two types are briefly discussed below.

(2.1) THE COINCIDENT CURRENT STORE

The hysteresis loop of a square loop core is shown in Fig. 108. In the absence of an applied field, the core will be in either of the two remanent states P or N defined as the '1' and '0'

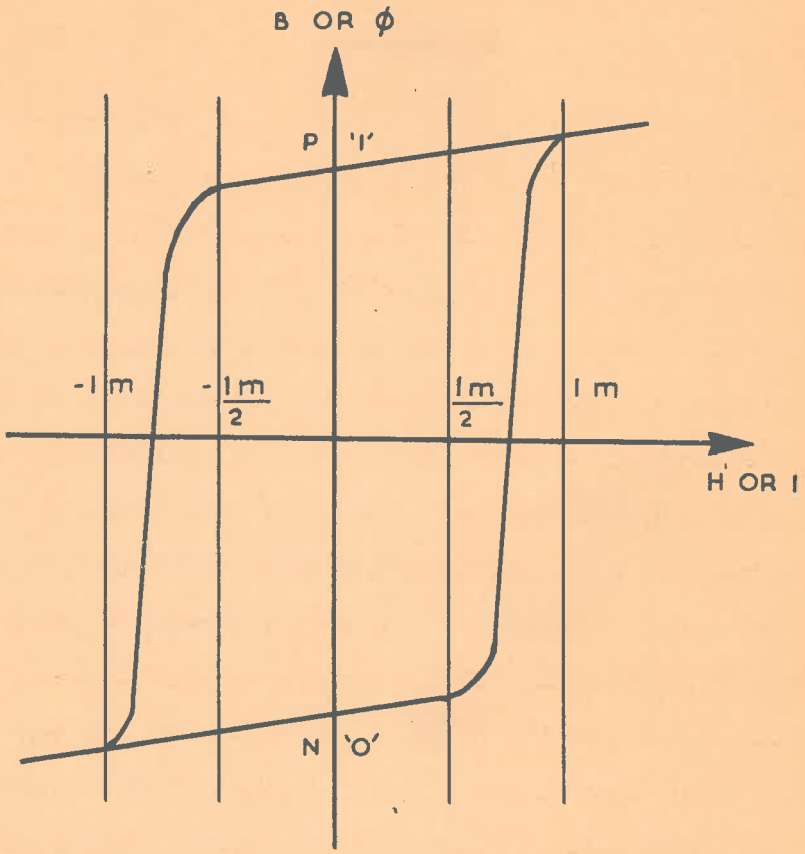
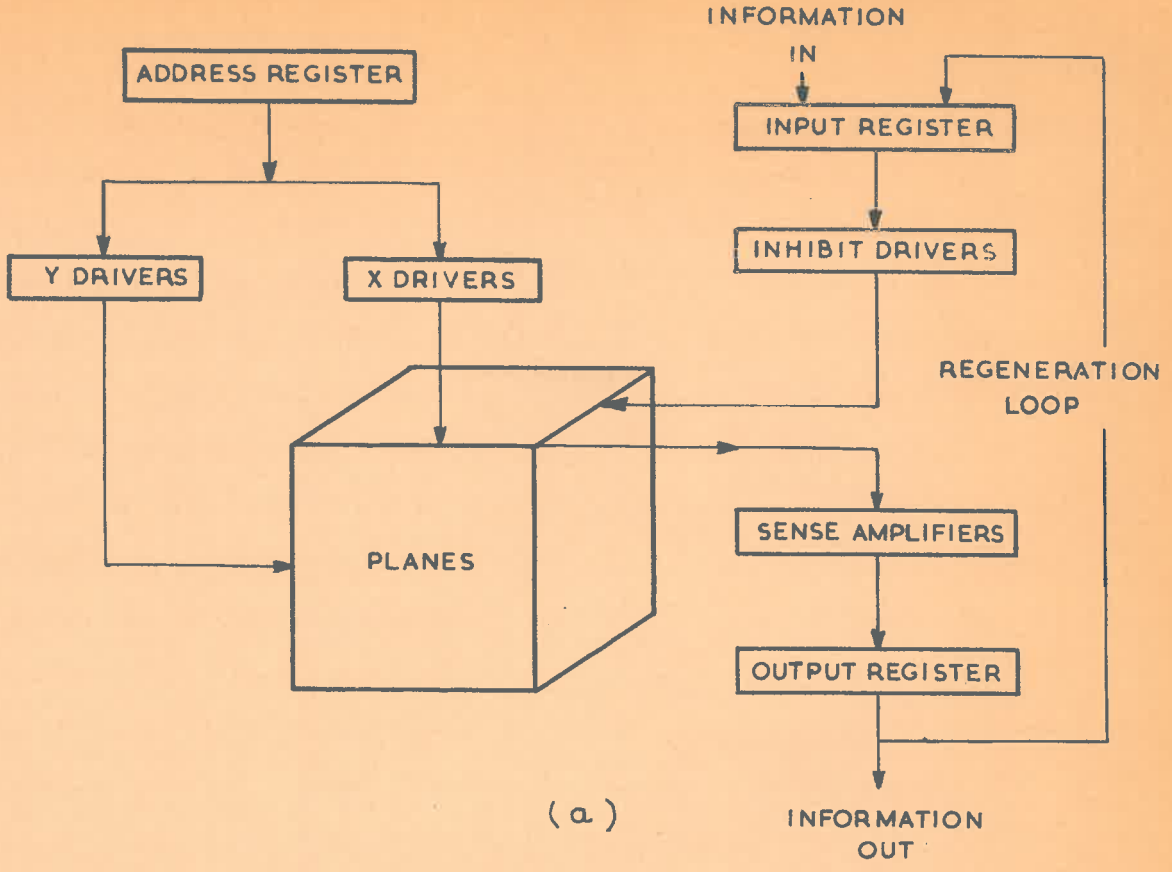
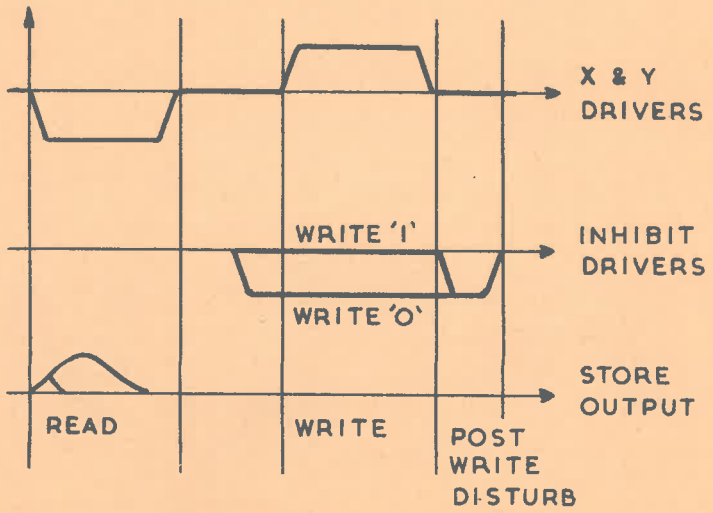


FIG.108. HYSTERESIS LOOP OF A STORAGE CORE

states respectively. As can be seen from the figure, there exists a current I_m such that this current will, if applied in the right direction, cause the core to change state, but due to the rectangular hysteresis loop a current of $\frac{1}{2} I_m$ will leave the core unchanged. This property is the basis of the coincident current selection principle. When wired into an array, a core is linked by four sets of wires. One set links all cores along each X co-ordinate, another links all cores along each Y co-ordinate and the other two, the sense wire and the inhibit wire link all cores in a plane. A memory is normally a three dimensional stack operated in a parallel mode. If a word has w digits, W planes are used and a word is stored in the Z direction, occupying the same core position in each plane. The corresponding X and Y windings of each plane are connected in series so that each plane receives the same drive current. The memory can then hold as many words as there are cores in a plane.

The block diagram and timing for a store using coincident current selection are shown in Fig. 109. During the read phase, currents of $-\frac{1}{2} I_m$ are applied to the appropriate X and Y lines and the core on the intersection of these lines is set to the '0' state. No other core can change state since the drive is less than the switching threshold. If a selected core had been in the '1' state, the resulting flux change will induce a voltage of 50-100 mV. in the sense wire. The flux change due to a '0' is much smaller, and induces a smaller voltage 5-10 mV. of shorter duration in the sense wire. A word will therefore appear in parallel on the W sense wires. For the write phase, currents of $+\frac{1}{2} I_m$ are sent down the X and Y lines. This however, would set all cores to the '1' state. If a '0' is to be written into a plane,





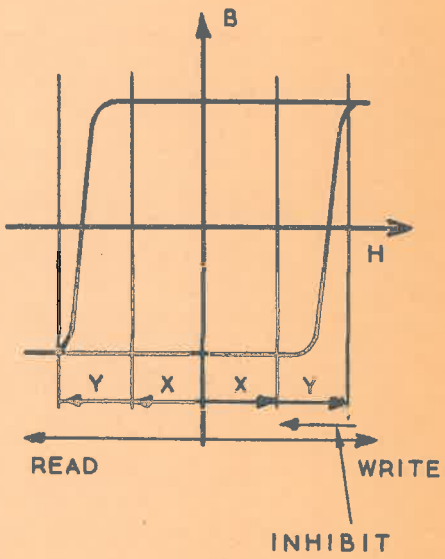


FIG. 109. BLOCK DIAGRAM AND TIMING FOR A STORE WITH COINCIDENT CURRENT SELECTION

the inhibit winding is energised with a current of $-\frac{1}{2} I_m$. The selected core then receives a nett current of $+\frac{1}{2} I_m$ and will remain in the '0' state to which it was set during the read phase. Since reading is destructive, if it is desired to retain the information in the core, it has to be restored during the write period. When operated in this manner, the cores perform both storage and switching functions, since the well defined switching threshold of the material allows part of the selection to be performed within the array itself.

(2.2) THE LINEAR SELECTION STORE

In the C.C.S., the number of 2-D matrices equals the number of bits/word and the number of cores/matrix equals the number of words in the store. In the L.S.S., the cores are arranged as a single 2-D matrix as shown in Fig. 110. The cores in a column form a word so there are as many words as columns and the number of rows is equal to the number of bits/word. The block diagram and timing for a L.S.S. are shown in Fig. 111. To read, a current of any magnitude $> I_m$ is sent through the relevant word line to set all cores on that line to the '0' state. Those cores which change state induce a voltage in the respective sense wires to indicate that a '1' had been stored. A '0' output consists of a small disturb voltage. Writing is achieved by a coincident current technique. A current pulse of $+Im_2$ is applied to the word line, and if a '1' is to be written, a current of $+Im_2$ is also sent down the relevant digit line. These currents add to set the core to the '1' state. If a '0' is to be written no digit current is required and the core is left in the '0' state.

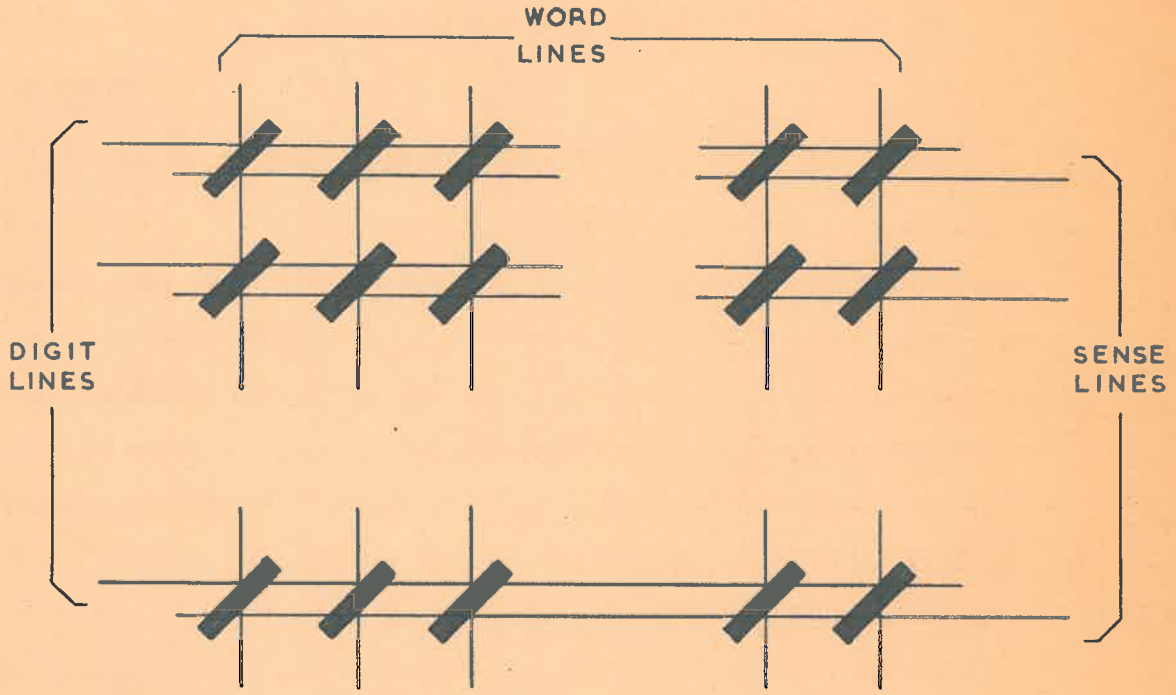
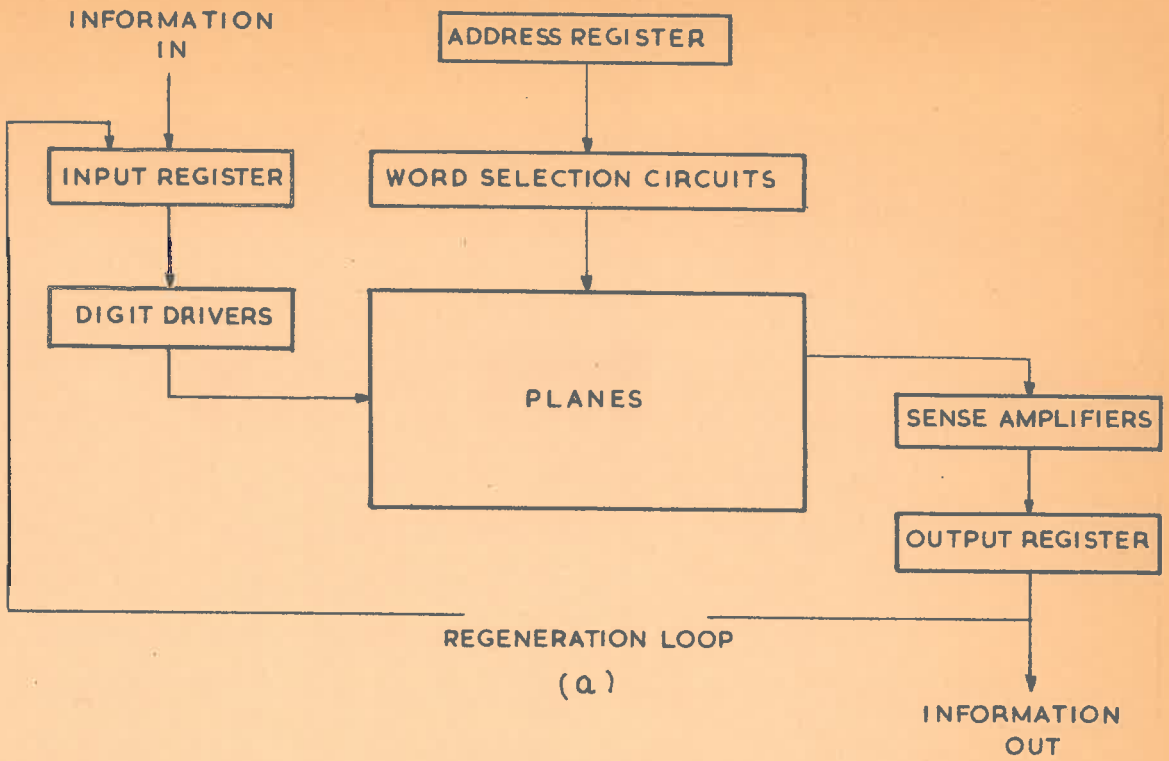


FIG.110. PLANE WIRING FOR LINEAR SELECTION STORE



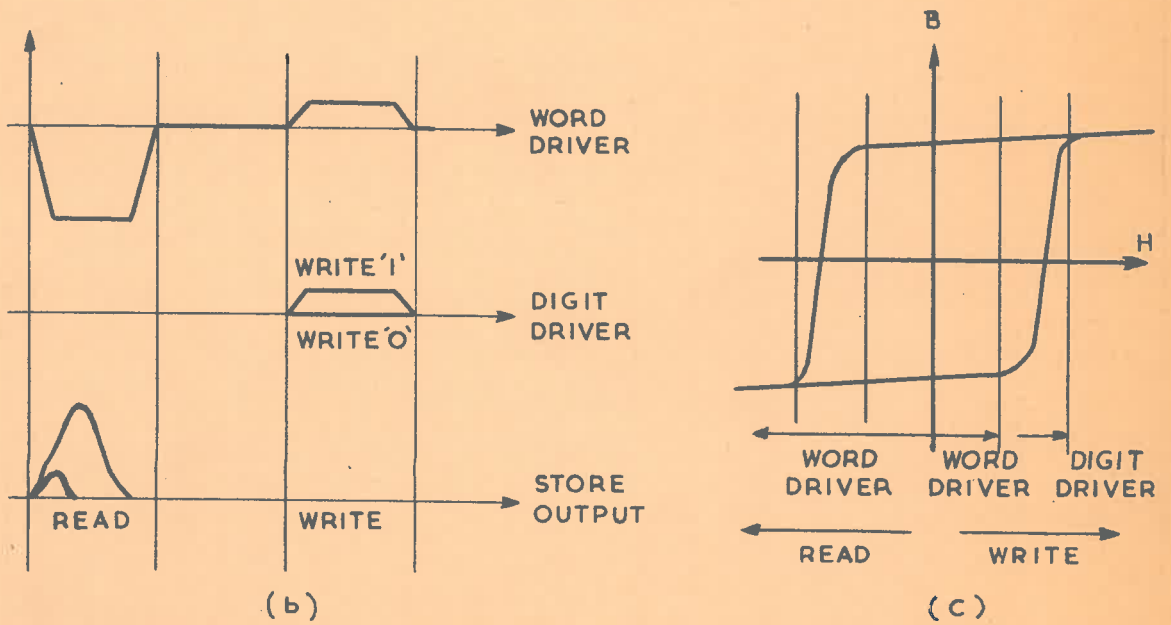


FIG. III. BLOCK DIAGRAM AND TIMING FOR A LINEAR SELECTION STORE.

(2.3) A COMPARISON OF THE TWO STORE ORGANISATIONS

The major advantage of the C.C.S. is the efficient usage of driving hardware. Only 4n drivers are required to select 1 of n^2 words or between $4\sqrt{n}$ and $8\sqrt{n}$ if some form of drive matrix is used. This is to be compared with 4n for the L.S.S. even when employing a drive matrix which is essential from cost considerations. A number of factors however make this ratio less unfavourable. The load presented by the store to the drivers is much higher for the C.C.S. due to the greater number of cores on each drive line and a greater accuracy of current definition is inherent in the method of selection. The C.C.S. typically has a drive tolerance of $\pm$ 10% as against $\pm$ 20% for the L.S.S. These figures however must also be related to the temperature sensitivity of the material used. The majority of materials suitable for C.C.S. have a low Curie temperature (150-250°C) and consequently a temperature coefficient on drive currents of approximately -0.5%/$^{\circ}$C under normal operating conditions. Operation over a reasonable temperature range (20°C) will reduce the drive tolerance below the above figure unless some form of temperature compensation is provided (C18, C20). Alternatively the recently developed wide range cores (C24) could be employed, but those announced to date are more expensive and require approximately twice the drive for an equivalent switching speed. The L.S.S. is inherently more tolerant and can work over a 40-50°C range without compensation. In addition the less stringent requirements on material for a L.S.S. allow the use of a different ferrite with lower drive currents and a less critical drive waveform. The need for unequal read and write currents is not normally a complication since the magnetic (A1, C3) or diode (C20, C37) switches employed can in general be set independently for the two currents. The variation of

load with stored information can be inconvenient with some drive systems employing magnetic switches. This can be overcome by using 2 cores/bit (C33, C35, C38) and in some cases flux limited partial switching (D1, C35). For all but very small stores the C.C.S. is cheaper to drive, the cost difference increasing rapidly with store size but the drive circuits required are more critical in operation.

The C.C.S. also requires more complex sense circuits. The flux changes in half-selected cores during read couple a signal from the drive wires to the sense wire which tends to mask the signal from the selected core. A first order cancellation can be achieved by wiring the sense wire so that equal numbers of cores produce positive and negative coupling from each drive wire (C26). The degree of cancellation is limited however since the noise voltages are dependent on both the state of the core and the history of pulses it has received (A4, B5, B6). This wiring method also produces positive and negative signals for a '1' output.

The most widely used technique to improve discrimination is to time strobe the output. The noise voltages are generated during the rise time of the drive currents, so a strobe commencing at approximately the peaking time of a '1' signal will sample the output when the discrimination is much higher and reliable sensing is easily achieved. This favours a fast rise of the drive currents, with a resulting increase in drive voltages, so a compromise must be reached. A rise time of approximately half the core peaking time is typical. Other techniques commonly employed are staggered X and Y drives (C14, C22) and a post-write- disturb pulse applied to the inhibit winding (A4, C26). The latter improves cancellation by optimising minor loop behaviour but is eliminated if possible since noise coupled

to the sense amplifier by pulses on the inhibit wire can saturate the read amplifier and cause recovery delays. Normally the number of cores on a sense winding is limited to 64 x 64 = 4096 and discrimination by strobing is satisfactory if care is taken with core operating conditions. Larger planes use multiple sense windings and amplifiers and combine the outputs after amplification and gating.

The L.S.S. is subject to much the same sources of noise but at reduced amplitude. Only the selected word is driven during read and ideally the outputs are those of a single '1' or '0'. In practice spurious outputs from the drive switch, especially if magnetic, and crosstalk between wires can add to the '0' signal. Due to the wiring method there is no inherent noise cancellation, but amplitude discrimination is normally adequate. This allows a simpler sense amplifier than that necessary for the C.C.S. The noise coupled from the digit winding can also be troublesome but can be approximately cancelled or gated out of the amplifier.

The L.S.S. is inherently faster than the C.C.S. which is subject to an inherent speed limitation due to the selection principle. The switching behaviour of a core is described by the relationship (B3):

$$T_s \ (H_m - H_o) = C$$

where T_s = switching time

Hm = applied field

$H_o = H_c$

C = const. (0.5 - 1.0 Oe - μsec.)

Since H_m cannot exceed 2 H_c for the C.C.S. and is in general in the

range 1.5 - 1.7 H_c, then $T_s = \frac{K}{H_c}$. Consequently fast switching requires high H_c which emphasises the need for smaller cores if the drive currents are to be kept to a reasonable value. The standard core size has fallen from 80 thou. to 50 thou. and 30 thou., with even smaller cores indicated in the near future. This is due largely to improvements in the technology of manufacture and assembly and the smaller cores have allowed a more favourable speed-drive ratio in recent stores. Smaller cores also permit a smaller array and reduce drive voltages and propagation delays. The more favourable surface to volume ratio of small cores gives better thermal characteristics and self heating at high switching rates, particularly objectionable with the C.C.S., is less troublesome. The cycle time of C.C.S. has been reduced to approximately 2 μsec. (C22) with a further reduction to 1 μsec. possible with smaller cores and/or increased drive. The L.S.S. by removing the basic selection task from the storage cores allows a much greater design flexibility and many variants of the basic system have been developed (C32, C33, C35, C36, C38). Special cores have been developed for use with the L.S.S. which operate on a partially switched loop (B9, C35) and have a much lower switching time for a given drive current. A typical 50 thou. C.C.S. core requires 500 mA full drive for a switching time of 0.8-1.0 μsec. or approximately 0.5 μsec. for the same drive with a 30 thou. core. A typical 30 thou. L.S.S. core will switch in 0.2 μsec. with a read current of 400 mA, a write current of 200 mA and a digit current of 100 mA. The simpler plane wiring of the L.S.S. would allow a smaller core to be employed. The cycle time of the L.S.S. has been reduced to 1.5 μsec. for large stores (C40) and 0.5 - 0.75 μsec for smaller stores (C35, C38). This could probably be reduced to less than $\frac{1}{4}$ μsec. with further development.

Due to the lower cost of the C.C.S. this has been more widely used especially for large stores where the economic considerations in

most cases are the dominant factor in the choice of configuration. The L.S.S. has a considerable speed advantage to offset the increase in cost and in some cases has a lower cost/bit/sec. than the C.C.S. In applications where speed is essential the L.S.S. can well be employed despite the cost and this type of store could be expected to find increasing use in the next few years as store speed at the moment is trailing logic speed. For smaller stores both the cost and the cost differential between the two systems are reduced and the L.S.S. has been mostly used for small very high speed stores or in applications where the more tolerant operation is required.

3. The Ferrite Plate.

The ferrite plate store (D1, D5) is a refinement of the conventional core store in which the storage elements are prepared as holes in a plate of square loop material. Each hole can act independently as a core due to the threshold inherent in square loop material. The configuration most widely known has an array of 16 x 16 holes each 25 thou. diameter and spaced on 50 thou. centres. The plate is 0.83" square and 20 thou. thick and has a sense-inhibit winding deposited directly on the plate by vacuum evaporation techniques. These plates can be operated as either a L.S.S. (D1, D6) or C.C.S. (D1, D3). Due to the linkage of the printed sense winding, it is necessary to use either 2 apertures/bit (D1, D2) or to connect the sense windings of groups of plates as a self cancelling unit (D3, D4) if used in a C.C.S. The production and assembly of a store are greatly simplified and drive currents can be reduced since a plate with holes is easier to handle than small cores. Despite these advantages, the ferrite plate store has not been widely used. Apparently the production yields were too low to allow the potentially low cost to be realised.

4. Multi-Apertured Devices.

Multi-apertured cores have also been described (E1, E2, E4, E7) which rely on device geometry rather than the existence of a well defined threshold in the material, consequently these elements allow a much wider drive tolerance and a greater temperature range. Large overdrives and very fast switching are possible for operation as either a L.S.S. (E2, E4) or a C.C.S. (E1, E7). These devices suffer from more difficult fabrication and more complex plane wiring. Drive currents tend to be excessive by current standards due to the difficulty of fabricating small elements, although a switching time of 100 nsec. for 500 mA drive has been reported. These elements have also been prepared from etched metallic sheet with printed drive windings (E6) and by vacuum deposition (F26). In these forms the principle is much more attractive and very fast switching (10's of nsecs.) has been achieved for reasonable drive currents.

5. The Twistor.

A storage element which employs an open helical flux path around a piece of wire was developed some five years ago (F1). It was called the "twistor" since the helical flux path was originally obtained by twisting a strain sensitive magnetic wire or a wire clad with a magnetic coating. This has also been obtained by wrapping a metallic tape around a conductor (F2, F4) and by special plating techniques (F3). All methods of preparation produce very square hysteresis loops. The driving circuits can be coupled to the helical path by currents in a solenoid around the wire and/or a current down the wire itself.
A storage element is formed from a short length (0.1") of twistor wire and the centre conductor used as the sense wire. Operation as both a L.S.S. (F1, F2, F3) and C.C.S. (F1, F3) is possible but the former is preferred due to easier fabrication, cleaner signals and increased

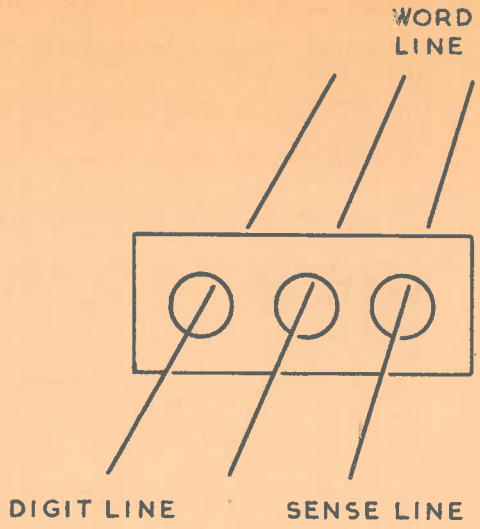


FIG.112. A MULTI-APERTURED CORE FOR LINEAR SELECTION

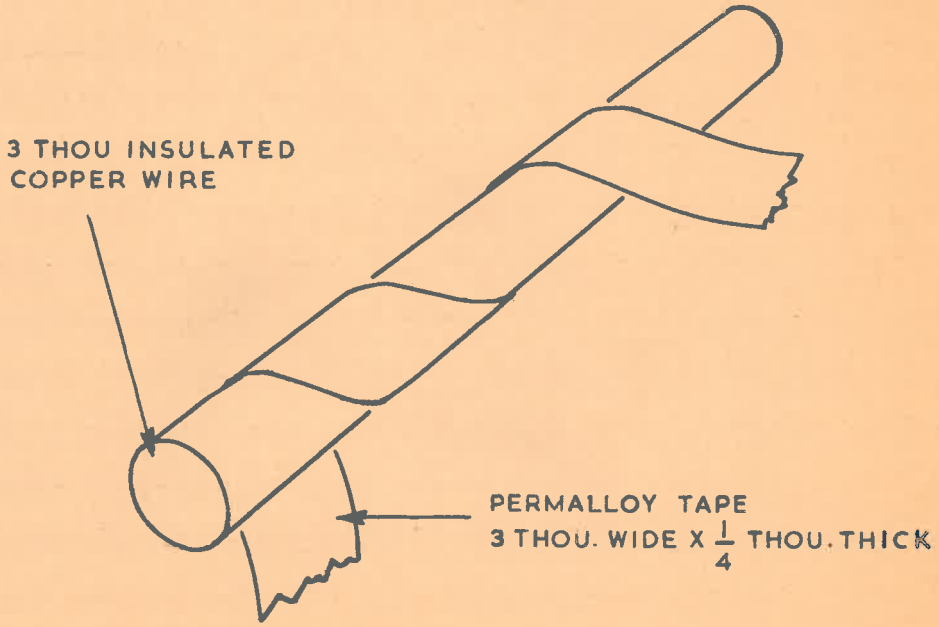


FIG. 113. "BARBER POLE" TWISTOR

margins. Operating speeds are comparable with those of a core store. The twistor has a wide temperature range, is very cheap to fabricate and reasonably cheap to drive despite the preference for L.S.S. since simple magnetic switches can be employed. It has found limited application in the past and has probably been superseded by improved and cheaper cores.

6. Thin Film Storage.

Thin metallic films were first investigated [G1, G17] in an effort to increase speed and reduce fabrication costs. It was quickly realised however that these elements possessed unique properties which could be exploited for very high speed operation. A typical thin film element is formed by vacuum evaporation [G16] of a non-magnetostrictive Ni-Fe alloy [G7, G22], 81% Ni, 19% Fe, onto a thin glass or metal [G39, G42] substrate. A typical element is 1-2 mm in diameter and 500-2,000 A thick. The required spot size and shape are obtained by evaporation through a mask or by selective etching of a continuous film. During evaporation a uniaxial magnetic anisotropy [G3, G5, G7, G8] is introduced into the film by a magnetic field of approximately 50 Oe acting in the plane of the film. The film acquires an easy axis along which the hysteresis loop is square but displays a linear loop perpendicular to this axis. Magnetisation reversal can occur by domain wall motion, incoherent rotation or uniform rotation, during which the film behaves as a single domain [G3, G5, B4]. The last mode is of particular interest since nanosecond switching has been observed for fields as low as 2 Oe [G4]. The mode of flux reversal is sensitive to both longitudinal and transverse fields, i.e., along or perpendicular to the easy axis, the latter being necessary for uniform rotation. The driving fields are applied by currents in

strip transmission lines placed adjacent to the substrate on which the films were deposited. Small arrays have been reported (G26, G31) in which the drive lines and insulating material were also evaporated but this has not yet been achieved in a store of significant size.

A variety of configurations are possible (G24, G31, G37, G38) similar to the C.C.S. or L.S.S. and with destructive or non-destructive readout but to date only the perpendicular mode L.S.S. with destructive readout has been extensively exploited with flat films (G18, G20, G30, G31, G38). This is largely due to the tolerance on material parameters which this configuration provides. The notable exception is one employing two films of different parameters to provide non-destructive sensing (G34, G35). This is also the largest film store so far constructed but is rather slow. Films of the required characteristics have also been successfully prepared by plating (G11, G29, G36), sputtering (G12, G13, G14), and chemical deposition (G15) and from material other than that stated above (G11, G36, G39). The work so far reported on ferrite films (G28) indicates that these do not exhibit the very fast rotational mode of reversal observed in metallic films although this has been achieved in toroids under different conditions. Thin film stores have also been fabricated using rectangular elements (G18, G31, G32) and continuous film (G30, G40) and from cylindrical rods with an axial (G27, G36), circumferential (G25, G29, G41) and helical (F3) easy direction. In general these behave in much the same manner as the films described above.

The attractive features of film storage are:-

(a) mass fabrication of elements and drive lines;

(b) high speed due to possibility of reversal by uniform rotation;

(c) a configuration favourable to high speed operation;

  (i) small amount of material minimises drive voltages;

  (ii) strip lines provide low impedance and wide frequency response;

(iii) self heating is negligible due to low energy involved and very high surface: volume ratio.

The present difficulties include:-

(a) preparation of film to close tolerance;

(b) noise coupled from drive to sense line;

(c) expensive driving circuits.

Recent progress in the preparation of more uniform film arrays is encouraging but much work remains to be done. Films prepared by sputtering (G12) and plating (G11) appear to be superior to those prepared by evaporation in this regard. A small percentage of Co (G11, G39) in the alloy also appears to yield better films. The current limits are film arrays of approximately 3" square (10^3 bits) and uniformity sufficient to allow L.S.S. operation with comfortable margins. In view of the expensive driving circuits required, film uniformity sufficient to allow C.C.S. operation would provide a substantial reduction in costs. The very small amount of material used introduces sensing problems due to the very low signal to drive ratio. A typical spot will produce a 1 mV signal when switched in 20 nsec. Great care is necessary to obtain an acceptable signal to noise ratio during read since both occur during the rise of the drive current. Digit noise is also troublesome. Careful choice of geometry and configuration (G24, G25, G30, D31) can reduce these problems but they impose a lower limit to spot size and probably an upper limit to plane size. The limits on cycle time are at present imposed by the associated electronics, i.e., circuit delays in the selection circuits and sense amplifier, recovery of the sense amplifier and possibly duty cycle of the drivers. A cycle time of 0.1-0.2 μsec would appear to be the best that can be achieved with current

techniques (G42). The hardware cost also imposes an economic limit to store size at the moment. It seems likely that film storage will be restricted to small high speed stores in the near future.

7. Cryogenic Storage Elements.

Following the original application of the phenomenon of super-conductivity to computer logic (H 1) considerable effort has been spent on the development of cryogenic storage. The majority of these devices rely on the variation of transition temperature with magnetic field either externally applied or generated by the current flowing in the element itself. Three basic storage elements are under development. The first employs a current flow in a closed loop of super-conducting metal (H2-H6). The loop currents are induced from the drive lines by transformer action, the direction of current flow representing the digit stored. Sensing is achieved by adding a fixed increment to the loop current. If the material is driven to the normal state, a voltage is induced in the sense line, otherwise no output is obtained. The Crowe cell (Fig. 114) has the advantage that drive and sense lines are separated by a super-conducting shield and the noise level is very low. The second type employs the crossed film cryotron (H7, H8) and again stores information as a persistent current but differs in that all driving and sensing operations are achieved logically with the crossed film cryotrons. A simple cell (Fig. 115) requires three cryotrons (H8, H9). This allows a great deal of freedom in store design and configurations have been proposed which allow multiple access, shifting, counting and transfer within store (H8) and addressing by content rather than position (L1-L4).

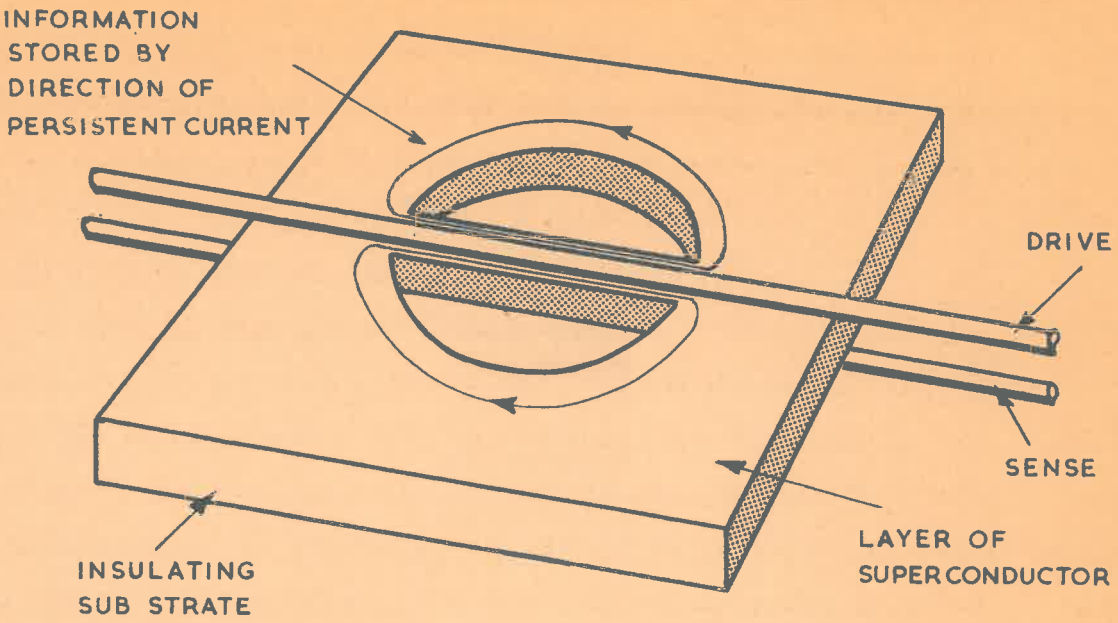


FIG. 114. CROWE CELL

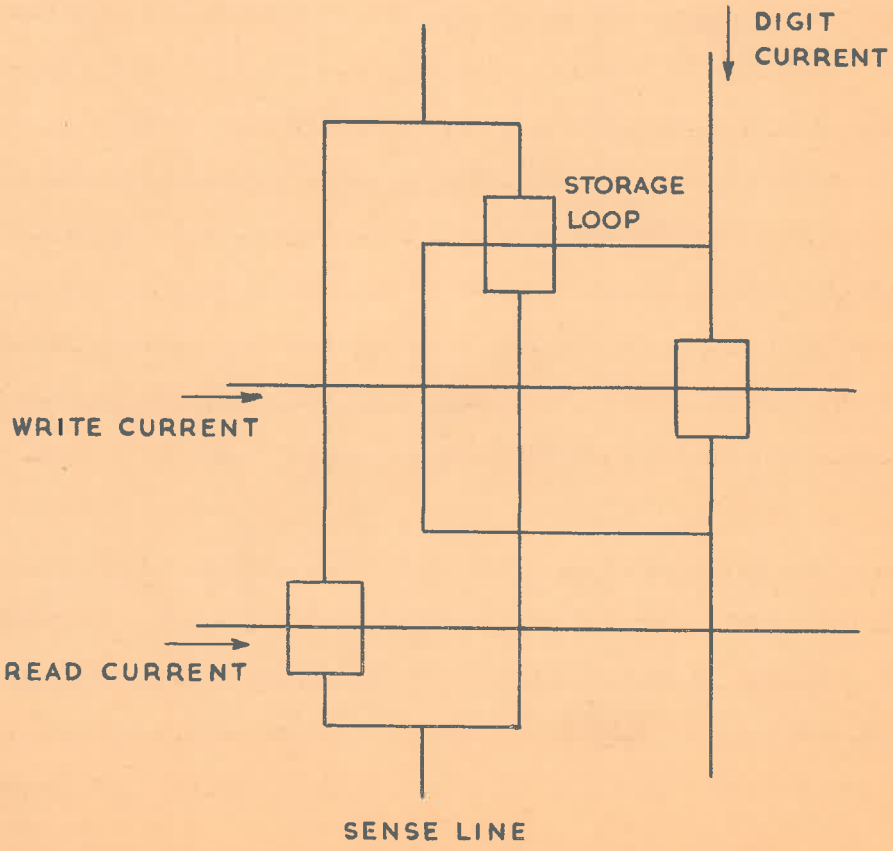


FIG.115. STORAGE CELL USING CROSSED FILM CRYOTRONS

Stores of the above types are capable of very high speed, switching times of 1-10 nsec. having been reported for single elements of each type. They are subject to thermal and circuit time constants which limit minimum cycle time but 10-100 nsecs. appears possible with suitable design. Circuit time constants are likely to increase this figure considerably for large stores. Full use can be made of vacuum evaporated techniques with arrays of storage elements and drive lines fabricated by a multi-stage process (H9) yielding very high density storage (up to 10^7 bits/c.ft.) and large capacity. Tin is most commonly used for the controlled films and lead for the drive and control lines due to the higher transition point of this metal. Element uniformity is better than that of thin ferromagnetic films since less parameters have to be controlled and drive currents are in general lower and less critical.

A third type of storage employs the cryosar, a two terminal semiconductor device utilising impact ionisation in germanium at liquid helium temperatures (H13). When prepared from compensated germanium the cryosar exhibits a negative resistance region similar to the tunnel diode and storage arrays have been successfully tested (H14). Cryosar stores of very high packing density could be fabricated by techniques similar to those currently employed in transistor production.

All the above storage systems are capable of L.S.S. or C.C.S. operation. They suffer from the obvious disadvantage of requiring refrigeration to liquid helium temperatures. A relatively cheap closed cycle refrigerating system has been developed (H16) which has a capacity sufficient for at least 10^5 bits. The advantage of cryogenic

stores, large capacity, high speed and the ability to combine logical and memory functions, could well outweigh the operating difficulties in some applications.

8. Storage Systems allowing Non-destructive Read.

The stores described above employ destructive readout and require operation on a read-write cycle to retain the stored information. An effective method of non-destructive readout (NDRO) would allow a considerable increase in both store and computing speed, since, on the average, read and regenerate operations substantially outnumber write operations. The potential benefit of this facility, however, is dependent on system organisation and a suitable structure can do much to offset the unbalance. A number of NDRO techniques have been reported for cores, including cross field interrogation (J1, J2) impulse sensing (B4, J3, J4), a.c. sensing (J3, J5, J6), bias restoration (J7) and multi-apertured cores (E3, E7, J8). In general these techniques are not very attractive. Drive currents tend to be high, and signal and discrimination are often low. Since interrogation must be word-oriented, and in general the interrogate circuits must be separate from those providing the clear and write functions, the cost of this facility is usually excessive. Consequently, NDRO stores have found very limited application.

NDRO of films has also been reported using paired films (G19, G34) and cross field interrogation (G24, G29, G41). The latter is inherently provided by the perpendicular mode film store but 'break-up' of the majority of films for relatively low angles of rotation

currently prevents the use of this facility. NDRO of cylindrical films is however a practical proposition [G29, G41]. Cryotron stores of the second type described above also inherently provide NDRO but only experimental models have so far been tested.

Another type of NDRO storage has also been extensively developed in recent years. These should more correctly be called "read-only" stores since the information content cannot be changed electrically. Those reported include pre-wired arrays of square loop cores [K1] magnetically biassed cores [K16, K17, L7] and twistors [K2-K5] electro-luminescent arrays [K6], linear coupling arrays employing inductive [K7-K11] and capacitive [K12-K14] coupling and photographic techniques [K15]. This type of store can provide rapid random access storage for permanent or semi-permanent information and in general are much cheaper than the variable stores described above, although intended for a different type of service. These stores are discussed in further detail in Section D of the thesis.

9. Miscellaneous Type of Storage.

Other types of storage have also been developed using tunnel diodes [I1-I7], a diode-capacitor combination [I8, I9] and magneto-strictive delay lines [I10, I11]. Although delay lines do not provide true random access, their access time can be sufficiently low to provide a reasonable approximation. Tunnel diode stores are capable of extremely fast operation but are rather expensive. Their use will probably be limited to small stores (10^4 bits) with a cycle time of 10-100 nsec.

Considerable effort has recently been directed toward the development of the associative store [L1-L7]. This involves a rather different concept of store organisation in which the data is addressed directly by matching all or part of the word with a key rather than indirectly by location. Since cryotrons can provide both the logical and memory functions required, these have been most widely used [L1-L4] although simplified forms using magnetic elements have been reported [L5-L7]. The success of this concept is difficult to predict independently. Present indications are that full exploitation requires the use of cryogenics but if production techniques allow a system of this complexity to be built then it is reasonable to suggest that the whole computer could be cryogenic. This could well initiate a major change in the structure of computers of which associative storage would only be a part.

10. Future Trends.

Ferrite cores have been and still are the most important medium for high speed data. Present stores provide a capacity of up to 10^6 bits with a 2 μsec. cycle using coincident current selection or a 1 μsec. cycle using linear selection. The advances in recent years suggest that faster cores can and will be developed and costs have fallen significantly, although store capacity is still limited by economics rather than techniques. A capacity of 10^7 bits with a cycle time of 2-3 μsec. and 10^4 bits with an 0.1-0.2 μsec. cycle will probably be feasible in the near future.

Further improvements are sought however in speed, capacity and cost. Thin films, both magnetic and cryogenic, are potentially capable of providing all these improvements, but still require considerable development before they are widely accepted. Tunnel diode storage is capable of extremely high speed but the capacity is limited by the high cost. Ferrite plates, twistors and multi-apertured devices have probably been superseded by the advances in cores and films but may well find limited application for a few years.

The read-only stores and the associative store are both intended for specialised applications. The former has already been widely used and should continue to be, but the latter is still being developed. If it can be made at a competitive cost, this form of storage could be used to advantage in many applications.

In a rapidly developing field such as this, it is difficult to predict more than a few years ahead. The last 10 years has seen tremendous progress in data storage and it is unlikely that the rate of development will decrease. The storage techniques 10 years hence could well bear little resemblance to current practice.

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