PERFORMANCE OF PHOTONIC OVERSAMPLED ANALOG-TO-DIGITAL CONVERTERS

by

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Supervisors: Prof. Jesper Munch and Dr. Kerry Corbett.

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Finally I would like to thank my parents for their support throughout this endeavour.

Abstract

In an increasingly digital world, the need for high speed and high fidelity analog-to-digital (A/D) converters is paramount. Performance improvements in electronic A/Ds have not kept pace with demand, hence the need to consider alternative technologies. One such technology is photonics, as it takes advantage of optical sampling, high speed optical switches and low cross-talk interconnects. Optical sampling derives its advantage from the application of ultra low timing jitter (<100fs) mode locked lasers utilised to provide high speed clock pulses.

In this thesis the feasibility and simulated performance of three different types of photonic oversampled A/D converters was investigated. The first, and simplest design is that of oversampled pulse-code-modulation (PCM), where a 2-level photonic comparator is used to sample the analog input at a frequency much greater than the Nyquist frequency. Subsequent low pass filtering produces a digital representation of the input. The other two architectures that were investigated are the first-order sigma-delta and error diffusion, which add one level of error correction to the PCM technique. These two architectures require the functional elements of a subtractor, comparator and delay. The photonic comparator and subtractor functionality was provided by Self-Electro-Optic Effect devices (SEED) based upon multiple quantum well (MQW) p-i-n devices.

To facilitate calculation of the performance of the different architectures and aid in device design, a simulation of SEED operation based upon experimental data was developed. The simulation's accuracy was demonstrated by agreement with the results from experimental S-SEED switching and optical subtraction. To emphasize the utility of the model, the simulation was subsequently used to demonstrate tristability of an S-SEED and critical slowing down in a bistable S-SEED. These effects were experimentally verified.

To provide enhanced comparator contrast ratio and subtractor dynamic range, resonantly enhanced microcavity multiple quantum well (MQW) p-i-n devices were designed and grown by MOCVD. The operation of the subtractor and comparator was experimentally demonstrated and utilising temperature tuning, optimised per-

formance was achieved with devices from the same wafer. Furthermore, the inclusion of gain was shown to improve the subtractor performance to that demanded by the sigma-delta.

The constraints on each architecture imposed by the unipolar nature of the light intensity were derived and the sigma delta architecture was shown to be superior to the error diffusion for a photonic implementation. Using the numerical simulation based upon experimentally derived data, the entire sigma delta architecture was simulated to calculate the expected performance. The signal-to-quantisation-noise ratio (SQNR) was calculated as a function input amplitude and a peak SQNR of 54dB was obtained for an oversampling ratio of 100.

List of Symbols

Throughout this thesis, several symbols will be used repeatedly to represent specific quantities or parameters, the following is a list of these symbols and short descriptions for the readers convenience. This list is not exhaustive but every effort has been made to maintain conformity of symbols used here. Wherever possible standard symbols and notation have been used which appear in most texts.

A/D	...	Analog to Digital Converter
$AlAs$	...	Aluminium Arsenide
$AlGaAs$	...	Aluminium Gallium Arsenide
AR	...	Anti-Reflection
a, L_w	...	Width of quantum well
a_0	...	Bohr radius
α	...	Absorption coefficient
C	...	Capacitance
CR	...	Contrast ratio
c	...	Speed of light in vacuum
Δ	...	Hysteresis width
E_g	...	Bandgap in eV
E_c	...	Minimum conduction band energy
E_v	...	Maximum valence band energy
E_b	...	Exciton binding energy
e	...	Charge of an electron
e_i	...	Error in comparison operation
ϵ_0	...	Permittivity of free space
ϵ_r	...	Relative permittivity
f_B, f_0	...	Input bandwidth
f_d	...	Dither frequency
f_s	...	Sampling frequency
$GaAs$	...	Gallium Arsenide

$GSPS$	...	Giga Samples per Second
G	...	Gain
$GPIB$	...	General Purpose Interface Bus
$\hbar$	...	Planck's constant
η	...	Quantum efficiency
I	...	Current
φ	...	Phase
φ_n	...	Wavefunction of quantum well
k	...	Extinction coefficient
l	...	Geometric pathlength in a laser crystal
λ	...	Wavelength
m^*	...	Effective mass
$MSPS$	...	Mega Samples per Second
$MOCVD$	...	Metal-Organo Chemical Vapour Deposition
MBE	...	Molecular Beam Epitaxy
MQW	...	Multiple Quantum Well
n	...	Refractive index
N	...	Number of quantum wells
n_{3D}	...	Density of states in for a particle in 3 dimensions
n_{2D}	...	Density of states in for a particle in 2 dimensions
NID	...	Non intentionally doped
ND	...	Neutral Density

OSR	...	Oversampling ratio
P	...	Power
$P_{\theta L}$	...	Lower bound of hysteresis
$P_{\theta H}$	...	Upper bound of hysteresis
P_{θ}	...	Midpoint of hysteresis width
PCM	...	Pulse Code Modulation
q_i	...	Output signal of A/D comparator
Q_L	...	Low output of comparator
Q_H	...	High output of comparator
$QCSE$	...	Quantum Confined Stark Effect
R	...	Reflectivity
$REAM$	...	Reflection Electro-Absorption Modulator
S	...	Responsivity
$SFDR$	...	Spur Free Dynamic Range
$SEED$	...	Self-Electro-Optic Effect Device
$S-SEED$	...	Symmetric Self-Electro-Optic Effect Device
$SQNR$	...	Signal to Quantisation Noise Ratio
t	...	Transmission
u_i	...	Input signal to A/D comparator
V_0	...	Applied SEED voltage
x	...	Input signal to A/D

Contents

Chapter 1

Introduction

In nature, physical processes are analogue. They occur continuously in time with a continuous amplitude. In today's information age we predominantly capture and record physical processes and information as digital signals. A digital signal is discrete in time and amplitude and can provide greater noise immunity and improved resolution, flexibility and accuracy for signal processing when compared to analogue techniques. The interface between these two domains is the analog-to-digital converter (A/D). Therefore, A/Ds are a vital element in today's information age.

As communication bandwidth is increased by the introduction of higher performance fibre optic communication systems and faster digital processors, the need for high speed A/Ds grows in proportion. Common applications for A/Ds are digital oscilloscopes, radar, sonar, electronic warfare, medical imaging, telecommunications and consumer electronics[1]. A particularly demanding application relevant to defence is the direct digitisation of a radio frequency (RF) carrier. The ability to digitise directly the RF carrier of communication signals at high resolution is very desirable, as it avoids the use of an intermediate frequency (IF) which degrades the signal-to-noise ratio. An increased signal-to-noise ratio can be translated into an increased communication bandwidth, or in the case of defence intelligence applications, an increased sensitivity. To enable carrier digitisation, high performance analog-to-digital converters are required that operate at a conversion frequency of greater than 500MHz at 16 bits of resolution. However, current state-of-the-art electronic technology is unable to provide sufficient speed at high resolutions, as

performance is limited by transistor switching speed and clock jitter [1]. The maximum sampling rate achievable by current commercially available 8 bit and 16 bit A/Ds is stated as 3 GSPS and 105 MSPS, respectively. However, due to additional quantisation noise and nonlinearities, the effective resolution of these A/Ds is reduced by up to a factor of two when operating at their maximum stated sampling rates.

Due to the slow pace of electronic A/D progress, relative to CMOS digital electronics [1], alternative technologies have been under investigation for many years. Photonics is one such technology, with inherent advantages of high-speed switching, low power consumption, low cross-talk, parallelism and immunity from electromagnetic interference[2]. A photonic A/D also removes the requirement to convert from optical to electronic, and back to optical signals in the high speed digital communications of optical sensing systems. However, the key advantage is optical sampling, which derives its benefit from the use of low noise and low timing jitter (<16fs) [3] mode-locked lasers. Current electronic A/Ds are limited by jitter of 0.5ps[1]. Photonics offers the possibility of extending the performance of state-of-the-art A/Ds, due to low jitter clocks, high speed switches and other advantages as discussed in the next chapter. Furthermore, oversampled A/Ds are well suited to a photonic implementation, which was first proposed by Shoop and Goodman[4], [5], [6], [7], as they require only a 1-bit comparator of modest quality, require low complexity and are easily scalable to high resolutions. The required functional elements in oversampled A/Ds can be supplied by SEEDs, which will also be described in the following chapter and these have also been demonstrated at very high switching speeds.

The work in this thesis is focused on demonstrating an oversampled photonic A/D, and three specific cases are considered, namely PCM, error diffusion and the first-order sigma-delta. The successful implementation of such a device could enable direct digitisation of RF signals and other applications important in the information age where electronics has been unable to provide sufficient A/D performance.

The central issues that need to be addressed to achieve a working photonic A/D are:

1. Selection of an A/D architecture and modification to function with unipo-

lar signals

2. Development of devices to be used in the chosen architecture

3. Simulation of architecture

4. Integration of devices into a working A/D.

Several of the different types of photonic A/D architectures are considered in the following chapter. However, as will be shown, the oversampling technique, first applied to photonic A/Ds by Shoop and Goodman[4], [5], [6],1 [7] holds the greatest promise of achieving high resolution and high speed conversion, even though the work has not been significantly extended since Shoop's original work. Shoop also

- Performed an error analysis of the error diffusion oversampled architecture
- Proposed dynamic optical subtraction using multiple quantum well (MQW) devices
- Experimentally demonstrated and characterised the errors of nonideal noninterferometric optical subtraction
- Experimentally demonstrated a proof-of-concept first-order optical modulator using MQW devices.

This thesis extends upon Shoop's work by

- Rigorously deriving the unipolar constraints for three different oversampled A/D architectures
- Demonstrating that the sigma-delta architecture is superior to the error diffusion architecture for a photonic implementation
- Design and fabrication of devices optimised for simultaneous subtractor and comparator performance, necessary for the sigma delta architecture
- Demonstrating the necessary conditions to achieve true optical subtraction

- Developing an accurate simulation of the devices used in the A/D and testing the simulation with experiment
- Constructing an accurate simulation of a photonic sigma-delta architecture and using it to estimate potential performance
- Proposing the design of an integrated sigma-delta quantiser.

1.1 Thesis Overview

The first step towards the realisation of a high speed photonic integrated circuit oversampled A/D, is the construction of a model to demonstrate feasibility and expected performance. This is the goal that this thesis seeks to achieve. By analysing the constraints that optics applies to the architecture, constructing a model based upon experimental data, and verifying the model with experiment, the first-order sigma delta oversampled architecture is demonstrated to be an appropriate choice for a photonic integrated circuit implementation.

Chapter 3 seeks to develop the underlying device model by solving the differential equation for a SEED equivalent circuit. Data for the components in the equivalent circuit was obtained experimentally from MBE grown MQW samples. S-SEED switching experiments were performed and agreement with simulation is demonstrated. Further, the simulation was used to predict the parameters where critical slowing down and tristability occur, which were subsequently verified experimentally. From these results accuracy of the simulation is demonstrated.

In Chapter 4 the unipolar constraints for a simple pulse code modulation (PCM) oversampled photonic quantiser are derived. The S-SEED simulation is extended to model the signal-to-quantisation-noise ratio (SQNR) performance of the PCM architecture and this is compared to an experimental demonstration of the PCM design. Unipolar constraints for the sigma-delta and error diffusion architectures that include comparator hysteresis are derived to enable a simulation of their performance. Assuming an ideal subtractor and a function for carrier collection efficiency reported in the literature, SQNR was calculated for the sigma-delta quantiser.

To extend the simulations further, MQW devices with an optical output were required, as the MBE grown devices used for electrical characterisation did not have an inbuilt mirror. Chapter 5 details the design and successful MOCVD fabrication of a Fabry-Perot microcavity device. A model of the microcavity was developed that uses experimentally determined absorption of the quantum wells. Agreement is demonstrated between the model and a commercial numerical simulation package. Since an integrated A/D would require the same device design to perform both comparison and subtraction function, this trade-off was analysed. A design was selected that optimised the compromise and experimental data for responsivity and reflectivity is presented for the grown material.

Chapter 6 discusses optical subtraction using SEEDs, presents an experimental demonstration of subtraction and details the required modifications necessary to idealise the performance, as required in the sigma-delta architecture. Experimental verification of the comparator operation with an optical output is given and calculations of achievable dynamic range and contrast ratio are presented. The sigma-delta and error diffusion architectures were analysed to determine the dynamic range performance required from the subtractor. It is shown that the sigma-delta has the lowest requirement. An optical implementation of the sigma-delta is proposed and the performance simulated using a subtractor and comparator based on experimental data. To improve the dynamic range, a simulation was performed that had SEEDs heated to different temperatures, shifting the exciton, and separately optimising the comparator and subtractor. Finally, having demonstrated the feasibility of the photonic sigma-delta quantiser, performance scaling to high operating speeds is discussed.

To provide a graphical overview of the thesis layout, a flow chart is presented below that is split into two separate figures Fig. 1.1 and Fig. 1.2.

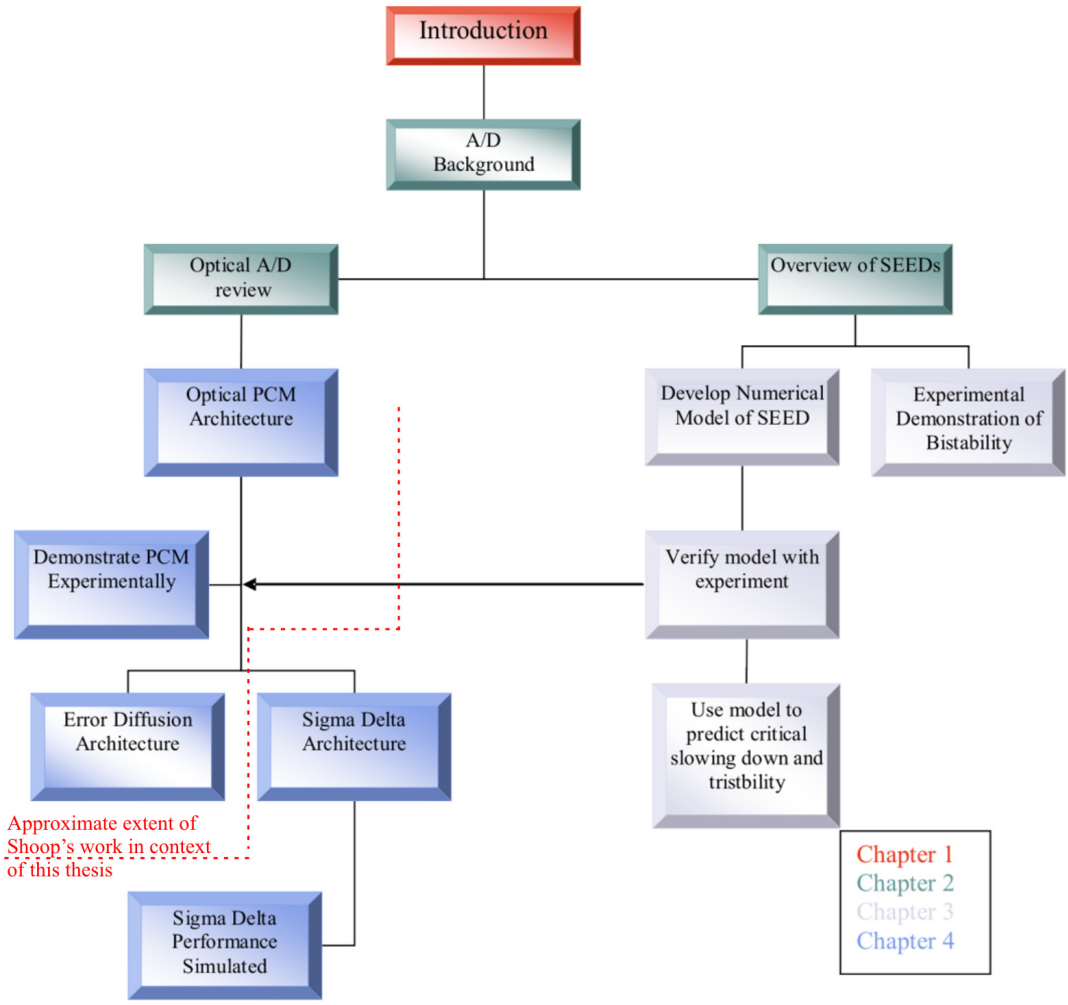

Figure 1.1: Flow chart of the thesis layout for the first threee chapters.

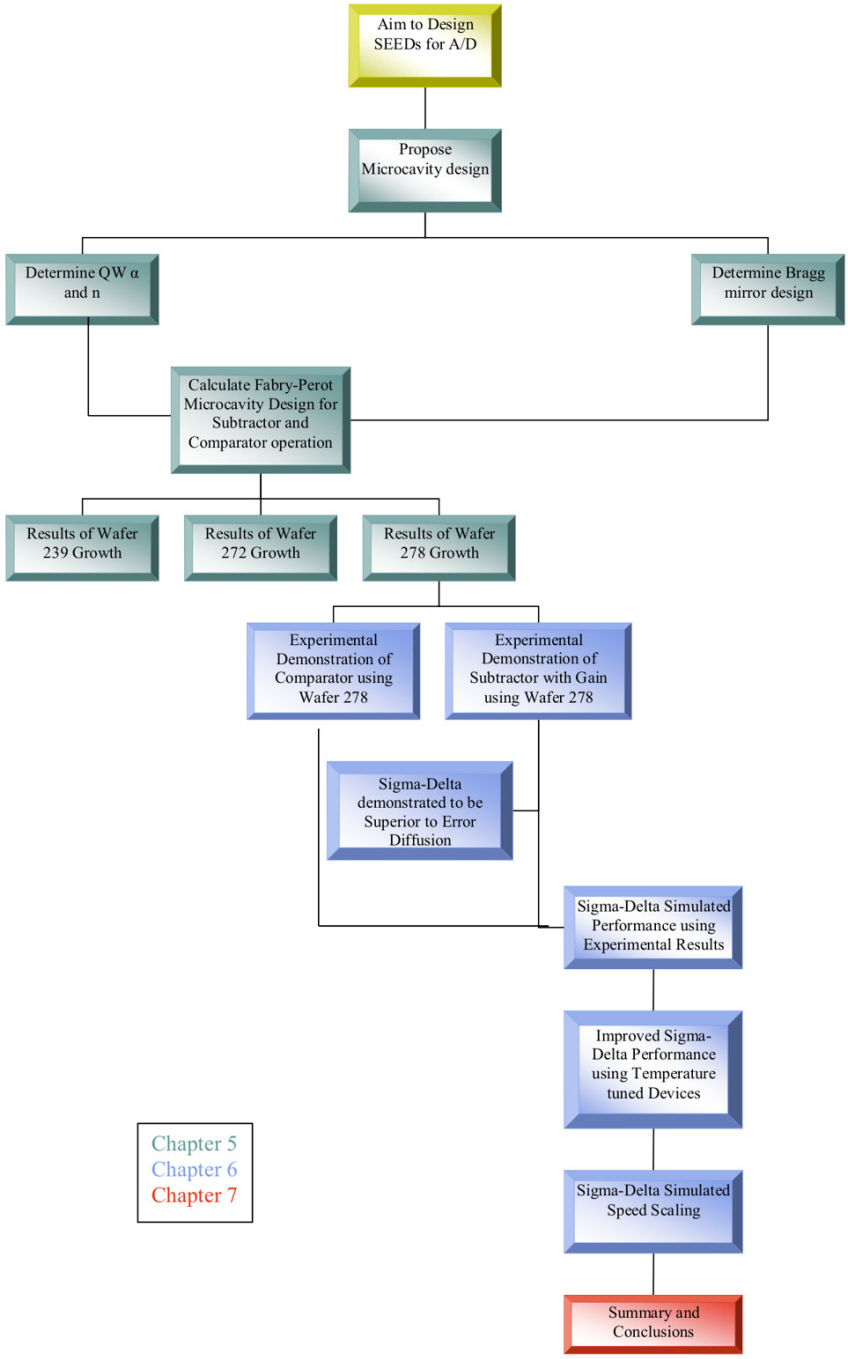

Figure 1.2: Flow chart of the thesis layout for the last four chapters.

Chapter 2

Background

To provide background information for the development of the photonic sigma-delta A/D, the following chapter presents an overview of the analog-to-digital conversion process, followed by a review of several photonic A/D techniques. The theory and operation of multiple quantum well devices is then discussed, as they form the building block of the functional elements used throughout this thesis.

2.1 A/D overview

The typical technique of converting an analogue signal to a digital representation that is discrete in time and amplitude, can be presented as a four step process[8], depicted in Fig. 2.1. The first step low-pass filters the input ($x(t)$), limiting $x(t)$ to a maximum frequency of f_0, in order to avoid the effects of aliasing (i.e. f_0 is equal to the A/D bandwidth). The subsequent sampling step converts the continuous time input into a series of analogue amplitude values ($x(nT_s)$), temporally separated by the sampling period $T_s = 1/f_s$ (where f_s is the sampling frequency). To satisfy the minimum Nyquist sampling criterion, the sampling frequency must be at least twice the input bandwidth ($f_s \geq 2f_0$). The process of amplitude quantisation follows, where each continuous amplitude ($x(nT_s)$) is converted into one of the discrete values ($q(nT_s)$), **and this is the part of the process examined in detail in this thesis**. The final step of digital coding generates a multi-bit digital word to approximate the input signal.

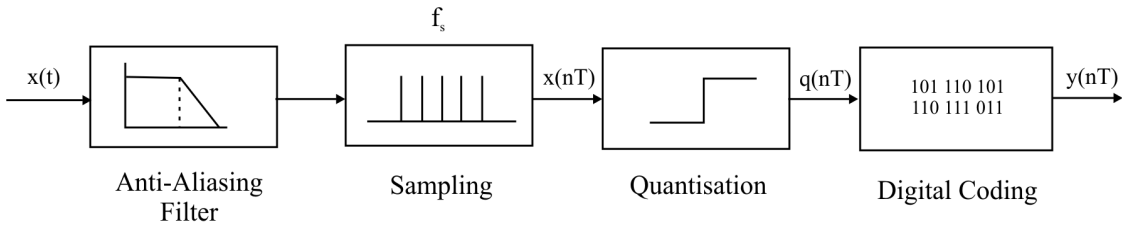

Figure 2.1: Schematic of the four processes in analogue to digital conversion - filtering, sampling, quantisation and coding.

The general description of Fig. 2.1 can be categorised into three types of A/D architectures: serial, parallel and oversampling. An example of a serial A/D is the successive approximation quantiser. In this architecture, a tree-structured search algorithm is applied to each input. Multiple operations are employed where the input is compared to a reference level. Each subsequent operation improves the approximation of the digital output to the analogue input. High resolution (12 to 14 bits)[4], [7] is achievable with this architecture, but due to the multiple operations for each output, speed is limited. However, this architecture has the advantage that complexity increases linearly with resolution. The parallel flash architecture simultaneously compares the input to all the different reference levels and hence requires $2^b - 1$ reference levels to attain a resolution of b bits. Therefore complexity increases exponentially with resolution, but the increased complexity of this parallel design gains a significant improvement in speed compared to the successive approximation approach. The previous two quantiser architectures are termed Nyquist rate converters, as the sampling rate occurs at twice the maximum input frequency.

In the third category, oversampling converters, the sampling rate is much greater than the Nyquist frequency[8], which spreads the quantisation noise power over a large bandwidth, thereby reducing the noise in the signal band. A further consequence of the high sampling frequency is that the complexity of the analog anti-aliasing filter of Fig. 2.1 is reduced. In the case of an A/D sampling at the Nyquist rate, to avoid signal attenuation and perform effective removal of aliasing artifacts, the anti-aliasing filter is required to have a very sharp cut-off at the Nyquist frequency[9]. However, in the oversampling case, the anti-aliasing filter can have a much slower roll-off and therefore a simpler design. The trade-off is that a

sharp low pass filter and downsampler, collectively referred to as a decimator, is required to be implemented digitally in the fourth step of Fig. 2.1. The oversampling technique trades sampling speed for resolution by averaging many quantiser output samples to converge to the input value. Therefore, oversampling architectures have the distinguishing feature that the tolerance and accuracy of the individual components can be less than the output resolution. Specifically, oversampling architectures require only a low resolution comparator, simplifying fabrication. Furthermore, complexity does not increase with increasing resolution, as resolution can be increased by increasing the oversampling ratio. Resolution can also be gained in an oversampling architecture by employing a feedback design that utilises a noise shaping filter in the feedback loop. The noise shaping filter removes noise from the signal band and shifts it to frequencies above the Nyquist frequency of the analog input, where it is removed in the decimation process. Oversampling data converters can be categorised by the order of feedback employed. The zero-order system, without feedback and also termed pulse code modulation (PCM), simply applies oversampling to a comparator. Higher order architectures feed back a number of samples, equal to the order of the system, to generate error signals and improve the quantiser accuracy. However, the cost of the additional resolution is increased complexity and orders higher than two pose further design challenges, as they are not unconditionally stable[8]. Therefore in this thesis we only consider first-order systems, of which two examples, the sigma-delta and error diffusion, are now considered in detail. A block diagram of the first-order error diffusion quantiser architecture is presented in Fig. 2.2. The quantiser architecture of Fig. 2.2 uses negative feedback of the comparator error. The error is calculated by subtracting the comparator input (u_i) from its output (q_i) at the subtractor node labelled S2. That is,

$$e_i = q_i - u_i. \tag{2.1}$$

The error is delayed by a sampling period, and is then subtracted from the analogue input x_i at the subtractor node S1. Therefore, the input to the comparator is given

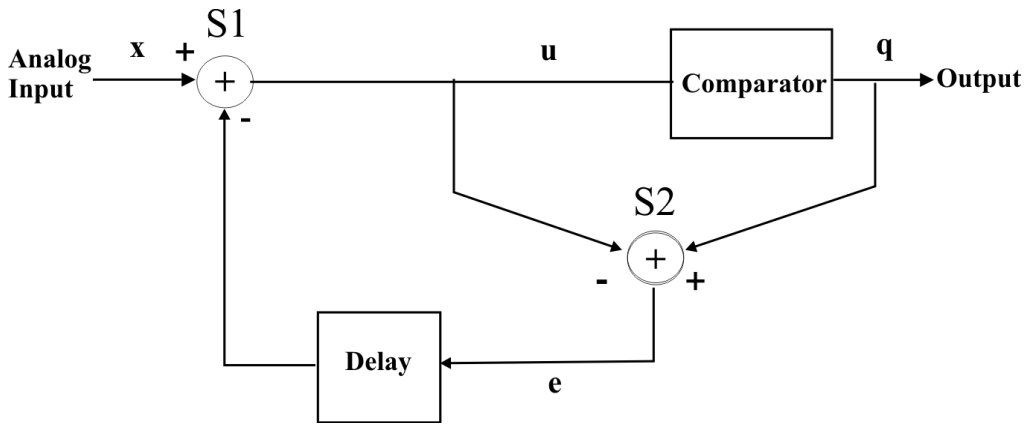

Figure 2.2: Block diagram of the first-order error diffusion quantiser architecture. The labels represent the analogue input x, comparator input u, comparator output q, and comparator error e.

by

$$u_i = x_i - e_{i-1}. \tag{2.2}$$

A significant benefit of this architecture can be demonstrated by considering the substitution of (2.2) into (2.1), yielding

$$q_i = x_i + e_i - e_{i-1}. \tag{2.3}$$

Due to the negative feedback, the discrete-time derivative of the comparator error $(e_i - e_{i-1})$ appears at the quantiser output, instead of the simple error (e_i), as would be the case without feedback[6]. The differentiation of the error, or quantisation noise, acts as a high pass filter of the quantisation noise. This is the origin of the spectral shaping, as most of the noise is shifted to frequencies above the Nyquist frequency of the input signal[6], where it can be removed by low-pass filtering. The spectral shaping of the noise is depicted in Fig. 2.3 [8]. The advantage of this approach is that it requires only a two level comparator of modest quality. Mathematically equivalent to the error diffusion is the sigma delta quantiser (shown in Fig. 2.4), which repositions the delay operation. Consequently, the calculation of error, and subtraction of the error from the input is performed in one operation.

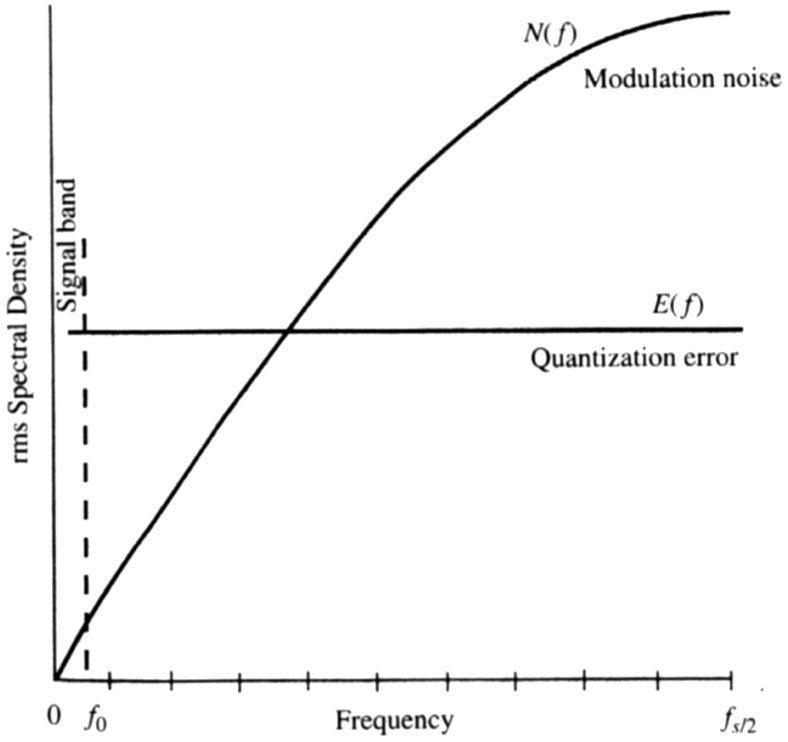

Figure 2.3: Spectral density of the noise, $N(f)$, from an error diffusion quantiser (with oversampling of 16 times), compared with that of ordinary quantisation $E(f)$, from [8].

Therefore the sigma delta quantiser requires one less subtractor than the error diffusion quantiser, and this is a significant advantage in an optical implementation. A schematic of the sigma delta is given in Fig. 2.4. For completeness, a schematic

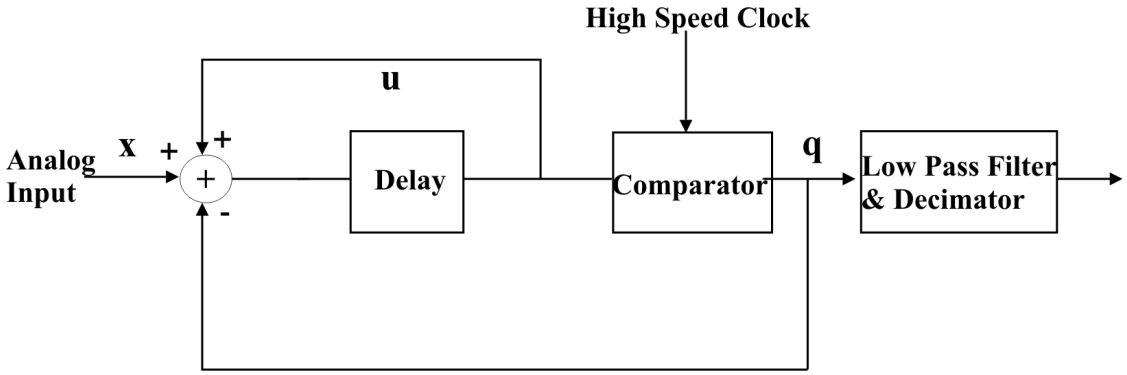

Figure 2.4: Schematic of an oversampled sigma-delta architecture.

of a second order system is given in Fig. 2.5, which demonstrates two levels of error feedback to improve the output resolution, at the cost of increased complexity. In [10] Shoop proposed a second order, multistage optical error diffusion system.

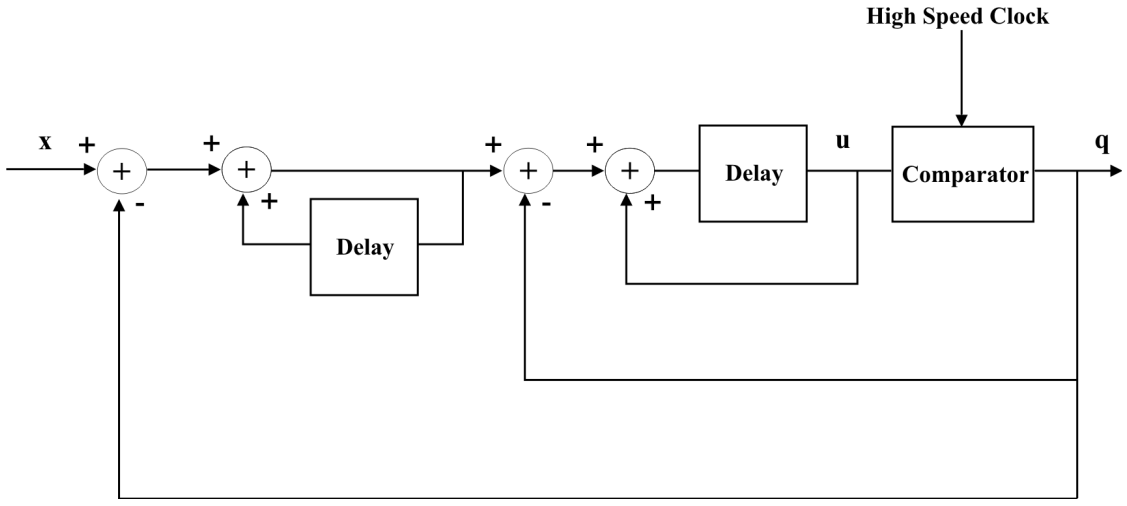

Figure 2.5: Schematic of a second order sigma-delta architecture[8], depicting the feedback of comparator error to two previous input samples.

The table below lists some examples of state-of-the-art (as of 2006) commercial sigma-delta A/Ds. The attributes listed include the maximum resolution in bits and

signal-to-noise ratio (SNR), the maximum input frequency, the oversampling ratio, the order of the architecture and the intended application.

Model	**AKM5394A**	**CS5381**	**TI PCM4204**	**AD9870**
# Bits (Resolution)	24	24	24	16
SNR (dB)	123	120	118	-
Oversampling Ratio	128	128	64-128	-
Max. Freq. (kHz)	216	216	216	300,000
Order	5^{th}	-	-	-
Application	Audio	Audio	Audio	Comms.

The very high resolutions achieved for audio applications demonstrate one of the main advantages of oversampling architectures, namely that bandwidth can be traded for resolution. This trade-off still applies to the high frequency AD9870 (input frequency up to 300 MHz), as it only accepts a total input bandwidth of 150 kHz. The high operating frequency is achieved by the use of a band-pass filter on the input to the A/D and a sampling frequency much greater than the input bandwidth[11].

One of the main reasons for investigating optical versions of the above A/Ds is the availability of optical clocks with ultra-low timing jitter. The reason this is significant is demonstrated by the following figure from [1]. Figure 2.6 plots the A/D performance limitation due to thermal noise, clock jitter (aperture uncertainty) and comparator ambiguity (probability that the comparator will make an ambiguous decision and is related to the comparator's switching time). It demonstrates that for fast sampling rates and fast switching comparators, clock jitter is the limiting factor in achieving high resolution A/D conversion. Such low jitter optical clocks would allow operation of optical oversampling A/Ds at high resolutions, as demonstrated in electronics, but at much higher operating frequencies than achievable with electronics alone. This elucidates the main concept of this work, to take the technology of high resolution audio A/Ds and increase the operating frequency, via optical techniques, to allow digitisation of wide bandwidth RF signals.

For a complete overview, other optical A/D implementations are discussed in the next section.

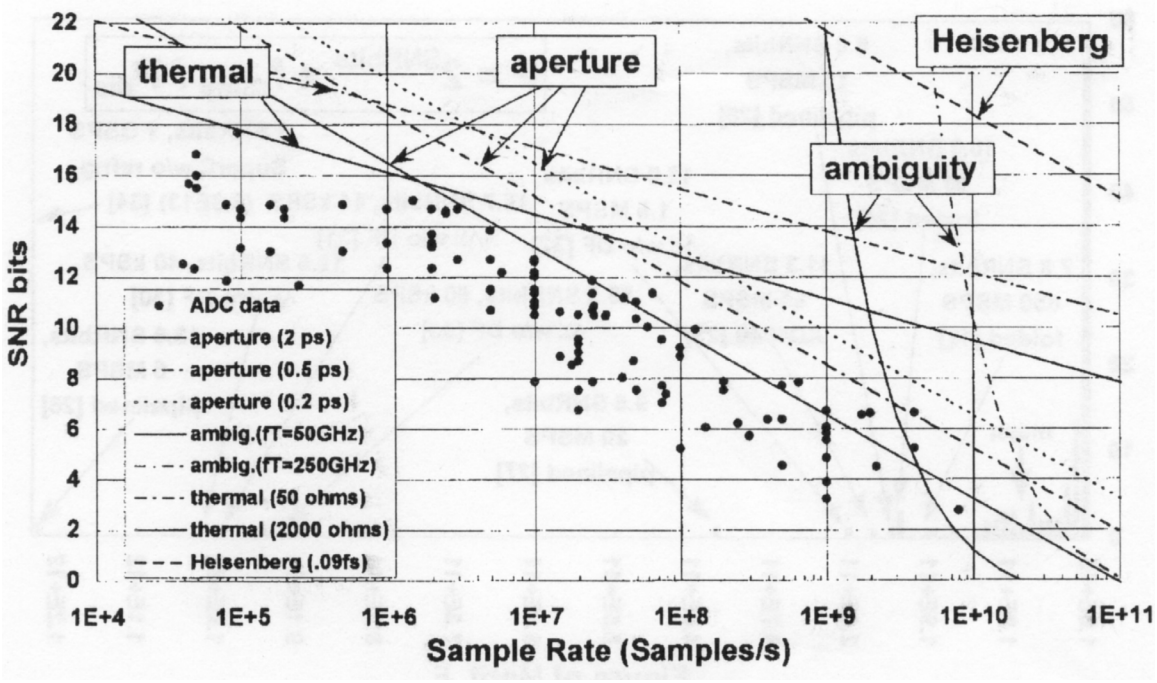

Figure 2.6: A/D performance resolution limitation due to thermal noise, aperture uncertainty (clock jitter) and comparator ambiguity, from [1].

2.1.1 Optical A/D review

The history of optical analogue-to-digital conversion began in 1974[12] with the invention of a novel electro-optic technique utilising Mach-Zender interferometric modulators, which had the speed of a flash architecture and the linear complexity of successive approximation methods. Such devices were realised[13], [14], but were limited by the small electro-optic coefficients of available materials and transit-time delays to approximately 6 bits at 1GHz[4].

Examples of optical flash converters demonstrated in alternative technologies are given in [15] and [16]. The first example[15], shown in Fig. 2.7, used comparators created from optoelectronic devices called Self-Electro-Optic Effect Devices (SEED), which will be described in more detail in the next section. Four comparators were employed, along with binary phase gratings to illuminate each comparator with the input and the correct reference level. A digital representation was read from the state of the multiple output beams. Operation at a clock frequency of 58kHz was achieved, and data rates of 1GS/s were calculated to be feasible. Two main drawbacks exist

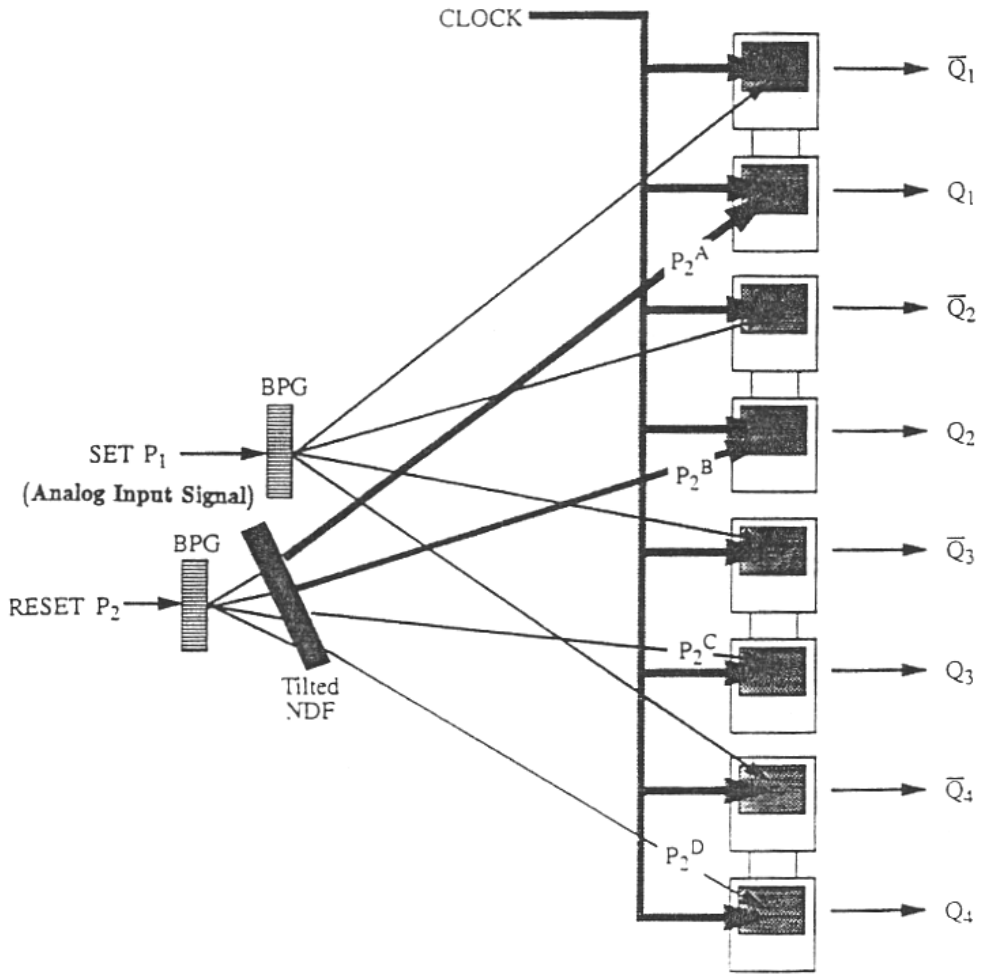

Figure 2.7: Schematic of the optical flash quantiser from [15].

with this design. The first is the complexity of the optical system. Achieving the precise setting of many beams, and construction of the optical layout shown in Fig. 2.7 for an A/D with significantly greater resolution than the demonstrated 2 bits would be very challenging. The second problem is the existence of hysteresis in the SEED comparators. Hysteresis limits the achievable resolution and also requires a complicated setup of optical pre-charging to create an unambiguous comparator[15].

The second example[16], which is represented in Fig. 2.8, achieved 2.5Gb/s (and 5Gb/s in [17]) by optically sampling an RF input signal with optoelectronic switches that were activated by mode-locked laser pulses. Eight samplers with corresponding

optical delays were used to achieve the reported sampling rate, which was eight times the mode-locked laser repetition frequency. To aid in the quantisation process, the amplitude of each sampled signal was electronically converted into a pulse width. To perform quantisation, eight different pulses, each of a different wavelength were propagated though an optical circulator and series of Bragg gratings to give each wavelength a different time delay. The time-multiplexed pulses were then incident on a modulator that was driven by the output of the samplers. The pulse width of the sampled input controlled how many different wavelengths were transmitted, representing the digital output by the number of different wavelengths. Further electronic processing produced gray-scale quantisation levels. This architecture has the advantage of optical sampling, low-power consumption and optical quantisation, but its speed is ultimately limited by the electronics used in the sampling and amplitude to pulse-width conversion processes.

Many groups [18], [19], [20] have investigated techniques of time, or wavelength, division multiplexing of optical signals to distribute the bandwidth of an analogue input into N signals of reduced bandwidth. Each relatively low bandwidth signal is then digitised by electronic A/Ds. This approach takes advantage of optical sampling, reviewed in detail in [21], and the functionality of existing electronic components. However, the sampling times of the different electronic A/Ds must be uniform, gains and offsets must be precisely set and crosstalk must be minimal[21]. These constraints make it difficult in practice to achieve high resolution and spur free dynamic range (SFDR). SFDR is a metric of A/D performance used to determine the available dynamic range that is free from spurious signals, which can be misinterpreted as real signals. The spurious signals are generated from unwanted nonlinear characteristics of components constituting the A/D, and SFDR is defined as

$$SFDR(dB) = 20\log_{10}(|X_{avg}(f_i)| \,/\, \max_{f_s,f_h}\{|X_{avg}(f_h)| \;\; or \;\; |X_{avg}(f_s)|\}), \tag{2.4}$$

where X_{avg} is the averaged spectrum of the A/D output, f_r is the frequency of the input sine wave and f_h and f_s are the frequencies of the set of harmonic and spurious

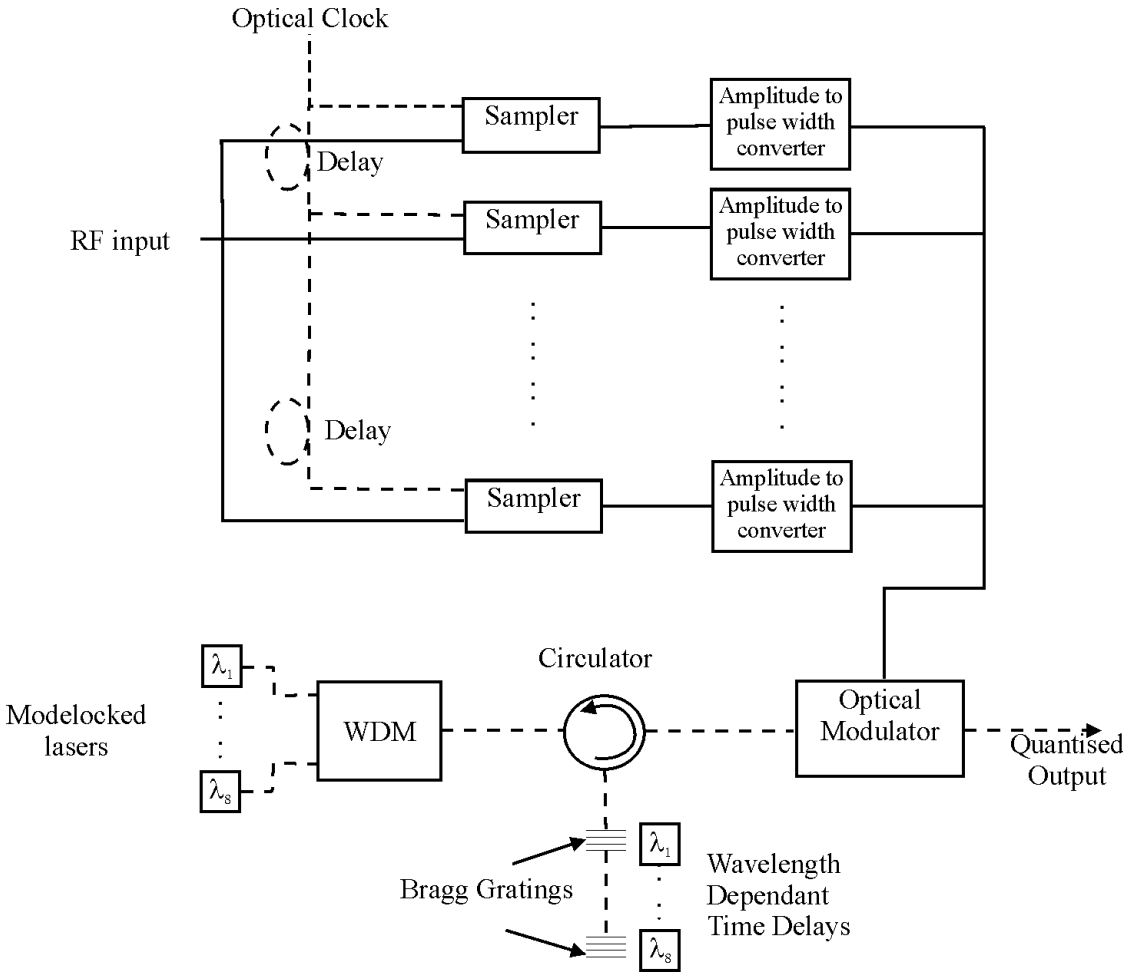

Figure 2.8: Schematic of the high speed optical A/D from [16] where solid lines represent electrical connections and dashed lines represent optical connections. Eight parallel samplers are used to achieve 2.5Gb/s sampling and eight different wavelengths are used to quantise the sampled value of the RF input.

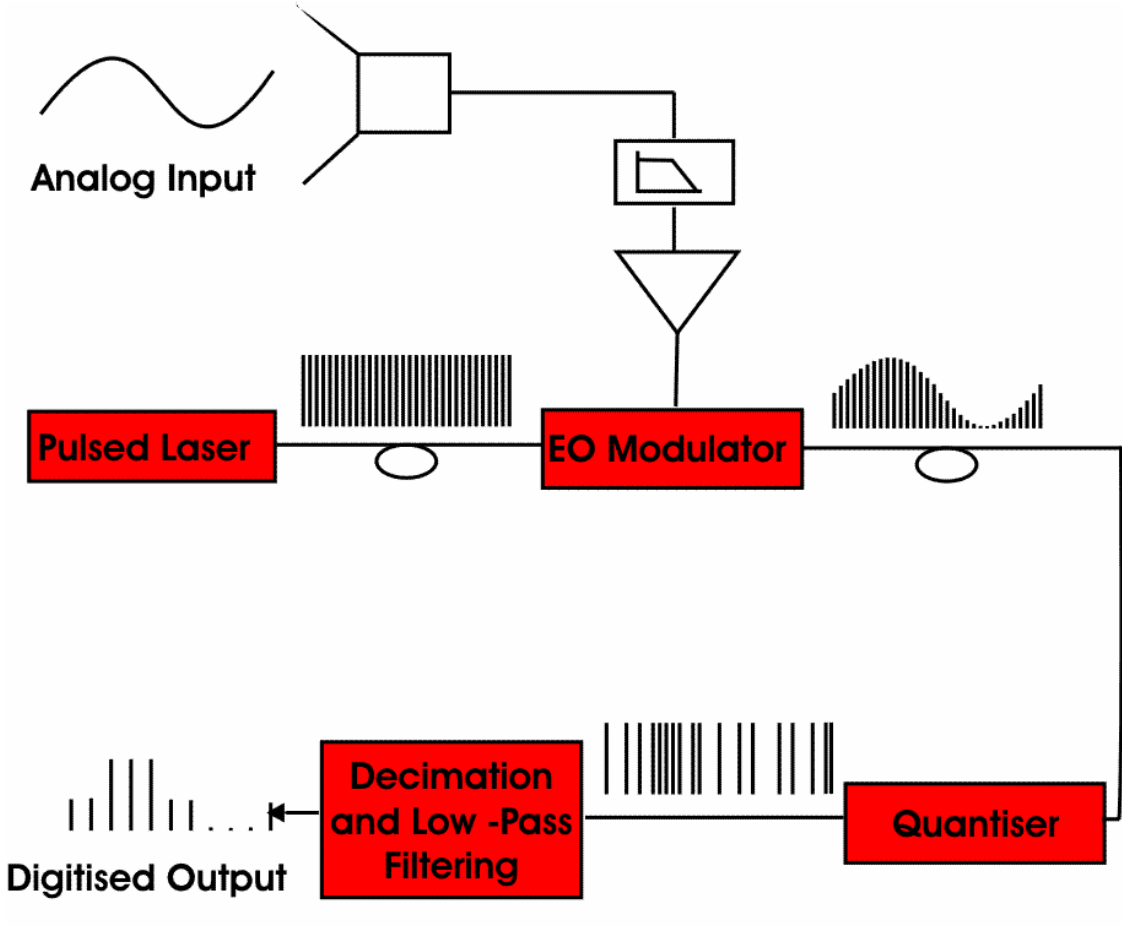

Figure 2.9: Illustration of an oversampled optical A/D, including representative signals.

spectral components[22]. Many optical time stretching techniques have also been proposed that are able to sample very high frequency analog inputs, but they are not considered here, as they are unable to digitise aperiodic continuous-time signals.

An optical oversampled error diffusion architecture was proposed by Shoop[4] that overcame many of the complexity problems, by trading speed for resolution. Further, the proposed design was able to be implemented using the aforementioned SEEDs to perform the required functions of comparison and subtraction. To aid in understanding of the optical A/D operation proposed by Shoop, it is helpful to consider the overall oversampled A/D system, illustrated in Fig. 2.9. A pulsed laser is used to generate a train of pulses at a repetition rate much faster than the Nyquist frequency of the low-pass filtered analogue input. A modulator imparts the analogue

amplitude information onto the pulse train, producing a discrete-time, continuous amplitude signal. The error diffusion (or mathematically equivalent sigma-delta, as will be demonstrated by (4.9) and (4.19)) quantiser converts the analogue amplitudes into a train of digitally encoded 1-bit pulses at the sampling frequency. Finally, low-pass filtering and decimation circuitry produces multi-bit output at the Nyquist rate, trading speed for resolution. Convergence of the two level output to the analogue input is demonstrated in [23] and is reproduced in Appendix A. As a consequence of the use of optical beams to carry information, negative values cannot be directly encoded. This requires modification to the error diffusion and sigma delta architectures, and is discussed in detail in Chapter 3.

The original work of Shoop[4], [6], [5] demonstrated proof-of-concept of the optical error diffusion architecture by substituting all but one subtractor with electronics. The experimental setup to perform optical subtraction[24] in an error diffusion quantiser is reproduced in Fig. 2.10. Contributing to this result, Shoop proposed and characterised the errors of dynamic optical subtraction using an MQW device that operated in reflection and was termed a REAM (Reflection Electro-Absorption Modulator), and analysed the errors of the error diffusion architecture. Shoop subsequently applied the work to a 2-dimensional array of smart pixels to perform A/D conversion[25], [7]. However, an experimental demonstration of an all optical error diffusion quantiser has yet to be performed. Due to the advantageous properties of low complexity, ability to trade speed for resolution and flexible component tolerances of the oversampled approach, the work in this thesis concentrates on further investigating optical error diffusion and sigma-delta quantisers. Specifically, Shoop's[4], [5], [6] work is extended by rigorously analysing the constraints that optical operation applies to PCM, first order sigma-delta and error diffusion oversampled architectures. Each of the architectures is modelled, using a simulation based on experimental data and verified with experiment. Further, A/D performance is calculated for all-optical implementations of each architecture and the sigma-delta is demonstrated to be the best choice for a photonic implementation, provided subtractor non-idealities are compensated.

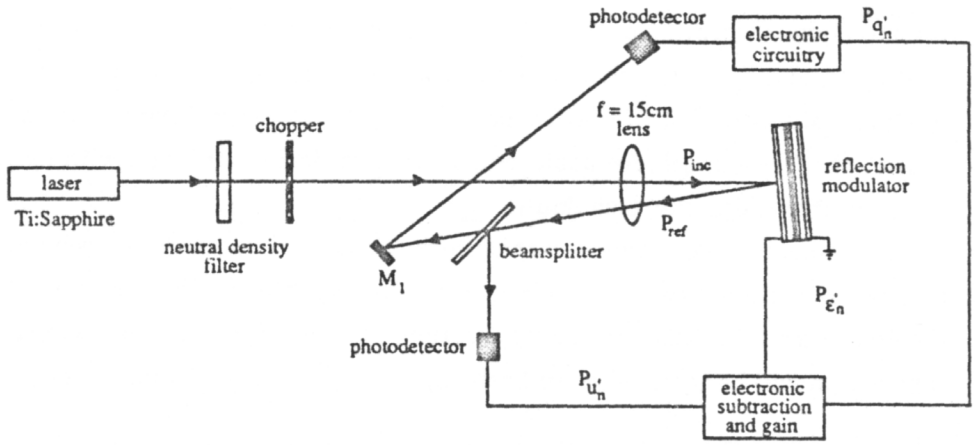

Figure 2.10: Experimental setup used by Shoop to demonstrate proof-of-principle first order error diffusion modulator[4]. Subtraction of the error from the input $(P_{x'_n} - P_{\varepsilon'_n})$ was implemented optically using a REAM, where $P_{inc} \equiv P_{x'_n}$ and $P_{ref} \equiv P_{u'_n}$. The comparison operation and the subtraction function used to generate the comparator error $(P_{q'_n} - P_{u'_n} = P_{\varepsilon'_n})$ were both performed electronically. Optical sampling was performed by a mechanical chopper and the quantiser output, $P_{q'_n}$, was captured by a digital storage oscilloscope.

2.2 Self-Electro-Optic Effect Device

The photonic oversampled A/D described above can be implemented with any optical technology that can supply the functional elements of a comparator and subtractor. At the present time, the only technology able to perform both functions is the Self-Electro-Optic Device (SEED)[26]. Further, SEED technology has the advantages of very high switching speed[27] and low switching power[28]. Hence, this thesis will concentrate on the implementation of an optical oversampled A/D using SEEDs.

The underlying technology of SEEDs, the semiconductor multiple quantum well (MQW) diode, is also appropriate for commercial realisation. Current commercial laser diodes, photodiodes and light emitting diodes employ multiple quantum wells and they have also been utilised commercially as 40Gb/s modulators for fibre optic communications [29]. Finally, SEEDs have been integrated into a 2D array to form the basis of a very high-speed digital signal processor [30].

2.2.1 Background

Before continuing the discussion of the utility of SEEDs, a brief overview of the physics underlying the technology will be given. Heterostructures will be introduced as the fundamental element of quantum confinement. The features of quantum wells that are important to device functions will be discussed, specifically excitons and the quantum confined stark effect (QCSE).

Heterostructures

Heterostructures are formed by the growth of semiconductors composed of more than one material. Different semiconductor materials have different bandgaps and lattice constants, allowing the band structure of the heterostructure to be engineered by fabricating structures of layers with different thicknesses and compositions. Figure 2.11 plots the lattice constant against bandgap for various common semiconductors. To maintain a crystalline structure without dislocations, the lattice constant of two combined semiconductors must be closely matched. For thin films a greater lattice mismatch can be tolerated. Referring to Fig. 2.11, we find the semiconductors GaAs and AlAs may be combined to form a crystalline interface with a bandgap discontinuity of 1.59eV (a heterojunction), or they may be alloyed to form the semiconductor $Al_xGa_{1-x}As$ which maintains a direct bandgap for $x < 38\%$. This flexibility in semiconductor properties is a significant factor in the popularity of the GaAs/AlGaAs material system, and it is exploited in the devices used in this study.

To manufacture high quality heterostructures the interfaces must be near perfect, which requires very low impurity concentrations and very tight control of the crystal growth conditions. Further, very thin layers of a few nanometres thickness are often required. The two dominant processing techniques in use today are molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD). MBE uses sources of high purity elements (e.g. Al, Ga, As, Si) that are vapourised in furnaces that produce beams of atoms in an ultra-high vacuum environment. Controlled by a shutter, the beam of a particular source impinges on a heated substrate and slowly grows the desired crystalline structure, layer by layer. This process is capable of producing very abrupt heterojunctions and with the use of reflected high-energy

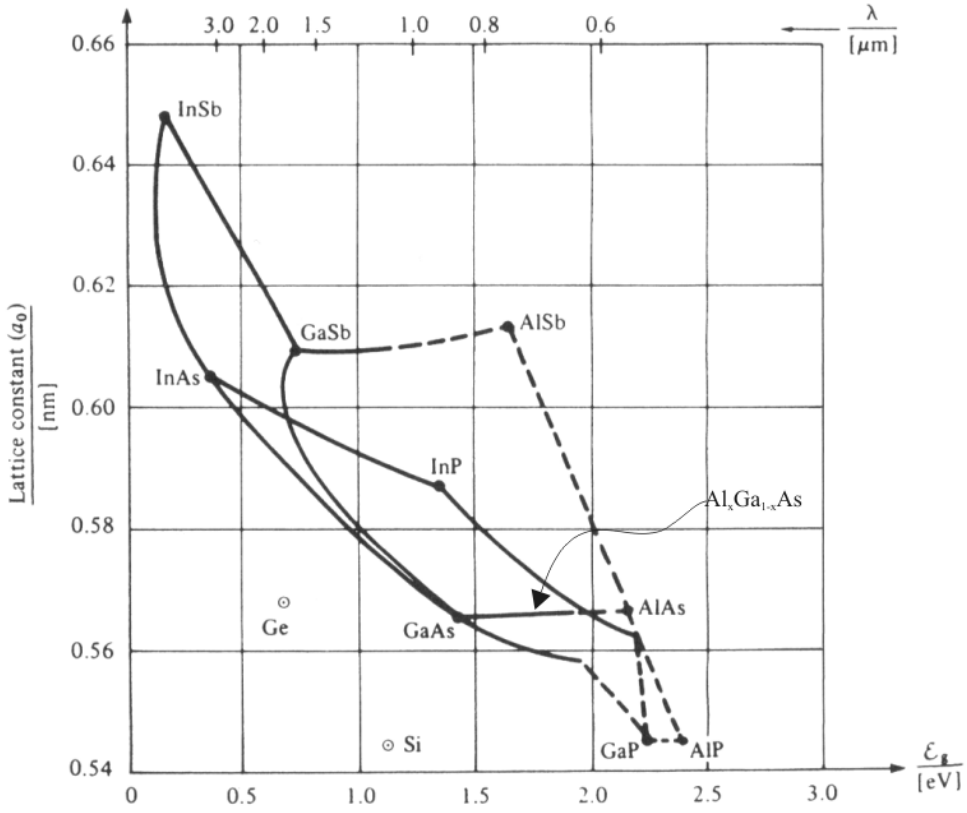

Figure 2.11: Plot of the lattice constant versus minimum bandgap, expressed in eV and as a wavelength in μm for a variety of semiconductors. The solid lines represent a direct bandgap and the dashed lines indirect bandgaps. (From [31]).

electron diffraction (RHEED), layer thickness can be precisely monitored and controlled. However, the requirement of ultra-high vacuum makes MBE very expensive and slow growth rates are not amenable to mass production. The MOCVD process flows metal-organic chemicals in a hydrogen carrier over a heated substrate, where the organic chemical decomposes, depositing the desired molecule for semiconductor growth. MOCVD can produce heterostructure material of similar quality to MBE and has been successfully deployed in large scale commercial production. However, a greater substrate temperature than MBE leads to greater diffusion and less abrupt heterojunctions, and operation near atmospheric pressure does not allow RHEED to be used. In this work GaAs-AlGaAs p-i(MQW)-n diodes, grown via both MBE and MOCVD processes have been used.

Quantum Wells

One of the most technologically important heterostructures is the quantum well. A quantum well is formed by the sandwiching of a thin layer of narrow bandgap semiconductor material between a wider bandgap semiconductor material. The structure is referred to as a type I quantum well when the bandgap discontinuity created by the heterojunctions, creates a potential well in both the conduction and valence band of the narrow bandgap material. Such a situation is illustrated in Fig. 2.12 for an AlGaAs-GaAs-AlGaAs quantum well. The bandgap discontinuity of a heterojunction is not distributed evenly between the conduction and valence band. Therefore different types of bandstructures can be formed. A type II quantum well exists when the potential well for the electrons and holes are formed in different materials. The final possibility, a type III quantum well, has overlapping conduction and valence bands causing electrons and holes to combine spontaneously until a sufficiently large electric field is created to impede the flow.

The confinement of carriers in a quantum well with a thickness comparable to the carrier Bohr radii leads to quantisation of the energy levels, as depicted in Fig. 2.12. In the plane of the well, where there is no confinement, the carriers exhibit the bulk material properties. An estimate of the energy levels in a quantum well can be gained by solving the Schrodinger equation for a particle contained in an infinitely

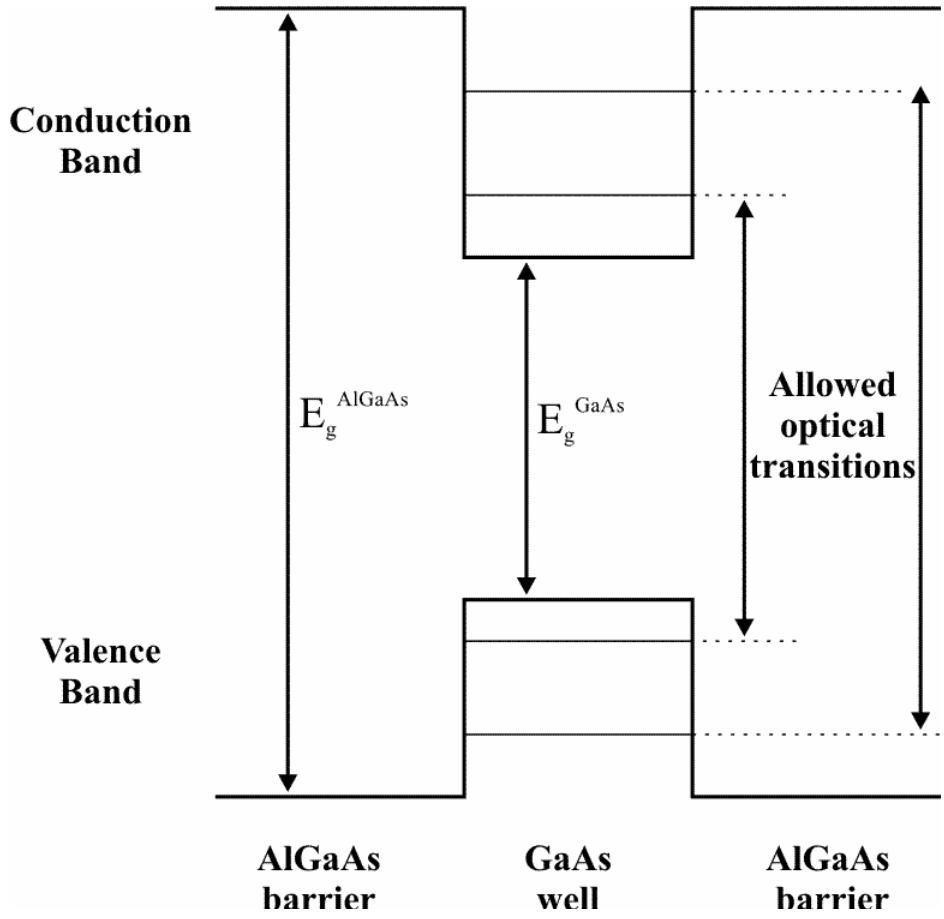

Figure 2.12: Schematic diagram of a type I quantum well using the GaAs/AlGaAs material system. Illustrative bound states of the conduction and valence bands are shown along with the allowed optical transistions.

deep potential well. The resulting wavefunctions and energy levels are[31]

$$\varphi_n(x) = A_n \sin(\frac{n\pi x}{a}) \tag{2.5}$$

$$\varepsilon_n = \frac{\hbar^2\pi^2 n^2}{2ma^2}, \tag{2.6}$$

where a is the well width and n is an integer greater than zero. Substituting effective mass m^* and adding the energy of the bandgap ($E_g = E_c - E_v$), the energy levels of a quantum well in a semiconductor conduction band with quantum number n_e become

$$\varepsilon_{en_e} \approx E_c + \frac{\hbar^2\pi^2 n_e^2}{2m_e^* a^2}, \tag{2.7}$$

and in the valence band with quantum number n_h

$$\varepsilon_{hn_h} \approx E_v + \frac{\hbar^2\pi^2 n_h^2}{2m_h^* a^2}. \tag{2.8}$$

This result captures the essential feature that the energy levels are quantised with the lowest level greater than the bottom of the band (E_c or E_v). The energy dependence on the well width (a) and material (m^*) is also represented in (2.7) and (2.8). The effect of quantum wells can be observed via the increase in energy of the optical absorption edge, compared to bulk material. Therefore, quantum wells allow the optical absorption of a device to be engineered, by altering the thickness and composition of the wells and barriers, and this provides an important optoelectronic design tool.

Since carrier motion in quantum wells is restricted in one dimension by the potential barriers, quantum wells are considered 2-dimensional structures. The density of states for a particle in 3-D is given by

$$n_{3D}(E) = \frac{m\sqrt{2mE}}{\pi^2\hbar^3} \tag{2.9}$$

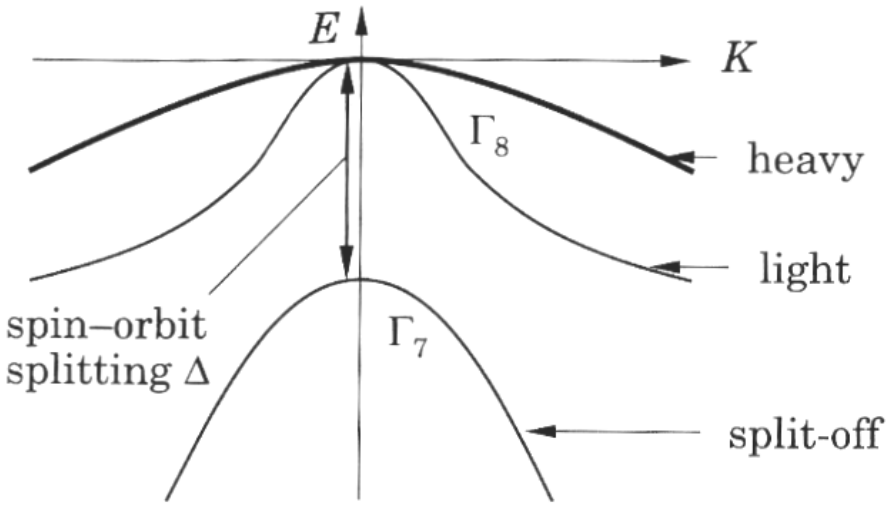

Figure 2.13: Schematic diagram of the $GaAs$ valence band when the effects of spin-orbit coupling are included[31].

and for 2-D

$$n_{2D}(E) = \frac{m}{\pi\hbar^2} \tag{2.10}$$

which is independent of energy. As the density of states near $E = 0$ is greater in two dimensions than in three, a structure employing quantum wells has greater absorption compared to bulk material, and therefore makes a more efficient optoelectronic device [31].

For a complete model of quantum wells, a numerical solution of the Schrodinger equation for finite wells that includes the full valence band structure, the periodic effects of the crystal lattice, excitons and spin-orbit coupling is required. Some of the significant results of such a treatment are that only a finite number of energy levels are bound in the quantum well. The inclusion of spin-orbit coupling results in a lifting of the degeneracy in the valence band, producing the light hole, split-off and heavy-hole bands, with each band having spin-up and spin-down states, as represented in Fig. 2.13. Further detail is given in [31].

Excitons

When an electron-hole pair is created, Coulomb attraction between the carriers can create a bound pair, labelled an exciton. An exciton is analogous to positronium, the bound state created between an electron and a positron. In bulk material the exciton binding energy E_b is given by

$$\begin{aligned} E_b &= -\frac{e^2}{8\pi\epsilon_0\epsilon_r a_0}, \\ a_0 &= \frac{4\pi\epsilon_0\epsilon_r\hbar^2}{e^2 m^*_{eh}} \end{aligned} \tag{2.11}$$

where m^*_{eh} is the reduced mass of the electron-hole pair, ϵ_r is the relative permittivity of the semiconductor and a_0 is identified as the exciton Bohr radius. In bulk GaAs the binding energy of an exciton is approximately 5meV[31], which is ionised at room temperature by phonons. Confined in an ideal two dimensional well, the binding energy of the exciton increases by a factor of 4[31], allowing observation at room temperature. The existence of excitons is revealed in measured optical absorption spectra via a large absorption peak close to the band edge of the bulk material. Absorption is increased by the presence of excitons as the oscillator strength is enhanced by the electron and hole wavefunction overlap created by confinement in the potential well and coulomb attraction. Further, the transition energy is reduced relative to the interband transition energy, due to the binding energy of the exciton.

For real quantum wells that have finite barriers, the exciton binding energy will be less than the ideal prediction. Figure 2.14 plots the heavy and light hole exciton binding energies as a function of well width for finite and infinitely deep wells[31]. As the well width is reduced, so too is the radius of the exciton and hence the binding energy increases. However, as the well width approaches zero, the wavefunctions tunnel into the finite barriers, and the confinement of the exciton is reduced. Hence a peak in the binding energy occurs, which is approximately half of the ideal prediction. This means that once formed, excitons will be quickly ionised by phonons at room temperature[32], leading to a broader absorption line than is expected from the ideal case.

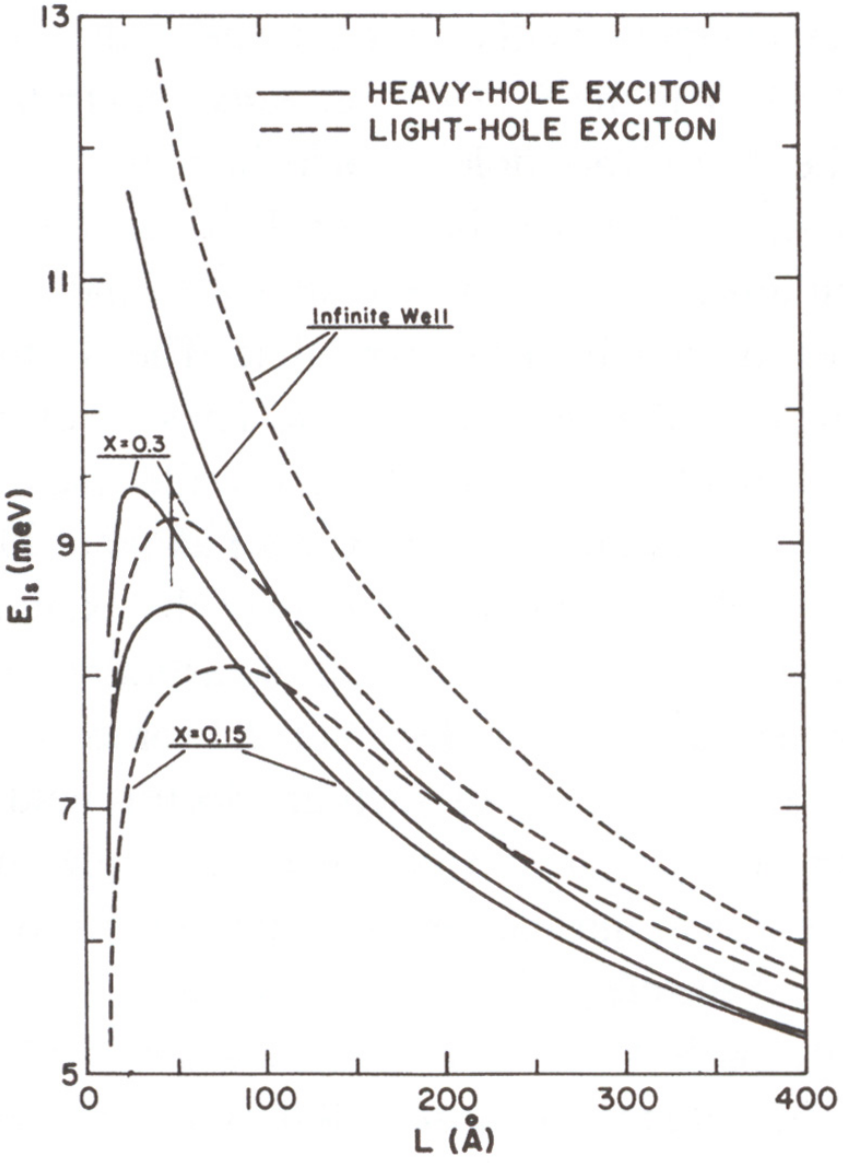

Figure 2.14: Binding energy of heavy and light hole excitons in GaAs-$Al_xGa_{1-x}As$ quantum wells as a function of well width[31]. An infinte well is compared to two different height finite wells.

Quantum Confined Stark Effect

To perform optical processing functions employing quantum well devices, such as switching, a mechanism for altering the absorption or phase of incident light is required. Absorption modulation is achieved with the application of an electric field normal to the quantum wells, and this is known as the quantum confined Stark effect (QCSE)[33]. The effect is pictured in Fig. 2.15. Part (a) depicts the wave-

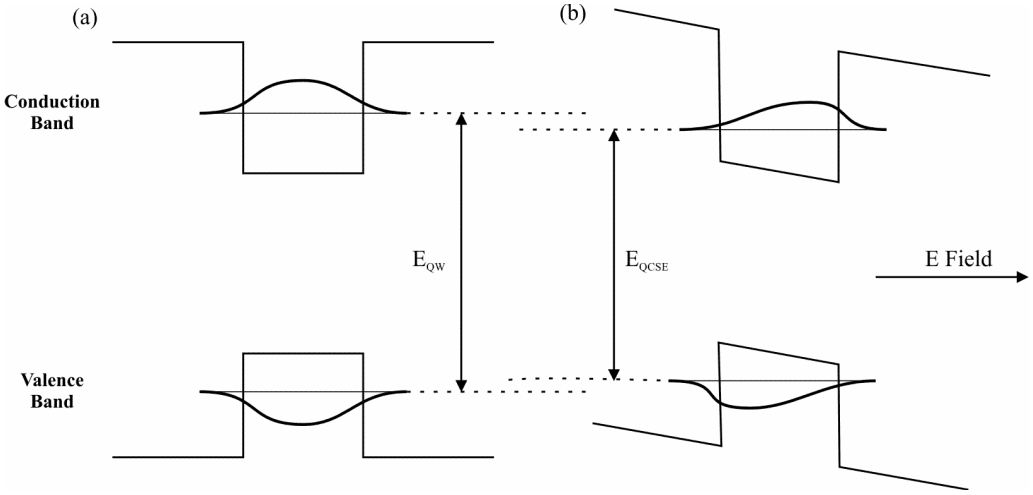

Figure 2.15: Part (a) depicts the wavefunctions, energy levels and interband transition energy (E_{QW}) for a finite quantum well. In part (b) an electric field is applied normal to the quantum well that tilts the bands, reduces the transition energy to E_{QCSE} and reduces the absorption.

functions, energy levels and interband transition energy of a finite quantum well with flat bands. Upon application of an electric field normal to the quantum well layers in part (b), the bands tilt, reducing the energy of both holes and electrons. As holes and electrons have charges of opposite sign, they are pulled to opposite sides of the quantum well, and the wavefunctions are distorted. Absorption is reduced by this distortion as the wavefunction overlap and hence oscillator strength is diminished. The applied field also reduces the symmetry of the quantum well which strengthens previously forbidden transitions. Fortunately, the confinement of the quantum well prevents the electric field ionising the excitons with applied fields of up to 100kVcm^{-1}[34].

A plot of MQW responsivity as a function of wavelength is given in Fig. 2.16

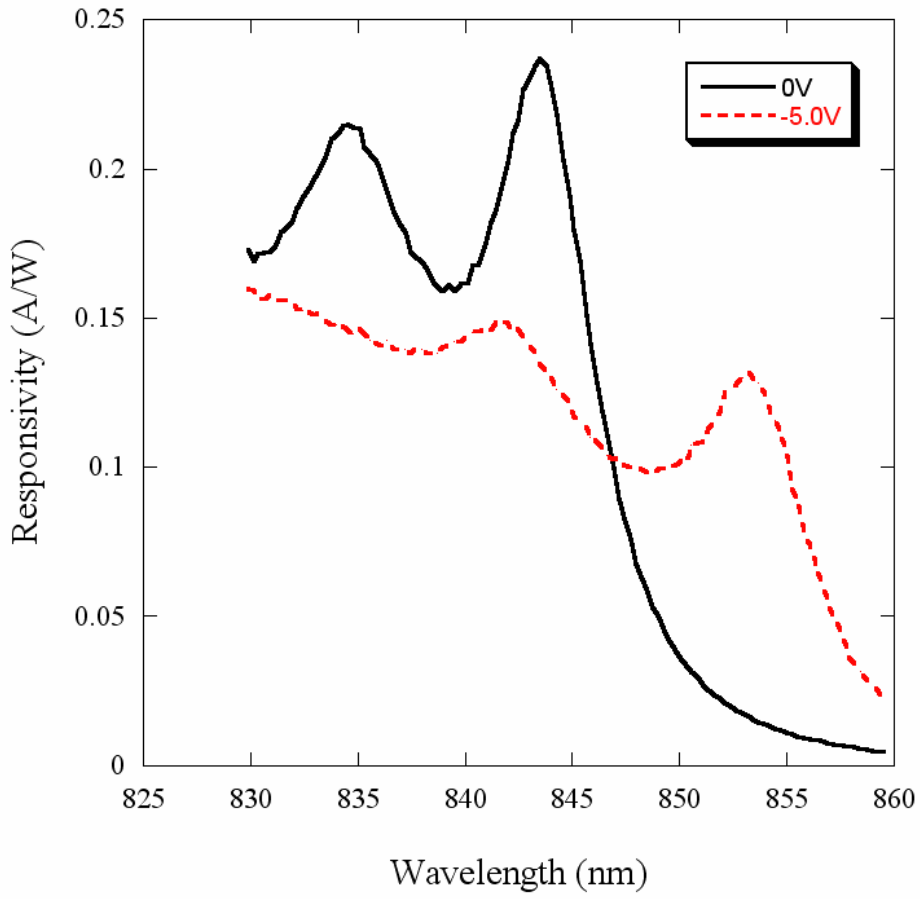

Figure 2.16: Responsivity as a function of wavelength for applied voltages of $0V$ and $-5V$. The larger electric field is seen to red-shift the excitons and reduce the peak responsivity.

for two different applied fields. Figure 2.16 demonstrates the relevant properties of QCSE for device operation, which are decreasing energy, or red-shift, of the exciton and reducing absorption as increasing voltage is applied. This allows optical modulators and switches to be readily constructed, as discussed in the following section.

2.2.2 Functionality

To utilise the benefits of quantum wells for applications, a p-i-n diode is conventionally constructed with multiple quantum wells (MQW) in the intrinsic (i) region. The number of quantum wells determines the total absorption. Operating under reverse bias conditions, the diode acts as a linear photodetector with low leakage current.

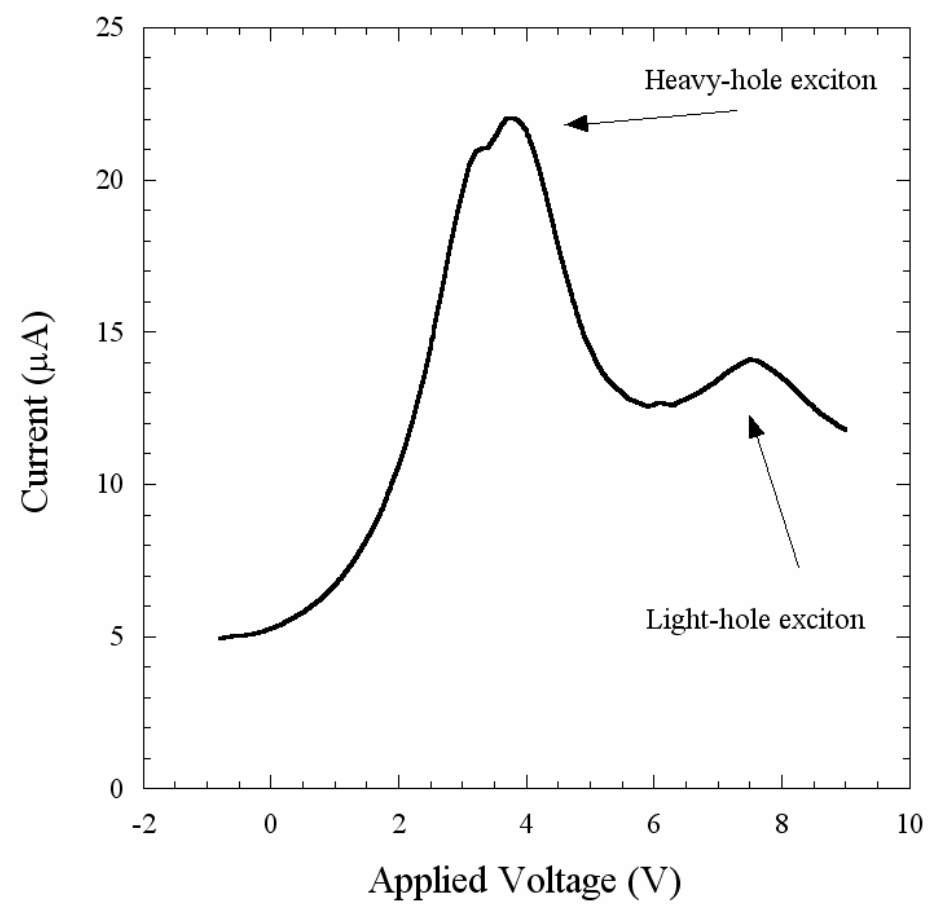

Figure 2.17: Current-Voltage plot of a MQW diode with applied light. The heavy-hole and light hole exciton peaks are labelled.

Provided the diode is maintained below the reverse bias breakdown threshold, the applied voltage can be widely varied to take advantage of QCSE without significantly increasing the leakage current. A representative current-voltage plot is given in Fig. 2.17 with 40 μW of incident light at a wavelength of 850 nm. With light applied at a longer wavelength (850 nm) than the lowest interband transition (844 nm in Fig. 2.16), the exciton enhanced heavy-hole and light hole interband transitions are scanned through resonance as the applied voltage is increased in magnitude. Figure 2.17 shows the large absorption peaks attributable to the excitons.

When a biased MQW device is placed in an electrical circuit with another element, a self-electro-optic effect device (SEED) is formed[26]. Feedback is created as MQW devices act as photodetectors and as voltage controlled modulators. As an example, consider a MQW device in series with a resistor and a voltage source.

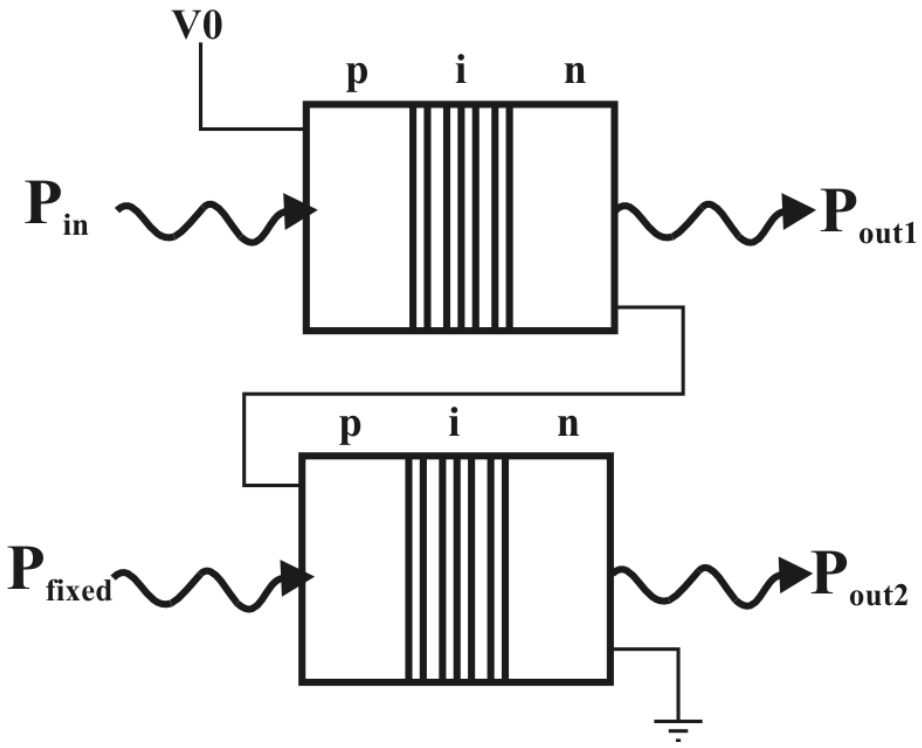

Figure 2.18: Schematic of the circuit used to construct a symmetric SEED (S-SEED), showing the voltage source V_0 and two MQW devices.

The current passing through the resistor, and hence voltage across it, is controlled by the optical power applied to the MQW device. When the applied power is altered, so too is the resistor voltage. As the elements are in electrical series, the voltage across the MQW device must change, altering the MQW device absorption and optical output. Hence feedback is created between the optical input and output of the SEED. The sign of the feedback can be negative, forming a self-linearised modulator[35], or the negative differential resistance of Fig. 2.17 can be exploited to create positive feedback and a bistable optical switch[36]. These two operating regimes are discussed further in Chapters 3 and 6. MQW diodes have been combined with resistors[28], transistors[37] and diodes[35] to form SEEDs, but this work concentrates on SEEDs formed with photodiodes[38] and a pair of MQWs, termed a symmetric SEED (S-SEED)[36] shown in Fig. 2.18.

The following chapters use SEEDs throughout to construct comparator and subtractor elements of the oversampled photonic A/Ds.

Chapter 3

Model Development and Verification

The proposed photonic A/D design uses a 1-bit comparator consisting of two SEEDs in series (an S-SEED) operating in bistable mode. In this chapter, a model is developed to simulate accurately S-SEED based circuits. Previous approaches to modelling S-SEED switching include those of [35] and [39]. In [35] a linear approximation to the differential equation of the S-SEED's equivalent circuit was used to derive an equation for the switching time. In [39] a piecewise linear approximation to the experimental responsivity curve of a MQW $p-i-n$ diode was used to investigate switching behaviour. However, neither of these approaches was accurate enough to include effects such as critical slowing down.

As a consequence of bistability, the comparator will exhibit critical slowing down [35]. The phenomenon of critical slowing down causes the switching time to tend toward infinity when the bistable system is close to a transition, or critical point. This will have a deleterious effect on the A/D operation, because an A/D accepts a continuous range of inputs. For inputs close to the transition points, critical slowing down will limit the response time of the comparator and cause output errors. Therefore, it is important to understand the variation of the switching time for values of parameters close to the critical ones in order to model the A/D accurately and predict the parameters that minimise the effect.

In our effort to model S-SEED switching as accurately as possible, we include

the measured device parameters of responsivity, dark current and capacitance in a numerical solution of the full nonlinear circuit equation. To validate the simulation, we compare the results from a clocked switching experiment, with the output of the simulation. The relevance of this comparison to a comparator is discussed in Section 3.4. We subsequently use the simulation to determine the parameters necessary to switch the S-SEED close to the critical points. The testing of the prediction with an S-SEED switching experiment reveals critical slowing down. We demonstrate a power law dependence for the switching time near a critical point. The simulation is then used to minimise critical slowing down and determine potential functions which aid in the understanding of the effect.

The accuracy of the simulation is further demonstrated by the prediction of the parameters necessary to realise tri-state switching. A third stable state is attributable to an anticrossing transition, the origins of which are discussed in Section 3.6. The results of a clocked switching experiment are subsequently compared to simulated results for a tristable S-SEED.

In this chapter we first describe the optical switching process in Section 3.1, where attention is paid to the parameters affecting switching and the necessary switching conditions. Section 3.3 provides a description of the computer simulation and details of the experimental data that was used. The experiment used to verify the simulation is discussed in Section 3.4. Section 3.5 presents experimental and simulated results for the phenomenon of critical slowing down. The simulation is used to predict the parameters required to demonstrate multi-state clocked switching utilising an anticrossing transition in section 3.6. Finally, conclusions are given in Section 3.7.

3.1 Description of Optical Switching

The comparator is formed by exploiting the bistable switching characteristics of two SEEDs connected in series (see Fig. 3.1 for an S-SEED schematic). To understand bistable operation, consider the experimental IV characteristics of two multiple quantum well $p-i-n$ diodes forming an S-SEED, with optical inputs P_{fixed} and

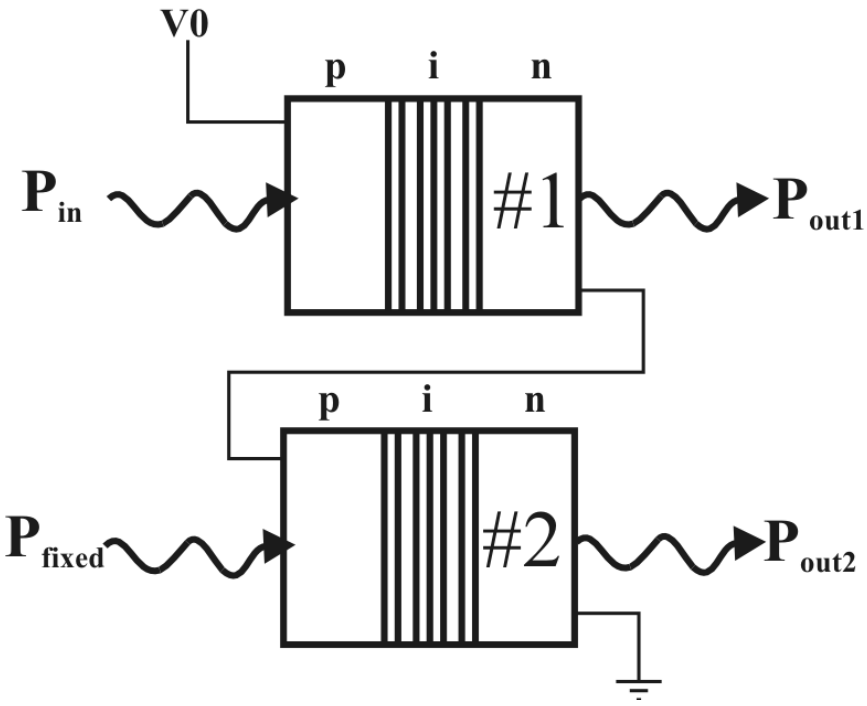

Figure 3.1: Schematic of an S-SEED showing the voltage source, V_0; the optical inputs, P_{in} and P_{fixed} and the optical outputs, P_{out1} and P_{out2} .

P_{in} that set the voltage and transmission state of the S-SEED, and applied bias V_0, as depicted in Fig. 3.2.

In Fig. 3.2 the loadline for SEED #2 (dashed line) is plotted for an applied bias of V and incident optical power $P_{fixed} = 40\,\mu$W. The loadline for SEED #1 (solid line) with voltage $V_0 - V$ is plotted for three different values of the input power P_{in}. The IV curves acquire their shape from QCSE, which causes the absorption peak to red shift as a function of applied electric field. Consider first the case of $P_{in} = 62\,\mu$W, where the curves of the two devices intersect at the point labelled E in Fig. 3.2. Since the two diodes are in series, the same current must pass through each. Therefore, the intersection gives the voltage solution for the S-SEED circuit. For the case of $P_{in} = 40\,\mu\mathrm{W} = P_{fixed}$, three intersections occur at the points labelled A, B and C. Following an analysis of stability[35], the solution labelled B is found to be unstable, while the other two are stable. It is bistability, the existence of two distinct stable solutions to the circuit, that is exploited in the creation of an optical switch. Finally, consider the case of $P_{in} = 29\,\mu$W where intersections occur

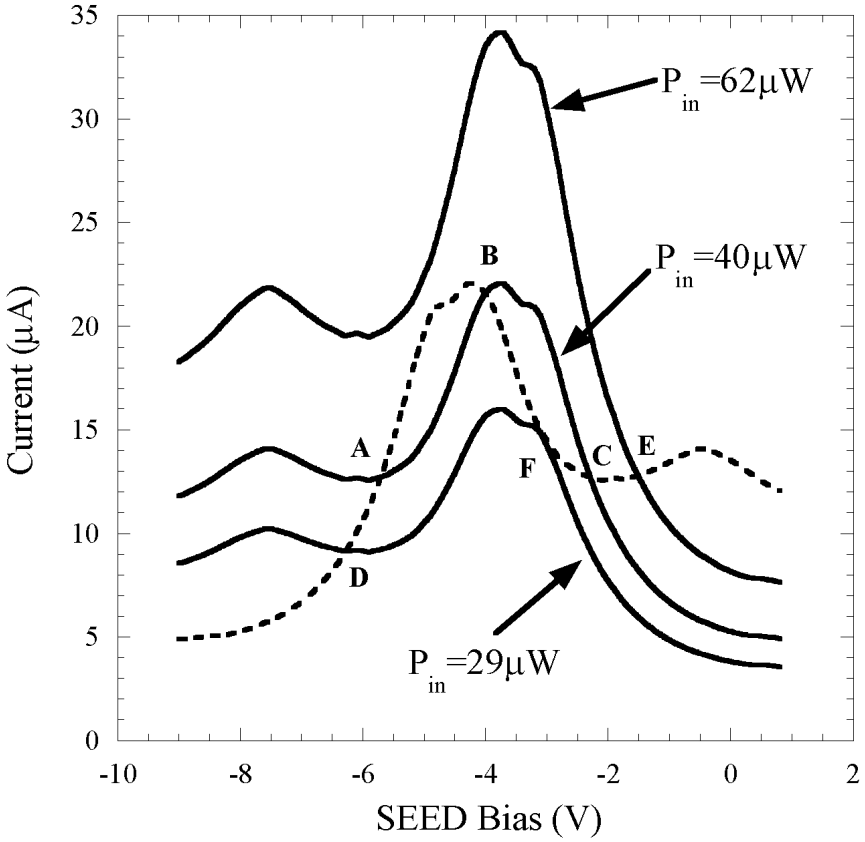

Figure 3.2: Loadline plot which consists of IV curves for each of the devices in an S-SEED with $V_0 = -8V$. The loadline is shown for three different values of P_{in} (solid) input into the top device of Fig. 3.1 and one value of P_{fixed} (dashed) input into the lower device of Fig. 3.1. The measurement of the IV curves is described in detail in Section 3.2.

at points D and F. The solution at point D is stable and in a region where only a single solution occurs, as was the case with point E. Whereas at point F, the two curves touch tangentially as the stable and unstable solutions, C and B, converge. This implies that point F is on the edge of stability and it is termed a critical point, and marks the edge of the hysteresis region. By plotting the solution V as a function of the input power P_{in}/P_{fixed}, as done in Fig. 3.3, the ranges of each of the two stable solutions can be seen. The overlap of the two ranges results in hysteresis of width Δ, and at the limits of the overlap the critical points exist, labelled $P_{\theta L}$ and $P_{\theta H}$. Due to the reciprocal relationship of the switching points,

$$P_{\theta H} = \frac{1}{P_{\theta L}}. \tag{3.1}$$

Combining (3.1) with the definition of Δ

$$\Delta = P_{\theta H} - P_{\theta L}, \tag{3.2}$$

and the constraints

$$P_{\theta H} > 0,\ P_{\theta L} \geq 0 \tag{3.3}$$

allow the switching points to be expressed as a function of Δ.That is,

$$P_{\theta H} = \frac{1}{2}(\Delta + \sqrt{\Delta^2 + 4}) \tag{3.4}$$

and

$$P_{\theta L} = \frac{1}{2}(-\Delta + \sqrt{\Delta^2 + 4}). \tag{3.5}$$

Therefore, to switch the S-SEED from $|V_{low}|$ to $|V_{high}|$ the input must be such that $P_{in}/P_{fixed} > \frac{1}{2}(\Delta + \sqrt{\Delta^2 + 4})$ and to switch in the opposite direction requires $P_{in}/P_{fixed} < \frac{1}{2}(-\Delta + \sqrt{\Delta^2 + 4})$.

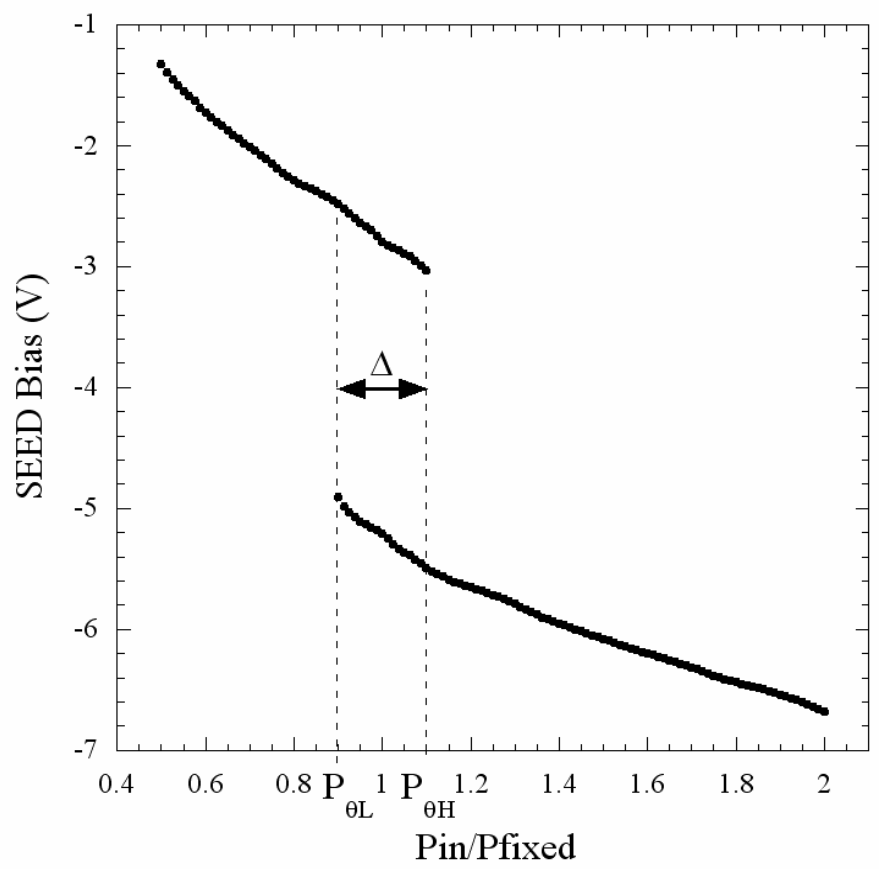

Figure 3.3: Simulated plot of the solution of the circuit, V, against the input power P_{in}/P_{fixed} for $V_0 = -8V$, depicting hysteresis of width Δ and limits $P_{\theta L}$ and $P_{\theta H}$.

3.2 Experiment Development

As will be described in detail Section 3.3, the numerical device simulation used in this thesis relies on measured device parameters. Therefore, accurate measurement with minimal noise is a crucial component to produce reliable modelling. To further motivate the need for capture of data free from amplitude fluctuations, consider the loadline of Fig. 3.2. If the loadline had small random variation, the analysis of the loadline performed in the previous section would falsely predict additional stable solutions. Therefore to obtain data suitable for the model, device dark current, capacitance and responsivity were required to be measured with peak-to-peak fluctuations of less than 2%. This goal was easily achieved for the dark current and capacitance measurements, as our requirement was well within the capability of the respective instruments used for the characterisation (Keithley K236 source meter and HP 4279A Capacitance-Voltage meter). However, for the responsivity characterisation, which required measurement of device current and applied optical power as wavelength and voltage were varied, significant effort was required to reach the goal of $< 1\%$ noise in the experiment. This section will document the development of the experimental setup used to accomplish this objective.

In our laboratory the laser was coupled into a fibre optic cable, to mitigate the effect of beam wander, by transforming beam wander into power fluctuations which could be removed with the noise eater. The fibre coupling also enabled safe and convenient transport of the light to the device characterisation experiment. Correct optical setup of the fibre coupling was very important, as mitigating backreflections that cause instability in the laser was the most important factor in achieving low laser noise. A schematic of the setup is given in Fig. 3.4.

Mirrors M1 and M2 in Fig. 3.4 were used to adjust the direction and height of the beam, and with the aid of the two alignment irises, ensure that the beam was parallel to the optical bench. A wedge was used to sample a portion of the beam for wavelength measurement by a wavemeter (Burleigh WA1000). Because the device characterisation experiment required the scanning of the wavelength over a large range (up to 120 nm), a second wedge was used to compensate beam deviation due to dispersion. The next component in the chain was a microscope objective lens

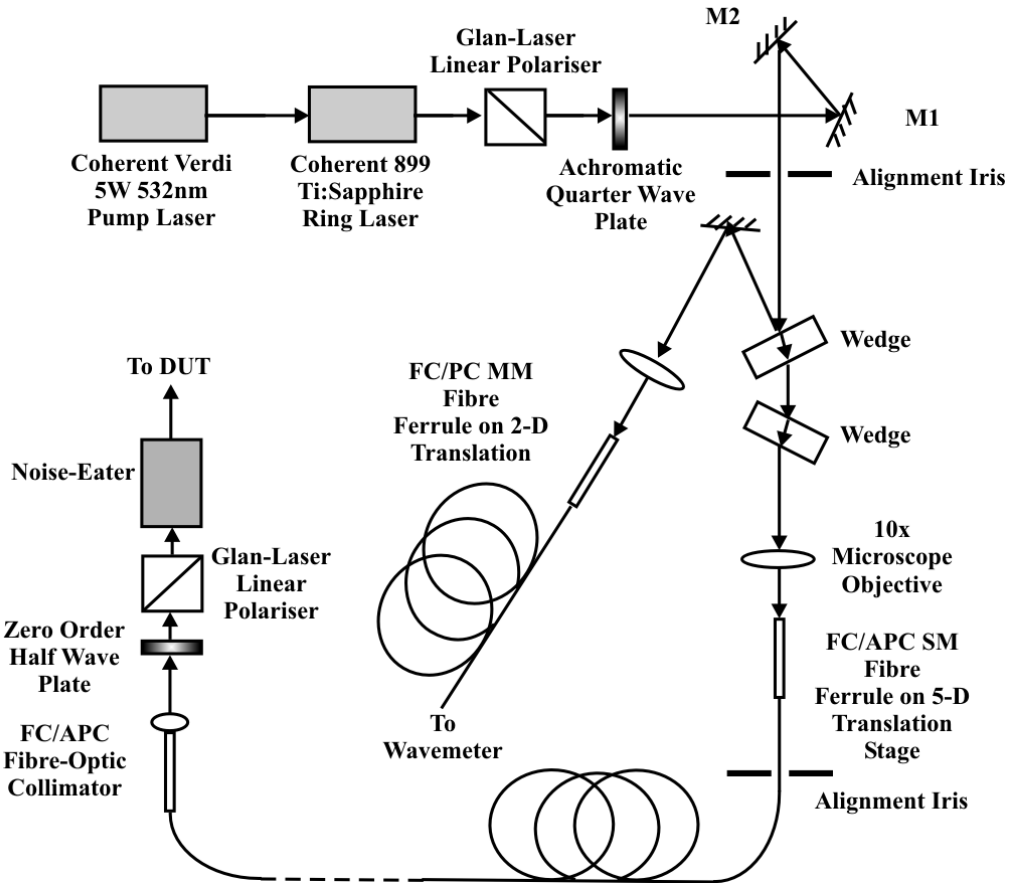

Figure 3.4: Schematic of the optical layout used to couple the laser into an optical fibre and output the light from the fibre to the device under test (DUT).

with a magnification factor of 10. The lens coupled the light into an optical fibre which supported only a single optical mode over the entire wavelength scan range used (780 nm to 900 nm). The maximum fibre coupling efficiency achieved was approximately 50%, therefore a significant amount of light was reflected back into the laser cavity. Since we did not have an optical isolator with sufficiently high damage threshold available, to minimise the effect of the backreflection, an achromatic quarter waveplate and Glan-Laser polariser was employed. This isolated the laser by transforming the backreflected circularly polarised light into linear polarised light rotated through 90°, causing it to be rejected at the linear polariser. Also important for low noise operation was the daily cleaning and alignment of the Coherent 899 ring laser's mirrors.

At the output end of the fibre a Cambridge Research and Instrumentation laser power controller (noise-eater) was used to remove small power fluctuations. The noise eater uses a liquid crystal panel and a linear polariser to modulate the light and maintain constant output power. Therefore it required the input light to be linearly polarised. It is noteworthy that MQW modulators have also been demonstrated to perform the same noise cancelling functions [40], [41] and they do not require polarised light. A zero order half wave plate and a linear polariser were used to supply the correct polarisation. Since the light exiting the fibre was circularly polarised, a loss of optical power was suffered in this process, but we did not have available a second achromatic quarter wave plate. Nevertheless, the setup as described minimised the laser power fluctuations, allowing data to be gathered with an indicative measured relative intensity noise (RIN) of 2.9%, where RIN is defined as the standard deviation, divided by the mean. That is,

$$RIN = \frac{\sqrt{\sum_i (x_i - \overline{x})^2}}{\sum_i x_i},$$

where $\overline{x}$ refers to the mean. The value of 2.9% RIN is derived from data presented in Fig, 4.10 and gives a typical value of laser noise. Due to day-to-day variations in laser alignment and laser cleanliness, the laser noise varied above and below the value of 2.9%.

Prior to the above solution, other techniques were attempted to minimise the

backreflection. They included misalignment of the fibre to direct the backreflected light away from the laser, but the coupling loss imparted was too great. The noise eater was also used before the implementation of the quarter wave plate, but it did not have sufficient dynamic range to remove the large amplitude noise. Finally, a diffuser was used in front of the device to be measured, to act like an integrating sphere, but this made the power calibration very difficult.

The optical setup used to characterise the device under test is given in Fig. 3.5. Light from the noise eater is incident on the SEED after passing through a variable neutral density (ND) filter and three beamsplitters. The ND filter gives fine control of the optical power and the first beamsplitter samples the power for a power meter. Sampling of the laser power at the same rate as the photocurrent, minimised the impact of the remaining laser noise on the measured responsivity data. To aid alignment of the laser onto the device under test, two pellicle beamsplitters are employed to direct a lamp and a CCD camera onto the SEED.

After the development of the optical setup, it was necessary to concentrate on the electrical setup. Automating the device characterisation process was important to enable practical collection of high resolution data. The following instruments were connected to a computer via the General Purpose Instrumentation Bus (GPIB): Keithley K236 source meter, HP 4279A Capacitance-Voltage meter, Newport 2832C power meter, Burleigh WA1000 wavemeter and a Newport ESP 300 stepper controller with a Newport 850B actuator to control the wavelength of the Coherent 899 Ti:Sapphire laser. All the instruments used, except for the C-V meter, were able to measure to an accuracy of at least $\pm 0.05\%$, which was more than able to provide data suitable for the model. The C-V meter was not able to achieve its specified accuracy, because with the MQW device mounted in the experiment, we were limited to the use of a two-point measurement, instead of the more accurate four-point probe. This limited the accuracy of the capacitance measurement to approximately 1%. However, the error in the measurement of responsivity ($S = \frac{I}{P}$) due to the instruments is 0.07%. This error is negligible compared to the amplitude noise of the laser. For example, the resulting amplitude noise of the measured responsivity of Fig. 3.12 was determined to be 0.4%. This value was calculated using a measure

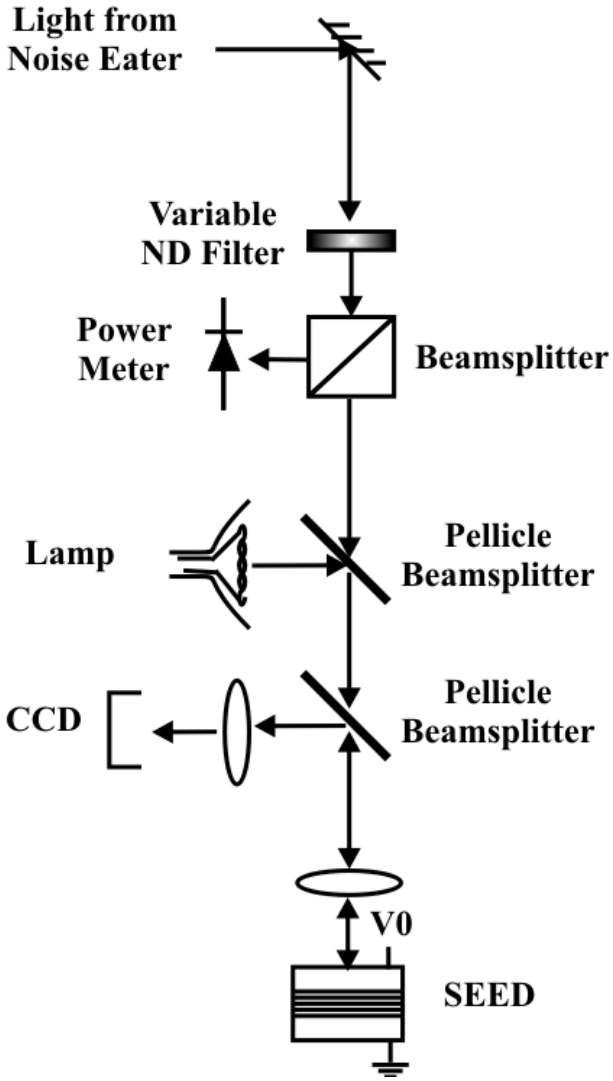

Figure 3.5: Optical setup to characterise a SEED. A variable Neautral Density (ND) filter is used to gain fine power control, and a lamp and CCD are used to aid alignment of the laser onto the device under test.

of the point to point variation, as is described in detail in Section 3.3, and is lower than the measured laser RIN due to the normalisation with the measured power.

A schematic of the equipment connections used to perform the measurement is given in Fig. 3.6. Using Visual Basic 6.0, programs were written to perform

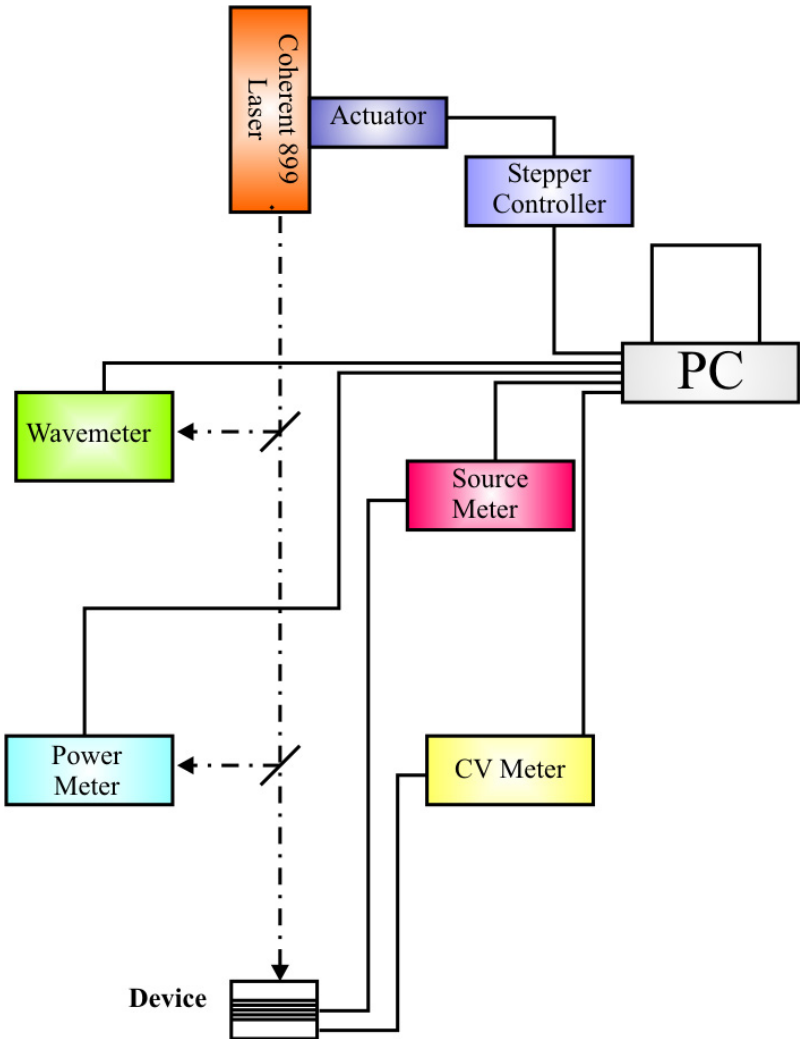

Figure 3.6: Schematic of the connections of all the instruments used in performing the MQW device characterisation. A solid line represents an electrical connection, and the dot-dash line represents the laser beam.

the following measurements and tasks: measure responsivity as a function of voltage and wavelength $S(V, \lambda)$, measure reflectivity as a function of voltage and wavelength $R(V, \lambda)$, measure dark current as a function of voltage $I_d(V)$, measure capacitance as a function of voltage $C(V)$, measure photocurrent as a function of voltage $I(V)$,

set the wavelength of the laser and read voltage ($V(t)$) data from the Tektronix TDS520 oscilloscope. A screen capture of the window used to select which action to perform is given in Fig. 3.7.

Clicking on the button labelled responsivity in Fig. 3.7 activated the program to measure device responsivity as a function of wavelength and applied voltage, causing the interface of Fig. 3.8 to appear. This program allowed the user to input a voltage and wavelength range over which to measure responsivity. For each of these ranges, the user was also asked to input the number of steps to perform the measurement in. The program stepped the laser wavelength incident on the MQW $p-i-n$ diode device in the calculated increment and at each value of λ, the supply voltage was ramped through the specified voltage range. The current was recorded at each step and divided by the incident power on the device to give responsivity. Also recorded in the file for each wavelength step was the incident power, wavelength, time, and delay as input from Fig. 3.8.

To achieve a correctly calibrated value of responsivity, the following procedure was followed

1. The light on the device and power meter was initially blocked to allow the cancellation of the power meter offset to be performed.

2. The light block was removed and the power at the device for the first wavelength step was measured with a second power meter placed directly in front of the device to give P_{actual}.

3. The power measured in step 2 (P_{actual}) was input into the responsivity measuring program to allow calculation of the calibration factor between the power measured by the power meter ($P_{measured}$) shown in Fig. 3.6 and the real power at the device. The calibration factor is calculated by

$$Calibration = \frac{P_{actual}}{P_{measured}}. \tag{3.6}$$

It was assumed that the optical loss of the elements between the power meter and device was constant over the wavelength range of interest. Therefore, the

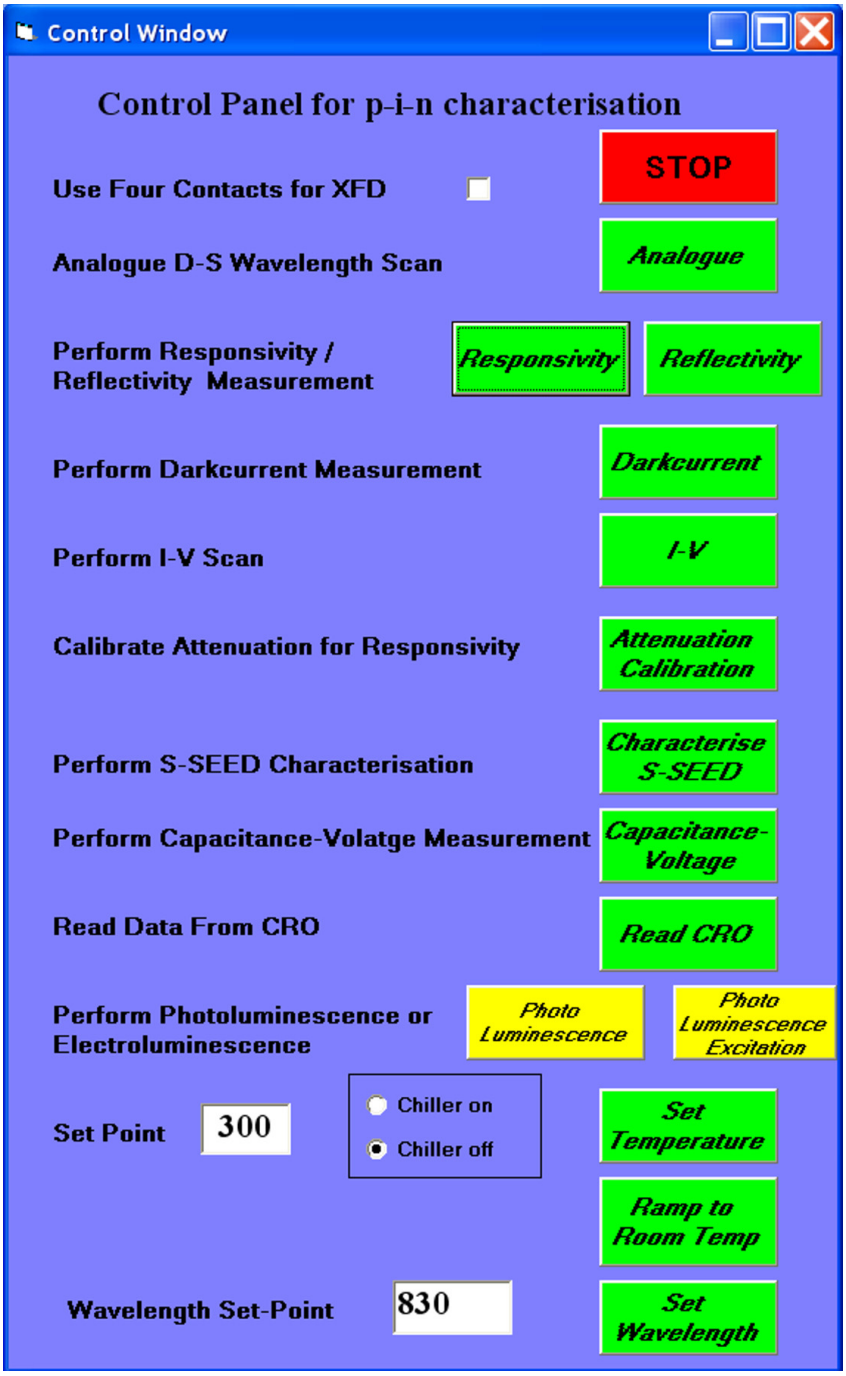

Figure 3.7: Screen capture of the window used to select the program to perform the desired action.

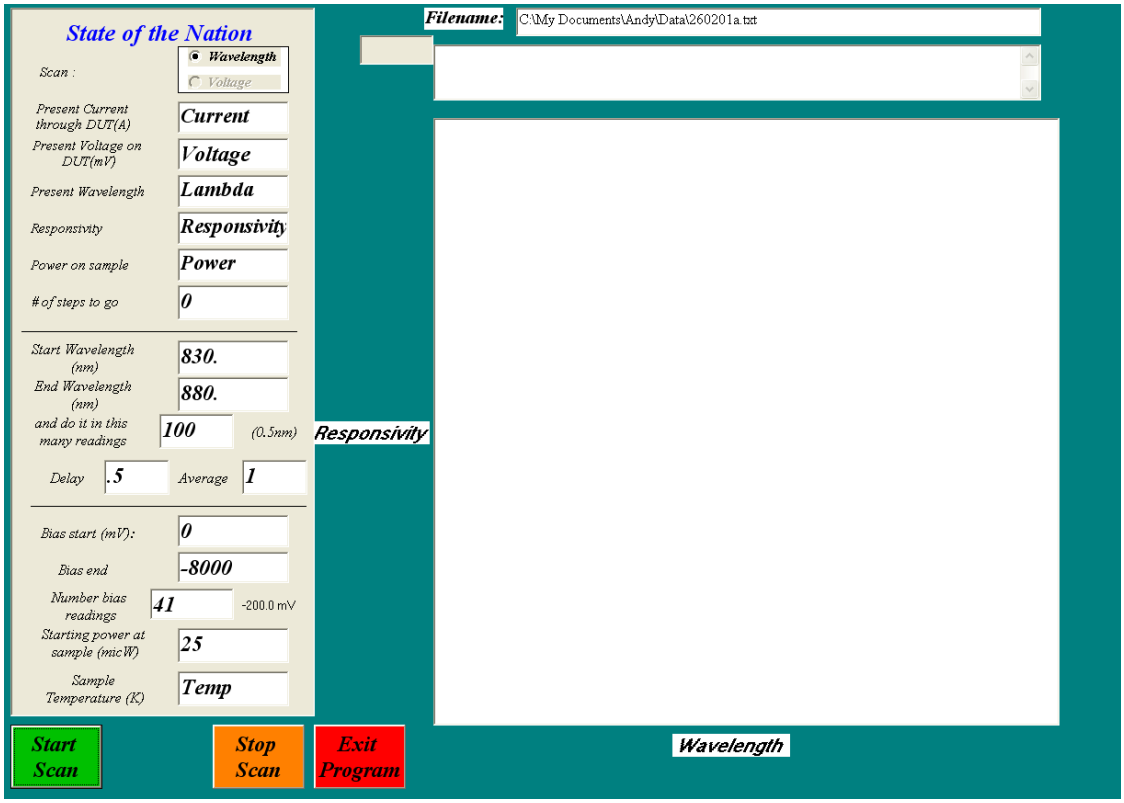

Figure 3.8: Screen capture of the interface used to control the program for measuring device responsivity as a function of wavelength and voltage. Text boxes are given to input the wavelength and voltage ranges, delay between voltage changes, number of measurements to average, the number of steps and power calibration. Also displayed are the measured current, voltage, responsivity, power and wavelength.

calibration factor calculated for the first wavelength step was valid over the whole wavelength range.

4. Finally dark current (which includes the diode characteristic I-V curve) was measured using the associated program, and using *Mathematica* the data files were read into the computer and dark current was subtracted from the responsivity. This allowed the photocurrent (I_{photo}) to be written as $I_{photo}(V, P, \lambda) = P\ S(V, \lambda)$, where S is responsivity. Note that the measured responsivity is not corrected for the Fresnel reflection from the front of the device. This is important to achieve correct modelling of the Fabry-Perot microcavity devices, as will be seen in Chapter 5.

An example of measured responsivity data will be given in the following section.

3.3 Simulation Method

To provide a better understanding of the S-SEED switching behaviour and to be able to predict the parameters necessary for an experiment, a computer simulation was developed. The simulation was based on the equivalent circuit model shown in Fig. 3.9, similar to those used in [39] and [42].

The model represents the $p - i - n$ diode as a current source dependent upon voltage, optical power and optical wavelength, $I_{photo}(V, P, \lambda)$. A voltage dependent capacitor, $C(V)$ and diode dark current, $I_d(V)$ are added in parallel. We have found that the diodes can become forward biased in an S-SEED, making the dark current an important component of the model.

Given the applied bias V_0 and optical inputs P_{in} and P_{fixed} to the S-SEED as depicted in Fig. 3.1, the application of Kirchoff's current law to the circuit shown in Fig. 3.9 yields the differential equation (3.7). The total current is defined in (3.8) and it is assumed that the photocurrent increases linearly with applied power (i.e. $I_{photo}(V, P, \lambda) = P\ S(V, \lambda)$, where S is responsivity).

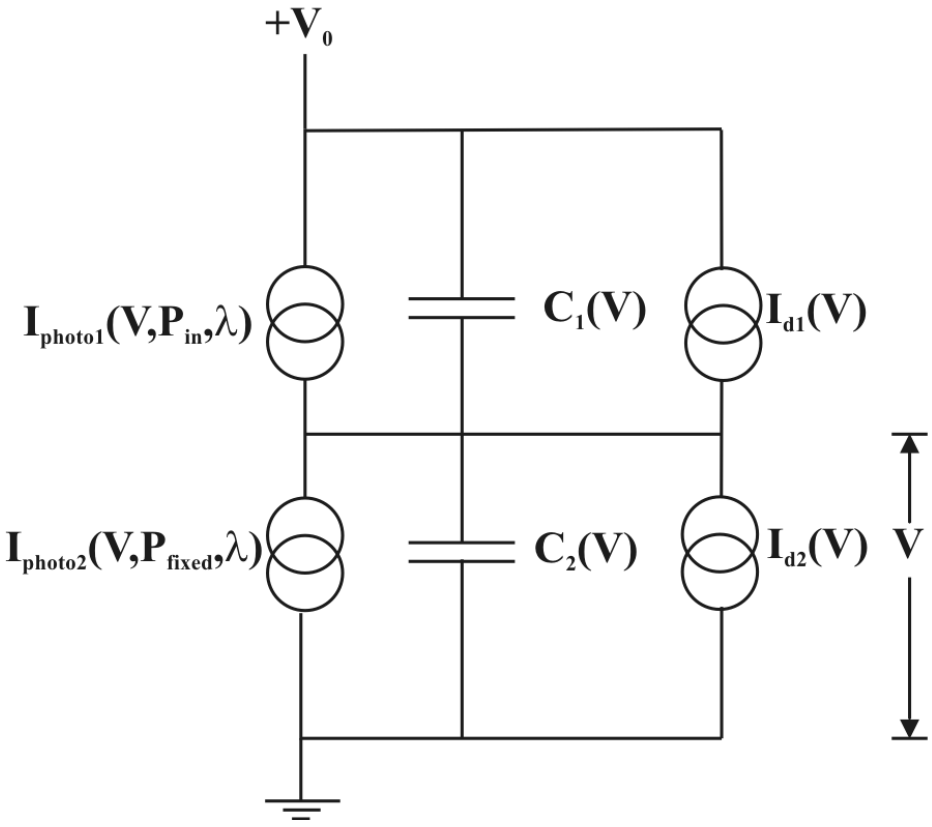

Figure 3.9: Equivalent circuit model of an S-SEED. $I_{photoi}(V, P, \lambda)$ represents the voltage and wavelength dependent photocurrent, $C(V)$ the voltage dependent capacitance and $I_d(V)$ represents the dark current of the diode.

$$\frac{dV}{dt} = \frac{I_{total}(V,\lambda)}{C_1(V_0 - V) + C_2(V)} \tag{3.7}$$

where

$$\begin{aligned} I_{total}(V,\lambda) &= P_{in}S(V_0 - V,\lambda) - I_{d2}(V) \\ &\quad -P_{fixed}S(V,\lambda) + I_{d1}(V_0 - V). \end{aligned}$$

Where our simulation departs from those previously published is in the use of experimental data for $S(V,\lambda)$, $C(V)$ and $I_d(V)$. The results are presented as a function of applied voltage in Fig. 3.10 and Fig. 3.11 for the dark current and capacitance, respectively.

The error in the simulated results due to measurement error can be calculated by simplifying the error in I_{total} to

$$\frac{\Delta I_{total}}{I_{total}} = 2\frac{\Delta S}{S} + 2\frac{\Delta P}{P} + \frac{\Delta I_d}{I_d} \tag{3.8}$$

and the total error in the capacitance to

$$\frac{\Delta C_{total}}{C_{total}} = 2\frac{\Delta C}{C}. \tag{3.9}$$

Therefore the total measurement error of (3.7) is given by

$$\sqrt{\left(\frac{\Delta I_{total}}{I_{total}}\right)^2 + \left(\frac{\Delta C_{total}}{C_{total}}\right)^2}. \tag{3.10}$$

For the measurement errors given in the previous section of $\frac{\Delta S}{S} = 0.4\%$, $\frac{\Delta P}{P} = 0.05\%$, $\frac{\Delta C}{C} = 1\%$ and $\frac{\Delta I_d}{I_d} = 0.05\%$, the total error in the simulation is 2.2%. The error is greater in the simulation than in the experiment predominantly due to the error in the capacitance measurement.

The measured responsivity as a function of wavelength and applied bias is shown in Fig. 3.12, revealing the heavy hole (larger peak) and light hole exciton peaks. Figure 3.12 shows how the QCSE reduces the magnitude and red shifts the wave-

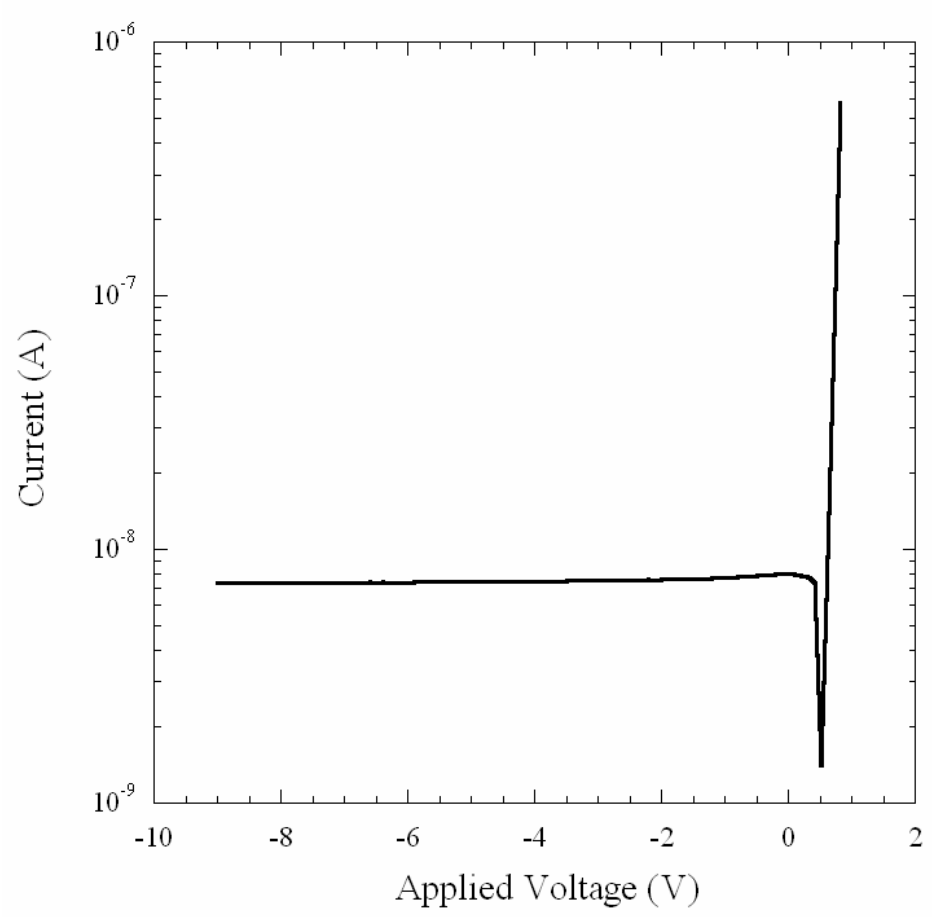

Figure 3.10: Measured diode darkcurrent, on a log scale, as a function of the applied voltage. The error in the measurement is 0.05%.

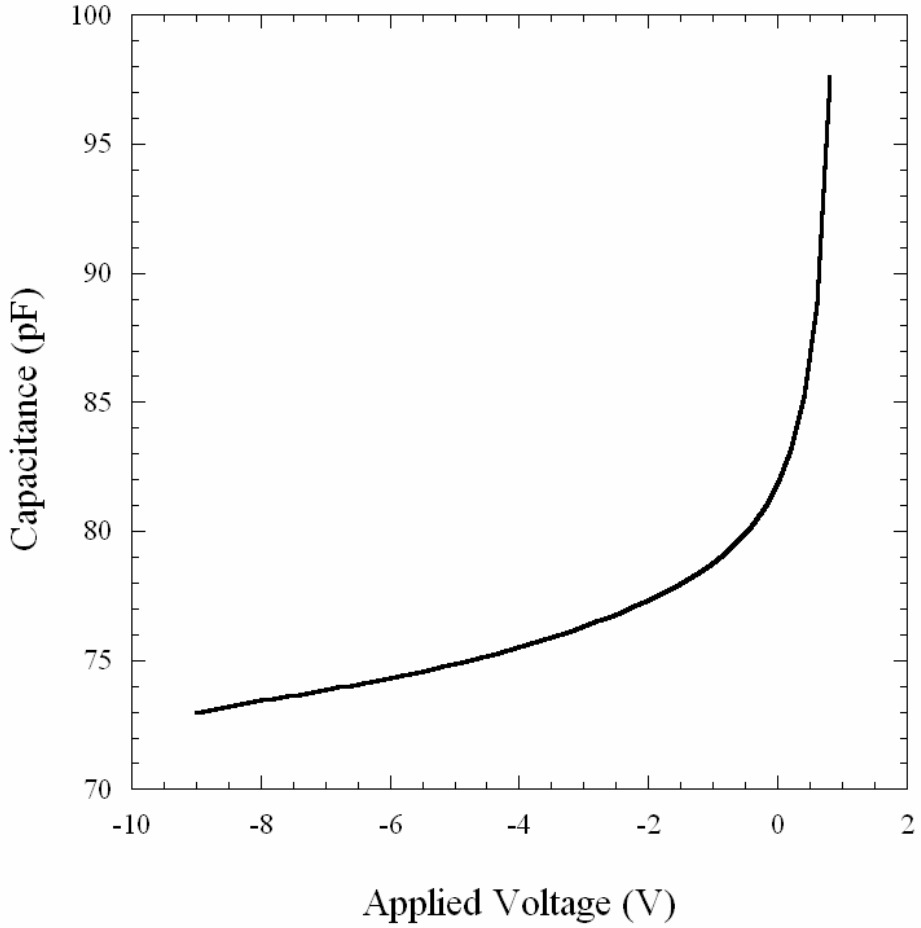

Figure 3.11: Measured diode capacitance as a function of applied voltage. The error in the measurement is 1%.

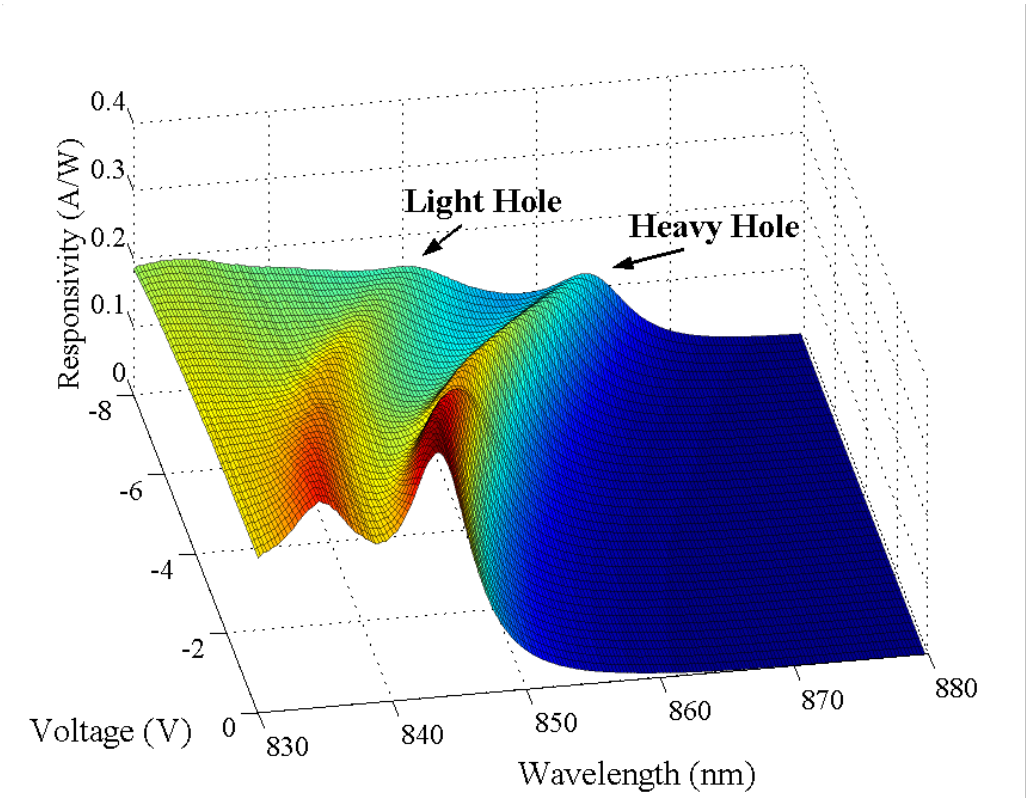

Figure 3.12: Measured responsivity in A/W as a function of wavelength and applied bias. The amplitude noise is 0.4%.

length of the excitons as the applied bias is increased. Figure 3.12 also demonstrates that the responsivity data measured with the experiment described in Section 3.2 has very low amplitude noise, which was measured to be 0.4% using a curve fitting package called *TableCurve2D*. The noise measurement was made by creating a cubic polynomial interpolation for each data point, using the two points to the left and the two to the right of the point under analysis. The difference between the interpolated and data values was used to generate a measure of the amplitude noise present.

To simulate the time dependent behaviour of the S-SEED it was necessary to solve (3.7) for $V(t)$. In order to represent our experimental data as accurately as possible, the data was linearly interpolated within the *Mathematica* environment to form what is termed an *Interpolating Function*. A numerical differential equation solving routine was applied, which implements Adam's or Gear methods, giving $V(t)$.

Results from the simulations are presented in the next section.

3.4 Results

A clocked switching experiment was performed to confirm the accuracy of the simulation. In the clocked switching process, two different low power beams are incident on the S-SEED. Depending on the relative power of the two beams, the S-SEED is set into one of two voltage states. Two equal high power beams are then applied to read the state of the S-SEED, without switching the device[35]. Such an experiment is most relevant to the optical A/D as it demonstrates the comparison function [43], where the signal input into the A/D is used as the low power set beam and compared to a reference beam, and in the process configuring the S-SEED into one of two bistable states. A high power clock is then used to read out the state of the S-SEED to determine the result of the comparison operation.

All the parameters affecting the switching process are included in the simulation, as demonstrated by excellent agreement between simulation and experiment presented in the following section.

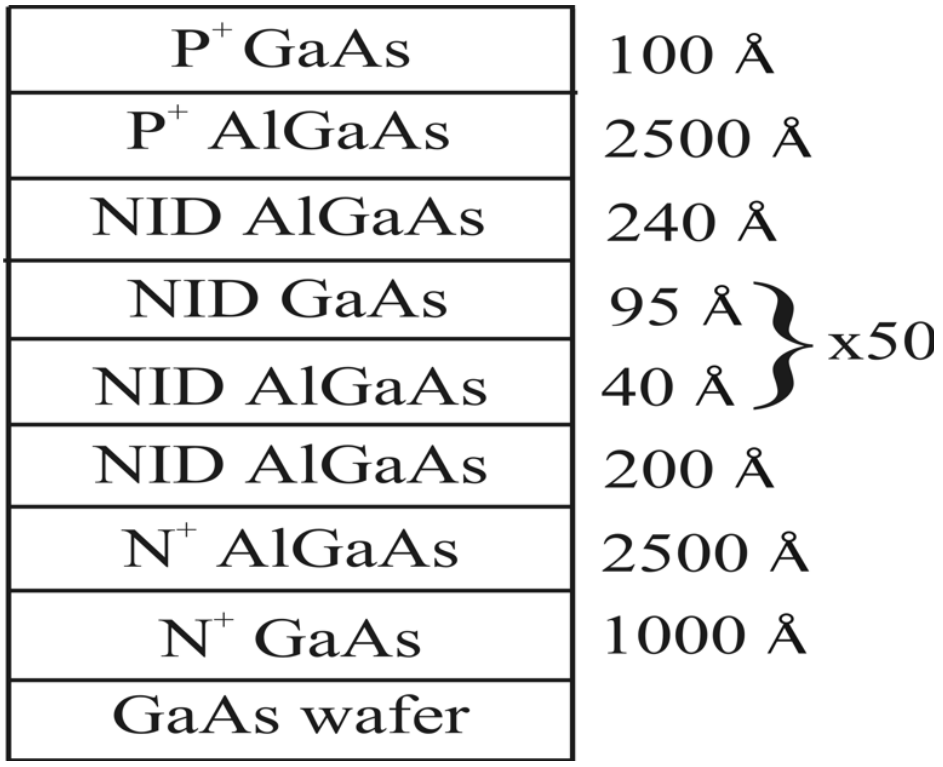

Figure 3.13: Schematic of the MBE grown $p-i-n$ structure that was produced at Stanford University. The Aluminium mole fraction of the AlGaAs layers is 31%. The active region contains 50 quantum wells with 95Å GaAs wells and 40Å AlGaAs barriers that are not intentionally doped (NID). This growth is referred to as wafer 436 in Appendic C.

3.4.1 Experimental Setup

The MBE grown multiple quantum well $p-i-n$ diodes that constitute our S-SEED were designed with 50 $Al_{0.31}Ga_{0.69}As/GaAs$ quantum wells and manufactured at Stanford University. To produce devices, $500\mu m$ x $500\mu m$ square mesas with ohmic contacts on the p and n doped layers were fabricated. The entire growth structure of the wafer labelled 436 is shown in Fig. 3.13. Since the $GaAs$ substrate absorbs the light transmitted through the quantum wells at the designed wavelength range of operation (830-865 nm), these devices did not produce an optical output. This initial design was chosen to simplify the fabrication process, as creating devices that reflect or transmit light is a challenging fabrication problem. This problem was later addressed in Chapter 5, where reflective devices were subsequently designed and fabricated.

To perform a time dependent experiment to test the simulation, it was important to accurately measure the S-SEED voltage (V of Fig. 3.9) and account for all the experimental influences that are not included in the simulation. Therefore, losses incurred by optical elements in the experiment had to be measured, overhead lights had to be switched off and instrument contributions to the S-SEED electrical circuit had to be minimised and quantified. The experimental setup for the clocked switching experiment is shown in Fig. 3.14, and a photograph of the experiment is presented in Fig. 3.15. The tunable Ti:Sapphire laser was coupled with a Cambridge Research and Instrumentation laser power controller to remove amplitude fluctuations. The beam was split into two, one arm providing the clock beam, while the other supplied lower power signal levels. Polarising beam splitters and half-wave plates were subsequently used to split each beam into P_{in} and P_{fixed} signals incident on each of the SEEDs, and to enable adjustment of the relative powers. Acousto-optic modulators were used to impart the signals on the beams, and were synchronised by locking the clocks of the driving signal generators together in a master/slave configuration. The typical impedance of a SEED is approximately 10 MΩ. Therefore, to measure accurately the voltage across the SEED connected to ground on a Tektronix TDS520 oscilloscope, it was necessary to use an AD620 instrumentation amplifier with an input impedance of 10 GΩ (and bandwidth of 1 MHz). As measured by the CV meter, the measurement equipment contributed 59 pF in parallel with the S-SEED. This additional contribution was included in the simulation.

3.4.2 Comparison of Simulation and Experiment

Experimental and simulated results for the clocked switching experiment are presented in Fig. 3.16. Figure 3.16 (a) plots the optical power applied to the top device, P_{in}, as a function of time with a solid line. The dashed line in Fig. 3.16 (a) represents the optical power applied to the bottom SEED, P_{fixed}. Since pulses of equal power are required to read the state of the S-SEED, P_{in} and P_{fixed} are interleaved with high power clock pulses between the low power values that are used to set the state of the S-SEED. This technique provides time sequential gain[36], as the power

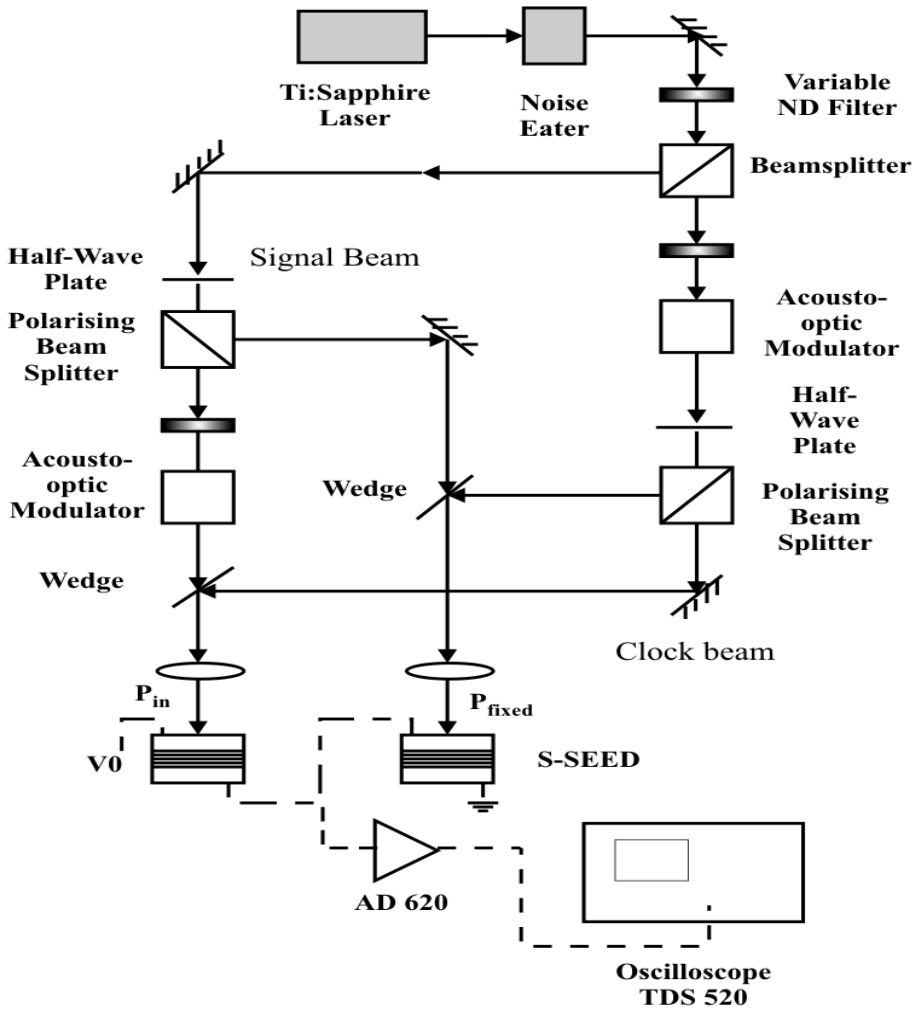

Figure 3.14: Experimental setup for the clocked switching experiment.

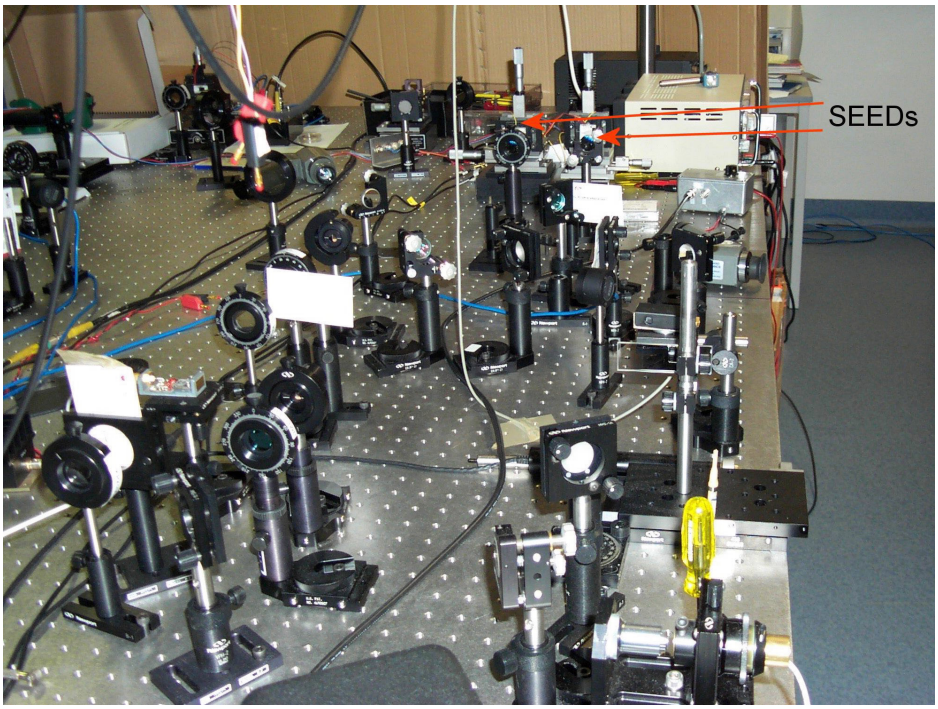

Figure 3.15: Photograph of the experimental setup. The position of the two SEEDs is labelled.

applied for the read-out pulses is greater than the input set pulses. The set and read pulses are labelled in Fig. 3.16 (a). Part (b) of Fig. 3.16 shows the comparison of experimental (dashed with diamonds) and simulated (solid) measurements for the voltage across the bottom SEED (V) as a function of time. The characteristics that are important for an A/D comparator are that the clock output has only two possible values (i.e. 1-bit), and the time sequential gain provides optical gain to overcome losses in the A/D system.

To measure the power levels of Fig. 3.16, the signals were reduced to a frequency of 0.1 Hz, enabling the direct reading of the power meter placed in the beam path. To compensate for power meter drift, the values of P_{in} and P_{fixed} used in the simulation were allowed a 3% window of adjustment. Within this error, very good agreement is seen between experiment and simulation, as evidenced by a calculated mean absolute percentage error of 2.7% between the experimental and simulated results. Not only are the switching levels accurate, but so is the transient behaviour. Therefore, the simple equivalent circuit of Fig. 3.9 has proven sufficient to achieve an accurate

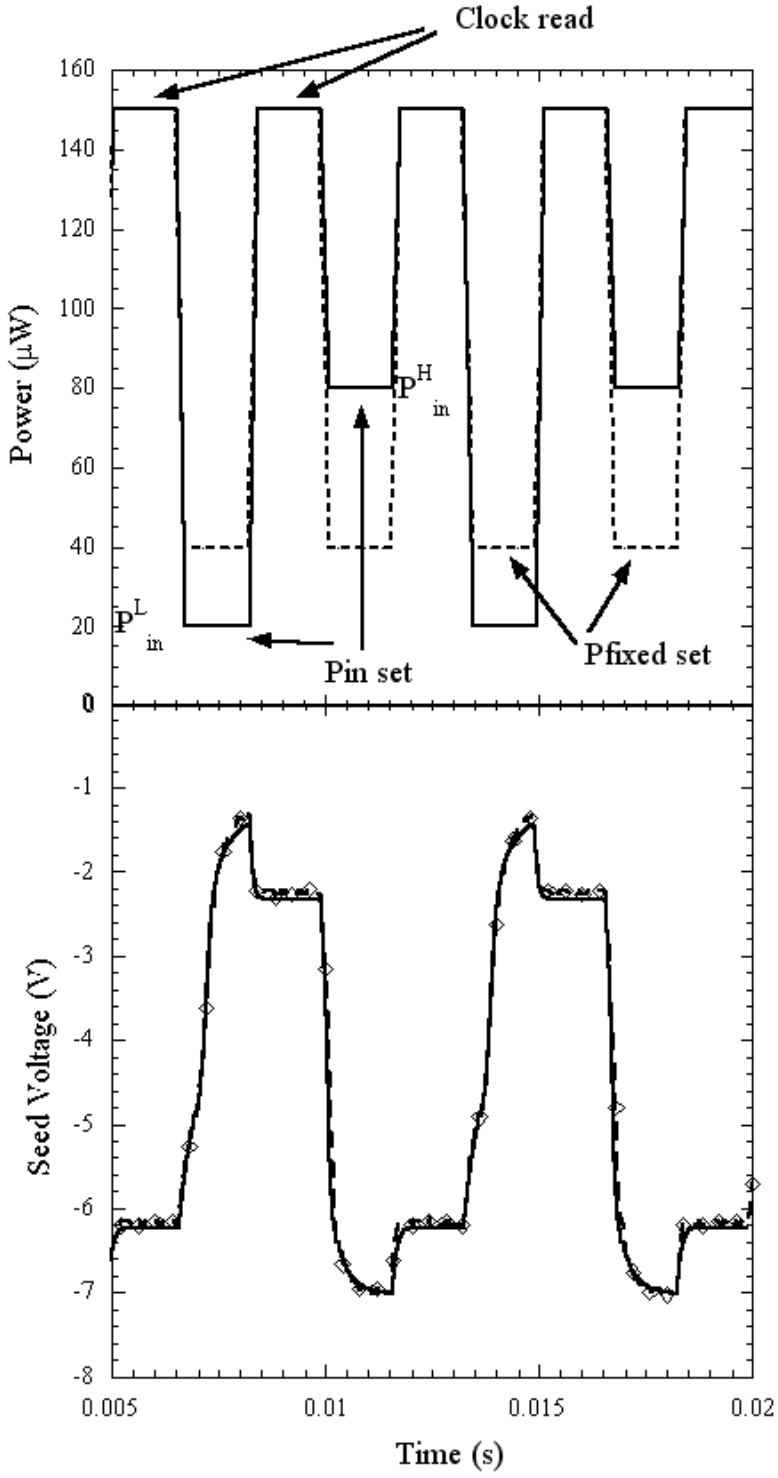

Figure 3.16: (a) Timing diagram for the optical inputs P_{in} (solid line) and P_{fixed} (dashed line) depicting the clock and signal pulses and the high and low values of P_{in} (P_{in}^H and P_{in}^L), as labelled. (b) Comparison of the simulated (solid line) and experimental (dashed line with diamonds) results for V from the clocked switching experiment performed at a wavelength of 850nm. The mean absolute percentage error bewteen the two was was calculated to be 2.7%, which is very close to the expected error between experiment and simulation of 2.6%.

simulation of S-SEED switching. It should be noted that the very slow switching speed is due to the SEED's large device size, and hence large capacitance (nominally 100 pF), and the relatively small difference in power between P_{in} and P_{fixed} of 20 μW [36].

Due to the slow switching speed, it was not necessary to model the effects on the transit time caused by tunnelling of the carriers through the quantum well barriers, since the RC time constant dominates. However, even for much faster devices, others [44] have demonstrated that the RC time constant is the limiting factor in determining the switching speed for devices with thin barrier quantum wells. Therefore, we believe that this simulation technique is useful for accurately modelling higher order structures, such as A/D architectures at significantly greater speeds.

3.5 Critical Slowing Down

As a dynamic system approaches an instability from a stable operating point, a phenomenon known as critical slowing down often occurs, in which the system exhibits an extremely slow return to steady state upon perturbation. In the case of bistable systems, the effect of critical slowing down is to increase the system's switching time near the transition, or critical points [45]. This has implications for the switching speed of the comparator in the optical A/D. Therefore it is important to ensure that this effect is included in our model of S-SEED switching. To understand critical slowing down, consider a system described by

$$\frac{dV}{dt} = Q(V) \tag{3.11}$$

with the fixed point solution at V^*. That is,

$$Q(V^*) = 0. \tag{3.12}$$

To determine the stability of V^* we linearise (3.11) about V^* via a Taylor expansion to first order

$$\frac{dV}{dt} = Q(V) \simeq Q(V^*) + \frac{dQ}{dV}_{V=V^*}(V - V^*). \tag{3.13}$$

Now define $\xi = V - V^*$ and set,

$$\lambda = \frac{dQ}{dV}|_{V=V^*} \tag{3.14}$$

then

$$\frac{d\xi}{dt} = \lambda\xi \tag{3.15}$$

which has the solution

$$\xi(t) = \xi(0)\, e^{\lambda t} \tag{3.16}$$

The parameter λ now determines stability. If $\lambda < 0$ then $\xi(t) \to 0$ as $t \to \infty$ which implies V^* is a stable solution. However, if $\lambda > 0$ then $\xi(t) \to \infty$ as $t \to \infty$ which implies V^* is unstable. Now consider the case $\lambda = 0$. Then $\xi(t) = \xi(0)$ and the system does not progress past its initial condition. From (3.15) we see that the velocity of the system, $\frac{d\xi}{dt}$, tends to 0 for the situation where $\lambda \to 0$, referred to as critical slowing down [45].

3.5.1 Results

To demonstrate the effect of critical slowing down, we performed an experiment similar to that of Section 3.4, with the omission of the clock pulses. By applying different optical powers to the two devices, the S-SEED was switched between two voltage states. By adjusting the power incident on SEED #1 (P_{in}) successively closer to the switching point, the lower voltage state altered to reveal the effect of the

exponent λ approaching zero. The experimental and simulated results are presented in Fig. 3.17 by points and lines, respectively. The value of P_{fixed} was maintained at $100\,\mu$W and the square wave applied to P_{in} varied between $P_{in}^H = 270\,\mu$W and three different values of P_{in}^L, equal to 74, 81 and $83\,\mu$W, as depicted in Fig. 3.17. The mean absolute percentage error was calculated between the experimental and simulated results as 2.4%, 2.4% and 3.9% for the $74, 81$ and $83\,\mu$W cases respectively. See also Fig. 3.16 for a graphical description of P_{in}^H and P_{in}^L. The figure demonstrates that the switching is much slower when P_{in}^L is equal to $83\,\mu$W, as compared to $74\,\mu$W. We can establish that critical slowing down is the cause of the decreasing switching speed by considering the λ parameter as a function of P_{in}^L. However, since the derivative of the interpolated data is only piecewise continuous, we were unable to calculate the behaviour of the λ parameter from the experimental data. To demonstrate qualitatively the behaviour of the λ parameter, we use an approach common in spectroscopy, and fit the responsivity data for a wavelength of 850nm with a sum of Gaussian curves (one for each peak). The resulting analytic expression is given in (3.17).

$$\begin{aligned} S(V) &= \beta_{hh}\, e^{(-0.5\,((V-\sigma_{hh})/\Gamma_{hh})^2)} \\ &\quad + \beta_{lh}\, e^{(-0.5\,((V-\sigma_{lh})/\Gamma_{lh})^2)} + \alpha \end{aligned}$$

Therefore (3.17) models the heavy hole (hh) and light hole (lh) excitonic responses as Gaussian curves, where fitting parameters Γ_i, β_i and σ_i represent the width, strength and position of the excitons and α is an additional parameter to represent the continuum absorption.

To find λ, (3.17) was first used to calculate the steady state solution of (3.7). The solution was substituted into (3.14), yielding the results presented in Fig. 3.18 (a).

Figure 3.18 (a) demonstrates how $\lambda \to 0$ at the critical points, which are identified by the dashed line at the limits of the hysteresis region from the accompanying curve in part (b). Therefore, according to the definition of critical slowing down as discussed in the introduction to this section, the system exhibits a decay time approaching infinity in the vicinity of these critical points. Figure 3.18 (b) also includes

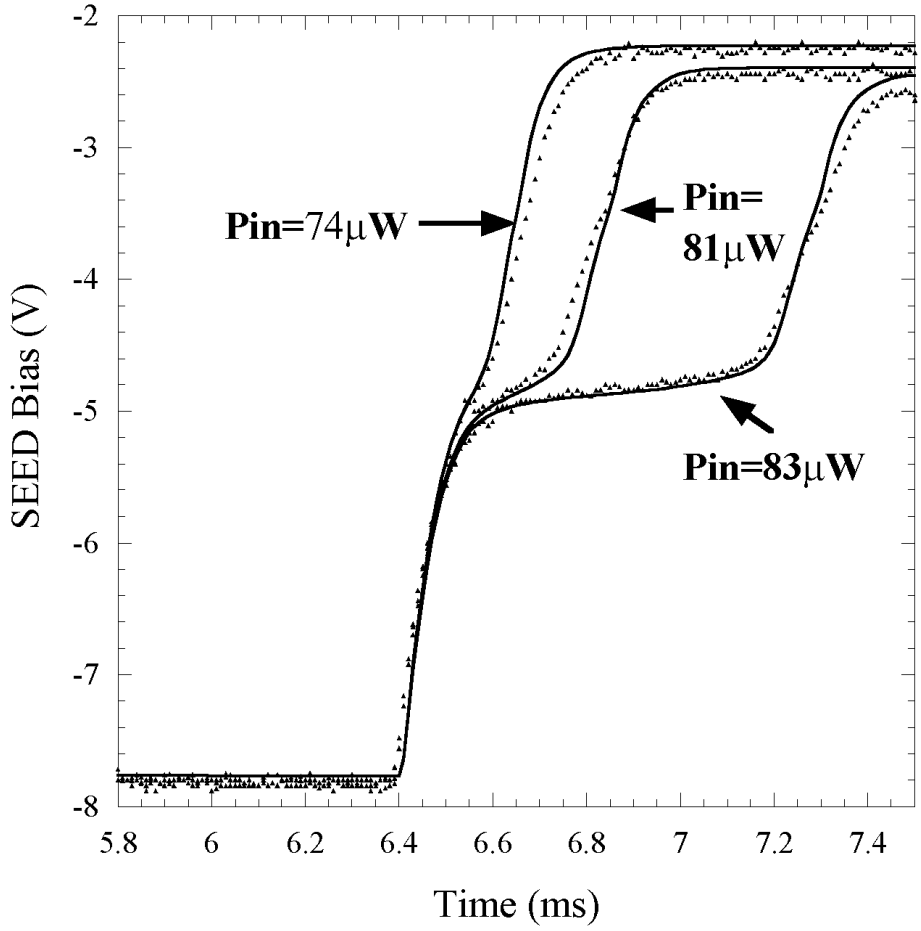

Figure 3.17: Switching of S-SEED with $P_{fixed} = 100\,\mu$W and P_{in} switched from $270\,\mu$W to the three different powers of $74, 81$ and $83\,\mu$W to demonstrate critical slowing down. The solid lines represent the simulation, while experimental results are depicted with points. The mean absolute percentage error was calculated bewteen the experimental and simulated results as 2.4%, 2.4% and 3.9% for the $74, 81$ and $83\,\mu$W cases respectively. The dominant sources of error can be seen as scatter in the experimental results due to laser noise, and a difference in the switching slope due to error in the capacitance measurement used in the simulation. These errors of 2.2% in the simulation and at least 0.4% in the experiment imply that the agreement between the simulation and experiement lie within the expected error for the 74 and $81\,\mu$W cases. However for the $83\,\mu$W case the error is greater than that expected due to a significant difference in the level of the final state.

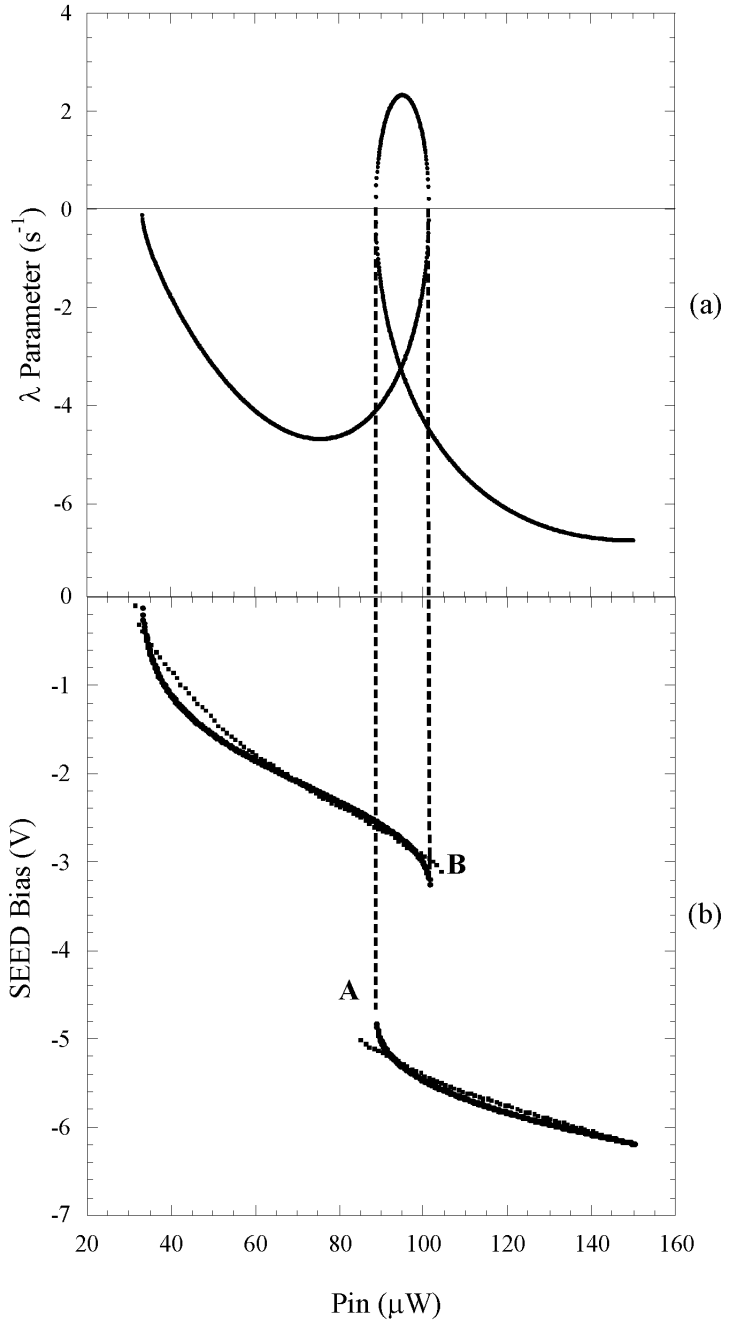

Figure 3.18: (a) Graph of the values of λ as a function of P_{in}^{L}, showing stable ($\lambda < 0$) and unstable solutions with $\lambda > 0$. (b) Plot of the hysteresis curve, generated from stable voltage solutions for the fitted data, as per Equation 3.17. Two devices of different peak responsivities were used, which caused the hysteresis region to shift from that depicted in Fig 3. Overlaid in a thinner line is the corresponding result using experimental data. The critical points are marked with the dashed line and the labels A and B.

steady state solutions derived from experimental data, depicted using a thinner line, demonstrating the validity of (3.17). For illustrative purposes Fig. 3.18 (a) includes the unstable static solutions, which have positive values of λ.

An alternative quantitative method of describing critical slowing down, that also includes transient effects, is to consider a potential function. If we take (3.7) as an equation of motion for V [46], then the potential function $U(V)$ is defined as follows

$$\frac{dV}{dt} = -\frac{\partial U}{\partial V}$$

$$U(V) = -\int_0^V \frac{I_{total}(V', \lambda)}{C_1(V_0 - V') + C_2(V')} dV' \tag{3.17}$$

The potential function has a local minimum at a stable solution and the slope of $U(V)$ determines the velocity and direction of movement of V. For this technique, critical slowing down is identified when $\frac{dU}{dV}(V) \to 0$ and V is not equal to a stable solution of the system. As this is a global definition, it has the advantage that it can be used to describe the transient behaviour on both sides of the transition point.

For the switching experiment of Fig. 3.17 we can plot three potential function curves, as shown in Fig. 3.19. The three curves correspond to the values of P_{in}^L equal to 74 (dashed line), 81 (dot-dashed) and 83 μW (solid).

In the process of switching P_{in} from 270 μW to P_{in}^L, the S-SEED voltage will traverse the path of the potential function from $-7.8V$ to the minimum at $-2.25V$. Figure 3.19 reveals that the slope of the potential function approaches zero as P_{in}^L is increased to 83 μW. Since the speed of the system traversing this curve is determined only by the slope, the system slows down around $-4.9V$ as P_{in}^L approaches the critical point labelled A in Fig. 3.18 (b). Thus the potential function shows that the S-SEED experiences critical slowing down and demonstrates the cause of the effect. Increasing P_{in}^L further so that P_{in}^L lies in the hysteresis region, will produce two local minima in $U(V)$. Following the treatment of [45] for optical bistability, the presence of two local minima indicate that the system is analogous to a first-order phase transition in a non-equilibrium situation, for which critical slowing down has been

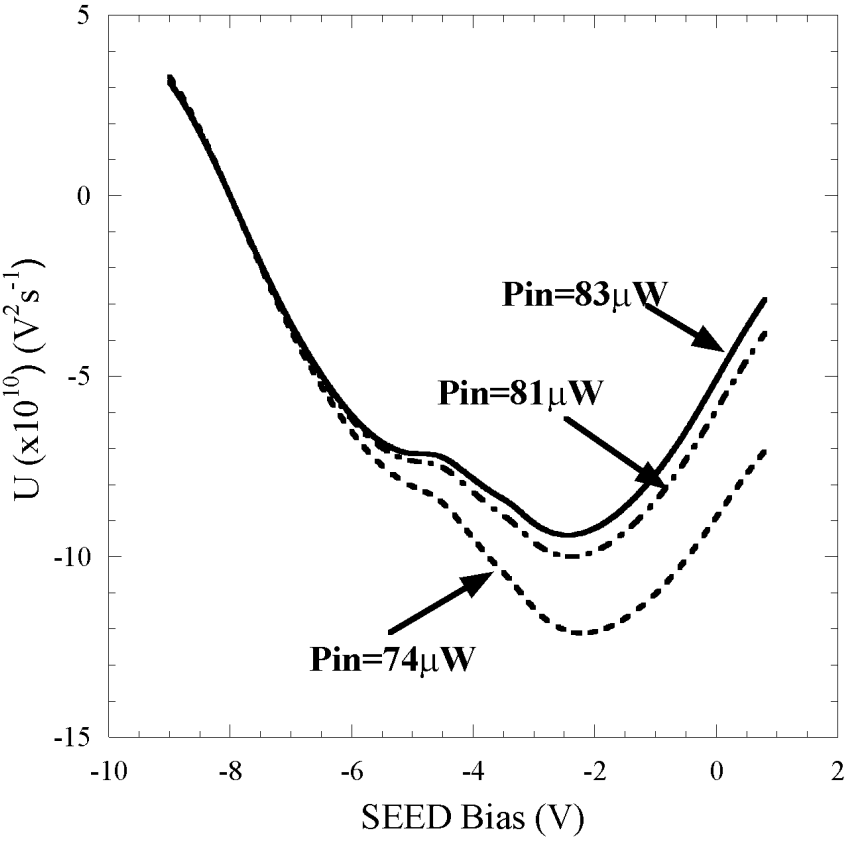

Figure 3.19: Potential function, $U(V)$, for three values of P_{in} : $74, 81$ and $83\,\mu$W. The stable solutions occurs around $-2.3V$ and critical slowing down can be seen at $-4.9V$.

demonstrated [47], [45].

An experimental technique to demonstrate that the S-SEED is experiencing critical slowing down is to measure the switching time as a function of P_{in}^{L}. The switching time was defined as the time taken for the system to get from the initial voltage state, V_i to 95% of the the final voltage state V_f, labelled as $V_{switch\ criterion}$ in (3.18). To measure the effect of critical slowing down, the experiment represented in Fig. 3.14 was repeated with several values of P_{in}^{L} ranging from 55 to 83 μW, and the switching times were measured directly from the plotted experimental switching data. The results are presented in Fig. 3.20.

$$V_{switch\ criterion} = V_i + 0.95 \times (V_f - V_i) \tag{3.18}$$

The data of Fig. 3.20 is fitted with a function of the form

$$t_s = a + \frac{b}{\sqrt{|P_{critical} - P_{in}|}} \tag{3.19}$$

where a and b are fitting parameters and $P_{critical}$ is the value of P_{in}^{L} at the critical point. For the data of Fig. 3.20 the parameters had values of 0.17 ms, 0.59 ms $\mu\mathrm{W}^{\frac{1}{2}}$ and 83.8 μW, respectively. References [48], [49] and [50] demonstrate that critical slowing down in optical bistability follows the form given in (3.19).

Finally, the simulation was used to study how variation of V_0, which alters the hysteresis width, affects the critical slowing down behaviour. To determine the switching time, the following integration was performed numerically

$$t_s = \int_{V_i}^{V_{switch\ criterion}} \frac{C_1(V_0 - V) + C_2(V)}{I_{total}(V, \lambda)} dV. \tag{3.20}$$

A threshold switching time was defined to be 0.7 ms for a hypothetical sigma delta quantiser, and depicted in Fig. 3.20. Switching times greater than the threshold will then fail to resolve the comparison operation in time and cause errors. The difference between the value of P_{in}^{L} at the switching threshold, P_{thresh}, and the value of $P_{critical}$ determines the range of comparator input powers where the switching time

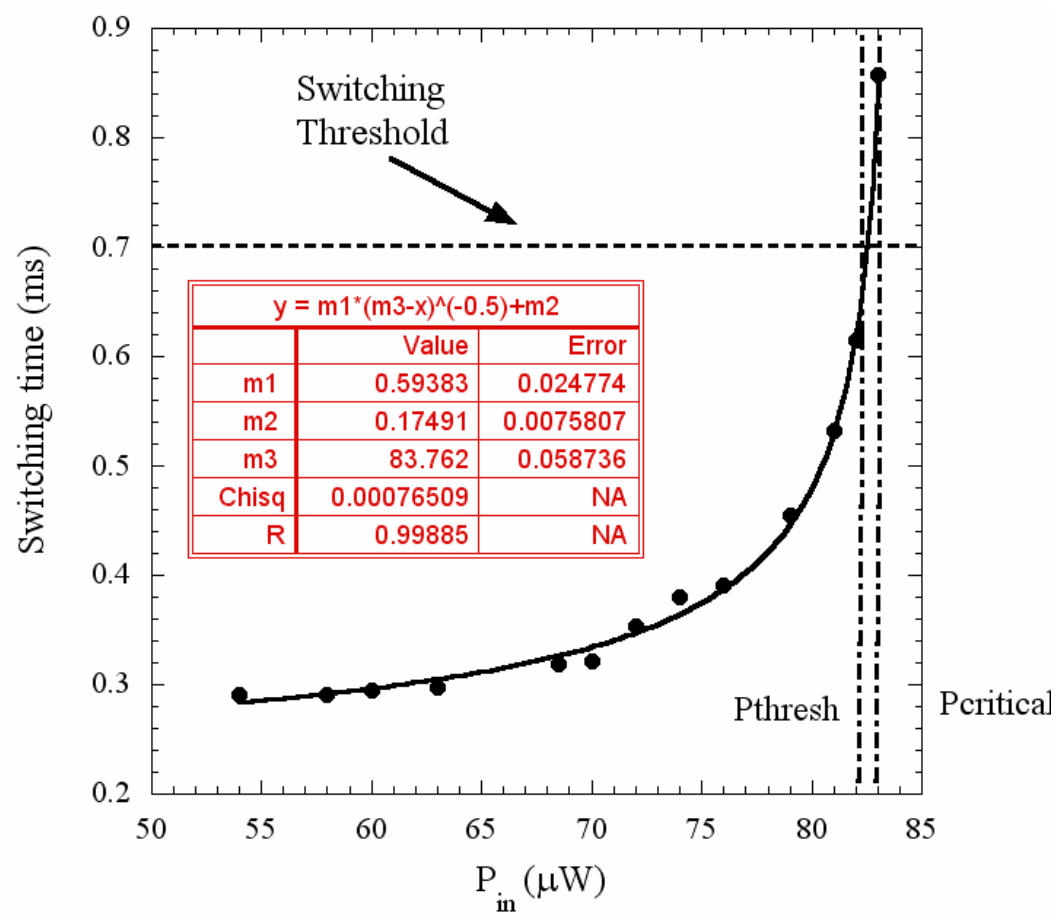

Figure 3.20: S-SEED switching time, as defined in the text, as a function of P_{in}^{L}. A power law as described by Equation 3.19 is fitted to the data with a high degree of correlation ($R^2 = 0.998$). An arbitray switching threshold of 0.7 ms is depicted with a dashed line and the values of $P_{critical}$ and P_{thresh} are illustrated.

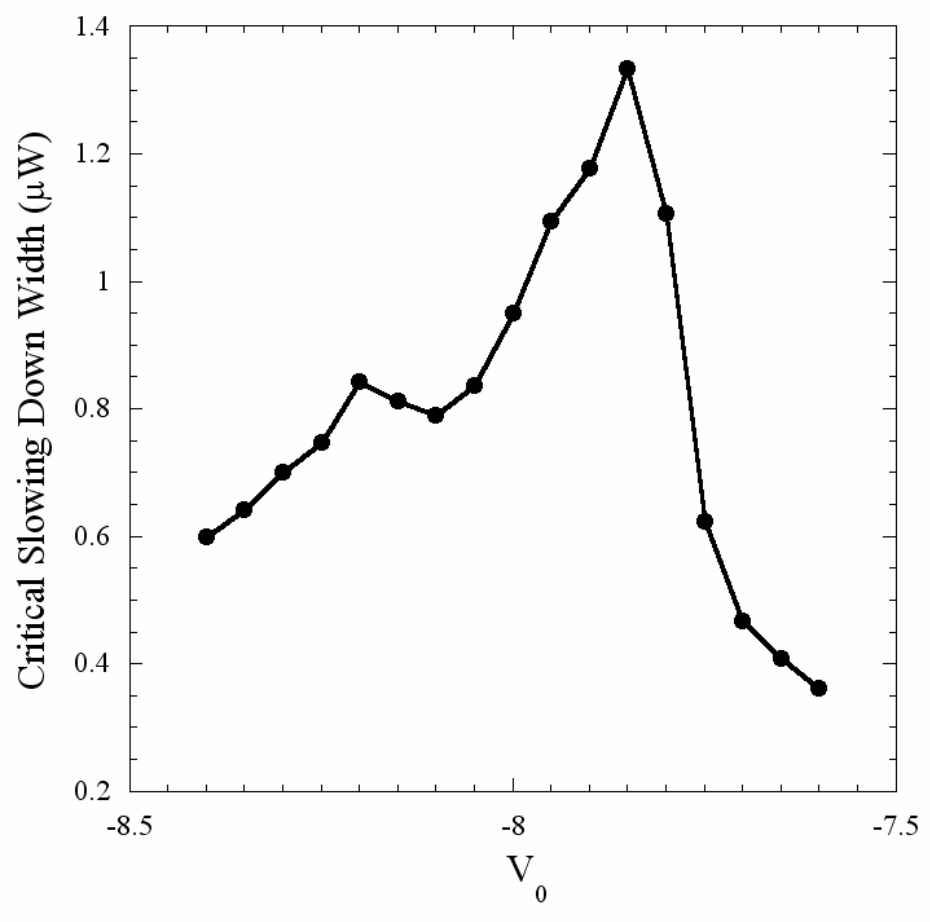

Figure 3.21: Width of the input region over which critical slowing down will have a significant effect on the switching time, as a function of V_0.

is slower than the defined threshold and therefore problematic. P_{thresh} and $P_{critical}$ are defined graphically in Fig. 3.20. The value $P_{critical} - P_{thresh}$ was calculated from a fit of (3.19) to data produced from (3.20), and plotted as a function of V_0 in Fig. 3.21.

Figure 3.21 demonstrates that the range of values of P_{in} where critical slowing down has a significant effect on device performance can be reduced by optimising the bias applied to the S-SEED.

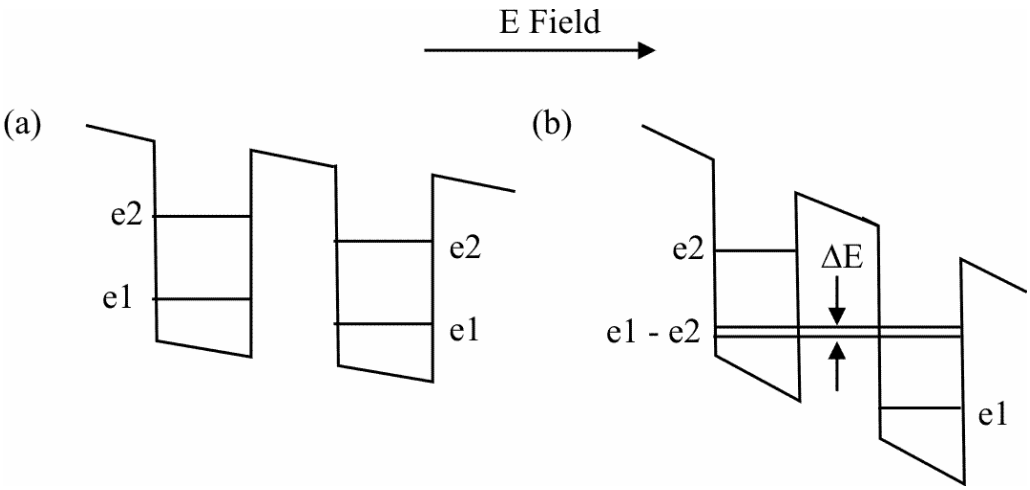

Figure 3.22: (a) Two coupled quantum wells with a low applied electric field showing electron sublevels e1 and e2. (b) Resonant electric field applied, depicting the minimum energy separation (ΔE) between sublevels.

3.6 Multi-State Switching

The utility of the simulation method was further demonstrated by the prediction of the parameters necessary to achieve multi-state clocked switching, using the effect of an anticrossing transition. In the context of quantum wells, anticrossing transitions can be observed for coupled quantum wells, when an applied electric field brings the first electron sublevel (e1) of one well into resonance with the second electron sublevel (e2) of an adjacent well, as shown in Fig. 3.22. Because of the coupling through the barrier, the levels extend across both wells. However, due to the Pauli exclusion principle, both electrons cannot occupy the same energy state. Therefore the levels repel as they approach resonance, demonstrating anticrossing and a minimum energy separation ΔE. The anticrossing transition is manifested in the optical absorption spectrum (or responsivity spectrum) as a dip and a wavelength shift of the exciton peak at the resonant field. This effect can be understood by considering the energy levels and oscillator strength close to the resonant field, and is schematically depicted in Fig. 3.23[51]. For the case that $E<E_{res}$, a strong heavy hole intrawell transition is observed, and a weaker transition at a higher energy between the heavy hole level and the adjacent well's e2 level is apparent. This transition is termed an interwell transition, as it arises due to the spreading of the

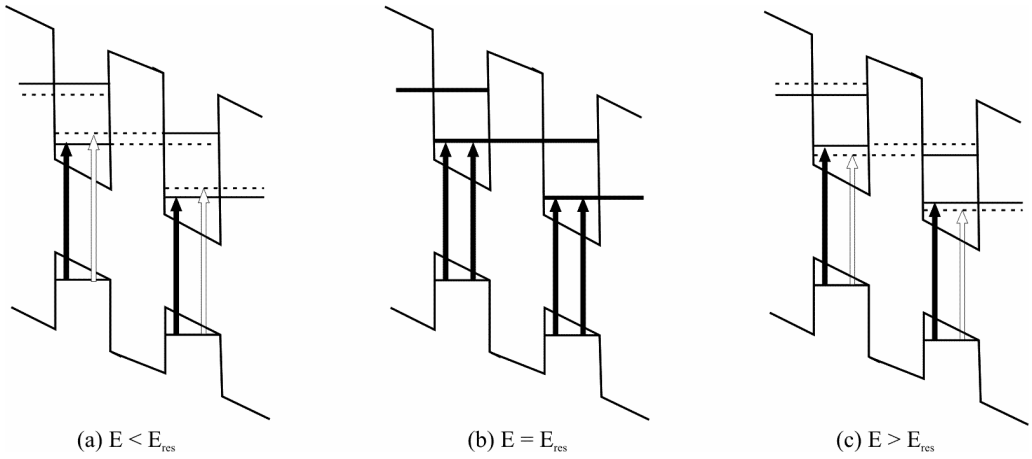

Figure 3.23: Schematic of the energy levels close to an applied resonant field. The solid lines for the levels indicate a large probability amplitude, while the dashed lines represent a smaller amplitude. The solid arrows indicate intrawell transitions and the open arrows indicate interwell transitions. Three cases are considered, (a) E slightly less than the resonant field, (b) E=E_{res} and (c) E slightly greater than E_{res}.

e1 and e2 levels into adjacent wells. The interwell transition's oscillator strength is low due to a weak overlap between the wavefunctions of the heavy hole and the delocalised electron levels[51]. When E=E_{res}, the two electron levels occupy both wells with equal probability amplitude, and have an energy separation equal to the minimum allowable, ΔE. The oscillator strength of each intrawell transition is equal to half that away from resonance, creating the aforementioned dip in absorption. As E becomes larger than E_{res}, as depicted in Fig. 3.23 (c), the larger energy transition becomes stronger and the electron levels become localised. Devices and concepts employing anticrossing transitions in quantum wells are further developed in [51], [52], [53], [54], [55], [56],[57].

Experimental demonstration of heavy and light hole anticrossing transitions is presented in Fig. 3.24 in the form of responsivity as a function of wavelength and applied voltage. To sharpen the transitions and enhance the anticrossing effect, the same device used to measure the data of Fig. 3.12 was placed in a closed cycle helium cryostat and cooled to $15K$. The anticrossing transition is apparent from the responsivity dip and shift in peak wavelength at around $4V$, as labelled in Fig. 3.24 (a).

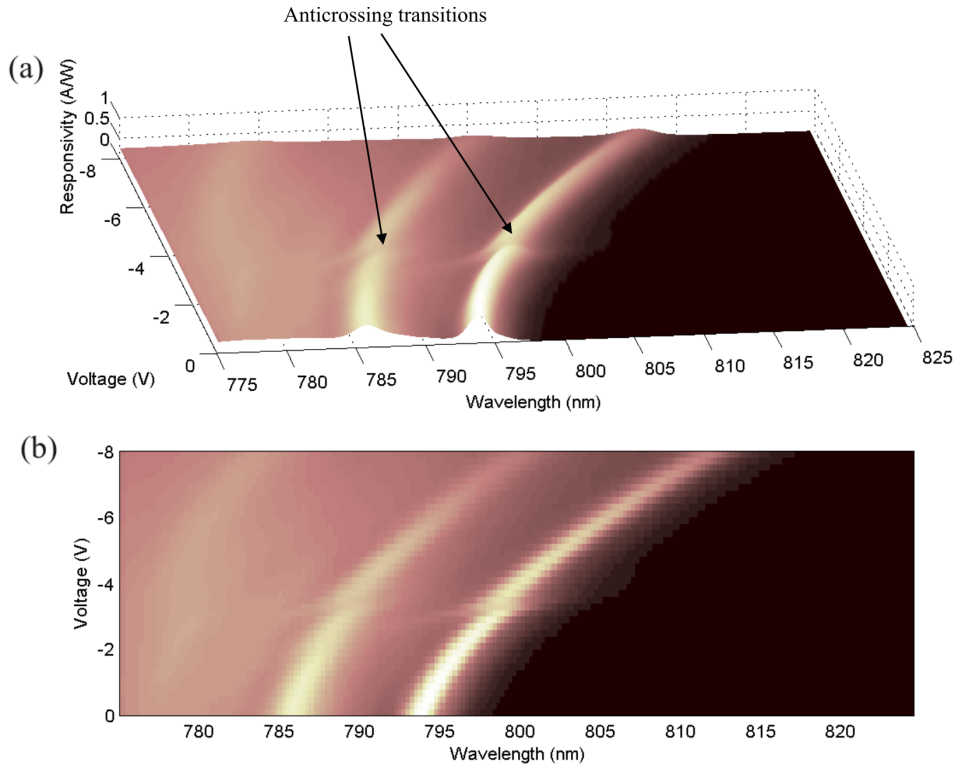

Figure 3.24: Responsivity (A/W) as a function of wavelength and applied voltage at a temperature of $15K$. Part (a) is a 3D plot with the anticrossing transitions labelled and (b) is a projection of (a) onto the x-y plane.

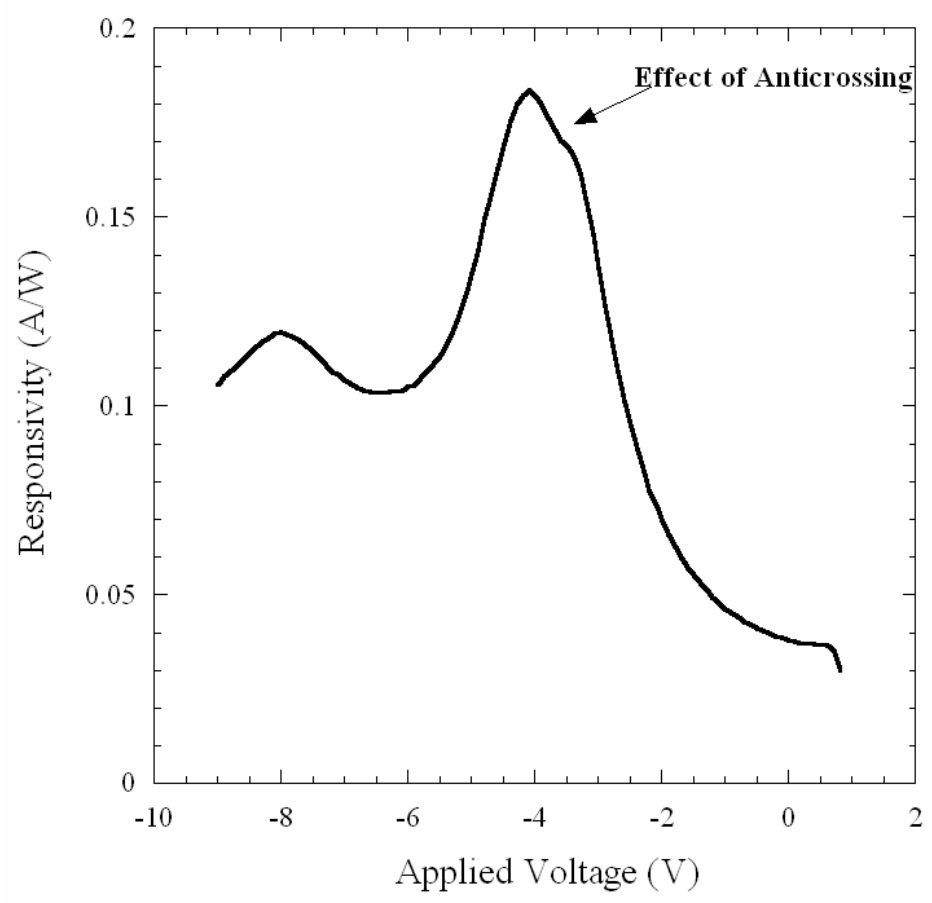

Figure 3.25: Room temperature measurement of responaivity as a function of voltage at $850nm$, depicting the effect of the anticrossing transition.

At room temperature the effect of the anticrossing transition is diminished, but it is still sufficient to create a second region of negative differential resistance, as depicted in the responsivity-voltage plot of Fig. 3.25. Using the experimental data based simulation of S-SEED switching, tri-stability (three stable solutions of the S-SEED circuit) was predicted to occur at a wavelength of 850.0 nm and applied voltage of $V_0 = -7.95\,\mathrm{V}$. This result was confirmed by the measurement of the hysteresis curve, given in Fig. 3.26. The third, small region of stability (circled in Fig. 3.26) is seen to occur between the larger two regions and this is attributable to the dip in responsivity created by the heavy-hole anticrossing transition.

The simulation was subsequently used to predict the powers required to perform clocked switching of three states. An experiment, equivalent to that described in section 3.4 with an added signal and clock state, was performed to verify the simu-

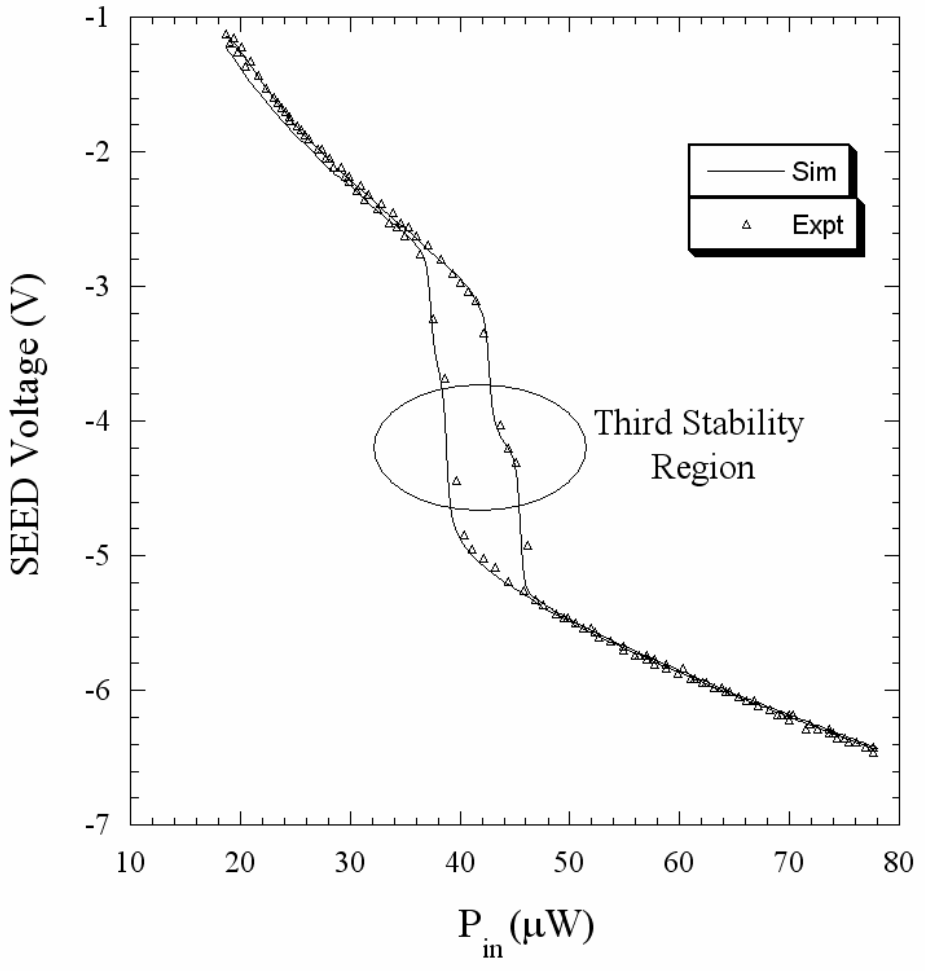

Figure 3.26: Comparison of experimental (triangle) and simulated (solid) results for the S-SEED voltage solution as a function of input power for $V_0 = -7.95V$ and $\lambda = 850.0nm$. A small, third region of stability (circled) is seen to exist between the larger two regions. The mean absolute percentage error between the experimental and simulated results was calculated to be 0.86%, which is well withink the total expected error of 2.6%.

lation. Results are presented in Fig. 3.27. Therefore, three state switching has been successfully demonstrated with agreement to better than 1% demonstrated between the experiment and simulation. Tri-stability using the effects of anticrossing has been previously published [58], [59], but we believe this is the first demonstration of clocked three state switching. Multi-state optical switching may find application in photonic A/Ds, as it has the potential to increase resolution without any increase in complexity.

3.7 Summary

We have developed an accurate model of the switching of an S-SEED, in which the differential equation for the circuit of an S-SEED was solved numerically. The model used experimentally measured device responsivity, dark current and capacitance. Hence the degree of accuracy of this approach is determined by the quality of the measured parameters. We have shown that results from the model for S-SEED switching demonstrate excellent agreement with the corresponding experiment.

The phenomenon of critical slowing down was demonstrated experimentally. The model was then used to replicate these results and interpret the effect. Since this is not a desirable effect for an A/D, the simulation was used to find values of a parameter that minimises this effect.

A potential benefit to photonic A/Ds is multi-state switching, and this was demonstrated using the effect of an anticrossing transition. Such an effect can not be predicted and compared with experimental behaviour without an accurate representation of device responsivity. This demonstrates the utility and strength of our approach, when compared to previous methods.

The simulation that has been described in this chapter will form the basis of photonic A/Ds modelling in the following chapters, and due to the demonstrated accuracy of the simulation it lays the foundation for accurate A/D performance calculations.

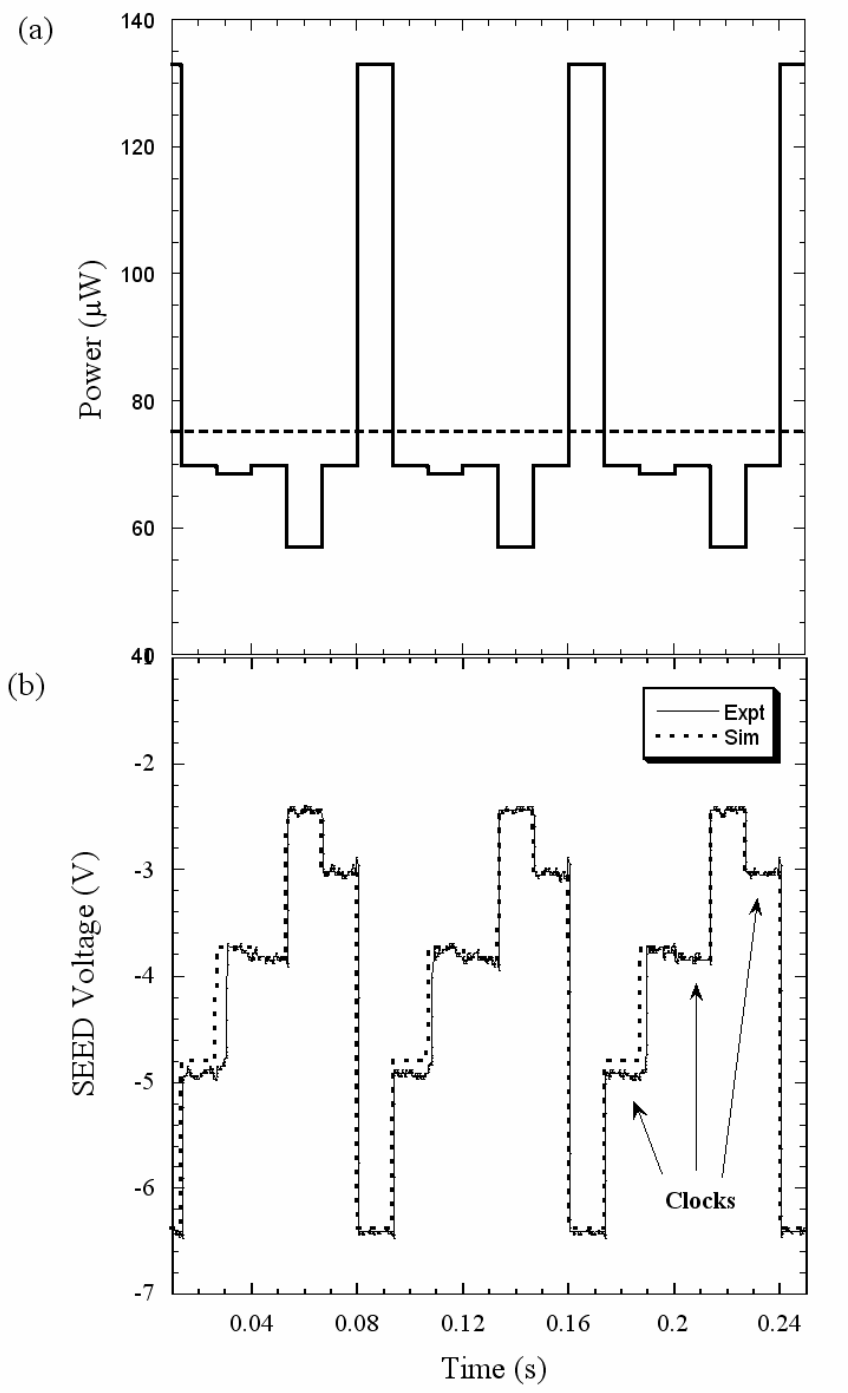

Figure 3.27: (a) Timing diagram for the optical inputs P_{in} (solid line) and P_{fixed} (dashed line). Due to the assymetric hysteresis curve, unequal clock powers were used on each device and on the reference device $P_{fixed} = P_{clock}$ (b) Comparison of the experimental (solid line) and simulated (dashed line) results for V from the clocked switching experiment performed at a wavelength of 850nm and $V_0 = -7.95V$. The difference between the two curves is 2.4%, within the expected error. The dominant error in this experiment is the timing of the switching of the middle state. Since this state switches on a weak slope, circled in Fig. 3.26, the switching point will be sensitive to laser amplitude noise.

Chapter 4

Photonic A/Ds Employing S-SEED Comparators

Our investigation of photonic A/Ds is concentrated on optical Pulse Code Modulation (PCM) and first order error diffusion and sigma-delta architectures. These techniques use oversampling to trade temporal resolution for amplitude resolution achieving high resolution from comparators of modest quality.

A photonic error diffusion A/D has been studied in previous investigations[4], where Self-Electro-Optic-Devices (SEEDs) were employed to create an optical subtractor, and electronics were used for the remainder of the A/D. In this chapter we use two SEEDs connected in series to create an optical switch known as an Symmetric-SEED (S-SEED) to demonstrate the applicability of an optical comparator in analog-to-digital conversion. The devices from Stanford University that were used in Chapter 3 to study the switching properties of an S-SEED comparator, are again used in this chapter.

In this chapter, we compare the performance of two different photonic A/D architectures. To begin our study of photonic oversampling architectures, a simple PCM architecture, that consists of a comparator without feedback is investigated using two different simulations and an experiment. The first simulation, referred to as the static simulation, uses the idealised static parameters of an experimentally measured comparator, and is fast to compute. The other is a more realistic dynamic

simulation that derives the comparator behaviour by numerically solving the differential equation of the S-SEED's circuit, utilising the properties of experimentally measured SEEDs. The results of the simulations are compared to an experiment. The straightforward PCM design is subsequently extended to first order sigma-delta and error-diffusion architectures, which include feedback of the comparator error. As the error diffusion and sigma-delta designs are shown to be mathematically equivalent, static and dynamic simulations of the sigma-delta are performed, using the appropriate experimentally measured data. An ideal subtractor is maintained, as our aim is to investigate the properties and performance of photonic A/Ds with an S-SEED comparator. The results demonstrate that the PCM design is simple to implement using photonics, but a significant performance gain is achieved by the more complex sigma-delta.

4.1 PCM Quantiser

Oversampling techniques trade high speed operation for high resolution, without requiring high precision components. These attributes lend themselves to a photonic implementation. The first step in our experimental study of photonic oversampling quantisers was to investigate the simplest possible architecture, namely, pulse code modulation (PCM) with a 1-bit comparator.

A conventional PCM oversampled architecture is depicted in Fig. 4.1. The architecture consists of a comparator that is operated at high speed, a dither that is added to the input and a filtering stage that performs the functions of a low pass filter and decimator. Together these features act to increase the resolution of the data stream at the expense of speed.

The application of this architecture to the optical domain constrains the system to unipolar operation, since optical powers are always positive. For a 1-bit comparator with the transfer function of Fig. 4.2, in order to improve the output resolution beyond the difference of the two comparator states, $Q_H - Q_L$, the application of a dither signal is necessary. To understand how a dither can give this improvement, consider a dc input to the comparator on the low power side of the hysteresis loop,

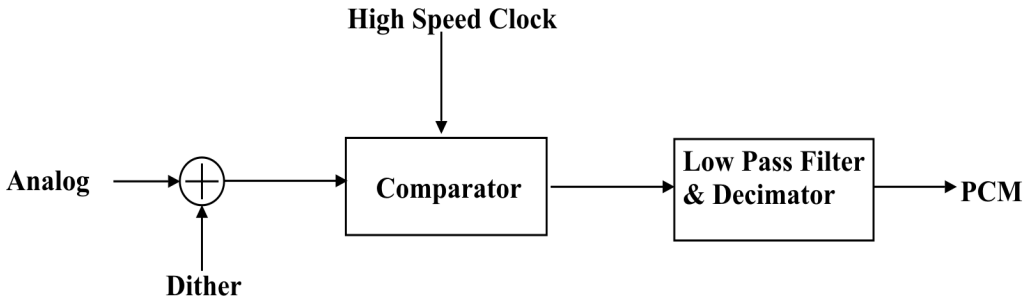

Figure 4.1: Schematic of an oversampled PCM architecture.

as labelled in Fig. 4.2. Without dither the output will consist entirely of low states Q_L. However, with a correctly chosen dither, the input will vary above and below the hysteresis region, giving a series of high and low states in the output. This will more accurately approximate a scaled representation of the input, once the average effect of the dither is removed. A graphical demonstration of the effect of dither is given in Fig. 4.3. Part (a) plots a constant input with and without dither and part (b) depicts the quantiser output with the two states scaled to 0 and 1, giving consistent scales between the input and output. Figure 4.3 (c) plots the low-pass filtered output of part (b), demonstrating the improved accuracy that the input dither provides.

Due to the unipolar nature of photonics, the total signal incident on the comparator (input + dither) must be positive and must not exceed $2P_\theta$. A triangle waveform was chosen as the dither in order to maintain the linearity of the comparator. A dither amplitude of $P_\theta/2$, with constant offset $P_\theta/2$ to constrain the dither to the range $[0, P_\theta]$, provides an improvement in resolution, assuming the hysteresis width $\Delta = 0$ and P_θ is defined as in Fig. 4.2. To ensure the total signal does not exceed $2P_\theta$, the allowable range for input signals is the same as the dither. That is, the input is constrained to the region $[0, P_\theta]$. For the example of a sine input, the maximum allowable amplitude is $P_\theta/2$, with a constant offset of $P_\theta/2$. As will be shown, in the case where $\Delta \neq 0$, the amplitude of a sine that can successfully quantised is reduced from the maximum of $P_\theta/2$.

For an ideal PCM architecture, the theoretical signal (P) to quantisation noise (n_0) ratio can be calculated. We start by assuming input frequencies lie in the band

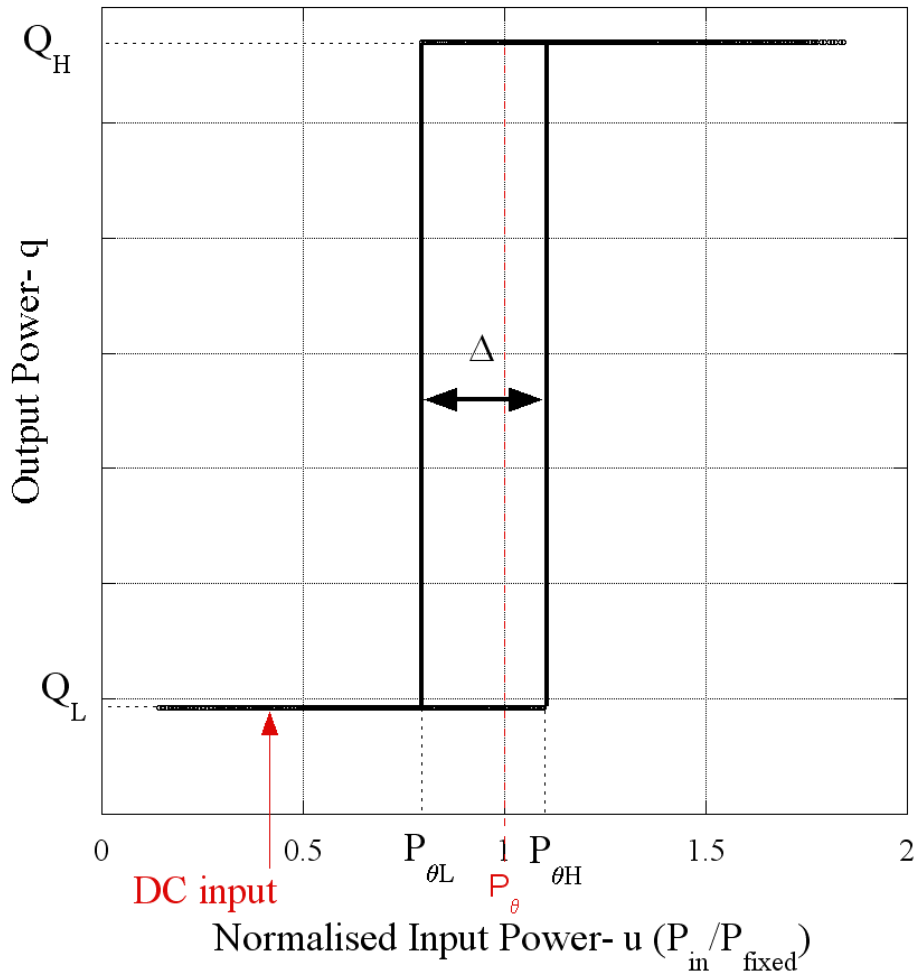

Figure 4.2: Schematic of the optical comparator transfer function with hysteresis. The output powers are labelled Q_H and Q_L, while the powers at the edge of the hysteresis region are labelled $P_{\theta H}$ and $P_{\theta L}$. Also labelled is the hysteresis width Δ, the DC input referred to in the text, and the switching point P_θ for the case when $\Delta = 0$.

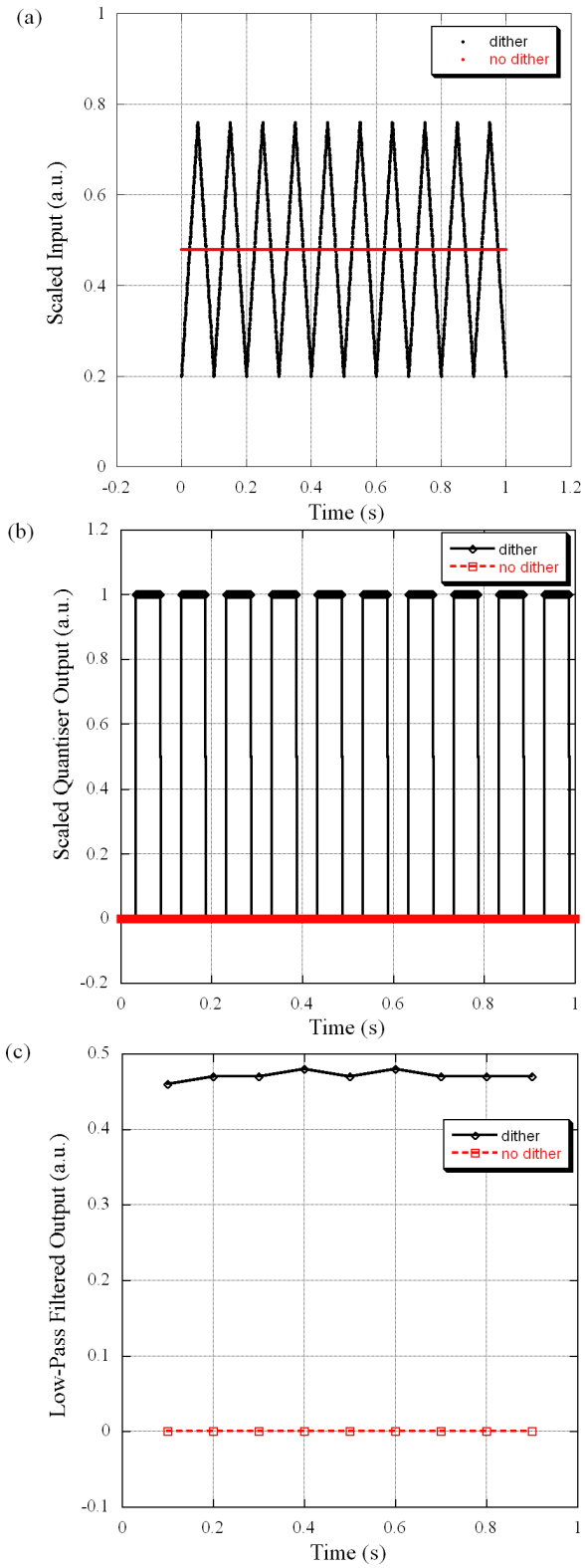

Figure 4.3: A graphical demonstration of the effect of dither for a quantiser with hysteresis and output states scaled such that $Q_H = 1$ and $Q_L = 0$. Part (a) depicts the constant input of 0.45 with and without dither. Part (b) plots the output of the quantiser with and without dither. In the case without dither, the output remains in the low state. Part (c) presents the low-pass filtered quantiser output. The case with dither more accurately approximates the input of part (a).

$0 \leq f < f_0$ and a white quantisation noise spectrum, which means that the quantiser error, e, has equal probability of lying anywhere in the range $[-\frac{Q_H-Q_L}{2}, \frac{Q_H-Q_L}{2}]$. That is,[8]

$$e_{rms}^2 = \frac{1}{\delta}\int_{-\delta/2}^{\delta/2} e^2 de = \frac{\delta^2}{12}, \tag{4.1}$$

where $\delta = Q_H - Q_L$. The oversampling ratio (OSR) is defined as the ratio of the sampling frequency f_s to the Nyquist frequency $2f_0$. The OSR must be an integer to ensure a whole number of clock pulses are averaged in the low-pass filtering stage

$$OSR = \frac{f_s}{2f_0}. \tag{4.2}$$

The noise power that falls into the signal band is given by[8]

$$n_0^2 = \int_0^{f_0} E^2(f)df = e_{rms}^2\left(\frac{2f_0}{f_s}\right) = \frac{e_{rms}^2}{OSR}, \tag{4.3}$$

where

$$E(f) = e_{rms}\sqrt{\frac{2}{f_s}} \tag{4.4}$$

is the spectral density of the sampled noise[8]. With substitution of (4.1), the signal (P) to quantisation noise (n_0) ratio in dB is then given for input normalised by $P_\theta/2$ and output normalised by $\delta/2$ as

$$SQNR(dB) = 20Log(P) + 10\ Log(OSR) + 10\ Log(3). \tag{4.5}$$

The use of the dither applies further constraints on the sampling and input signal frequencies. Firstly, to ensure the average of the triangle dither is the same value for each output sample, the ratio of the sampling frequency to the dither frequency (f_d) must be an integer. That is,

$$\frac{f_s}{f_d} = n, \text{ where } n \text{ is an integer} > 1. \tag{4.6}$$

Secondly, to satisfy the Nyquist criterion, the dither frequency must remain in the range $f_0 \leq f_d < \frac{f_s}{2}$. However, for a significant improvement in resolution, $f_0 \ll f_d$ is necessary. The lower limit of the achievable amplitude resolution, which we shall label q, can be calculated by again considering the case of the the PCM quantiser with constant input of Fig. 4.3. For a comparator without dither, the comparator doesn't switch, and the resolution is undefined. Each time the dither causes the comparator to switch within one oversampling period, the smallest resolvable amplitude decreases by a factor of $Q_H - Q_L$. For example, if the comparator switches ten times in a given oversampling period, after low-pass filtering the smallest resolvable amplitude of the PCM quantiser is $\frac{Q_H - Q_L}{10}$. Therefore, the smallest resolvable amplitude is given by the reciprocal of the oversampling period ($\frac{OSR}{f_s}$) divided by the dither period ($\frac{1}{f_d}$), multiplied by $Q_H - Q_L$. That is,

$$q \equiv \left(\frac{OSR}{f_s} / \frac{1}{f_d} \right)^{-1} (Q_H - Q_L), \tag{4.7}$$

and substituting (4.2) gives

$$q = \frac{2\ f_0}{f_d} (Q_H - Q_L). \tag{4.8}$$

Therefore, the smallest resolvable amplitude of the PCM quantiser is inversely proportional to the dither frequency, but as the dither frequency approaches the upper limit of half the clock frequency, less dither periods are averaged and the output will be distorted by the dither signal. Thus the dither frequency must be selected to optimise the resolution and accuracy for a given application.

4.1.1 PCM Simulations

To study the performance of the PCM architecture, simulations were performed using two different approaches. A static simulation that is fast to compute used the ideal comparator transfer function shown in Fig. 4.4. The output voltages of the transfer function, Q_H and Q_L, correspond to the clocked output voltage states of the experimentally measured comparator of Section 3.4.2. In the static simulation,

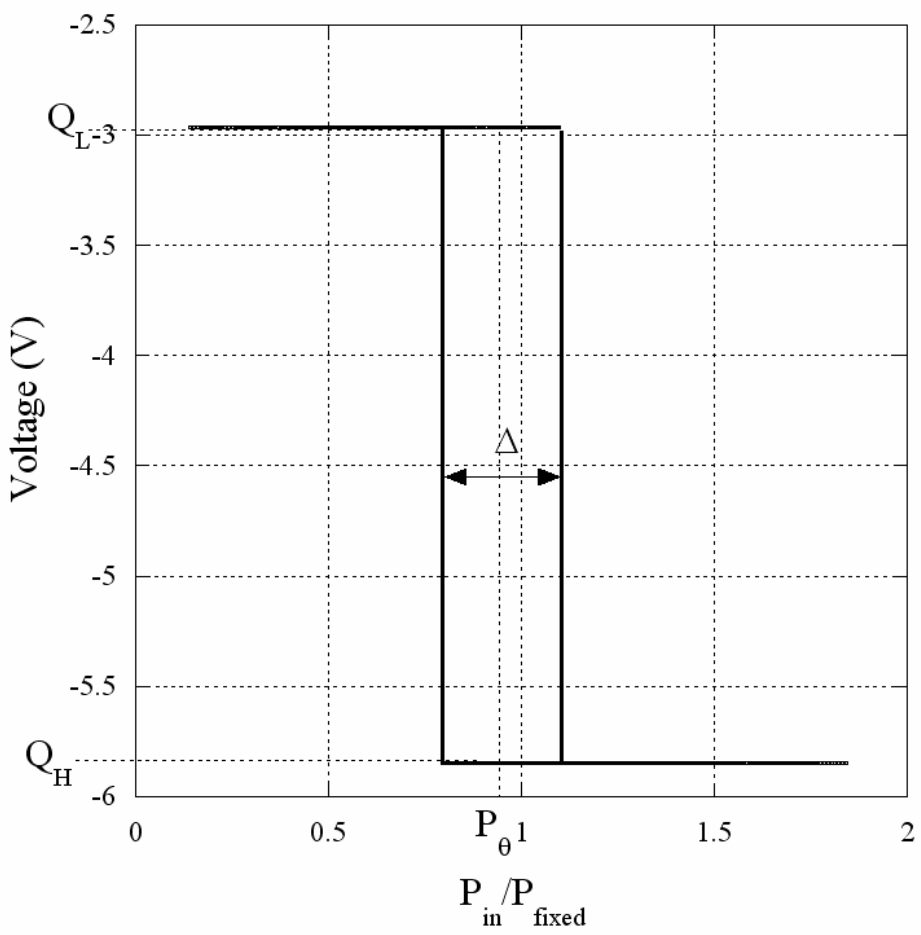

Figure 4.4: Transfer function of the comparator used in the static simulation. The input is the ratio of P_{in} to P_{fixed} and the ouptut is the voltage solution of the S-SEED. Q_H, Q_L , Δ and P_θ are labelled.

the input composed of signal plus dither was sampled at the clock sample period and applied to the transfer function of Fig. 4.4, yielding a sequence of output Q_H and Q_L states. The quantiser performance was quantified with the use of the signal-to-quantisation-noise ratio (SQNR)[8], which is a measure of the signal-to-noise ratio (SNR) including only the noise contributed by the quantisation process. To calculate the SQNR of the output, a power spectrum was calculated. The ratio of the signal power and the total integrated power in the noise gives the SQNR, with the bandwidth of noise integration dependent on the oversampling ratio. The signal-to-quantisation-noise ratio determined from the power spectrum is compared to the ideal result from (4.5) in Section 4.1.3.

The second simulation was based on the accurate S-SEED simulation, described in Section 3.3. This method, termed the dynamic simulation, was expected to provide greater accuracy than the static simulation, but it requires a significantly longer computation time. Figure 4.4 was used to determine P_θ, and hence set the input and dither's amplitude and offset. To generate two fixed output states from the S-SEED, two equal power clock beams were interleaved with the signal and applied to each of the SEEDs in the S-SEED, as described in Section 3.4. The clock has the effect of flattening the hysteresis curve of Fig. 3.3, leading to a comparator transfer function approaching the idealised case of Fig. 4.4. Solving the S-SEED circuit equation (3.7) for the given input and extracting the levels produced by the clock yields the required output states of the comparator, Q_H or Q_L, as depicted in Fig. 4.4. The signal-to-quantisation-noise ratio of the architecture was again determined from the power spectrum. The results of the simulations are presented in Section 4.1.3, where it is demonstrated that the prediction of the PCM's performance using the static simulation agrees with the dynamic simulation. The static simulation is then used to investigate the effect of hysteresis on the architecture's performance, while the dynamic version is demonstrated to provide accurate transient information that the static case is unable to supply.

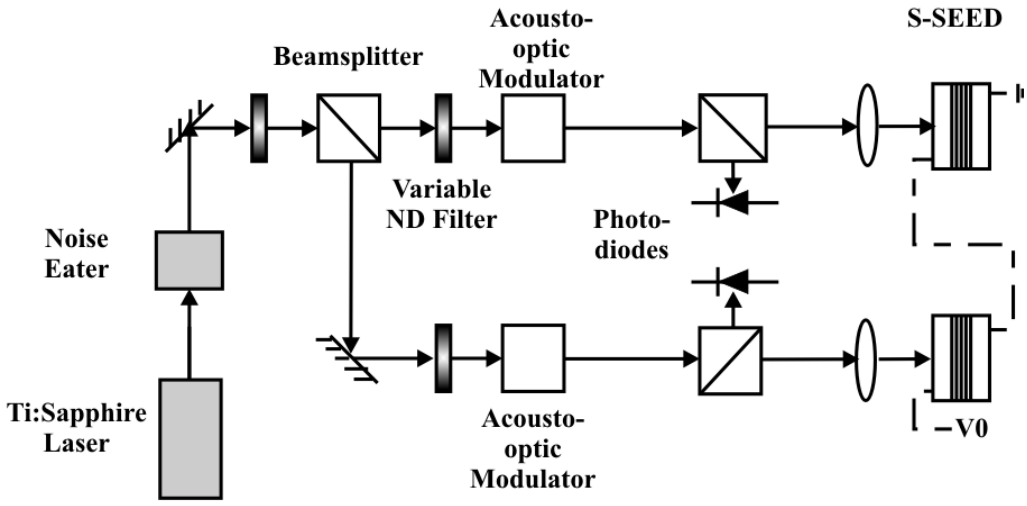

Figure 4.5: Schematic of the experimental setup to test the PCM architecture using an S-SEED comparator.

4.1.2 PCM Experiment

To test the validity of the simulations and demonstrate a photonic oversampled quantiser, an experiment similar to the clocked switching setup of Fig. 3.14 was constructed. This experiment was used to measure the SQNR of the output of the PCM architecture with a sine input and compare to the predicted SQNR from the simulation. A schematic of the experimental setup is given in Fig. 4.5. A tunable Ti:Sapphire laser was coupled with a laser power controller to reduce amplitude noise. The beam was split into two, one for each SEED. Synchronised acousto-optic modulators (AOM) were used to impart the signals on the beams. One beam was encoded with a square wave, representing a high clock pulse and a low fixed reference power (P_{fixed}). The other beam was encoded with the sum of the triangle dither, sine input and constant offset, interleaved with the high clock pulse. To reduce the AOM distortion, the inverse of the AOM's transfer function was applied to the sine and triangle modulating waveforms. The two clock pulses were synchronised in time.

The SEEDs used in our experiment (labelled wafer 436) were MBE grown $p-i-n$ diodes with 50 $Al_{0.31}Ga_{0.69}As/GaAs$ quantum wells in the intrinsic region. Fabricated devices were defined by 500 μm$\times$ 500 μm square mesas. Since the devices

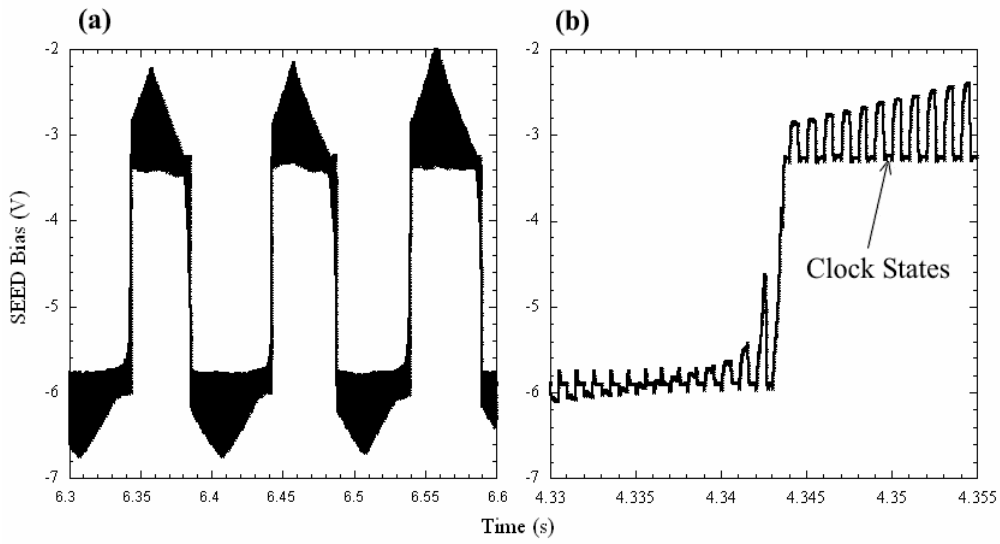

Figure 4.6: Output of the comparator on a long (a) and short (b) time scale.

were constructed without internal mirrors, there was no optical output. Therefore the voltage dropped across one device in the S-SEED was measured to determine the output state. An instrumentation amplifier with 10 GΩ input impedance was used to interface the S-SEED to a 12-bit, 1 MHz data capture card. A computer was used to extract the clock output and calculate the signal-to-noise ratio from the power spectrum.

A sample of the unprocessed comparator output is given in Fig. 4.6, where the following optimised parameters were used: $V_0 = -9\,\mathrm{V}$, input wavelength $\lambda = 851.1\,\mathrm{nm}$, $P_{fixed} = 59\,\mu\mathrm{W}$, $P_{clock} = 200\,\mu\mathrm{W}$, input signal amplitude $= 6\,\mu\mathrm{W}$, dither amplitude $= 30\,\mu\mathrm{W}$, clock frequency $= 1\,\mathrm{kHz}$, dither frequency $= 10\,\mathrm{Hz}$, input signal frequency $= 1\,\mathrm{Hz}$. Figure 4.6 depicts the comparator output on a large (part a) and short (part b) time scale. The short time scale allows the effect of individual clock pulses to be resolved, as indicated by the arrow. It is the application of P_{clock} to both SEEDs that performs the clocking function, yielding one of only two output levels. The larger time scale of Fig. 4.6 (a) illustrates the function of the triangle dither, to oscillate the output from low to high.

For the powers used in the experiment, the maximum clock frequency of the S-SEED was limited to 1 kHz, due to the large area and therefore large capacitance (100 pF) of the SEEDs. However, switching speed is not a limitation of the tech-

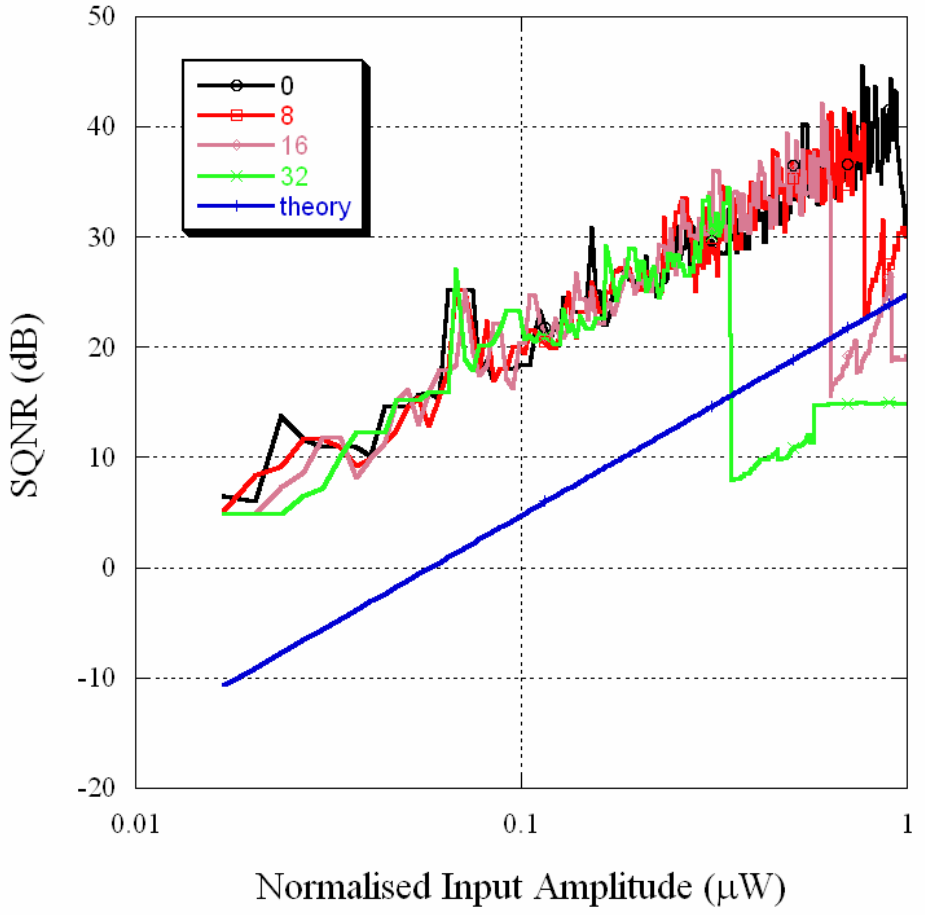

Figure 4.7: Signal-to-quantisation-noise ratio as a function of normalised input amplitude for the static PCM simulation. Theory is compared to hysteresis widths of $0, 8, 16$ and $32\,\mu$W. A large deterioration in the SQNR is observed when the signal amplitude becomes large enough to enter the hystersis region.

nology, since by reducing the capacitance and increasing the peak power, switching speeds of the order of 10 ps can be achieved [44] [27].

4.1.3 PCM Results

In the following section results from the static and dynamic simulations are presented, and compared with the successful experimental demonstration of the photonic PCM quantiser.

Firstly, the SQNR as a function of normalised input amplitude from the ideal static simulation using the idealised comparator transfer function is given in Fig.

4.7. The theory of (4.5) is compared to the PCM simulation with hysteresis widths of 0, 8, 16 and 32 μW. The results are calculated for an oversampling ratio of 100, output states of -2.96 and -5.95 V with $P_\theta = 56\,\mu$W, triangle dither frequency equal to 10 Hz, sampling frequency of 1 kHz and a signal frequency of 1 Hz. Fig. 4.7 demonstrates the reduction in useful input range as the hysteresis width increases. The input range is reduced because at sufficiently large input values and hysteresis widths, the triangle dither is unable to switch the comparator into the low state. Fig. 4.7 also depicts a large discrepancy between the theory of (4.5) and the simulation. Since the triangle dither is not random, it does not whiten the comparator noise sufficiently. Therefore, the assumption that the noise in the system is white is not fulfilled, causing the observed discrepancy. The noise is in fact composed of many large spurious components [8] that alter the total noise in the signal band, compared to the theory.

The results of the dynamic simulation are now discussed, for which the following parameters were used: wavelength =851.1 nm, $V_0 = -9$ V, $\Delta = 16\,\mu$W, $P_\theta = 56\,\mu$W, $P_{clock} = 265\,\mu$W, $P_{fixed} = 59\,\mu$W and frequencies of 1 kHz, 10 Hz and 1 Hz for the clock, dither and signal, respectively. Fig. 4.8 depicts the SQNR as a function of normalised amplitude for the dynamic simulation with a solid line and the static case with a dashed line. The two cases agree for all but the highest amplitudes. The advantage of the dynamic simulation is that it produces a solution, shown in Fig. 4.9, that matches the experimental output of Fig. 4.6. This provides information about the transient performance, which can be used to predict the performance and limiting speed of the S-SEED.

Finally, the results of the experiment, described in 4.1.2 are presented. At an input amplitude of 6 μW, the experiment achieved an SQNR of 19.47dB. However, the simulated results presented in Fig. 4.8 predict an output of 25dB. The discrepancy can be attributed to the noise in the experimental system. To account for this noise, a noise spectrum of the input to the SEEDs was measured and is shown in Fig. 4.10. Including the noise in the dynamic simulation resulted in a SQNR value of 22.9dB. The noise originates from the characteristic 1/f acoustic and vibrational fluctuations of the laser. Due to the low signal frequency of 1Hz, the noise makes

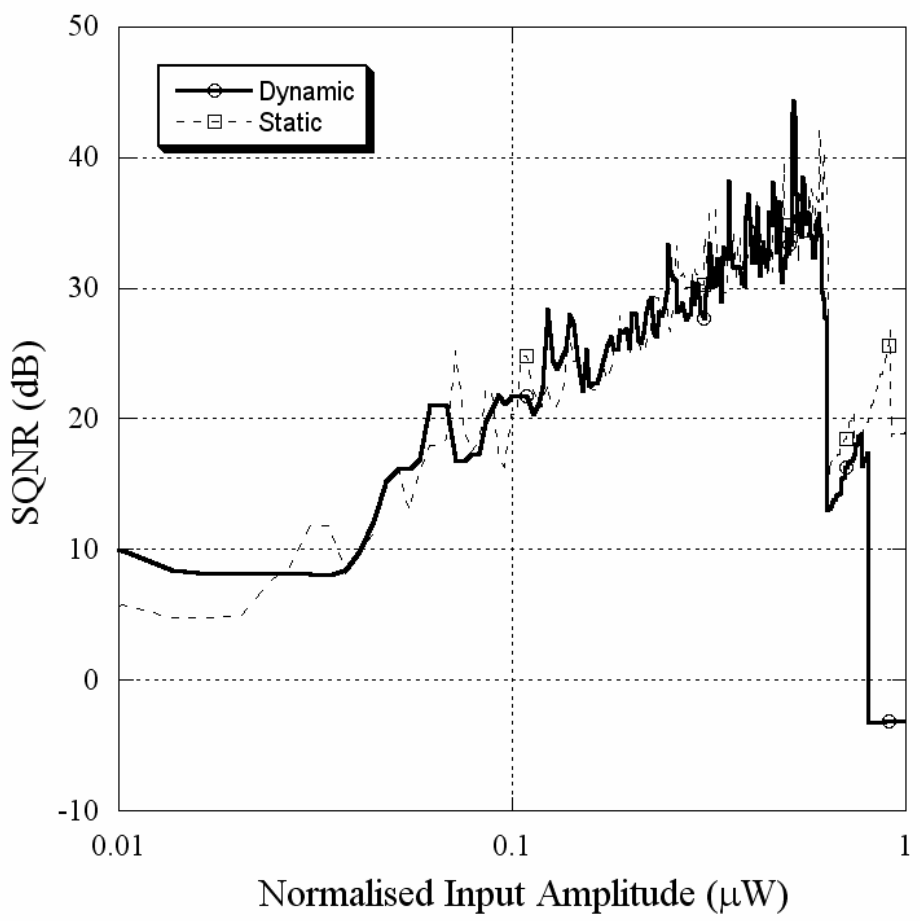

Figure 4.8: Results from the dynamic PCM simulation for a clock frequency of 1 kHz, dither frequency 10 Hz and signal frequency 1 Hz.

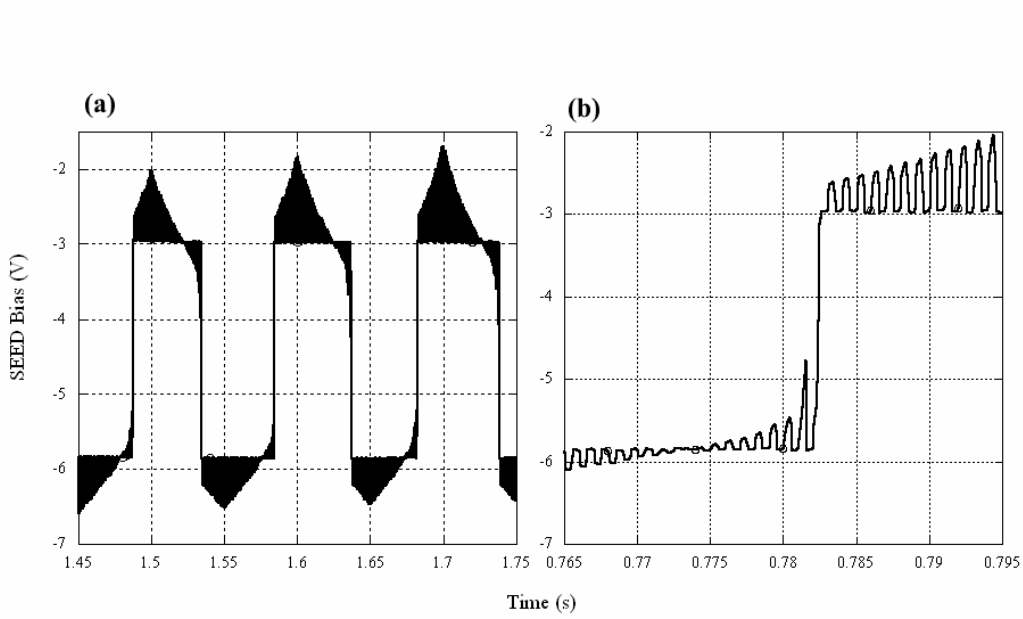

Figure 4.9: Output of the dynamic simulation, for a long (a) and short (b) time scale. The voltage levels and transient behaviour agree with the experimental results.

a significant contribution. However, for a system using much faster devices, this noise is expected to be insignificant. The remaining discrepancy between simulation and experiment is due to uncompensated distortion of the AOM used to impart the signals on the laser beam.

Therefore, by demonstrating correct qualitative behaviour of a PCM A/D, the experiment successfully presented the use of an S-SEED as a comparator and the photonic PCM concept . However, quantitative comparison with the simulations is difficult due to the significant non-idealities of the experiment.

4.2 First-Order Architectures

To increase the output resolution of an oversampled A/D, one can increase the oversampling ratio. Alternatively, one can choose to increase the architecture complexity by adding one or more feedback loops to improve the accuracy of the quantisation. The two cases considered here involve the addition of a single negative feedback loop to the PCM architecture to create a first order architecture. The two alternative

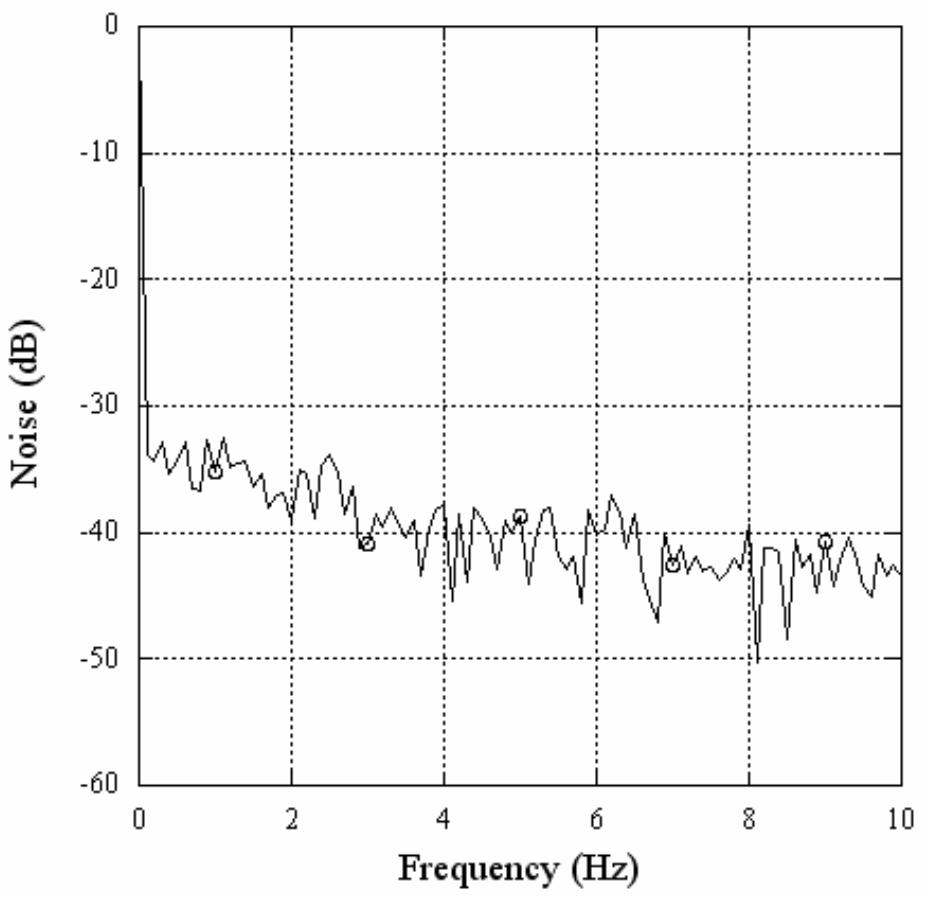

Figure 4.10: Noise spectrum of the light incident on the SEEDs for which the RIN was calculated to be 2.9%. For static measurement experiments where the incident laser power is normalised, the effect of this noise will be significantly lower. However, for dynamic time-dependent experiments, the power meter's response was too slow. Hence the measured RIN will directly impact the accuracy of the results.

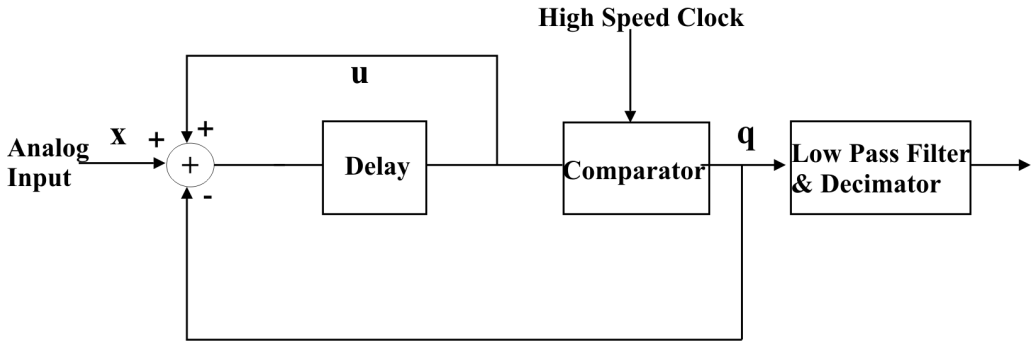

Figure 4.11: Schematic of an oversampled Sigma-Delta architecture.

forms are termed the sigma-delta and the error diffusion architecture[8].

4.2.1 Sigma-Delta Architecture

A schematic of the first order sigma-delta architecture is depicted in Fig. 4.11. Instead of using dither, the sigma-delta architecture feeds back the comparator output (q) and input (u) to a subtractor and adder node, respectively. A delay is utilised to ensure the signals fed back are deferred an appropriate number of clock periods. The following equation describes the relation between successive values of q_n, u_n and x_n (input)

$$u_n = x_n - q_{n-1} + u_{n-1}. \tag{4.9}$$

A proof that the output q converges to the input x is given in [23].

To implement the sigma-delta architecture in photonics requires photonic versions of a comparator, subtractor, adder and delay. The first part of this chapter has demonstrated a photonic comparator, as used in the PCM A/D. Addition and delay are straight-forward in the optical domain, while subtraction has been successfully demonstrated [60] [61]. Optical subtraction will be discussed in detail in Chapter 6.

We now determine the conditions necessary to maintain unipolar operation of this architecture. The first constraint is that the input x must lie between the comparator output states, since values outside this range cannot be quantised. That

is,

$$Q_L \leq x \leq Q_H. \tag{4.10}$$

Consider an all optical comparator with hysteresis, pictured in Fig. 4.2, and defined as follows

$$If\ u_n < P_{\theta L}\ then\ q_n = Q_L$$
$$If\ P_{\theta L} \leq u_n \leq P_{\theta H}\ then\ q_n = q_{n-1}$$
$$If\ u_n > P_{\theta H}\ then\ q_n = Q_H,$$

where Q_H, Q_L, $P_{\theta H}$, $P_{\theta L}$ are all positive. Following the treatment of [23], the unipolar constraints are derived by considering the maximum and minimum values of (4.9) for the cases when $q_{n-1} = Q_H$ and when $q_{n-1} = Q_L$. For the first case when $q_{n-1} = Q_H$, u_n is maximised when $x_n = Q_H$ and $u_{n-1} = u_{\max}$. It is minimised when $x_n = Q_L$ and $u_{n-1} = P_{\theta L}$, by inspection of Fig. 4.2. The opposite argument applies to the case of $q_{n-1} = Q_L$, to give

$$u_{\max} = Q_H - Q_L + P_{\theta H} \tag{4.11}$$
$$or\ u_{\max} = Q_H - Q_H + u_{\max} = u_{\max} \tag{4.12}$$

and

$$u_{\min} = Q_L - Q_H + P_{\theta L} \tag{4.13}$$
$$or\ u_{\min} = Q_L - Q_L + u_{\min} = u_{\min}. \tag{4.14}$$

Since equations (4.12) and (4.14) do not provide any information, we can write

$$Q_L - Q_H + P_{\theta L} \leq u_n \leq Q_H - Q_L + P_{\theta H}. \tag{4.15}$$

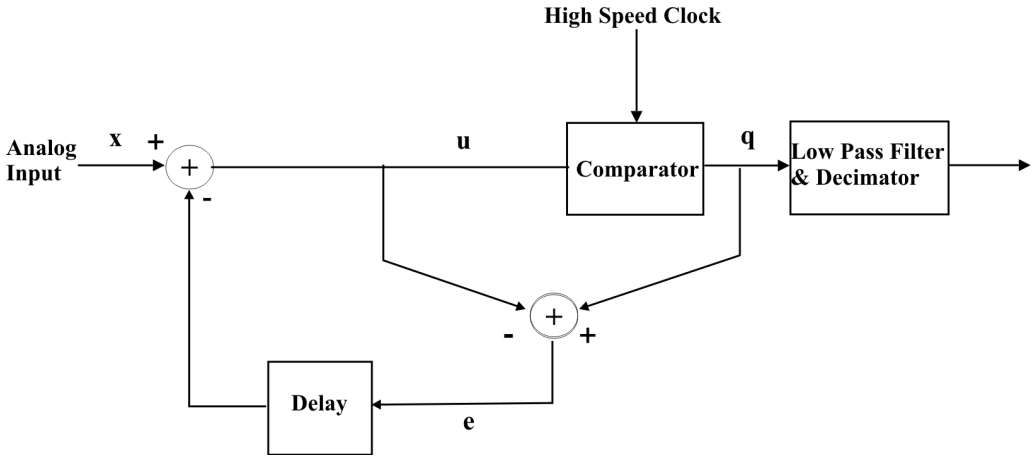

Figure 4.12: Schematic of the oversampled error diffusion architecture.

To maintain unipolarity we require $u_n \geq 0$, therefore the unipolar constraint is

$$Q_H - Q_L \leq P_{\theta L}. \tag{4.16}$$

The reader is referred to [23] for the proof that the condition (4.16) is also necessary and sufficient.

Expressing (4.16) in terms of the contrast ratio CR gives

$$CR = \frac{Q_H}{Q_L} \leq 1 + \frac{P_{\theta L}}{Q_L}. \tag{4.17}$$

4.2.2 Error Diffusion Architecture

A schematic of the alternative first order architecture is given in Fig. 4.12. Compared to the sigma-delta design, the error diffusion has an extra subtractor node. The equations governing the relationship between q_n, u_n, x_n and e_n (error) are

$$\begin{aligned} u_n &= x_n - e_{n-1} \\ e_n &= q_n - u_n. \end{aligned} \tag{4.18}$$

Substitution of (4.18) into (4.18) yields

$$u_n = x_n - q_{n-1} + u_{n-1}, \tag{4.19}$$

which is identical to (4.9), demonstrating that the error diffusion architecture is mathematically equivalent to the sigma-delta. However, an additional unipolarity constraint exists for the error diffusion, since we require $u_n \geq 0$ and $e_n \geq 0$. Following the procedure of the previous subsection, the minimum and maximum values of the error (4.18) can be written as

$$\begin{aligned} e_{\max} &= Q_H - P_{\theta L} \\ or\ e_{\max} &= Q_L - u_{\min} \end{aligned} \tag{4.20}$$

and

$$e_{\min} = Q_H - u_{\max} \tag{4.21}$$

$$or\ e_{\min} = Q_L - P_{\theta H}. \tag{4.22}$$

Substitution of $e_{\min}$ and $e_{\max}$ into (4.18) then yields the following possibilities for u_n

$$u_{\max} = Q_H - Q_H + u_{\max} = u_{\max} \tag{4.23}$$

$$or\ u_{\max} = Q_H - Q_L + P_{\theta H} \tag{4.24}$$

and

$$u_{\min} = Q_L - Q_H + P_{\theta L} \tag{4.25}$$

$$or\ u_{\min} = Q_L - Q_L + u_{\min} = u_{\min}. \tag{4.26}$$

As before, (4.23) and (4.26) yield no information, and the application of $u_n \geq 0$ implies

$$Q_H - Q_L \leq P_{\theta L}. \tag{4.27}$$

However, e_n can now be constrained to

$$Q_L - P_{\theta H} \leq e_n \leq Q_H - P_{\theta L} \tag{4.28}$$

and the constraint $e_n \geq 0$ yields

$$P_{\theta H} \leq Q_L \tag{4.29}$$

as the additional unipolar constraint for the error diffusion architecture.

Since the error-diffusion and sigma-delta architectures are mathematically equivalent, performance simulations will produce identical results when ideal subtractors are used. As the sigma-delta has weaker constraints to maintain unipolarity, only simulations of the sigma-delta are considered in the following sections. The question of which architecture is most appropriate for a photonic implementation will be revisited in Chapter 6 when the performance of a realistic subtractor is analysed.

Finally, for the ideal case, the theoretical quantisation noise power in the signal band (n_0^2) of the sigma-delta can be calculated using the spectral modulation noise density ($N(f)$)[8]

$$N(f) = E(f)\left|1 - e^{-i2\pi f/f_s}\right| \tag{4.30}$$

$$\therefore n_0^2 = \int_0^{f_0} |N(f)|^2 \, df. \tag{4.31}$$

Substituting (4.4) and (4.2)

$$\begin{aligned} n_0^2 &= \int_0^{f_0} \left| 2e_{rms}\sqrt{\frac{2}{f_s}} sin(\frac{\pi f}{f_s}) \right|^2 df \\ &= e_{rms}^2 \frac{\pi^2}{3}(OSR)^{-3} \text{ for } f_s^2 >> f_0^2. \end{aligned}$$

With substitution of (4.1), the SQNR, with input and output normalised by the maximum amplitude of $\frac{Q_H - Q_L}{2}$, is given by

$$SQNR(dB) = 20\ Log(P) + 30\ Log(OSR) - 20Log(\frac{\pi}{3}). \tag{4.32}$$

The only constraint on the frequencies of operation is that the OSR must be an integer.

The minimum resolvable amplitude (q) for the error diffusion and sigma-delta architectures is given by the minimum resolvable amplitude of the PCM architecture,

$$q = \frac{Q_H - Q_L}{OSR}, \tag{4.33}$$

where f_d in (4.8) is set equal to f_s and (4.2) is substituted.

4.2.3 Sigma-Delta Simulations

As with the PCM architecture, the performance of the sigma-delta architecture was studied with both a static and an experimental data based dynamic simulation. In the static case, perfect subtraction and delay were used. The comparator had the same form as Fig. 4.4 and in order to satisfy (4.16) the following parameters were used: $P_\theta = 56.5\,\mu\text{W}$, $P_{fixed} = 60\,\mu\text{W}, Q_H = -2.60\,\text{V}$, $Q_L = -5.48\,\text{V}$. Since optical feedback is used in the sigma-delta architecture, it was necessary to calculate the optical output (P_{out}) of the SEED for a given bias, wavelength and optical input (P_{in}). This was calculated using

$$P_{out}(P_{in}, V, \lambda) = P_{in}\frac{hc}{\eta(V)\lambda e}S(V, \lambda), \tag{4.34}$$

where h is Planck's constant, c the speed of light in air, e the charge of an electron and $\eta(V)$ the carrier collection efficiency[36] of the device. Since our devices did not provide an optical output, we were unable to determine $\eta(V)$ experimentally. Therefore, the carrier collection efficiency was assumed to be equal to published data [35] and calculated using the fitted function

$$\eta(V) = 1 - e^{-0.005(V-1)^6 - 0.5}. \tag{4.35}$$

Assuming a clock power of $P_{clock} = 200\,\mu\text{W}$, combining (4.34) and (4.35) yields the optical output values for the comparator of $Q_H = 105\,\mu\text{W}$ and $Q_L = 91.1\,\mu\text{W}$.

Our aim was to investigate the performance of the S-SEED comparator in dif-

ferent architectures, therefore ideal subtraction and delay were also used in the dynamic simulation. The following parameters were chosen to ensure unipolarity and bistability: $\lambda = 850\,\text{nm},\ V_0 = -7.8V,\ P_{fixed} = 60\,\mu\text{W},\ P_{clock} = 200\,\mu\text{W}$, clock frequency= 1 kHz, input signal frequency= 1 Hz. The S-SEED was clocked in the same manner described in 4.1.1 and only the clock outputs were fedback to the subtractor depicted in Fig. 4.11.

In each case, the SQNR was determined via a power spectrum using an OSR of 100 and the results are presented in the following section.

4.2.4 Sigma-Delta Results

In this section simulations of the first-order Sigma Delta architecture are presented that demonstrate its feasibility and improved performance compared to the PCM design.

The graph presenting SQNR as a function of normalised input amplitude for the static simulation is given in Fig. 4.13. The multiple curves in Fig. 4.13 represent the simulation with hysteresis widths of 0, 16 and 64 μW. The theory of (4.32) is plotted for comparison and approximates the simulated results. There is a 26.2% and 6.6% difference between the slope and offset, respectively of the theory and the line fitted to the zero hysteresis results ($SQNR(dB) = 27.1\ Log(P) + 63.8,\ R = 0.995$).

In contrast to the PCM case, the hysteresis width has only a minor effect on the SQNR performance, as the quantisation error caused by the hysteresis is reduced by the negative feedback between the comparator's output and input. Importantly, the sigma-delta architecture outputs a correctly scaled digitised version of the input, as the negative feedback compares the output to the input. However, for the chosen system parameters the sigma-delta has a smaller input range, compared to the PCM, which accepts input in the range of 0 to P_θ. Whereas, for the sigma-delta it is 0 to $Q_H - Q_L$, when an offset of Q_L is used. Comparing equal normalised input amplitudes reveals that the sigma-delta has up to a 30dB improvement in SQNR over the PCM architecture. This improvement justifies the increase in design complexity.

The comparison of the dynamic and static simulated results are presented in Fig. 4.14 for $\Delta = 19\,\mu\text{W}$. As in the PCM case, little difference is seen between

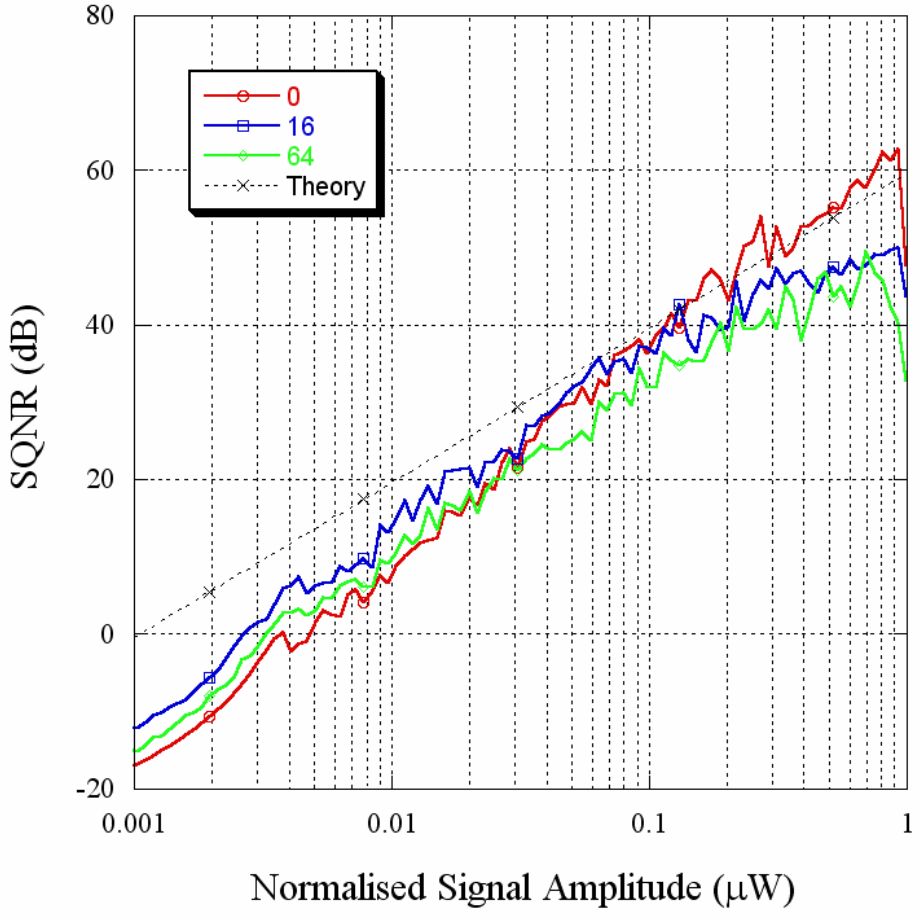

Figure 4.13: The SQNR as a function of input amplitude of the static sigma-delta simulation for hysteresis widths of 0, 16 and 64 μW. The theory is plotted for comparison.

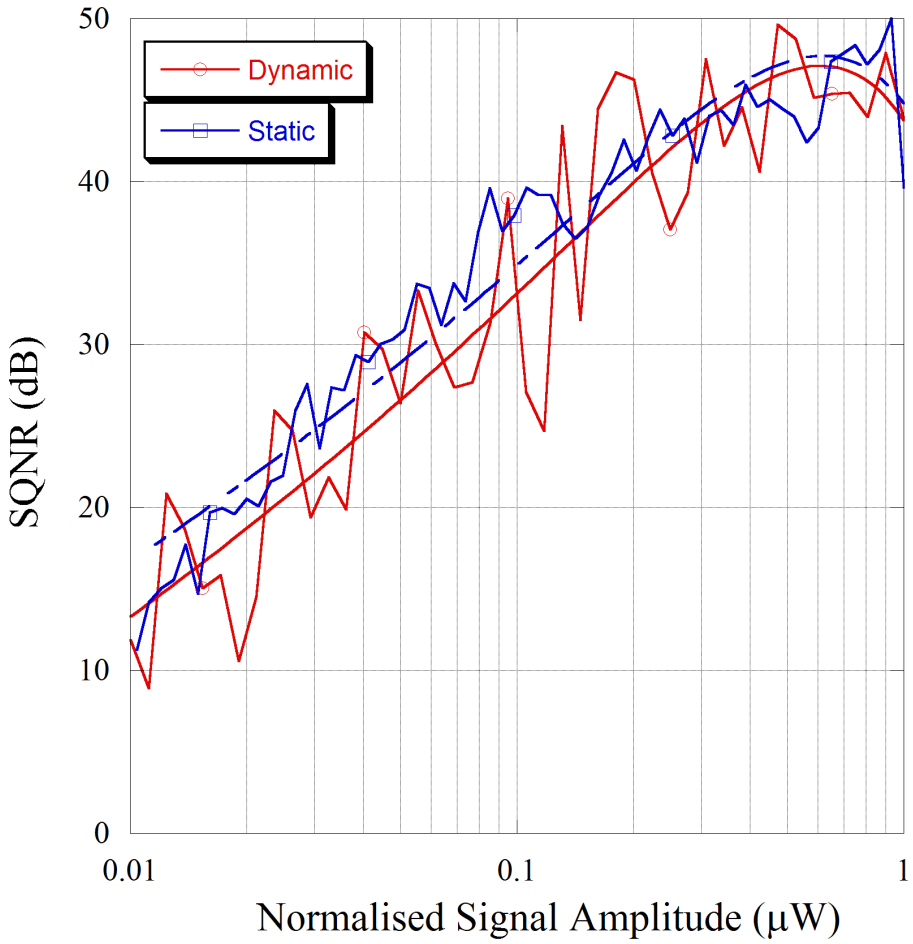

Figure 4.14: SQNR plotted as a function of input amplitude for the static and dynamic simulations of the sigma-delta acrhitecture. To demonstrate the data trend the curves $SQNR(P) = 44.79 + 14.53\log(P) - 46.126P\log(P)$ (R=0.96) and $SQNR(P) = 43.76 + 15.77\log(P) - 51.42P\log(P)$ (R=0.93) are fitted to the static and dynamic results respectively.

the trend of the static and dynamic case, with 7.6% difference in the mean absolute percentage error of the fitted curves. The advantage of the dynamic simulation is demonstrated in Fig. 4.15, a plot of the comparator output for a short period of time. The clocked outputs of the comparator at values of 105 μW and 91.1 μW are seen in Fig. 4.15, and so are the lower power values as a result of the input u to set the comparator state. On many of these comparator levels, a spike in power is seen. This spike is due to the finite time it takes the comparator to settle to a steady state. The speed of the sigma-delta loop must be controlled so that these spikes do not dominate the result, leading to a degradation in SQNR.

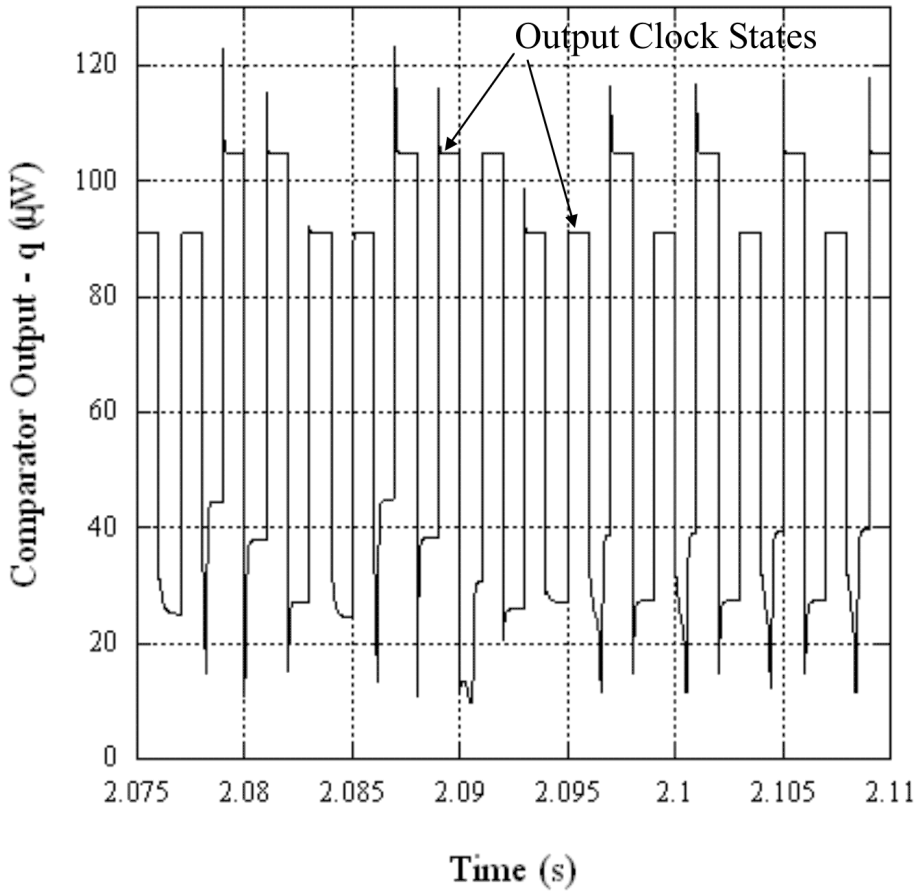

Figure 4.15: Output of the comparator, calculated by the dynamic sigma-delta simulation.

4.3 Summary

The performance of two different photonic A/D architectures utilising an S-SEED comparator has been simulated. First, the PCM was analysed and demonstrated via simulation and experiment. The PCM was then extended in simulation to sigma-delta and error diffusion architectures. The results showed that the sigma-delta architecture produces a much higher SQNR, with reduced sensitivity to hysteresis as compared to the PCM architecture.

Static and dynamic simulations were developed for both architectures. The less computationally intensive static simulation was based on ideal components, hence demonstrated the maximum achievable performance of the quantisers using a comparator with hysteresis. The dynamic simulation included the non-idealities of real devices and the transient behaviour of the S-SEED comparator. Nevertheless, good agreement was demonstrated between the static and dynamic methods. Therefore, the S-SEED comparator has been demonstrated to function correctly.

Following from this work, subtraction using SEEDs is demonstrated in Chapter 6, and the results are integrated into a simulation used to predict real world performance and assist the selection of system parameters to experimentally demonstrate the sigma-delta architecture.

Chapter 5

Microcavity Device Design

To implement the A/D architectures, devices with optical outputs are required. The addition of a Bragg mirror under the quantum wells of a device provides the necessary reflected output and together with the Fresnel reflection from the air-semiconductor interface, creates a Fabry-Perot microcavity. This chapter describes the design and resulting performance of three successive iterations of Fabry-Perot MQW p-i-n device fabrications (also termed REAM) using the Metal-Organo Chemical Vapour Deposition (MOCVD) reactor and processing facilities of the Electronic Material Engineering group at the Australian National University. Section 5.1 describes the issues considered in designing a Fabry-Perot microcavity device. The calculation of the quantum well's refractive index and absorption based upon photocurrent data and the Fabry-Perot's reflectivity spectrum are discussed in Section 5.2. These calculations are used to simulate expected device characteristics, which are input into the comparator and subtractor simulation in Section 5.3 in order to choose the optimum design for our application. Finally, in Section 5.4 the experimental results from the realised devices are compared to the design.

5.1 Design Considerations

To minimise the number of uncertainties in the design process, it was decided to modify the design of the MBE grown chip 436, shown in Fig. 5.1, to produce an

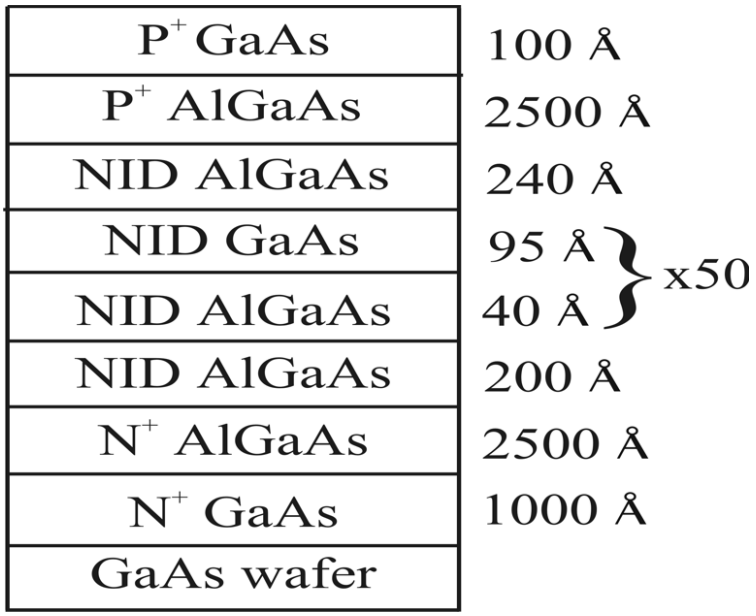

Figure 5.1: Layer structure of p-i-n sample number 436, grown by molecular beam epitaxy (MBE) at Stanford University.

optical output. An optical output can be produced via reflection or transmission. For a transmissive device, the GaAs substrate must be removed, since it absorbs at the design wavelength range of 830-865 nm. Substrate removal is a difficult fabrication step, resulting in very thin and fragile devices. The alternative of a reflective device simplifies fabrication, but produces a Fabry-Perot microcavity that requires increased design complexity and stringent growth tolerances. The growth tolerance can be relaxed by anti-reflection coating the top surface of the device, removing the Fabry-Perot resonance, at the expense of an added fabrication process. However, the Fabry-Perot provides the additional benefit of increased contrast ratio, since rays reflected from the Bragg mirror and the air-semiconductor interface interfere. If the two rays are correctly phase matched, destructive interference eliminates the reflected output, producing an infinite contrast ratio. Furthermore, a reflective device has a greatly increased absorption length as the Fabry-Perot causes the light to pass through the quantum wells multiple times, creating the observed resonantly enhanced absorption. For these reasons a reflective device was the chosen design.

The main aim of our design was to produce a device that could operate as a com-

parator and a subtractor. As was discussed in Chapter 2, the comparator operates in positive feedback mode utilising the negative differential resistance created by the exciton peaks seen in the IV plot. Conversely, the subtractor operates in negative feedback mode, utilising the leading edge of the heavy-hole exciton peak. Due to the negative feedback, this mode of operation has been termed self-linearised [35], and will be discussed further in the next chapter. The Fabry-Perot resonance can be utilised to enhance the dynamic range of the subtractor, by reducing the minimum reflectivity achievable. The analysis of the trade-off of maximising the dynamic range and achieving comparator and subtractor operation at a single wavelength is presented in Section 5.3.

In the event that the growth tolerances required for the correct positioning of the Fabry-Perot resonance were not achievable, it was decided to design the device so that anti-reflection (AR) coating the top surface of the device would remove the resonance. The AR coat reduces the reflectivity of the air-GaAs interface from 31% to less than 1%, effectively eliminating the Fabry-Perot. To enable this design option it was decided to utilise the air-GaAs interface as the top mirror, instead of adding an extra top Bragg mirror which would have allowed greater enhancement of the Fabry-Perot finesse. It is worth noting that in [62], a 31% reflectivity top mirror was found to achieve an optimum compromise between high reflectivity change and low sensitivity to temperature change and wafer growth variation, when compared to high finesse designs using a top Bragg mirror.

One final design consideration was that our devices were to be grown by MOCVD, as opposed to MBE that was employed for chip 436. MOCVD growths are performed at higher temperatures (T), compared to MBE. Since diffusion varies exponentially with 1/T[63], MOCVD has a significantly greater rate of dopant diffusion than MBE, leading to quantum well heterojunctions that are not as abrupt and consequently, a broader exciton peak. As the wavefunction does not add in phase in our multiple quantum well structure, more quantum wells lead to a broader exciton peak. Therefore, to reduce the broadening, the number of quantum wells in the design was decreased from 50 to 40.

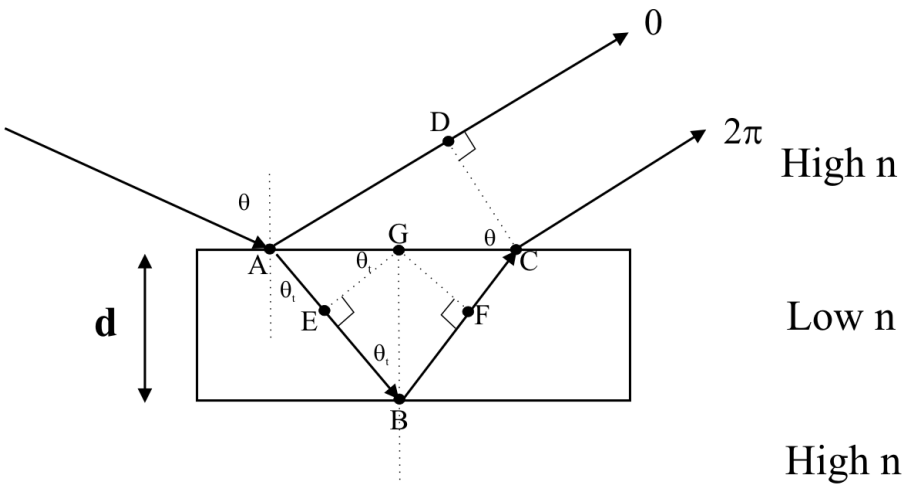

Figure 5.2: A low refractive index layer of thickness d, sandwiched between two high refractive index layers. For high reflectivity, the ray ABC is required to experience a total phase difference of 2π, compared to AD.

5.2 Calculations

The following section describes the calculations used to determine the reflectivity of the total device structure. We first discuss the design for the Bragg mirror, followed by the calculation of the electrorefractive and electroabsorptive contributions of the quantum wells. A detailed discussion of the total optical path length of the device is given.

5.2.1 Bragg Mirror Design

A distributed Bragg reflector is created by growing layers of alternating high and low refractive index materials, such that all the reflected rays add in phase to produce high reflectivity. To calculate the thickness of each layer, consider three such layers, as shown in Fig. 5.2. Following the treatment in [64], Fig. 5.2 depicts the reflection of two rays. The incident ray propagates from a high refractive index material (n_h) to a material with low refractive index (n_l) at an angle of incidence θ. Ray AD undergoes reflection at the first boundary and experiences zero phase shift. The second ray, ABC, propagates from low to high refractive indices, and undergoes a reflection at the second interface that incurs a π phase shift. To ensure

high reflectivity a total phase difference between the two rays of $2\pi k$ (where k is an integer) is necessary. The total optical path difference between the two rays is given by

$$\Delta = n_l(AE + FC + EB + BF) - n_h(AD). \tag{5.1}$$

From inspection of Fig. 5.2

$$AE = AG\sin(\theta_t) = \frac{AC}{2}\sin(\theta_t) \tag{5.2}$$

and

$$AD = AC\sin(\theta). \tag{5.3}$$

Applying Snell's law gives

$$n_h\sin(\theta) = n_l\sin(\theta_t). \tag{5.4}$$

The substitution of (5.3) into (5.2) and the use of Snell's law yields

$$2AE = AC\sin(\theta_t) = AD\frac{\sin(\theta_t)}{\sin(\theta)} = AD\frac{n_h}{n_l}. \tag{5.5}$$

Therefore,

$$n_hAD = 2n_lAE = n_l(AE + FC) \tag{5.6}$$

and (5.1) becomes

$$\begin{aligned}\Delta &= n_l(EB + BF) = 2n_lEB \\ &= 2n_ld\cos(\theta_t).\end{aligned}$$

The phase difference required for constructive interference then becomes

$$\begin{aligned} \varphi = 2\pi k &= \frac{2\pi 2 n_l d\cos(\theta_t)}{\lambda} + \pi \\ \therefore \pi(2k-1) &= \frac{4\pi n_l d\cos(\theta_t)}{\lambda} = q\pi, \end{aligned} \tag{5.7}$$

where q is an odd integer.

For normal incidence ($\theta = 0°$) the thickness required for the rays to add in phase is

$$d = \frac{q\lambda}{4n_l}. \tag{5.8}$$

The same argument applies for a high refractive index material sandwiched between two low refractive index layers, giving the result that for a Bragg reflector the thickness of each layer must be an odd multiple of a quarter of a wavelength (λ) in the given material.

Assuming no absorption, the peak reflectivity of the Bragg mirror with q layers, of thickness d_r and refractive index n_r can be calculated using the characteristic matrix of the thin film stack at normal incidence, defining the elements B and C as[65]

$$\begin{bmatrix} B \\ C \end{bmatrix} \equiv \left\{ \prod_{r=1}^{q} \begin{bmatrix} \cos\delta_r & (i\sin\delta_r)/n_r \\ in_r\sin\delta_r & \cos\delta_r \end{bmatrix} \right\} \begin{bmatrix} 1 \\ n_{q+1} \end{bmatrix}, \tag{5.9}$$

and

$$\delta_r = \frac{2\pi n_r d_r}{\lambda}. \tag{5.10}$$

For an optical thickness of a quarter of a wavelength

$$\delta_r = \frac{\pi}{2}. \tag{5.11}$$

Therefore (5.9) reduces to

$$\begin{bmatrix} B \\ C \end{bmatrix} = \left\{ \prod_{r=1}^{q} \begin{bmatrix} 0 & i/n_r \\ in_r & 0 \end{bmatrix} \right\} \begin{bmatrix} 1 \\ n_{q+1} \end{bmatrix}. \tag{5.12}$$

The reflectivity is then calculated via,

$$r = \left(\frac{1 - C/B}{1 + C/B} \right) \left(\frac{1 - C/B}{1 + C/B} \right)^{*}, \tag{5.13}$$

where $*$ denotes complex conjugate. Therefore, for $2p + 1$ layers surrounded by air and a substrate, the peak reflectivity is given by [65]

$$r_p = \left(\frac{1 - (n_h/n_l)^{2p} (n_h^2/n_s)}{1 + (n_h/n_l)^{2p} (n_h^2/n_s)} \right)^2$$

where n_h, n_l and n_s refer to the high, low and substrate refractive indices. For a given pair of materials with n_h and n_l, the peak reflectivity can be improved by increasing the number of layers. However, the wavelength span of the high reflectivity region, or mirror bandwidth at half width half maximum (HWHM)[66]

$$HWHM = \frac{2}{\pi} \arcsin \left(\frac{n_h - n_l}{n_h + n_l} \right) \tag{5.14}$$

only depends upon the fractional difference of the refractive indices of the chosen materials.

For a design using the $GaAs/AlGaAs$ material system, the choice of materials is constrained by the growth process and the fact that the mirror layers must not absorb at the wavelengths of interest.

Given the bandgap of $Al_xGa_{1-x}As$ in eV [67]

$$E_g = 1.424 + 1.247x, \qquad (0 \leq x \leq 0.415),$$

the refractive index of $Al_xGa_{1-x}As$ [67]

$$n(x) = 3.59 - 0.71x + 0.091x^2$$

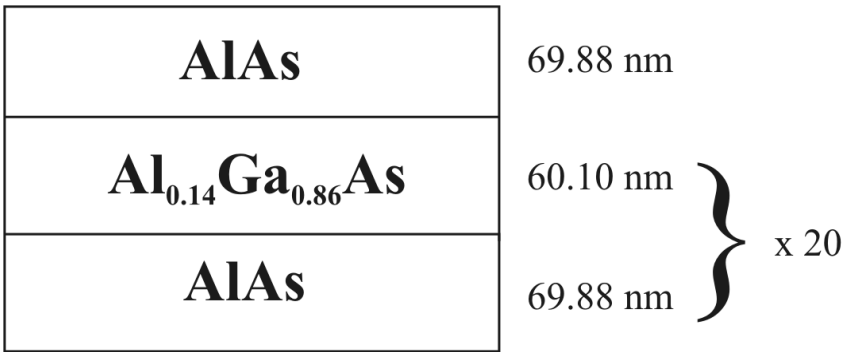

Figure 5.3: Shown is the layer structure for the Bragg mirror centred at 840nm. The mirror designed for the first wafer (growth 239) was the same structure, but centred at 850nm. For that design the layer thicknesses were 71.46 nm for $AlAs$ and 60.96 nm for $Al_{0.14}Ga_{0.86}As$. This structure was not grown independently of the quantum well structure, so we were unable to test the predicted reflectivity directly.

and an effective operating range of 800-900 nm, $AlAs$ was chosen for the low n material and $Al_{0.14}Ga_{0.86}As$ for the high n mirror layers. With regards to the third listed constraint, the MOCVD process allows continuous choice of the Al fraction in AlGaAs, whereas in MBE the growth in practice is limited by the number of different Al cells.

The final issues left to consider are the terminating layers and the total number of layers in the mirror stack. As shown in Fig. 5.2 the pattern of high-low-high refractive indices must be maintained to ensure constructive interference of all the rays. Since the materials surrounding the Bragg stack are both high refractive index ($GaAs$ substrate and $Al_{0.31}Ga_{0.69}As$ buffer), then the stack must consist of an odd number of layers [65], terminated with $AlAs$, or low n layers. Based on numerical calculation, using the transfer matrix method in the software package $Concise\ \ MacLeod$, 20.5 periods of $AlAs$ / $Al_{0.14}Ga_{0.86}As$ layers were chosen to give sufficient peak reflectivity. The final mirror design is shown in Fig. 5.3 and the simulated reflectivity in Fig. 5.4. The peak simulated reflectivity reaches 98.2% and the bandwidth is approximately 105nm, centred at 840nm to allow observation of the light home exciton peak (the heavy-hole exciton was designed to occur at 843 nm).

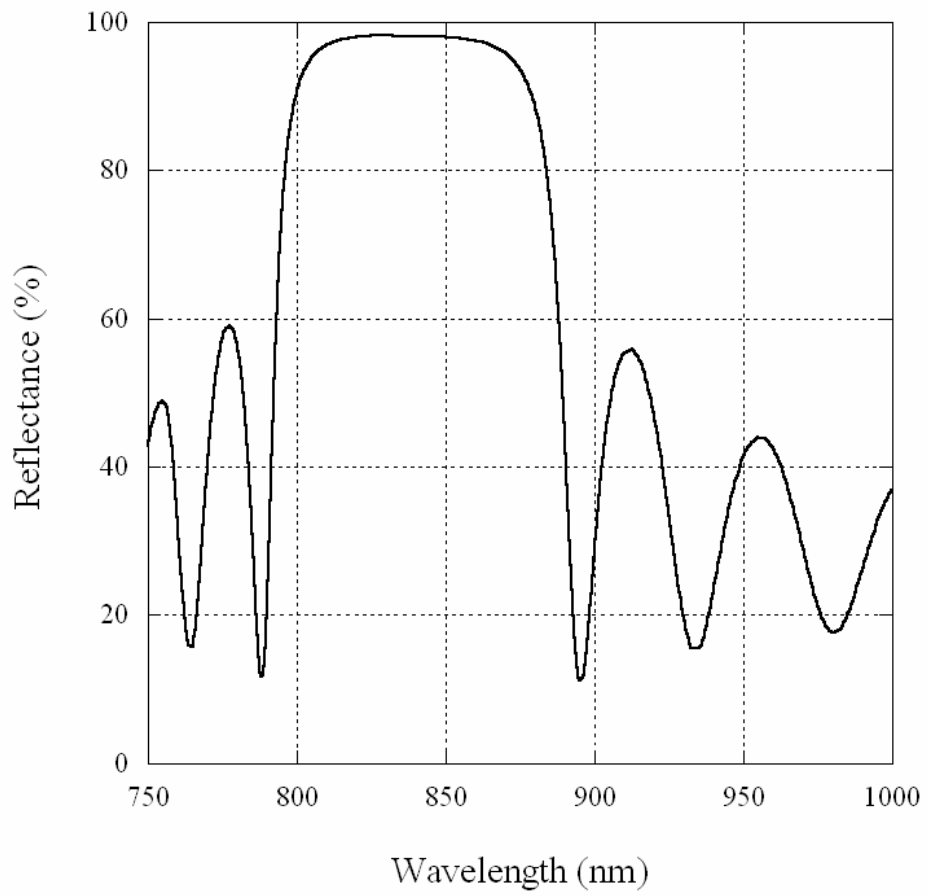

Figure 5.4: Shown is the simulated reflectivity spectrum for the Bragg mirror design of Fig. 5.3, calculated using the software package *Concise MacLeod*. Absorption is included in the numerical calculation.

5.2.2 Quantum Well Absorption Coefficient and Refractive Index

To model correctly the reflectivity of the Fabry-Perot cavity, the variation of absorption coefficient (α) and refractive index (n) of the quantum wells with applied electric field (electroabsorption and electrorefraction) must be included. To calculate α and n of the quantum wells, we have followed the approach taken in [68], namely, experimental responsivity data was used to determine the quantum well absorption coefficient ($\alpha_{QW}(\lambda, V)$), and the Kramers-Kronig transformation was applied to compute the quantum well refractive index ($n_{QW}(\lambda, V)$).

The absorption coefficient was calculated using [69]

$$\alpha_{QW}(\lambda, V) = -\frac{b}{W} \ln \left[1 - \frac{S(\lambda, V) hc}{e\lambda\eta(1-R)} \right] \tag{5.15}$$

where W is the total thickness of the wells, not including the barriers, $S(\lambda, V)$ the experimentally measured responsivity of the diode with units of A/W, h Plank's constant, c the speed of light in vacuum, λ the wavelength of the incident light, e the charge of an electron, η the quantum efficiency (the number of electron-hole pairs created per absorbed photon) and R is the reflectivity of the front surface of the diode. The term b is a correction factor that accounts for experimental losses and is used to match the zero field absorption peak to the value of $\alpha_{QW}(\lambda, 0) = 20000\ \mathrm{cm}^{-1}$ reported in the literature[70],[68]. The calculated absorption is shown in Fig. 5.5 for $R = 0.31$ and $\eta(V) = 1$ with applied voltages from 0 to $6V$. The assumption of unity quantum efficiency was shown to be valid in [71] for devices with thin barriers ($35\mathring{A}$) in the quantum wells, which is the case with our structure.

Given the particular form of the Kramers-Kronig transformation used in [62]

$$\Delta n(\lambda, V) = \frac{1}{2\pi^2} P \int_0^\infty \frac{\Delta\alpha(\lambda', V)}{\left[1 - \left(\frac{\lambda'}{\lambda} \right)^2 \right]} d\lambda', \tag{5.16}$$

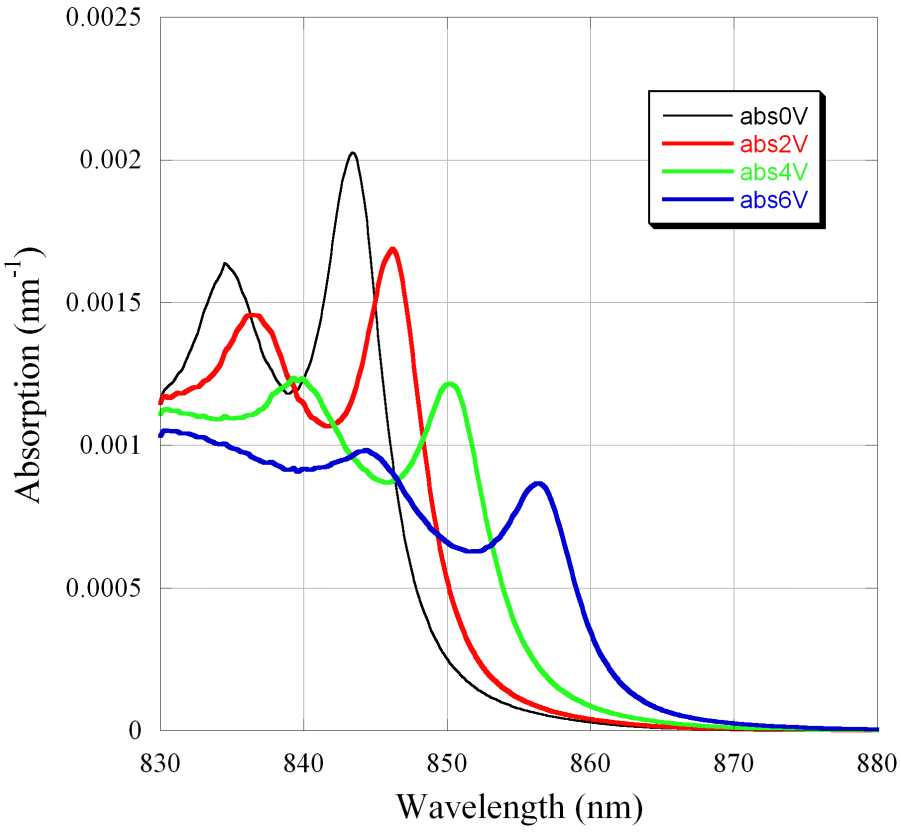

Figure 5.5: Calculated absorption coefficient per nm as a function of wavelength for applied voltages of $0V$, $2V$, $4V$, and $6V$.

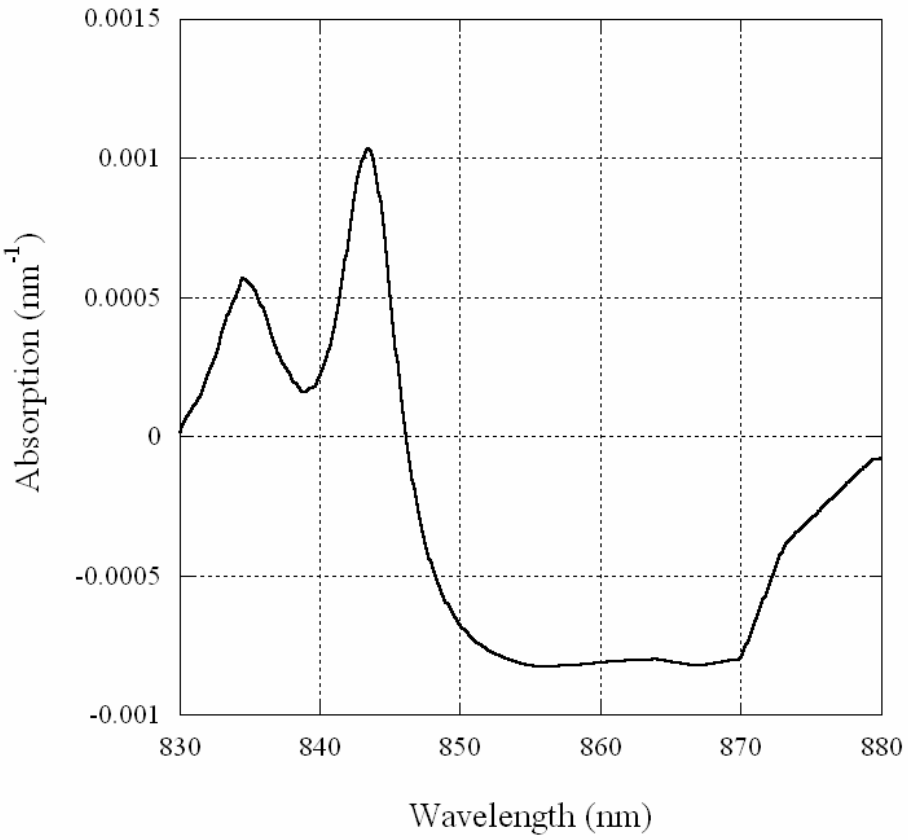

Figure 5.6: Calculated absorption difference of the quantum wells and bulk GaAs per nm as a function of wavelength for an applied voltage of $0V$.

where P is the Cauchy principal

$$P\int_0^\infty f(x)dx = \lim_{\delta\to 0}\left[\int_0^{\lambda-\delta} + \int_{\lambda+\delta}^\infty\right] f(x)dx \tag{5.17}$$

which is used to accommodate the singularity at $\lambda' = \lambda$, and where $\Delta\alpha(\lambda, V)$ is defined by

$$\Delta\alpha(\lambda, V) = \alpha_{QW}(\lambda, V) - \alpha_{GaAs}(\lambda), \tag{5.18}$$

then the integral (5.16) is simplified by the use of $\Delta\alpha(\lambda, V)$, as it is zero beyond the wavelength range where the quantum wells no longer absorb light. Using (5.18), $\Delta\alpha(\lambda, 0)$ was calculated and the result is plotted in Fig. 5.6. The absorption coefficient for bulk $GaAs$ ($\alpha_{GaAs}(\lambda)$) was calculated from the extinction coefficient

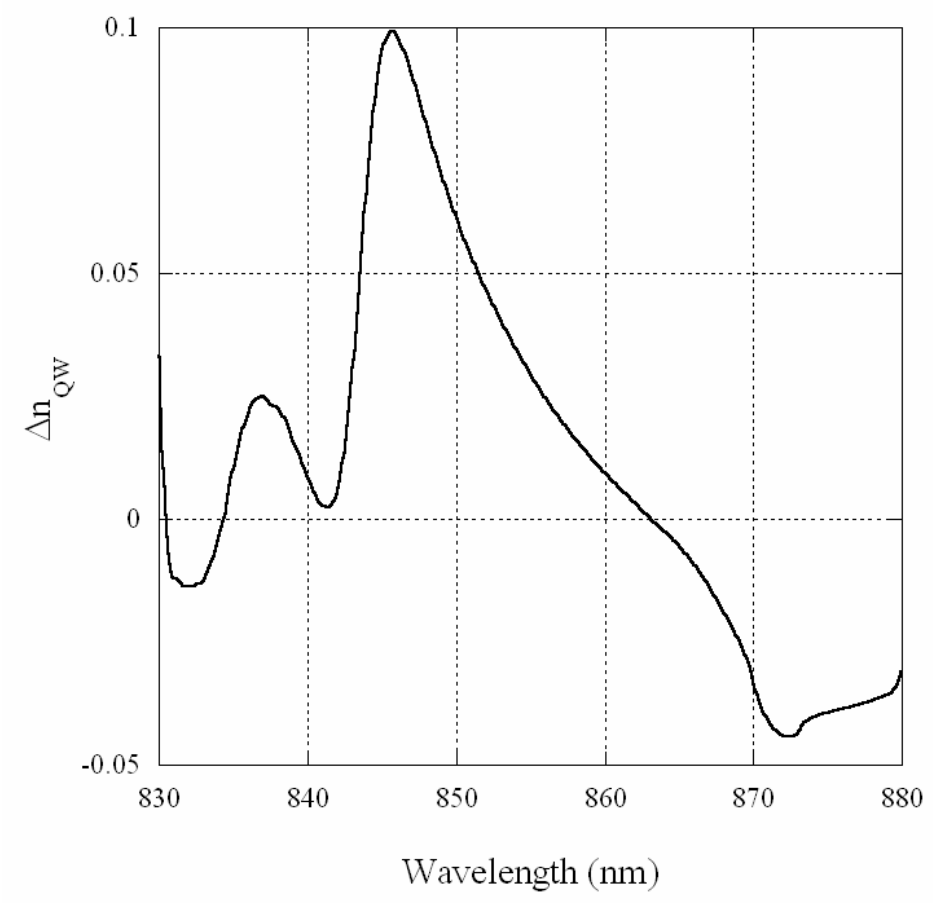

Figure 5.7: Calculated difference in refractive index between the quantum wells and bulk GaAs for an applied bias of $0V$.

(k) data of [72] by

$$\alpha(\lambda) = \frac{4\pi k(\lambda)}{\lambda}. \tag{5.19}$$

The application of the Kramers-Kronig transformation to $\Delta\alpha(\lambda, V)$, yields $\Delta n(\lambda, V)$, where

$$\Delta n(\lambda, V) = n_{QW}(\lambda, V) - n_{GaAs}(\lambda). \tag{5.20}$$

Figure 5.7 depicts a plot of $\Delta n(\lambda, 0)$.

5.2.3 Fabry-Perot Reflectivity

Having calculated all the necessary components, the calculation of the reflectivity of the Fabry-Perot is now considered. The reflectivity of the total Fabry-Perot structure for free space wavelength λ and applied voltage V is given by [73]

$$R(\lambda, V) = \frac{(\sqrt{r_1} - t(\lambda, V)\sqrt{r_2})^2 + 4t(\lambda, V)\sqrt{r_1 r_2}\sin^2\phi(\lambda, V)}{(1 - t(\lambda, V)\sqrt{r_1 r_2})^2 + 4t(\lambda, V)\sqrt{r_1 r_2}\sin^2\phi(\lambda, V)} \tag{5.21}$$

where r_1 and r_2 are the reflectivity coefficients of the top and bottom lossless mirrors respectively (i.e. $r_{1,2}+t_{1,2} = 1$). The single pass transmission coefficient, t, is defined by

$$t(\lambda, V) = \exp(-\alpha_{QW}(\lambda, V)L_w N) \tag{5.22}$$

where L_w is the quantum well width and N is the number of quantum wells. For a composite structure such as Fig. 5.1, with layers having thickness L_i and refractive index $n_i(\lambda, V)$, the phase shift ϕ of the total structure is

$$\phi(\lambda, V) = 2\pi \sum_i \frac{n_i(\lambda, V)L_i}{\lambda}. \tag{5.23}$$

Contributing to the sum in the calculation of ϕ are the bulk layers of $GaAs$ and $AlGaAs$, the quantum wells with refractive index $n_{QW}(\lambda, V)$, the quantum well barriers with refractive index of the bulk material, and finally the Bragg mirror of reflectivity r_2 adds a phase and penetration depth L_{Bragg}.

To identify a penetration depth of the Bragg mirror, at which the energy falls to $\frac{1}{e}$ of the initial value, it is assumed that it is a linear phase reflector, and can be modelled as a fixed phase mirror at a distance L_{Bragg} into the original mirror. The penetration depth at the mirror's centre wavelength (λ_0) is then given by [74]

$$L_{Bragg}(\lambda_0, m) = \frac{\lambda_0}{4}\frac{q}{1-p}\frac{(1 - a^2p^{m-1})(1 - p^m)}{(1 - q^2a^2p^{2m-2})} \tag{5.24}$$

where m is the number of layers in the mirror and the parameters p, a and q are ratios of refractive indices. The parameter $p = n_l/n_h$, while a is given by the ratio

of refractive indices at the exit interface, $a = n_l/n_{GaAs}$ in our case. The final factor q is the ratio of the refractive indices at the incident interface, and for our structure $q = n_l/n_{AlGaAs}$. In the case when $n_h - n_l << n_l$ [74], (5.24) can be approximated to

$$L_{Bragg\_approx}(\lambda) = \frac{\tanh(\kappa L)}{2\kappa}, \tag{5.25}$$

where $\kappa = 2(n_h - n_l)/\lambda$ and L is the total mirror length. In several cases in the literature [73],[68],[66] the value of the phase contribution of the mirror used in the calculations was

$$\phi_{Bragg}(\lambda) = \frac{2\pi}{\lambda}\frac{n_h + n_l}{2}L_{Bragg\_approx}(\lambda). \tag{5.26}$$

For a mirror surrounded by high index material, the model of a fixed phase mirror contributes a phase shift of zero at the centre wavelength (λ_0). However, at $\lambda = \lambda_0$ (5.26) is not equal to zero, therefore leads to erroneous calculated reflectivity spectra. The correct analytic expression for the total contribution of the Bragg mirror to the phase shift $\phi(\lambda, V)$ is given by [74]

$$\phi_{Bragg}(\lambda) = \frac{2\pi}{\lambda}L_{Bragg}(\lambda_0, m) - \frac{2\pi}{\lambda_0}L_{Bragg}(\lambda_0, m). \tag{5.27}$$

The difference between (5.26) and (5.27) can be significant when the approximation $n_h - n_l << n_l$ is not valid and $\lambda \neq \lambda_0$.

The position of the Fabry-Perot resonance is defined as the wavelength at which the reflectivity of a lossless cavity has a minimum[68]. The resonance occurs when $\phi(\lambda, V)$ is equal to an odd multiple of π. For a cavity without absorption and a mirror with $\lambda_0 = 840\,\text{nm}$, it was calculated that the position of the Fabry-Perot resonance was equal to 852 nm using (5.27) and 845 nm when the erroneous expression (5.26) for the phase of the Bragg mirror was used. Even though the error caused by the use of (5.26) is less than 1%, that error can have a significant effect on device performance.

5.2.4 Anti-Reflection Coating Design

As a contingency plan for the situation where we were unable to fabricate the Fabry-Perot resonance at the correct position, the structure was designed to provide the option of an anti-reflection coating that would remove the Fabry-Perot resonance. Therefore, it was necessary to design a coating that was easy to fabricate with the available equipment. Two common dielectric materials, with reasonable refractive index difference that we had available were SiO_2 and TiO_2. Several AR coating designs are described in [75], but the simplest possible design consists of one layer, a quarter of a wavelength thick, with refractive index of

$$n = \sqrt{n_0 n_s}, \tag{5.28}$$

where n_0 is the refractive index of air and n_s is the refractive index of the coated material. For our case at 840 nm, *GaAs* has a refractive index of 3.65. Therefore, we would require a material with $n = 1.91$. At 840 nm the refractive indices of SiO_2 and TiO_2 are 1.45 and 2.78, respectively. Therefore, more complex designs are required. A two layer design is possible that uses two different materials to form an average refractive index equal to that given in (5.28), but the reflectivity is low only over a narrow bandwidth. A three layer design that uses three different materials can be used to increase that bandwidth, but this is more complex to fabricate than a 4 layer design that only uses two different materials. The four layer design arranges the materials in a low-high-low-high pattern of refractive indices with thicknesses of $\lambda/4 - \lambda/2 - \lambda/2 - \lambda/4$. This design was used as a starting point for the nonlinear simplex refinement algorithm employed in the software package *Concise MacLeod*. The final parameters of the design are given in the table below.

Layer	Material	Refractive Index	Layer Thickness (nm)
1	SiO_2	1.453	128.2
2	TiO_2	2.780	130.7
3	SiO_2	1.453	266.3
4	TiO_2	2.780	69.8
Device	GaAs	3.645	

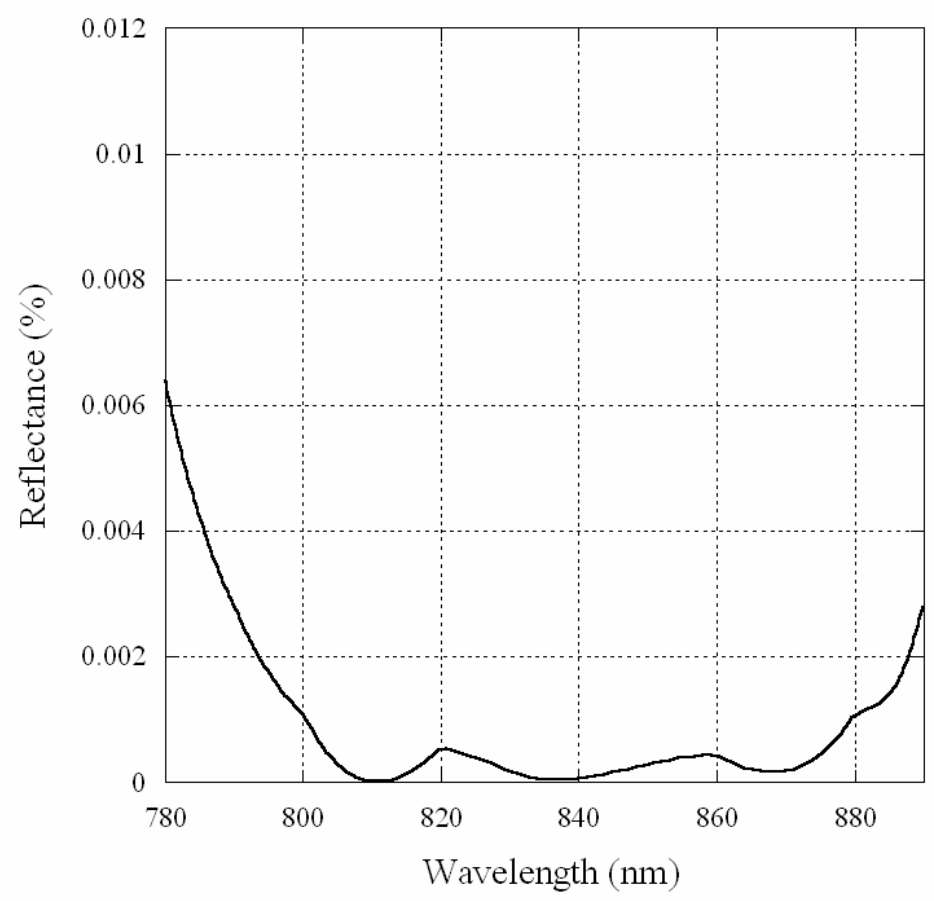

Figure 5.8: Numerically simulated reflectivity spectrum of the AR coating design.

The numerically simulated reflectivity spectrum of the AR coating design is given in Fig. 5.8. The reflectivity of the design is very low, having been calculated to be less than $4.4 \times 10^{-4}\%$ over the operating range 830-870 nm. Additionally, it is relatively straight-forward to fabricate. However, as will be seen in Section 5.4, the AR coating was not required, as the desired device performance was achieved. Therefore the AR coating design was not fabricated to enable testing of the prediction of Fig. 5.8.

5.3 Expected Performance

As discussed in Section 5.1, the quantum well structure was constrained to forty 9.5 nm $GaAs$ wells with 4.0 nm $Al_{0.31}Ga_{0.69}As$ barriers. A Bragg mirror design was described in Section 5.2 and to allow AR coating to eliminate the Fabry-Perot, a

top mirror formed by the air-$GaAs$ interface was chosen. The only parameter in the device design left to choose is the thickness of the p and n doped $Al_{0.31}Ga_{0.69}As$ layers, which affect the wavelength position of the Fabry-Perot resonance.

Three general possibilities exist for the positioning of the Fabry-Perot resonance. Firstly, it can be made resonant with the zero field heavy-hole exciton peak, forming a normally off modulator [73]. For this case the reflectivity will be low for zero applied electric field, when operated at the wavelength of the heavy-hole exciton absorption peak. If the Fabry-Perot resonance is positioned at a wavelength sufficiently longer than the zero field exciton peak, a normally on modulator is formed when operated at the wavelength of the Fabry-Perot resonance. That is, the reflectivity is high for zero applied field and decreases to a minimum when the applied electric field shifts the heavy-hole exciton to the position of the Fabry-Perot resonance. Finally, the Fabry-Perot resonance can be shifted outside the bandwidth of interest, provided the free spectral range is sufficiently large.

A common motivation for using a Fabry-Perot cavity around a MQW device is to increase the contrast ratio [73] of a single SEED used as a modulator. However, for the S-SEED in our comparator application discussed in Chapter 2, the contrast ratio is not greatly affected by the Fabry-Perot. This is because the two devices in an S-SEED are connected electrically in series, therefore the same current must pass through each device. When the S-SEED is clocked by two equal power beams, equal currents will pass through each SEED, causing each device to absorb the same optical power. Therefore, the same power is reflected from each device. Thus the only way to achieve a contrast greater than one between the two bistable states of an S-SEED is to utilise the voltage dependence of carrier collection efficiency (η) [36]. The carrier collection efficiency is defined as the fractional number of electrons collected by the circuit per absorbed photon [71] and is ideally one. For quantum well structures with thin barriers, forward bias voltages greater than approximately 0.5 V [71] oppose the in-built electric field of the p-n junction creating a nett electric field that is no longer strong enough to sweep out all the carriers in the intrinsic region of the device. This allows some carriers to recombine, reducing the carrier collection efficiency below one. If one of the two bistable states of the S-SEED

is above 0.5 V then this SEED will need to absorb more light to produce enough current, producing a contrast ratio greater than one. Further, it will be shown in the following chapter that a contrast ratio of less than two is a condition to achieve unipolar operation of the quantiser. Therefore, it is desirable to use the Fabry-Perot to enhance the dynamic range when the SEED is used as a subtractor. The condition on the position of the Fabry-Perot resonance then becomes that the placement must enhance the dynamic range of subtraction at a wavelength where the S-SEED can also operate in a bistable mode.

To analyse the trade-off and find an optimum solution, a simulation was performed to determine the dynamic range of a subtractor formed by a photodiode and a SEED as a function of the device structure. The reflectivity was calculated using the method discussed in Section 5.2.3 as the thickness of the doped $AlGaAs$ layers in Fig. 5.1 were adjusted to vary the Fabry-Perot resonance position. The responsivity data used in the simulation was determined from the calculated reflectivity via

$$S(\lambda, V) = \frac{\eta(V)\ e\ \lambda}{hc}(1 - R(\lambda, V)), \tag{5.29}$$

assuming $\eta(V) = 1$ for $V < 0$. The dynamic range was defined as the difference between the incident power on the photodiode that set the SEED within 5% of the peak responsivity and 5% of the responsivity at 0 V. Figure 5.9 illustrates the principle. To express the dynamic range as a percentage, the calculated difference was divided by the fixed power incident on the SEED. The dynamic range was calculated as a function of operating wavelength for different positions of the Fabry-Perot resonance. The results for the maximum dynamic range for each different Fabry-Perot position are presented in Fig. 5.10.

Figure 5.10 demonstrates that the position of the Fabry-Perot resonance has a significant effect on the dynamic range of a subtractor. The maximum dynamic range of 56.5% for forty 9.5 nm quantum wells occurs when the Fabry-Perot peak is placed at 857 nm and the wavelength of operation is 862.5 nm. However, we require that an S-SEED operating at such a wavelength must also exhibit bistability with an applied voltage (V_0) of 10 V or less. Applying this constraint to the simulations produced the results presented in Fig. 5.11. Figure 5.11 depicts the maximum

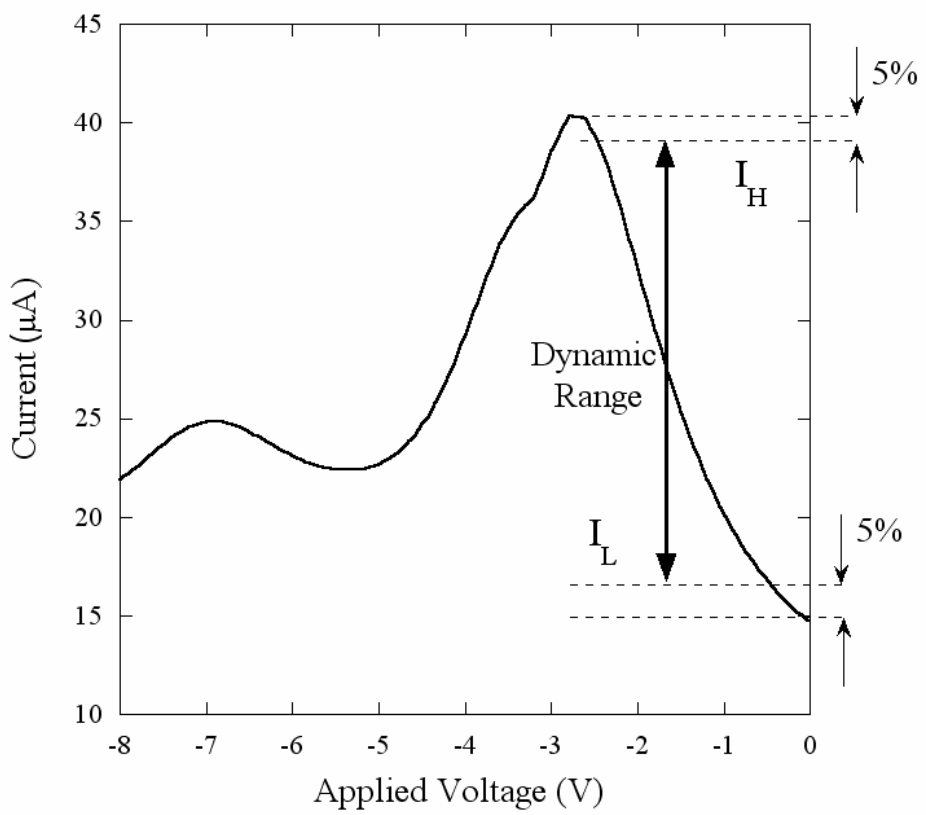

Figure 5.9: Illustration of the technique used to measure the dynamic range of a subtractor as $P_H - P_L$ for a fixed power of 100 μW applied to the SEED. The labels I_H and I_L correspond to the current produced by the photodiode for applied powers P_H and P_L.

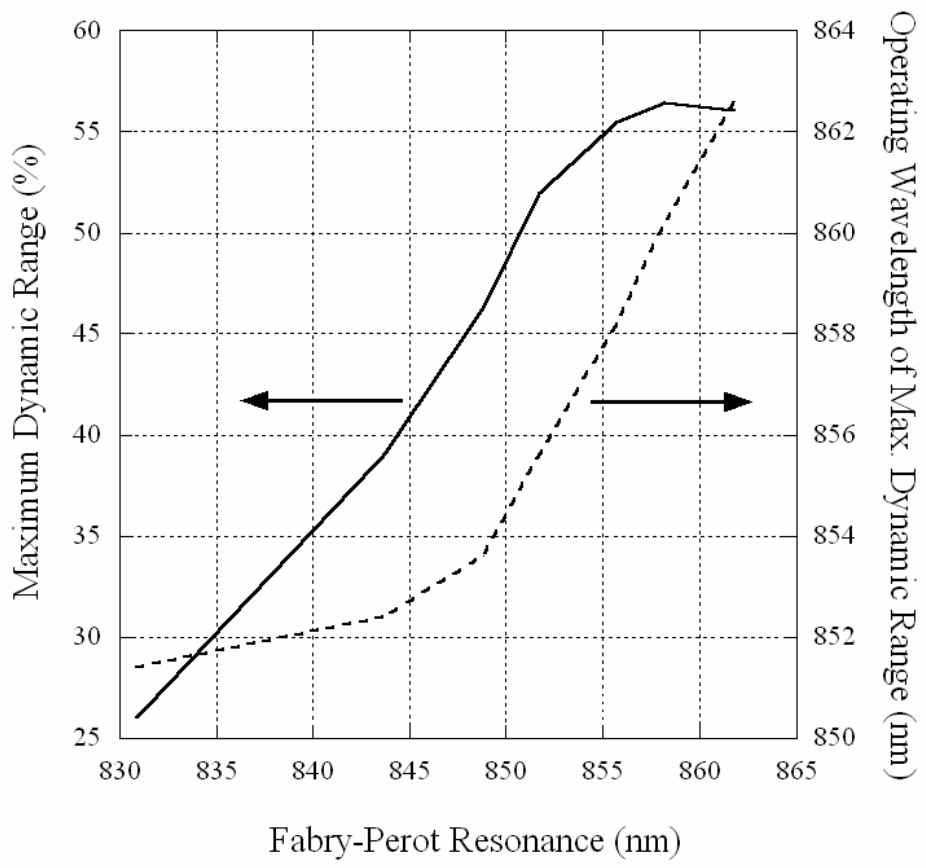

Figure 5.10: The maximum dynamic range of a photodiode-SEED subtractor is presented as a function of the position of the Fabry-Perot resonance. The right hand axis identifies the operating wavelength where the maximum dynamic range occurs.

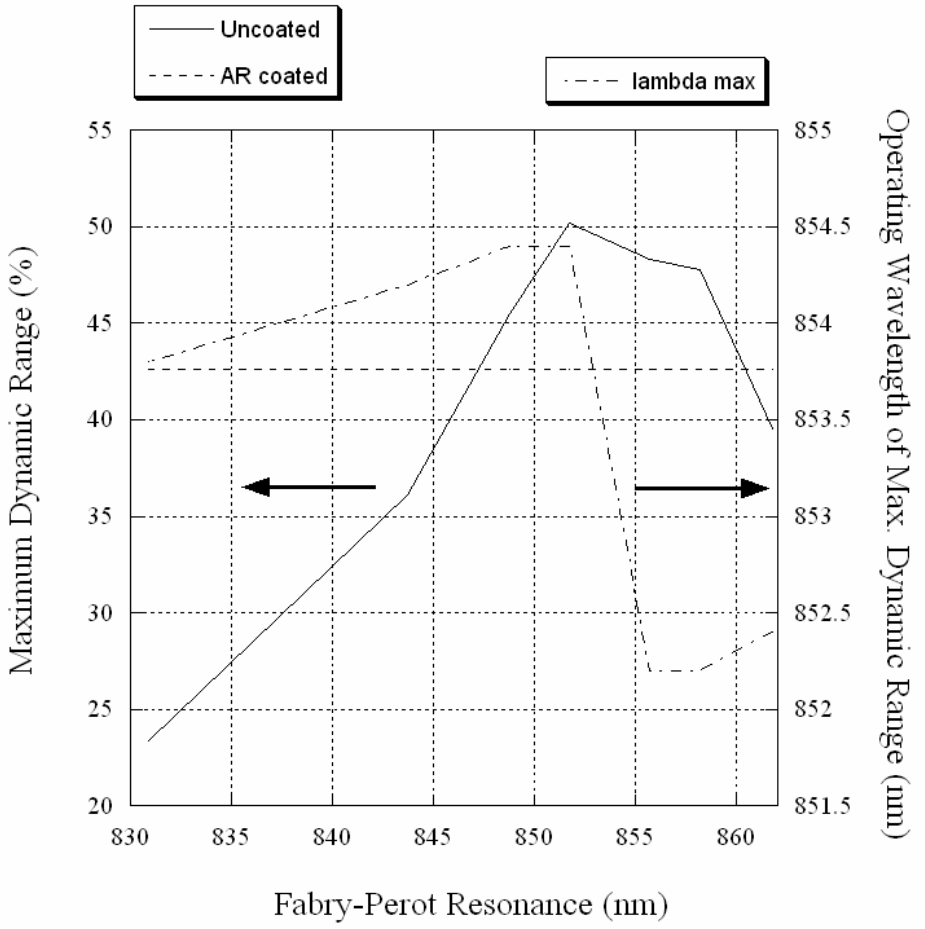

Figure 5.11: Maximum dynamic range as a function of Fabry-Perot position for an operating wavelength where an S-SEED will operate in bistable mode. The dynamic range of an anti-reflected coated SEED, with a top surface reflectivity of 0, is added for comparison. The right hand scale plots the operating wavelength of the maximum dynamic range, as in Fig. 5.10.

dynamic range for different Fabry-Perot resonance positions on the left axis and the operating wavelength on the right hand axis. With the application of this constraint, the maximum dynamic has been reduced to 50.2% at a Fabry-Perot position of 851.7 nm and an operating wavelength of 854.4 nm. The dynamic range of an AR coated device is presented for comparison, demonstrating that the Fabry-Perot design enhances the available dynamic range by around 8%. Even greater improvement is possible with the use of a matched cavity, where the ray reflected from the top surface of the Fabry-Perot is equal in amplitude to the ray reflected from the bottom Bragg mirror, that undergoes absorption from two passes through the quantum wells. If this condition, expressed as [73]

$$r_1 = r_2 t^2, \tag{5.30}$$

is met, the total reflectivity (from (5.21)) becomes

$$R(\lambda, V) = \frac{4t^2(\lambda, V) r_2 \sin^2 \phi(\lambda, V)}{1 + t^4(\lambda, V) r_2^2 - 2 r_2 t^2(\lambda, V) \cos 2\phi(\lambda, V)} \tag{5.31}$$

and is equal to zero when $\phi(\lambda, V) = 0$, demonstrating that complete destructive interference is possible. However, to achieve a matched cavity in our case would have produced the undesirable consequences of added complexity caused by a top Bragg mirror of greater reflectivity that the air-$GaAs$ interface, or additional exciton broadening due to more quantum wells.

Therefore, Fig. 5.11 permits the choice of the optimum design, where the subtractor dynamic range is maximised whilst maintaining bistable operation. The thickness of doped the $Al_{0.31}Ga_{0.69}As$ layers that produces a Fabry-Perot resonance at 851.7 nm is 236 nm. The final device structure is presented in Fig. 5.12.

5.3.1 Photon Lifetime

One final design issue to consider is the photon lifetime in the Fabry-Perot cavity. If the lifetime is sufficiently long, it would ultimately limit the switching time of an

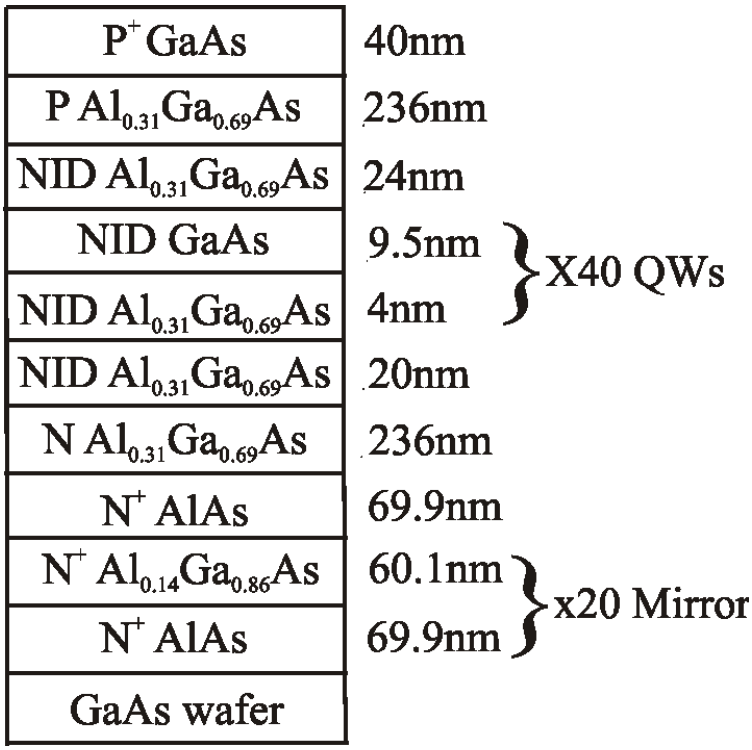

Figure 5.12: Layer structure of optimum design with Fabry-Perot cavity. (NID = Not Intentionally Doped)

S-SEED comparator. We calculate the photon lifetime (t_{ph}) according to[76]

$$t_{ph} = \frac{n}{c[\alpha - (1/l)\ln\sqrt{r_1 r_2}]}, \tag{5.32}$$

where n is the average distributed refractive index, c is the speed of light in vacuum, α is the average distributed absorption in the cavity, l is the cavity length and r_1 and r_2 are the two mirror reflectivities. For our device design the photon lifetime is calculated to be 0.01 fs. Therefore, due to the low air-semiconductor interface reflectivity and large intracavity absorption, the photon lifetime will not limit the device switching time.

5.4 Results

A total of three wafer growth and device fabrications were performed by the EME group at ANU to achieve the desired Fabry-Perot resonance position. This section analyses the results of simulated and experimental reflectivity and responsivity spectra for each of the growths. The details of each of the growths is summarised in Appendix C.

Before discussing the experimental results, a simulation of a reflectivity spectrum for the structure of Fig. 5.12 is presented using two different methods. The first method is that described in Section 5.2, while second method uses the *Concise MacLeod* numerical simulation package. To represent the quantum wells in *Concise MacLeod* a layer with the absorption and refractive index of the 40 quantum wells was used in the simulation. The comparison is presented in Fig. 5.13. The positions of the excitons and Fabry-Perot resonance coincide in both simulations, demonstrating the accuracy of the analytic expression. The difference in the two curves is due to the improved accuracy of the mirror reflectivity in the numerical simulation.

5.4.1 Experiment

With the addition of a mirror to the device design, an additional parameter was required to be measured for the new devices, namely reflectivity. Therefore, to

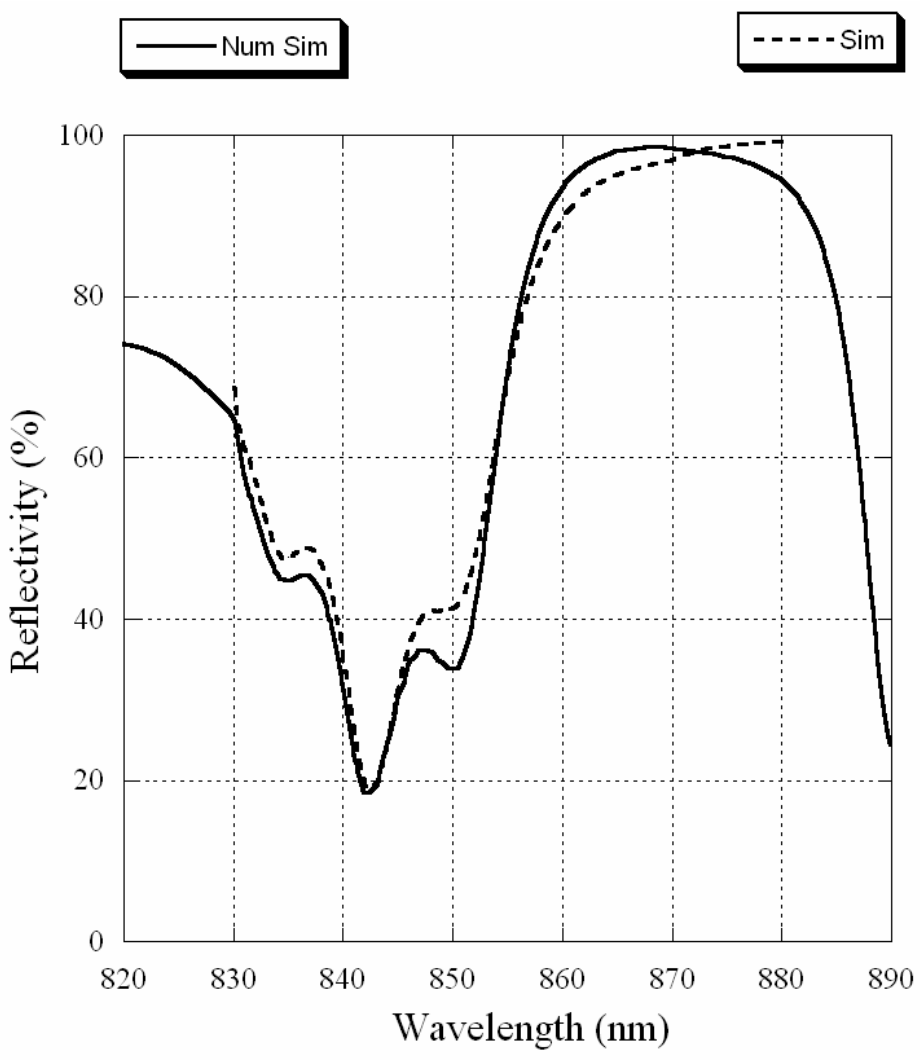

Figure 5.13: Comparison of simulations of reflectivity using *Concise MacLeod* (solid line) and the analytic expression of (5.21) (dashed line).

accurately model the new devices, it was necessary to extend the characterisation experiment, described in Section 3.2, to measure reflectivity with amplitude noise of less than 1%. A schematic of the experiment to measure responsivity and reflectivity as a function of wavelength and applied voltage is given in Fig. 5.14. A tunable Ti:Sapphire ring laser, which was coupled to a noise eater to remove amplitude fluctuations, was used as the source. A beamsplitter sampled the output of the laser to enable measurement of the wavelength by a Burleigh WA1000 wavemeter. The wavelength of the laser was controlled by a Newport 850B linear actuator driven by a Newport ESP300 driver. The beam power was controlled by a neutral density filter wheel and was measured using a beamsplitter to direct a portion of the beam onto a Silicon detector head of a Newport 2832C power meter. To allow measurement of the power reflected from the SEED, a half waveplate, polarising beam splitter and quarter waveplate were set up as depicted in Fig. 5.14 to enable separation of the incident and reflected beams. A Keithley K236 source meter applied voltage (V_0) and measured current passing through the SEED. All the instruments communicated via GPIB to a computer that controlled the experiment and collected data, as described in Section 3.2. Reflectivity was calibrated in the experiment by placing a high reflectivity Newport dielectric mirror (part number 10D20BD.2) in front of the SEED, and measuring the optical loss incurred in the experiment. Results of the characterisation are presented in the following subsection, but amplitude noise achieved for the reflectivity measurements was very low. Using the same technique employed in Section 3.3, the amplitude noise for the results of Fig. 5.15 was determined to be 0.13%

5.4.2 Characterisation Results

The first wafer growth (labelled 239) was intended to test if the MOCVD growth and fabrication process used at ANU was sufficient to provide material with resolved excitons. To simplify observation of the excitons, the Fabry-Perot resonance was designed to occur at a wavelength past the bandedge (at 870 nm), approximately half a free spectral range from the expected heavy-hole exciton peak. This was achieved by specifying the thickness of the doped $Al_{0.31}Ga_{0.69}As$ layers at 145 nm. The exper-

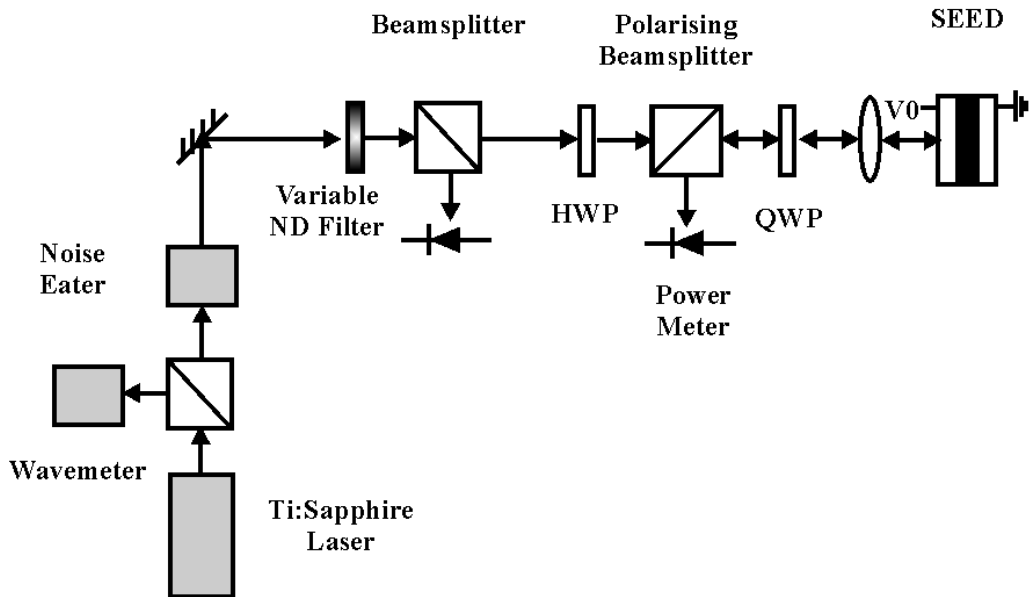

Figure 5.14: Schematic of the experiment to characterise the responsivity and reflectivity of the SEEDs. (QWP and HWP and abbreviations for quarter and half wave plates, respectively.)

imentally determined reflectivity and responsivity curves as functions of wavelength and applied voltage are shown in Fig. 5.15 and Fig. 5.16, respectively. A comparison of the zero-field reflectivity spectra for the simulation and experiment is also shown in Fig. 5.17. Figures 5.15 and 5.16 illustrate the quadratic red-shift of the heavy-hole exciton peak as a function of bias[31], and the zero-field exciton position of 842 nm. These features agreed with expectation from the simulation and demonstrated that material was of sufficiently high quality that the heavy-hole exciton peak is resolved. However, the Fabry-Perot resonance, which is identified as the peak that does not shift with voltage, occurs at around 835 nm. This result departs from the simulated position of 870 nm, as shown in Fig. 5.17. The discrepancy is caused by variation of layer thicknesses in the Fabry-Perot cavity from that specified. The tolerance in the growth process is around 5%, however, this growth error can be treated as a systematic error, and compensated for, if the growth process is repeated within a short period of time. The observed error is consistent with the growth tolerance specification, as a total cavity thickness error of 4% is required in the simulation to reproduce a resonance position of 835 nm. The realised position

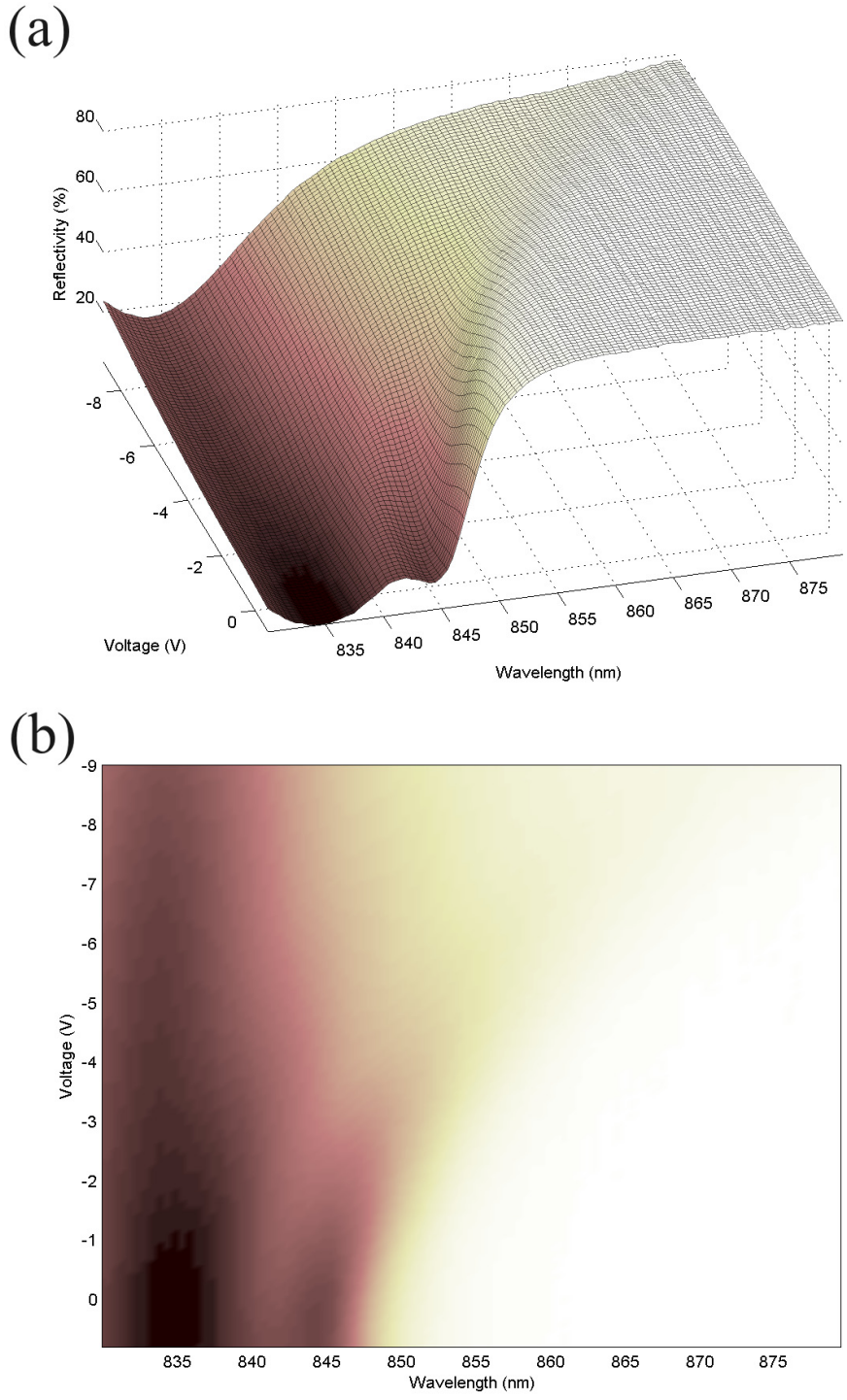

Figure 5.15: (a) Measured reflectivity as a function of wavelength and voltage for the first wafer (labelled 239). (b) Projection (a) onto the x-y plane to elucidate the position of the features.

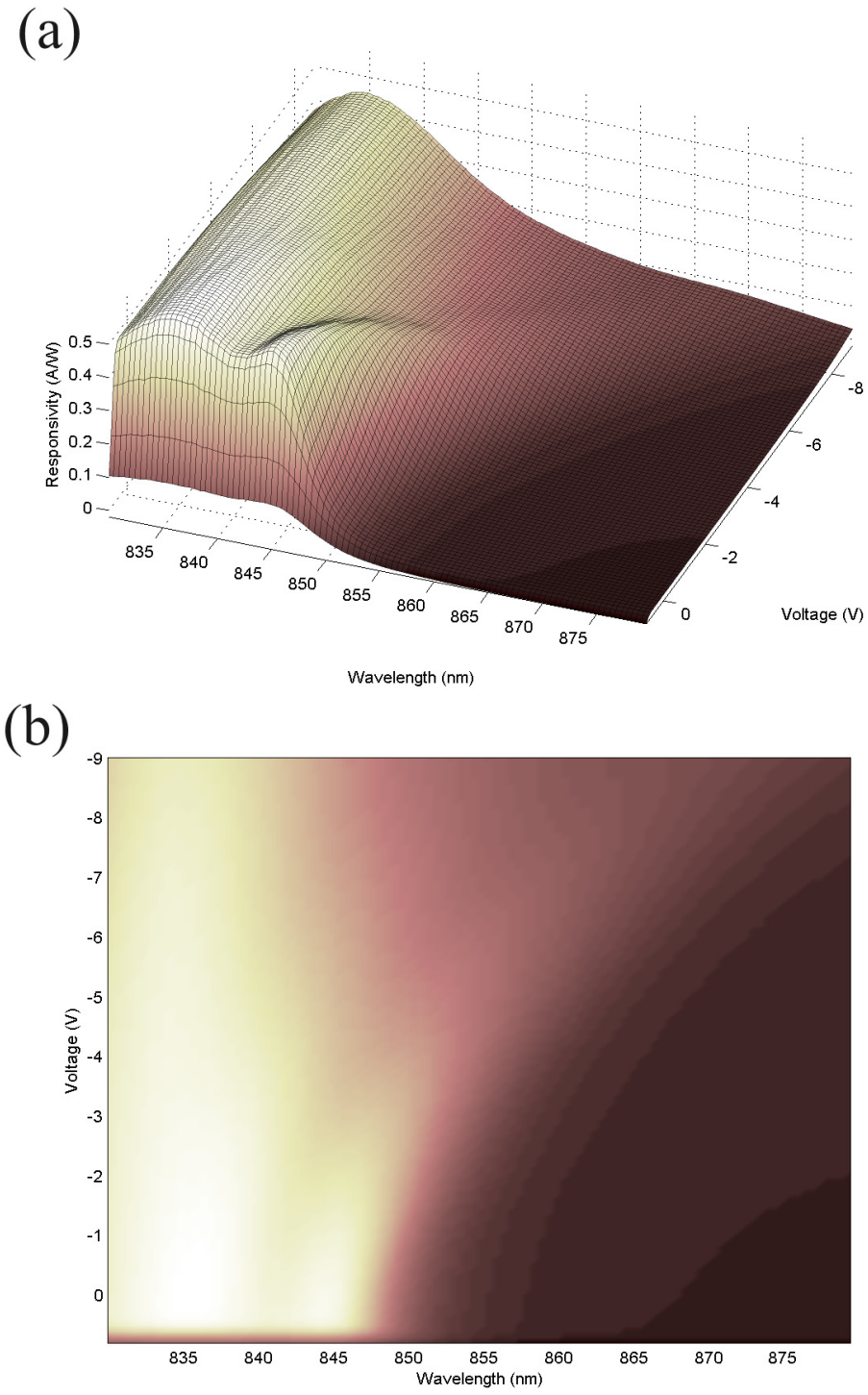

Figure 5.16: (a) Measured responsivity as a function of wavelength and voltage for wafer 239. (b) Projection of (a) onto the x-y plane.

of 835 nm also causes a large reduction in the reflectivity at the exciton, as the two features are close to coincidence. Nevertheless, wafer 239 demonstrated that the fabrication capability was sufficient to meet our requirements.

The second growth that was performed (labelled 272) was intended for use as a calibration tool, by using the error in the position of the Fabry-Perot resonance to adjust the doped $Al_{0.31}Ga_{0.69}As$ layer thicknesses in a subsequent growth. Therefore it was necessary to use a structure designed to have the desired Fabry-Perot resonance position of 851.7 nm, with doped $Al_{0.31}Ga_{0.69}As$ layers initially specified at 236 nm. The measured reflectivity and responsivity results are given in Fig. 5.18 and Fig. 5.19, depicting a resonance position at a wavelength less than 830 nm.

The comparison of simulation and experimental spectra at zero applied bias, shown in Fig. 5.20, also demonstrates a red shift of the heavy-hole exciton as compared to the simulation. This red shift could be due to incorrect quantum well thickness and/or incorrect barrier composition [31].

The third and final growth (labelled 278) used the corrected layer thickness calibration based upon the error in 272 to achieve the desired resonance position. The experimental characterisation of reflectivity and responsivity is given in Fig. 5.21 and Fig. 5.22. In this growth the Fabry-Perot resonance occurs at 857 nm and the heavy-hole exciton is positioned at 847 nm, as was the case with wafer 272. Even though the absolute wavelength positions of the features are not what was designed, since the relative positions are as required, this wafer meets our requirements for subtractor and comparator demonstrations.

A comparison of reflectivity and responsivity of devices from each of the three different chips is presented in Fig. 5.23 and Fig. 5.24 respectively, at applied voltages of 0 V and −5 V. The positions of the heavy-hole exciton and Fabry-Perot resonance at 0 V are labelled. Figures 5.23 and 5.24 demonstrate that the exciton position was within 5 nm in the three growths, but the Fabry-Perot resonance position shifted approximately 25 nm from growth 239 to growth 278. This was the design intention, to only shift the Fabry-Perot resonance.

A direct comparison between simulation and experiment is given in Fig. 5.25 for an applied voltage of 0 V and an applied voltage of −5 V in Fig. 5.26. Importantly,

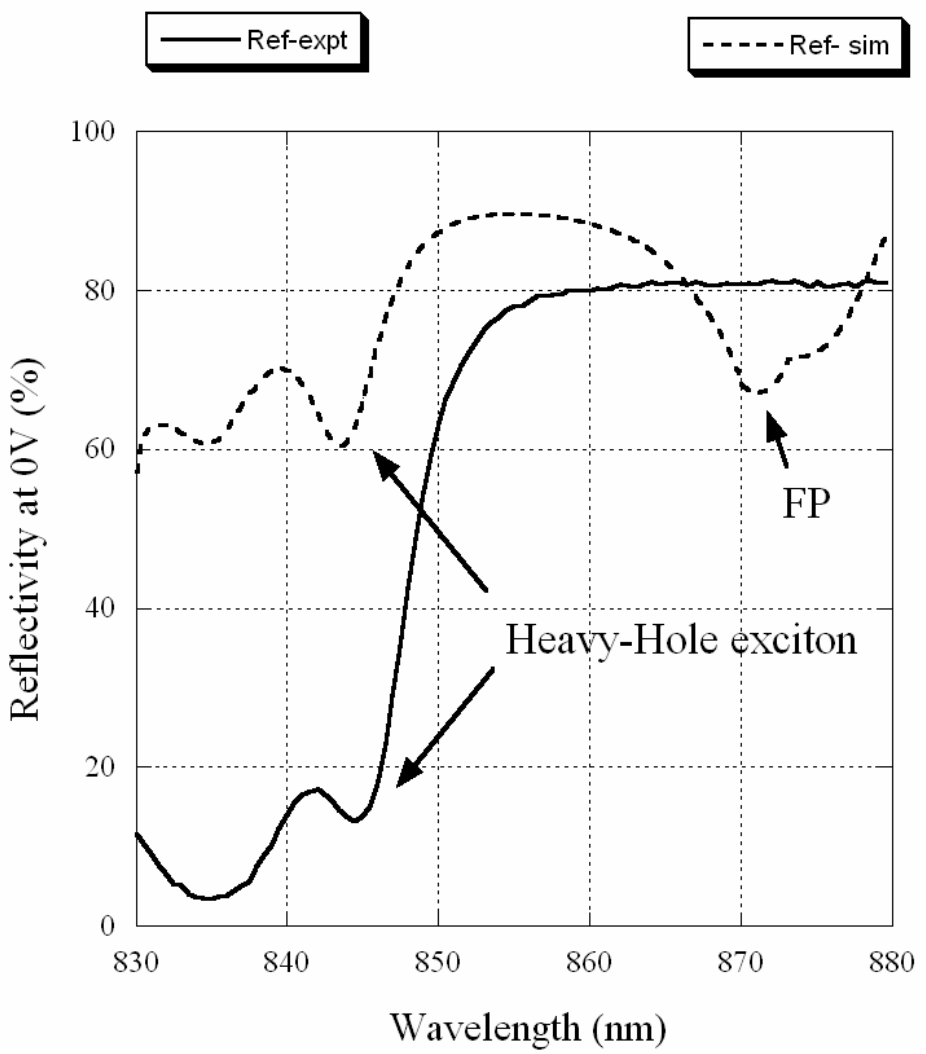

Figure 5.17: Comparison of the simulated (dashed) and experimental (solid) reflectivity spectra for the first grown wafer. The Fabry-Perot (FP) resonance and heavy-hole exciton positions are labelled, respectively.

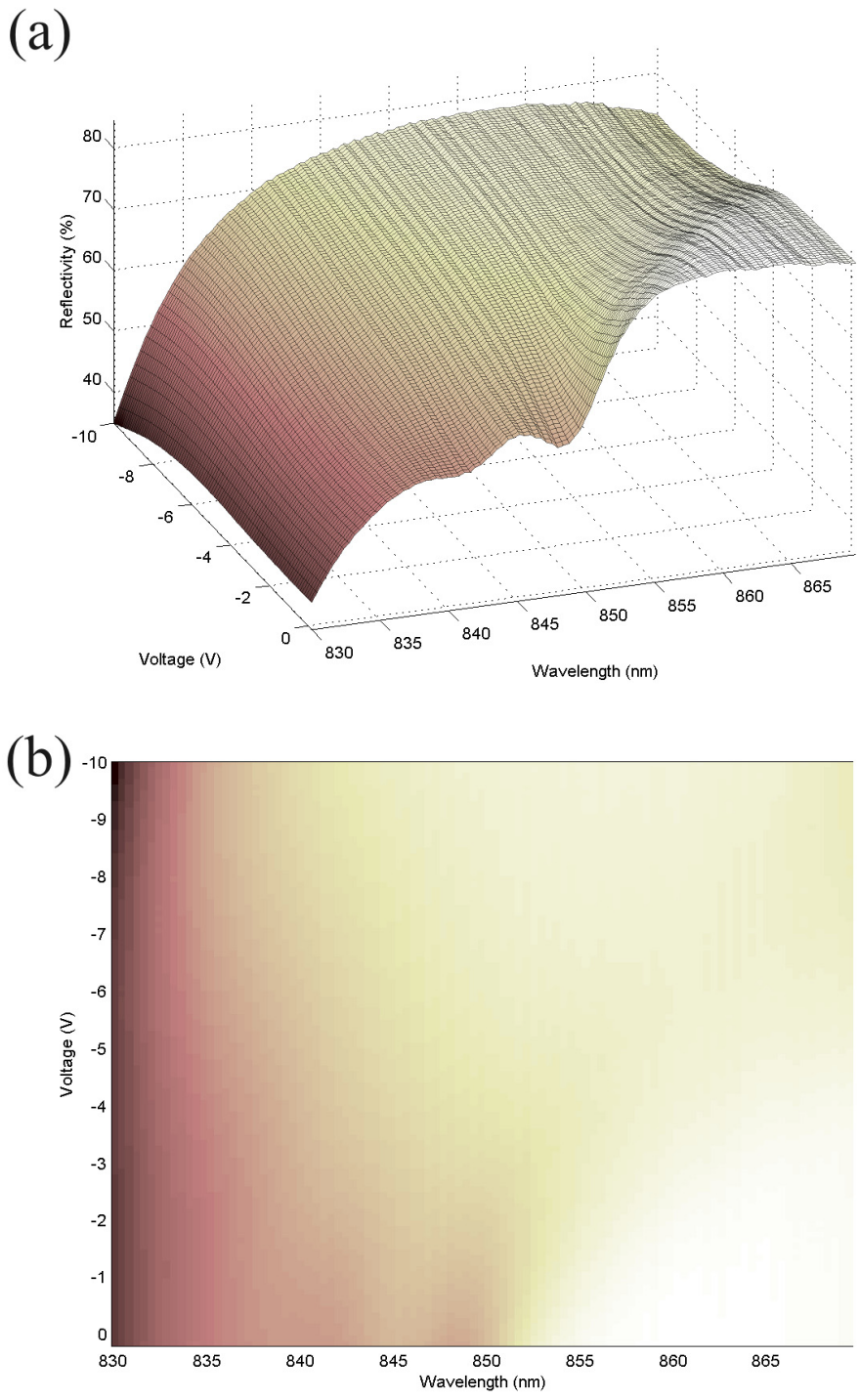

Figure 5.18: (a) Measured reflectivity as a function of wavelength and voltage for the second growth, labelled 272. (b) Projection (a) onto the x-y plane to elucidate the position of the features.

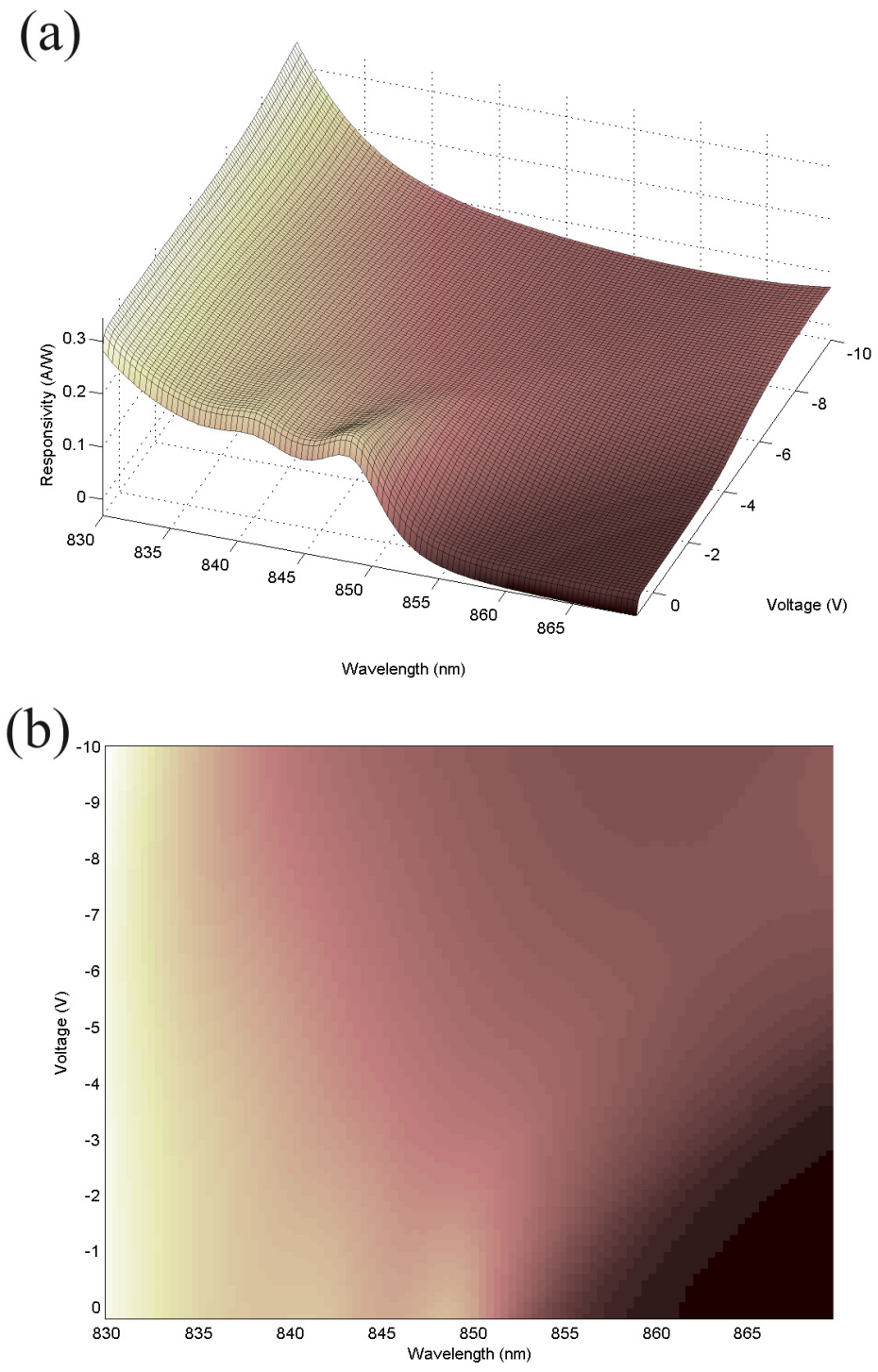

Figure 5.19: (a) Measured responsivity as a function of wavelength and voltage for the second growth, labelled 272. (b) Projection of (a) onto the x-y plane.

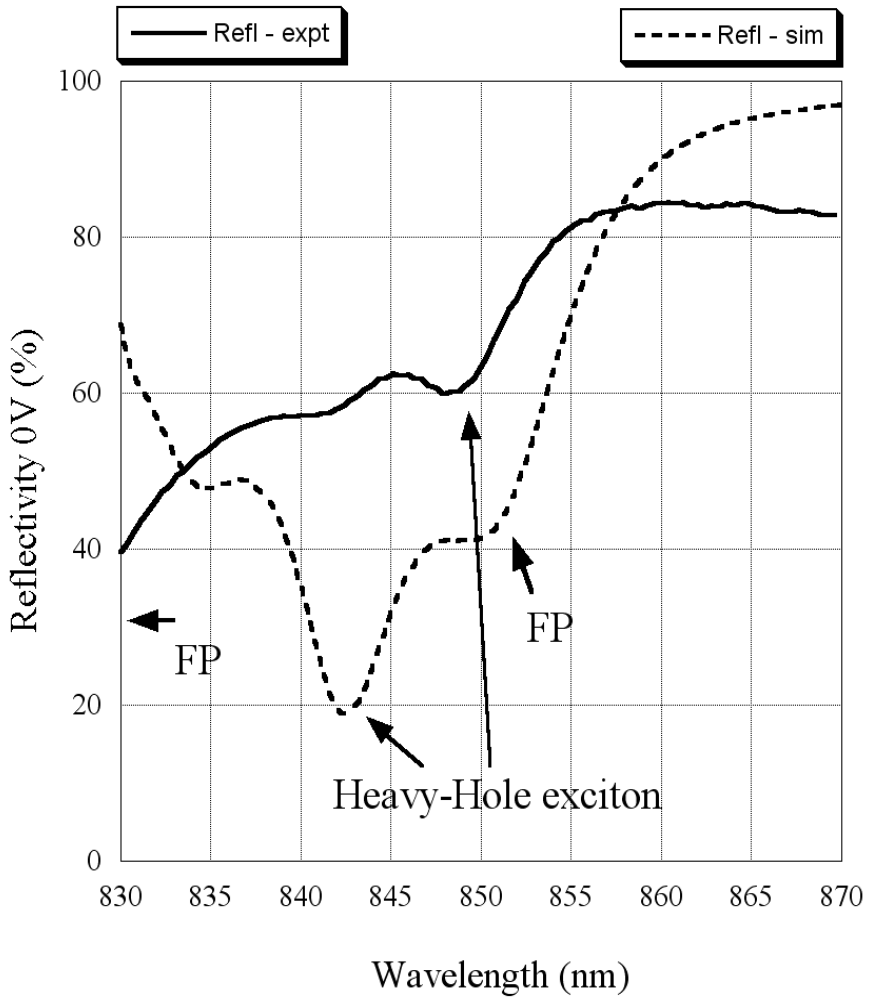

Figure 5.20: Comparison of the simulated (dashed) and experimental (solid) reflectivity spectra for the second grown wafer.

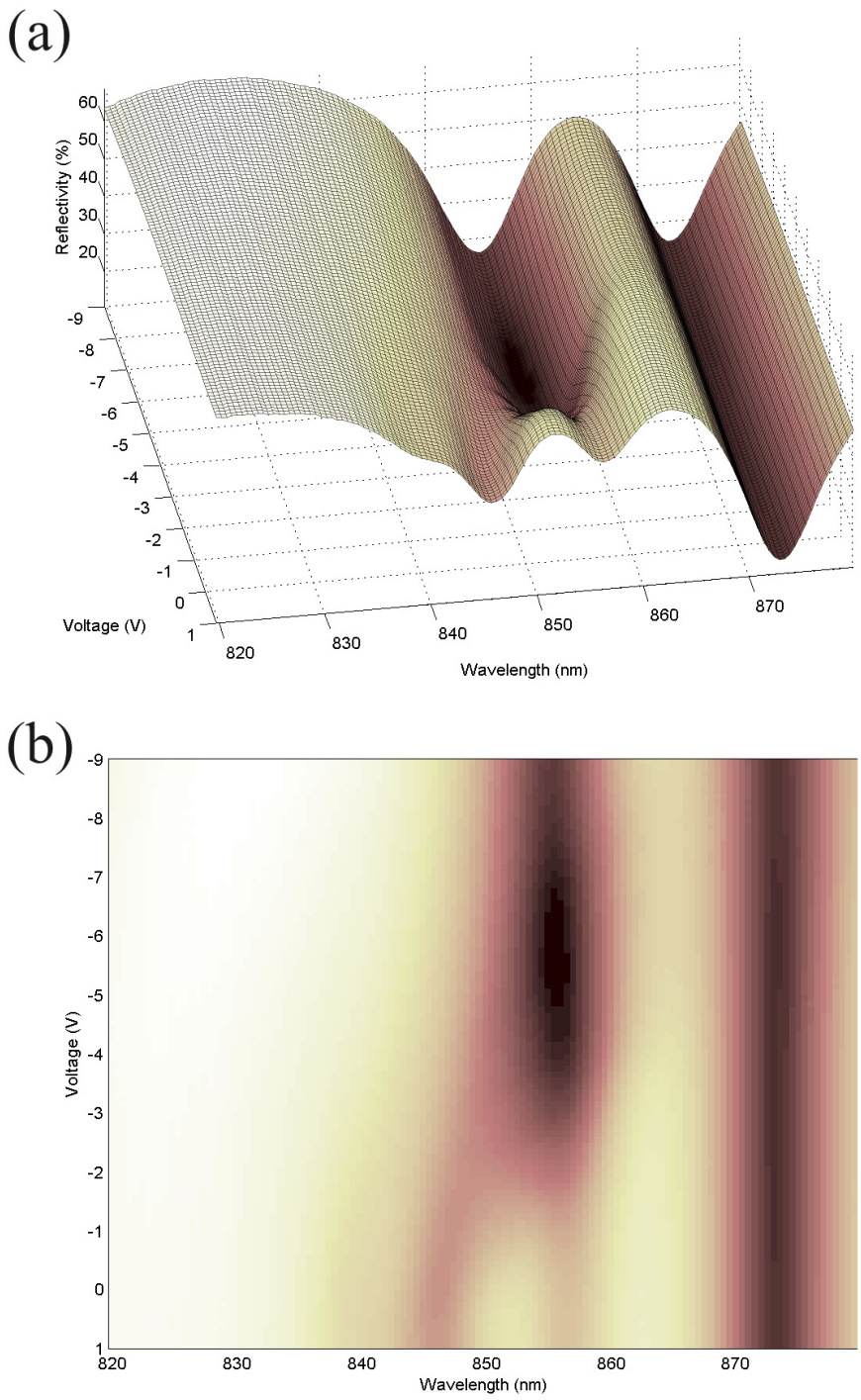

Figure 5.21: (a) Measured reflectivity as a function of wavelength and voltage for the third growth, labelled 278. (b) Projection of (a) onto the x-y plane.

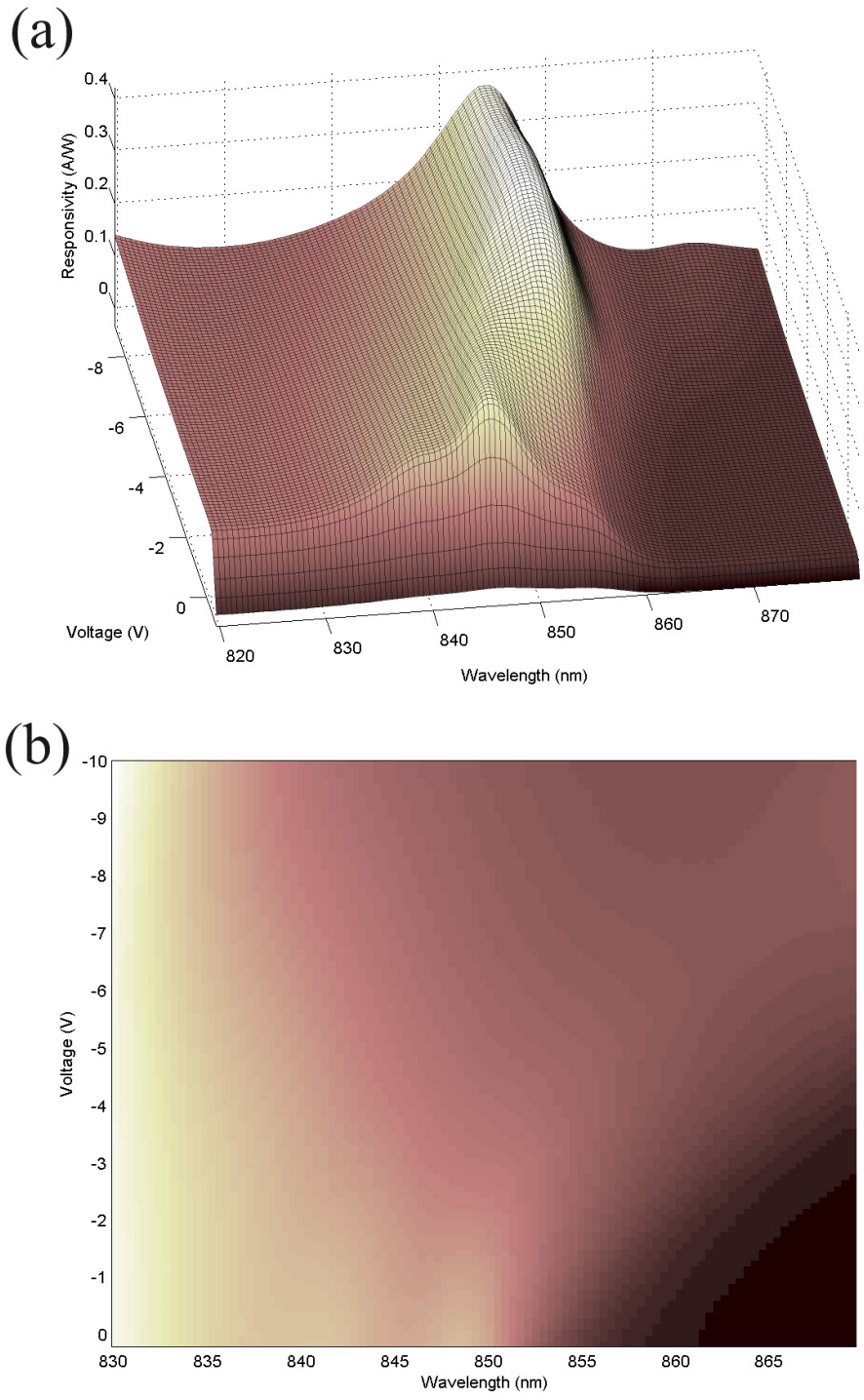

Figure 5.22: (a) Measured responsivity as a function of wavelength and voltage for the third growth, labelled 278. (b) Projection of (a) onto the x-y plane.

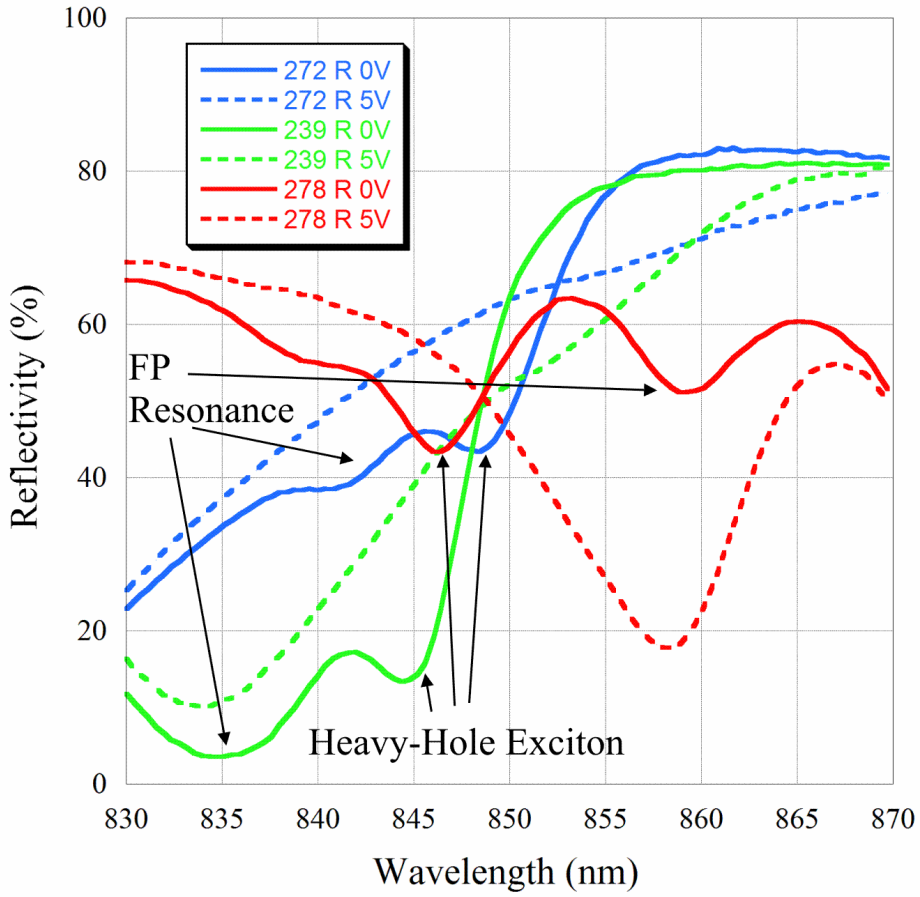

Figure 5.23: Comparison of the reflectivity at 0V(solid) and -5V (dashed) applied bias for chips 239 (green), 272 (blue) and 278 (red). The positions of the heavy-hole exciton and Fabry-Perot resonance at 0 V are labelled. The exciton position was within 5 nm in the three growths, but the Fabry-Perot resonance position shifted approximately 25 nm from growth 239 to growth 278, as designed.

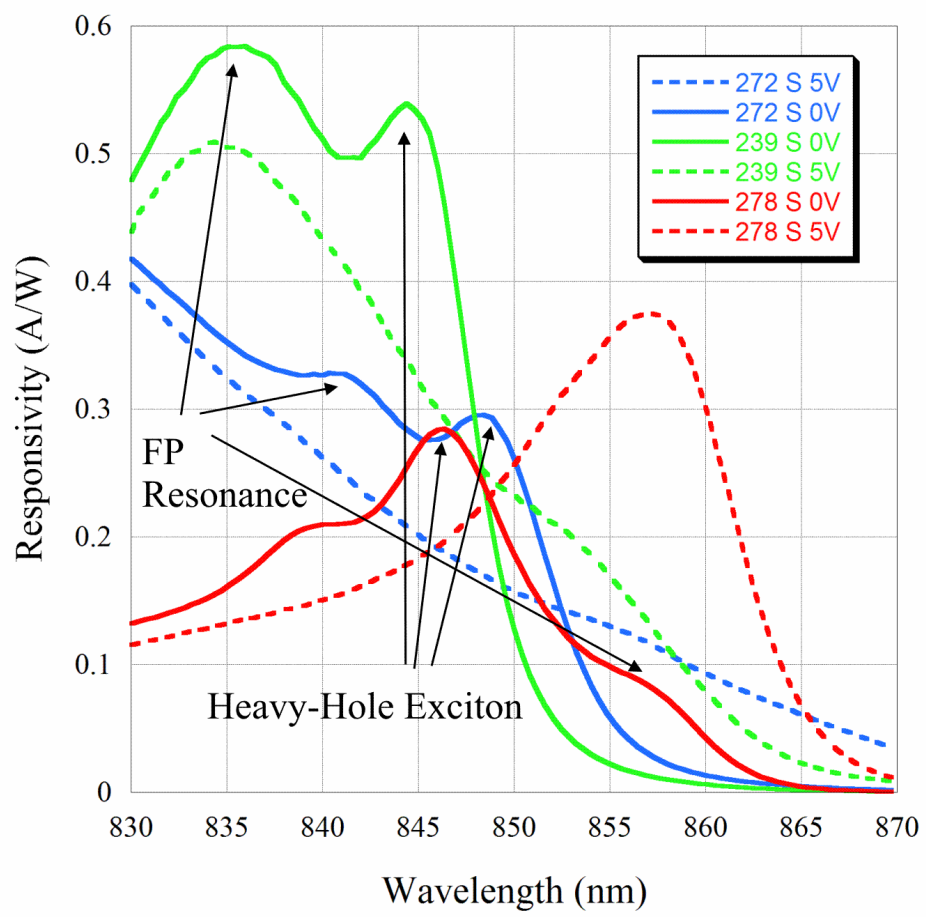

Figure 5.24: Comparison of the responsivity at 0V(solid) and -5V (dashed) applied bias for chips 239 (green), 272 (blue) and 278 (red). The positions of the heavy-hole exciton and Fabry-Perot resonance at 0 V are labelled. The exciton position was within 5 nm in the three growths, but the Fabry-Perot resonance position shifted approximately 25 nm from growth 239 to growth 278, as designed.

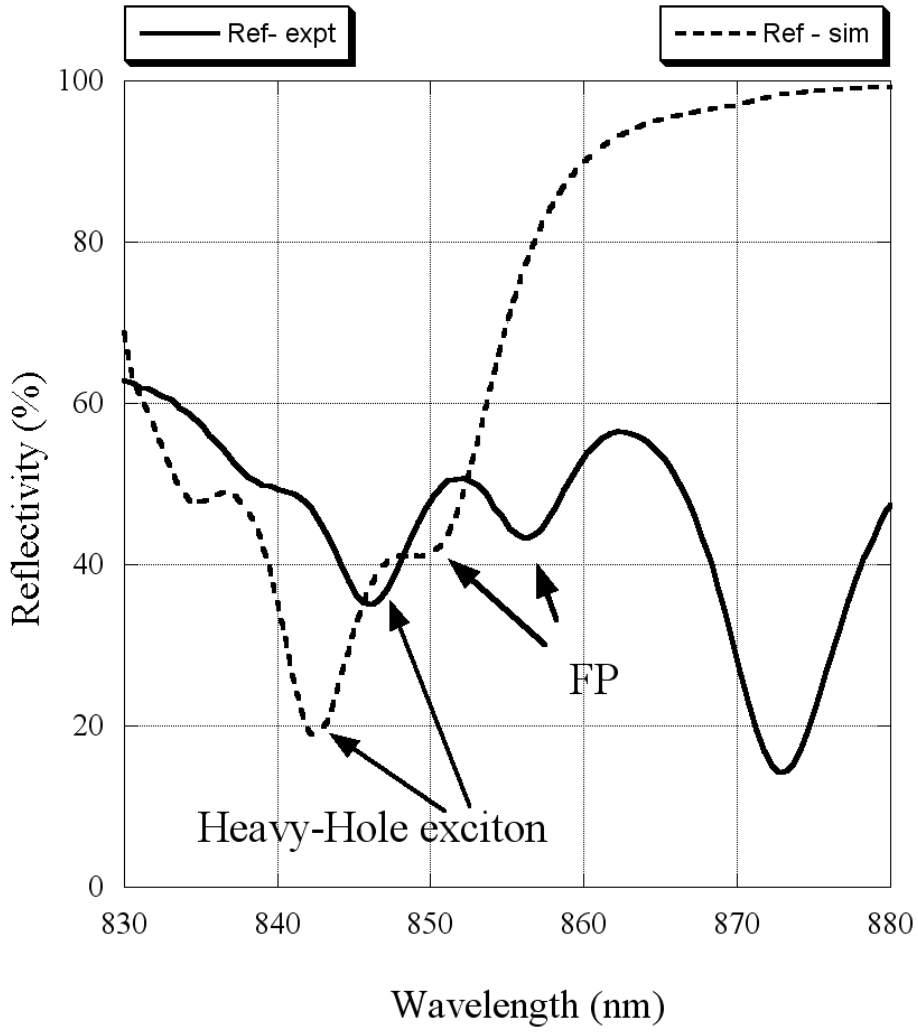

Figure 5.25: Comparison of the simulated (dashed) and experimental (solid) reflectivity spectra for the third grown wafer for an applied voltage of 0V. Note, the dip in reflectivity at 875 nm is caused by the edge of the Bragg mirror.

the value of the reflectivity at the position of the Fabry-Perot resonance agrees to within 4%, in the simulation and experiment. Together figures 5.25 and 5.26 demonstrate that the exciton red shifts via QCSE approximately the same distance in both simulation and experiment. This implies that the intrinsic region is the same length in the simulation and experiment, as the same applied voltage produces that same electric field. However, only a small change in thickness of the quantum wells is required to produce the error in exciton position and due to the difficulty of growing such thin layers, this is the most likely explanation for this discrepancy. One final issue is that the exciton peak is significantly broader in the fabricated devices, than

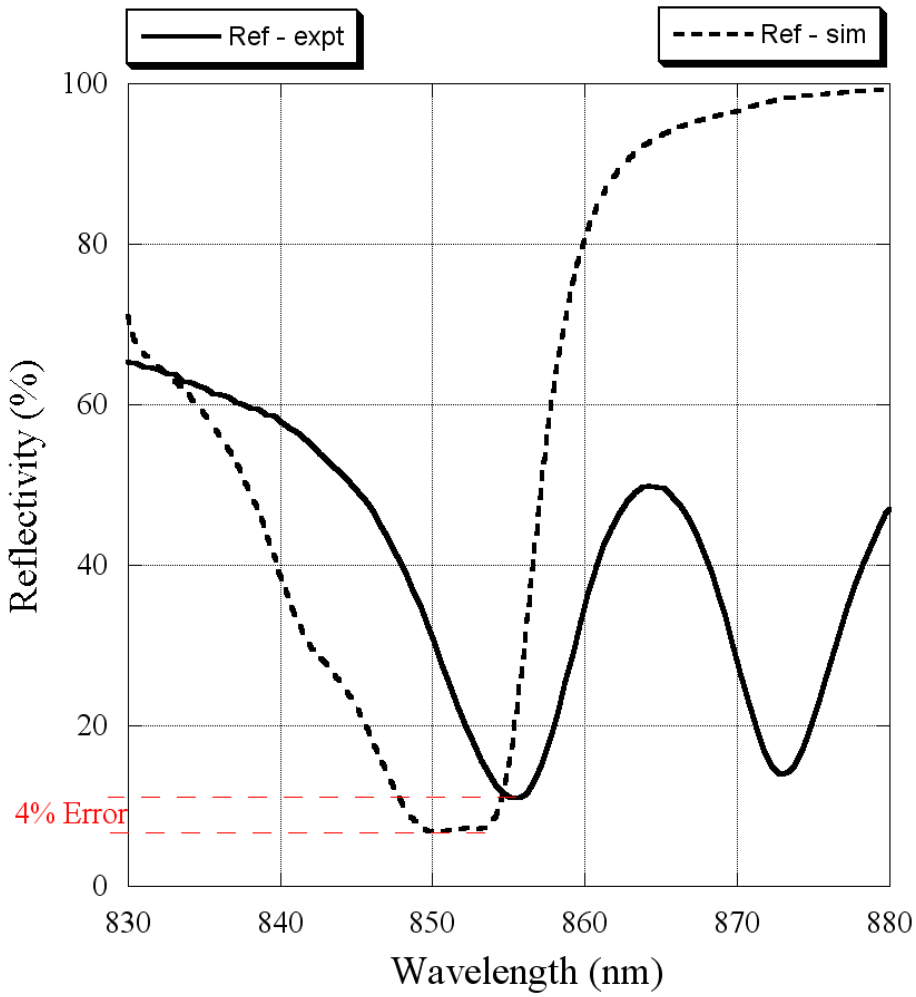

Figure 5.26: Comparison of the simulated (dashed) and experimental (solid) reflectivity spectra for the thrid grown wafer for an applied voltage of -5V. The large difference at $\lambda > 870\,\text{nm}$ is due to the Bragg mirror having a narrower bandwidth than expected from simulations. However, this did not impact on device performance. The dashed red line depicts the 4% difference in reflectivity between the simulation and realised device for the heavy-hole exciton in resonance with the Fabry-Perot.

was used in the simulation based upon an MBE grown device. The increased width of the peak will reduce the range over which bistability can be achieved, as a higher bias is required to achieve three intersections of the S-SEED load-line for a broader and lower peak.

In summary, an analytic method of designing a Fabry-Perot microcavity SEED that was based on experimental data was developed and verified by a numerical simulation. The design methodology was extended to optimise the Fabry-Perot position for simultaneous comparator and subtractor operation in a Sigma-Delta quantiser. The final structure was successfully fabricated by utilising a preliminary growth to improve the layer thickness calibration accuracy.

Chapter 6

Performance of the Sigma-Delta Quantiser

The ultimate aim of this work is the production of a photonic integrated circuit implementing the sigma-delta A/D architecture. To this end, the design approach employed was to experimentally demonstrate the individual components, and subsequently demonstrate integration of the components in a simulation of the sigma-delta architecture. Having verified the accuracy of the simulation technique, by comparison with experimental results in Chapter 3, a successful demonstration of operation of the simulated architecture enables us to confirm the feasibility of the design.

This chapter describes in Section 6.1 the operation and experimental performance of the subtractor and comparator components utilising the devices designed in Chapter 5. Additionally, photonic implementations of the clock, gain and delay components are discussed. In section 6.2 a comparison between sigma-delta and error diffusion architectures is presented. The constraints for unipolar operation are given and an optical layout of the sigma-delta architecture is proposed. Section 6.3 presents results from the simulation of the architecture and expected performance scaling. The final section proposes an improved architecture that is the subject of future work.

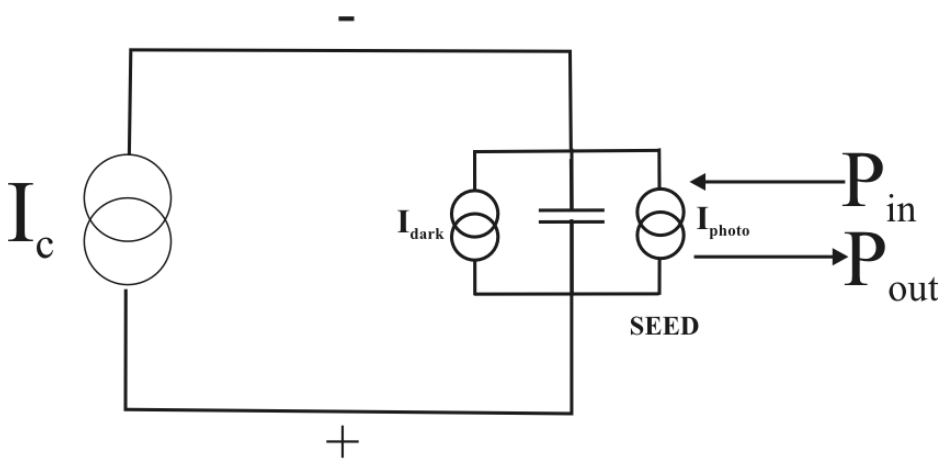

Figure 6.1: Schematic of a MQW p-i-n SEED equivalent circuit driven by a current source (I_c). Since the SEED is in electrical series with the driving current, I_c must flow through the SEED.

6.1 Components

The following section describes the operation of the photonic elements required to construct sigma-delta or error diffusion quantisers. The subtractor and comparator components are demonstrated experimentally using SEEDs, and compared to the results of numerical simulation. Results from the literature are presented for the clock, gain and delay elements.

6.1.1 Subtractor

To understand how an optical subtractor can be formed using a SEED, it is first necessary to describe the self-linearised mode of operation of a SEED. Consider the action of a current source driving a SEED with input power P_{in}, as per Fig. 6.1. The current source (I_c) provides carriers to charge the capacitance of the SEED[35]. The photocurrent (I_{photo}) then acts to discharge it.

Now consider the loadline of a SEED and a current source (I_c) with an intersection at point A, in Fig. 6.2. As the SEED is in electrical series with the current source, the total current in the circuit is fixed by the current source at I_c. If the current source is altered to increase I_c, then the voltage across the SEED will increase

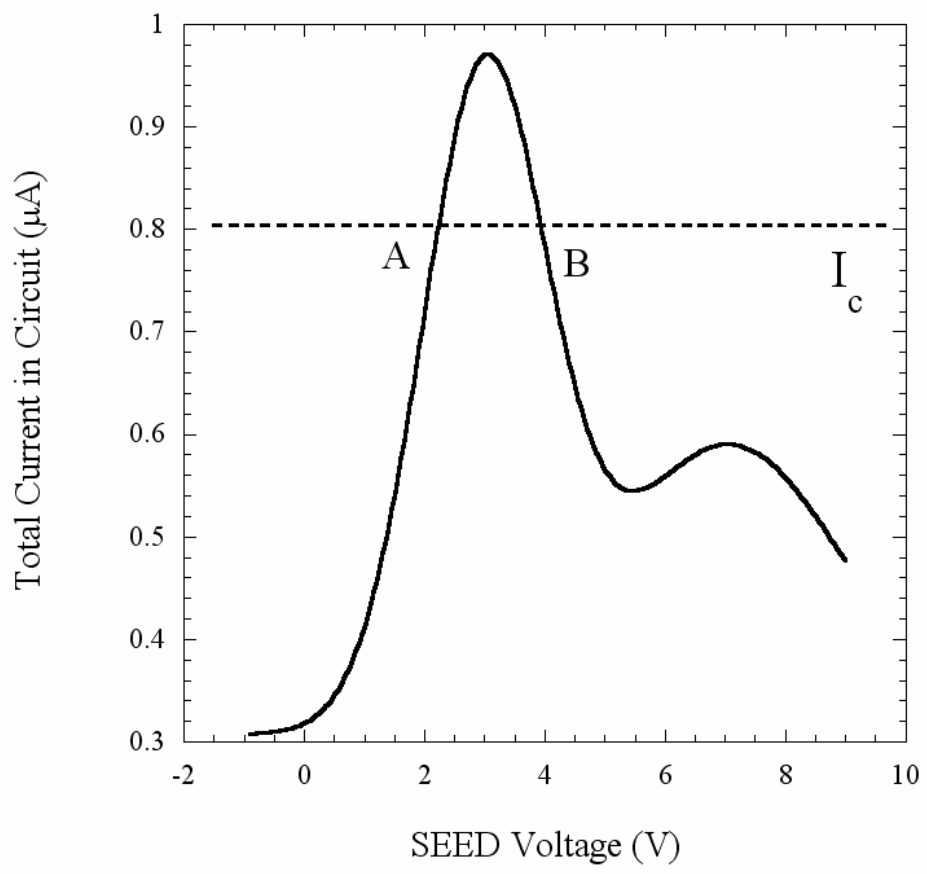

Figure 6.2: Loadline of a current source and a SEED with input power P and responsivity $S(V)$. From the stability analysis in [35], the solution at A is stable, while, due to positive feedback, B is unstable.

as it is charged. Since $\frac{dI}{dV}$ is positive around A, the photocurrent will also increase. Conversely, if the photocurrent exceeds I_c, the voltage falls and the photocurrent decreases. Therefore, due to negative feedback the circuit will reach a stable operating point at which the source current and photocurrent are equal. However, at point B, $\frac{dI}{dV}$ is negative, so an increase in voltage will lead to a reduction in photocurrent and due to positive feedback, no stable point will be reached. The power that is absorbed ($P_{absorbed}$) and converted to photocurrent (I_{photo}) is given by,

$$\begin{aligned} P_{absorbed} &= \frac{P_{in}S(V)h\nu}{\eta e} \\ &= \frac{h\nu}{\eta e}I_{photo}, \end{aligned} \tag{6.1}$$

where η is the carrier collection efficiency of the SEED and $I_{photo} \equiv SP_{in}$. Since the photocurrent and circuit current are equal at equilibrium ($I_{photo} = I_c$ and neglecting I_{dark} of Fig. 6.1), then

$$P_{absorbed} = \frac{h\nu}{\eta e}I_c. \tag{6.2}$$

That is, the power absorbed by the SEED is proportional to the current set by the current source. This mode of operation is termed self-linearised [35], as the negative feedback maintains the proportionality between the absorbed power and the current, provided η is independent of V. By utilising a photodiode as the current source[35], an optical subtractor can be formed[24], depicted in Fig. 6.3. The $S - V$ plot of the photodiode is given in Fig. 6.4 illustrating that a photodiode acts like a current source when reverse biased and light is applied.

To demonstrate how subtraction occurs, consider the conservation of optical power, neglecting losses, at the SEED[35]

$$P_{out} = P_{in} - P_{absorbed}. \tag{6.3}$$

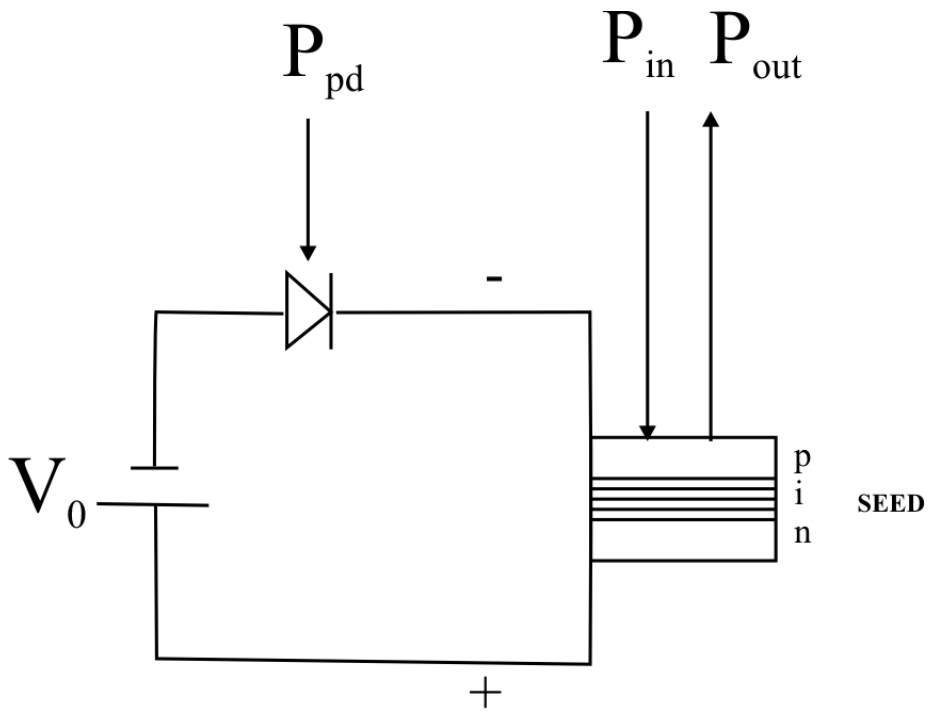

Figure 6.3: Schematic of an optical subtractor using a voltage source V_0 and photodiode with input P_{pd} as the current source.

Substituting (6.2) gives

$$P_{out} = P_{in} - \frac{h\nu}{\eta e} I_c. \tag{6.4}$$

If we now define I_c as now the current produced by the photodiode, that is,

$$I_c = P_{pd} S_{pd}, \tag{6.5}$$

then substitution of (6.5) into (6.4) yields the equation for optical subtraction

$$P_{out} = P_{in} - \left(\frac{h\nu}{\eta_{seed} e} S_{pd} \right) P_{pd}, \tag{6.6}$$

where we have labelled $\eta \rightarrow \eta_{seed}$ to indicate that it is the carrier collection efficiency of the SEED. Therefore, to achieve ideal optical subtraction ($P_{out} = P_{in} - P_{pd}$) values of $\eta_{seed} = 1$ and $S_{pd} = e/h\nu$ are required.

An experiment was performed to test (6.6). A schematic of the experimental

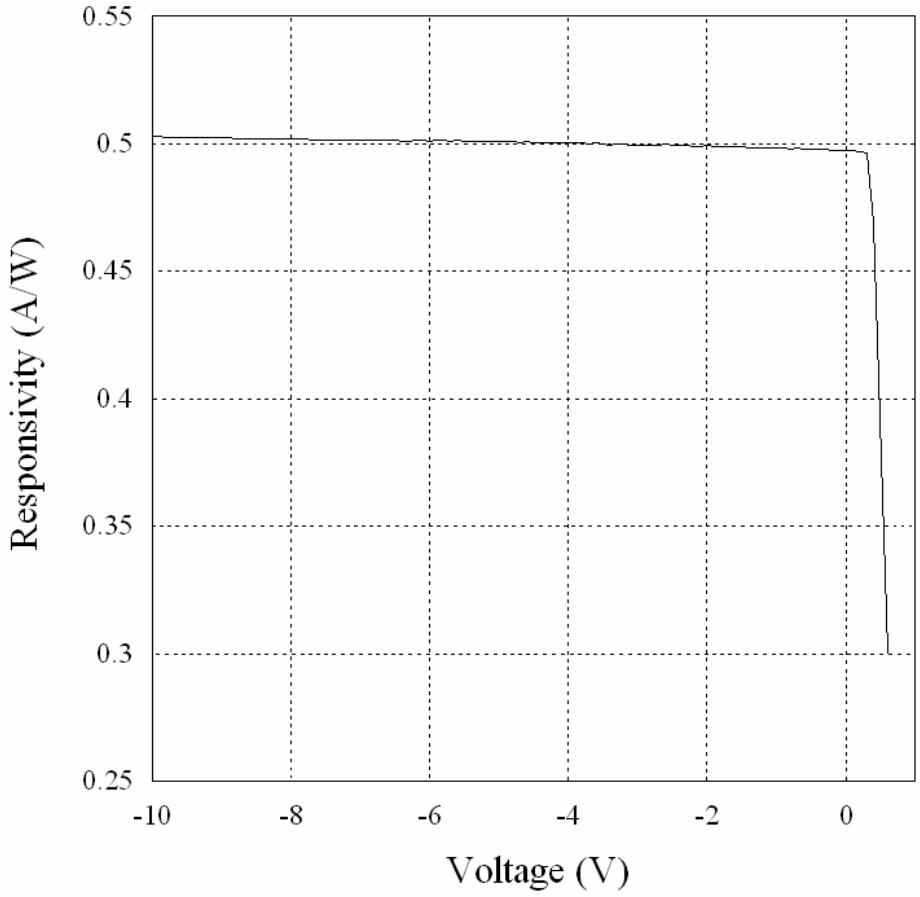

Figure 6.4: Responsivity against voltage plot of a Si photodiode, demonstrating a current source characteristic in reverse bias.

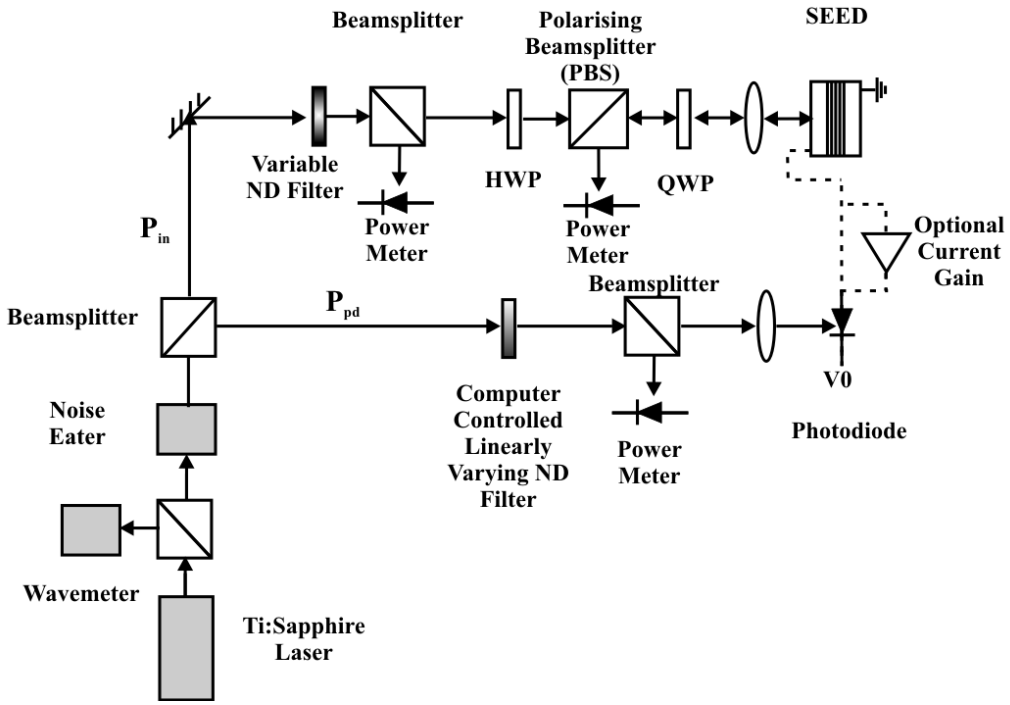

Figure 6.5: Schematic of the experimental setup to characterise subtractor operation. Included is the optional current gain. Dashed lines represent electrical connections and solid lines optical beams.

setup is given in Fig. 6.5. The experimental setup is similar to that described in Chapter 5 for the measurement of the SEED's reflectivity and responsivity, except for an extra beam (P_{pd}) that has been added to apply light to a Silicon photodiode. Included in the path of the additional beam were a beamsplitter, to sample the power incident on the photodiode, and a linearly varying neutral density (ND) filter slide. This filter slide was mounted on a linear translation stage, driven by a Newport 850G actuator. To perform the subtractor characterisation experiment, a voltage was applied to the circuit and a beam of fixed power was applied to the SEED. A computer stepped the position of the ND slide to vary slowly the power applied to the photodiode. At each step the computer recorded the measured power at the input to the SEED and photodiode, and the reflected power from the SEED at equilibrium. An additional complication of this experiment was that careful selection of the photodiode input power range is required. This can be understood by considering the loadline plot of Fig. 6.2. If too much current is applied, the SEED will not be able to supply enough photocurrent to equal the supply current (i.e. there

will not be an intersection in Fig. 6.2). Since the same current must flow through the components in a series circuit, the SEED will achieve the required current by undergoing reverse bias breakdown, which often causes catastrophic failure of the diode junction and must be avoided. To predict the limit of the input range, the responsivity of the photodiode and SEED was measured. The maximum input power to the photodiode is then given by

$$P_{pd(\max)} = \frac{P_{in}S(V_{\max})}{S_{pd}}, \tag{6.7}$$

where $V_{\max}$ is the voltage at the peak of the SEED responsivity. The other limit of the input power P_{pd} can be set at $V_{\min} = 0$, as the assumption of $\eta_{seed} = 1$ is no longer valid in forward bias[71]. Therefore the photodiode input range for linear subtraction is

$$\frac{P_{in}S(0)}{S_{pd}} \leq P_{pd} \leq \frac{P_{in}S(V_{\max})}{S_{pd}}. \tag{6.8}$$

For example, with $100\,\mu$W of power applied to the SEED (P_{in}), the power applied to the photodiode (P_{pd}) was able to be varied between $10\,\mu$W and $42\,\mu$W.

The results obtained for the subtractor characterisation experiment and simulation, with $\lambda = 853\,$nm and $V_0 = -5.5\,$V, are given in Fig. 6.6 for a device on the final grown wafer (278). A linear fit of the data produces a slope of 0.684 and a y-intercept of $14.5\,\mu$W. For an ideal subtractor, these parameters would be equal to 1 and 0, respectively. Nevertheless, the behaviour is linear, with a coefficient of determination (R^2) value of 0.9998, demonstrating self-linearised operation. The first step in idealising the performance of the subtractor was to correct for the coefficient of P_{pd} in (6.6). The term $\frac{h\nu}{e}$ gives the ideal conversion of energy from light to current in Watts per Ampere. When this is multiplied by responsivity in A/W, the ideal value of $\frac{h\nu}{e}S_{pd}$ is 1. Assuming $\eta = 1$, and using measured data, the calculated value of $\frac{h\nu}{\eta_{seed}e}S_{pd}$ was 0.733 at 850 nm. The dominant effect in reducing the conversion ratio is the 32% reflection loss from the photodiode air-silicon interface. Therefore, one option would be to anti-reflection coat the photodiode to reduce optical losses. Another possibility would be to use optical gain to increase P_{pd}. Alternatively, a

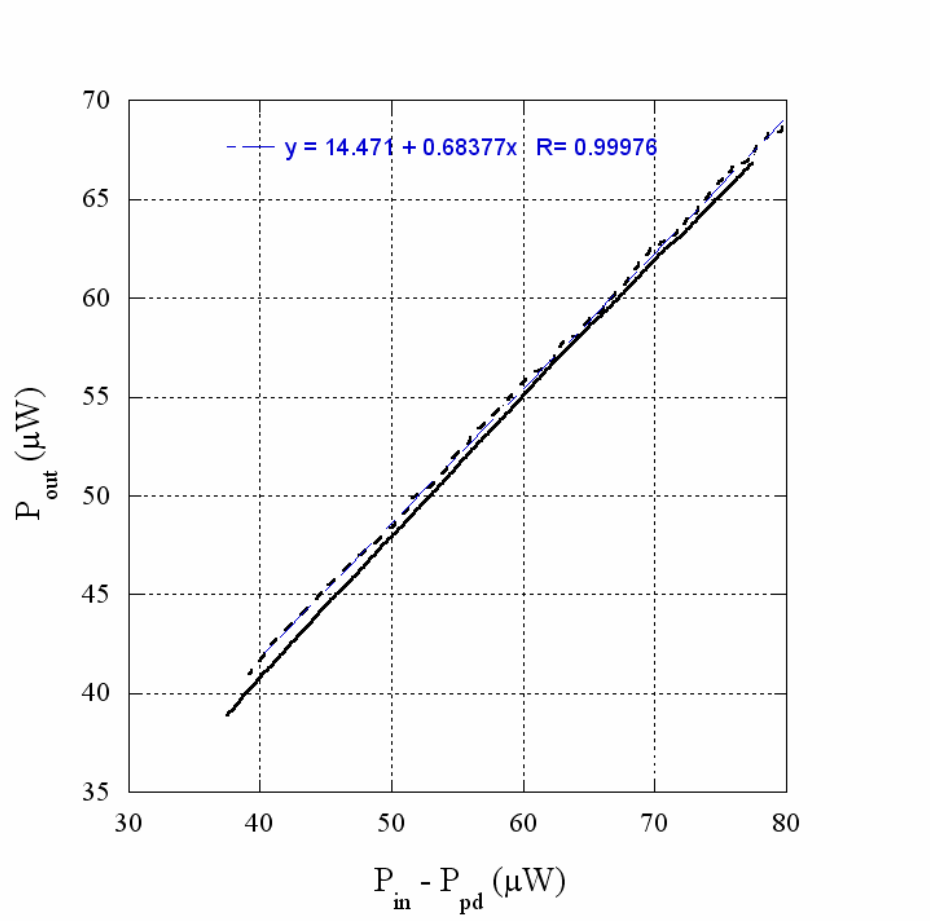

Figure 6.6: Experimental results (dashed) for P_{out} vs $P_{in} - P_{pd}$, measured at 853 nm from a device on the final wafer (278). The equation for a linear fit (blue solid) and simulated performance (black solid) are shown.

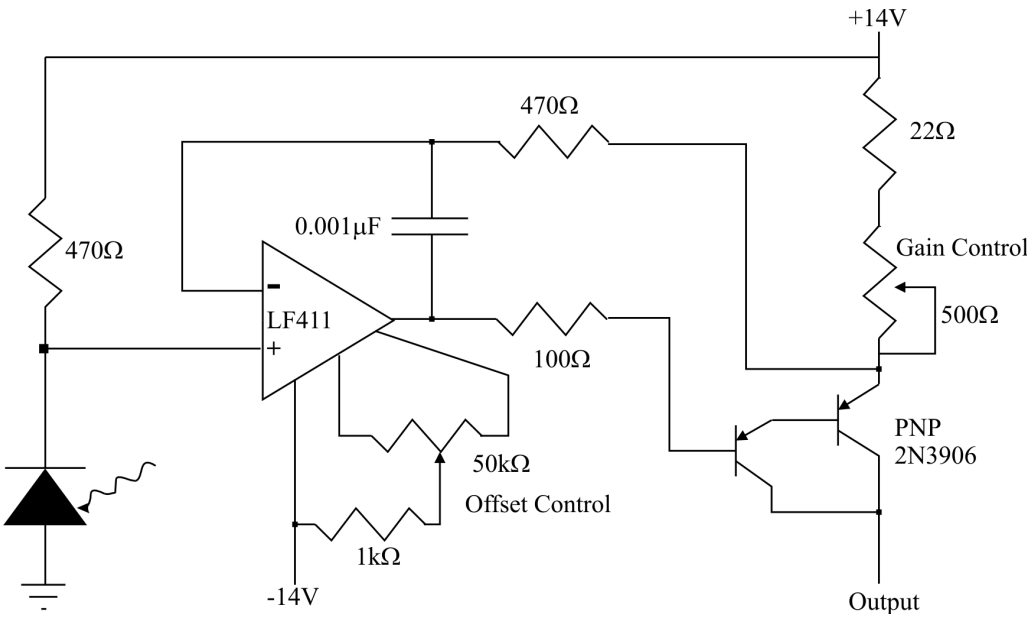

Figure 6.7: Circuit diagram of a current amplifier used to correct for loss in the photodiode.

current gain applied to the electrical output of the photodiode could be used to idealise the coefficient of P_{pd} in (6.6), and this option was implemented experimentally. A circuit diagram for the current amplifier is given in Fig. 6.7.

In the following Figs. 6.8 (a), (b) and (c), results of experimental subtractor performance with current gain are presented at wavelengths of 850 nm, 853 nm and 855 nm for $V_0 = -5.5$ V. In each case, the current gain was adjusted to achieve a slope of 1. This is demonstrated by the slope coefficient of the linear fit equation in each of the plots. The performance was simulated using the calculation method described in Section 3.3, where the current source, capacitance and dark current characteristics of one MQW device in the equivalent circuit, were replaced with those of a photodiode. The results of the experiment are also compared to simulations in Figs. 6.8 (a), (b) and (c). The three results demonstrate agreement between experiment and simulation to within the accuracy of the optical power measurement ($\sim$2%). However, non-idealities were observed that include a non-zero y-intercept and different gain required for each wavelength. These observations are not explained by simple correction to the non-ideal photodiode responsivity. It will be shown that this can be resolved by the inclusion of wavelength dependent loss in

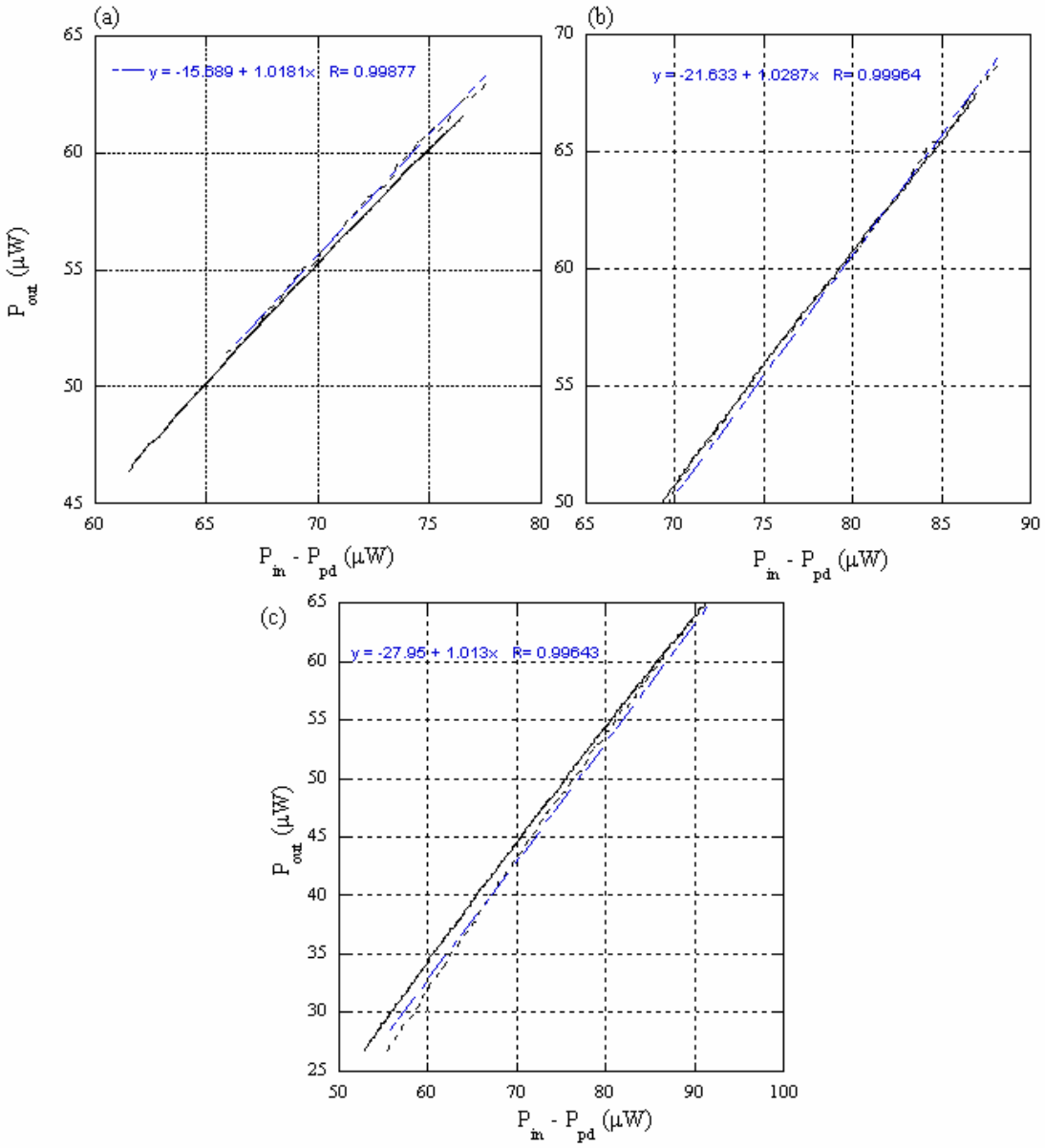

Figure 6.8: Experimental (dashed) and simulated (black solid) subtractor performance of a device on wafer 278 at 850 nm, 853 nm and 855 nm, in figures (a), (b) and (c), respectively. Electrical gain was applied to the photodiode to achieve a gradient close to 1. A current gain of 1.32 was used in (a), 1.38 in (b) and 1.43 in (c). A fit to the experimental data (blue) gives the slope.

the Bragg mirror and a corresponding optical gain to correct the problem.

Firstly, if the mirror has loss, then power conservation at the Bragg mirror yields

$$P_{reflected} = P_{in} - P_{transmitted}. \tag{6.9}$$

Including this transmitted loss in (6.6) gives

$$P_{out} = P_{in} - P_{transmitted} - \left(\frac{h\nu}{\eta_{seed}e} S_{pd}\right) P_{pd}. \tag{6.10}$$

Including an optical gain on the output of the SEED, G_1, and an optical or electrical gain on the photodiode input, G_2, yields

$$\begin{aligned} P_{out}^{gain} &= G_1(P_{in} - P_{transmitted} - G_2\left(\frac{h\nu}{\eta_{seed}e} S_{pd}\right) P_{pd}) \\ &= G_1(P_{in} - P_{transmitted}) - G_1G_2\left(\frac{h\nu}{\eta_{seed}e} S_{pd}\right) P_{pd}. \end{aligned} \tag{6.11}$$

An ideal subtractor that satisfies $P_{out}^{gain} \equiv P_{out} = P_{in} - P_{pd}$ can be created by setting

$$G_1(P_{in} - P_{transmitted}) = P_{in} \tag{6.12}$$

and

$$G_1G_2\left(\frac{h\nu}{\eta_{seed}e} S_{pd}\right) = 1. \tag{6.13}$$

Therefore, solving 6.12 for G_1 yields

$$G_1 = \frac{P_{in}}{P_{in} - P_{transmitted}} \tag{6.14}$$

and on substitution of (6.14) into (6.13) G_2 becomes

$$G_2 = \frac{P_{in} - P_{transmitted}}{\frac{h\nu}{\eta_{seed}e} S_{pd} P_{in}}. \tag{6.15}$$

However, without removing the substrate from a fabricated device, the direct measurement of $P_{transmitted}$ and η_{seed} are not possible. An alternative method for deter-

mining G_1 and G_2 is to measure the y-intercept (A) and slope (B) from a plot of P_{out} against P_{pd} for the subtractor experiment. The values of G_1 and G_2 to give an ideal subtractor are then given by

$$G_1 = \frac{P_{in}}{A} \tag{6.16}$$

and

$$G_2 = -\frac{1}{G_1 B}. \tag{6.17}$$

As an example, the simulation of Fig. 6.6 was plotted against P_{pd} (instead of $P_{in} - P_{pd}$ as in Fig. 6.6) yielding $A = 88.16\,\mu\text{W}$ and $B = -0.700\,\mu\text{W}^{-1}$. The simulation is replotted in Fig. 6.9 with $G_1 = 1.22$ and $G_2 = 1.17$. The result is a y-intercept of -0.04 μW and a slope of $1.00\,\mu\text{W}^{-1}$, demonstrating the effectiveness of the technique.

Revisiting the non-idealities of the experiment, we can explain the increasing y-intercept and required current gain observed in Figs. 6.8 (a)-(c), as a variation of Bragg mirror loss ($P_{transmitted}$) with wavelength. The mirror loss at 855 nm was greater than at 850 nm, due to the close proximity of the operating wavelength to the edge of the mirror's high reflectivity region, seen in Chapter 5 Fig. 5.21 (a). Improving the growth so that the Bragg mirror is centred at the operating wavelength ($\sim$853 nm) should significantly reduce the optical gain required to achieve ideal subtractor operation.

Next to linearity, dynamic range is an important subtractor performance parameter in application to the A/D. Using the same measurement criterion developed in Chapter 5 Fig. 5.9, dynamic range was calculated as a function of wavelength for the devices of wafer 278. Experimental reflectivity and responsivity data were used in the simulation. A comparison with the dynamic range expected from the design calculations is presented in Fig. 6.10. Gain was not applied to the photodiode in either case. The figure demonstrates that the realised dynamic range almost equals the expected value. To show the effect that the Fabry-Perot resonance has on subtractor dynamic range, we compare the performance of wafers 278 and 272 in Fig.

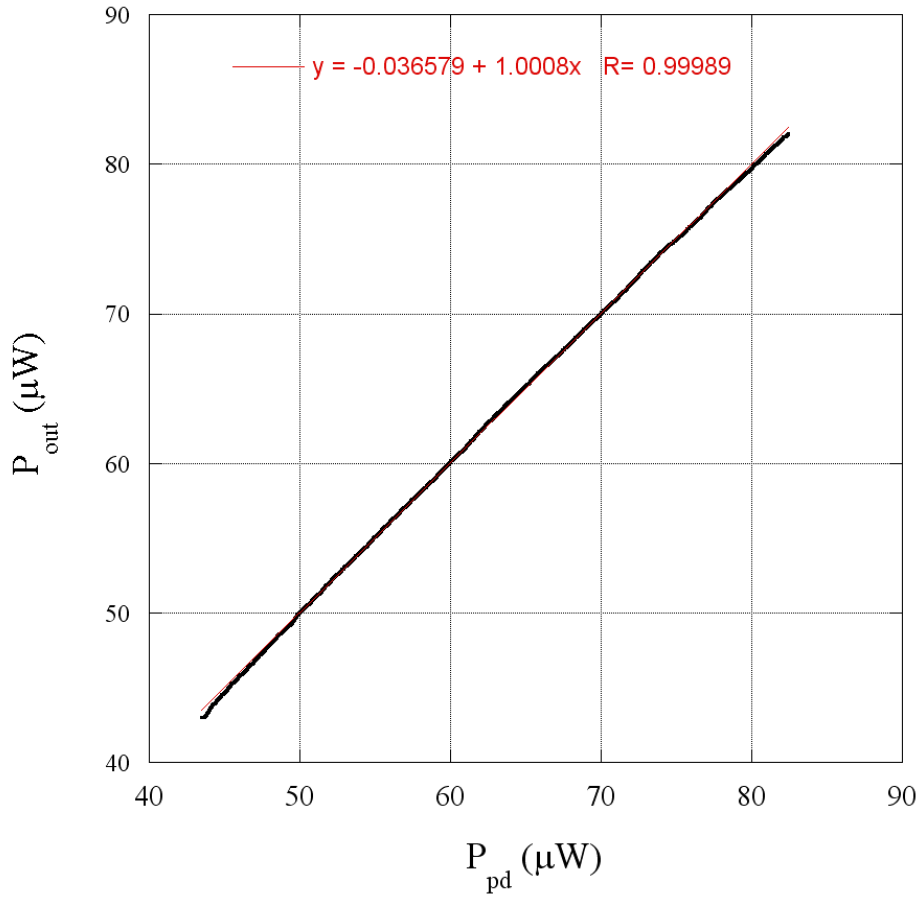

Figure 6.9: Simulated subtractor performance with optical and electrical gain to idealise performance.

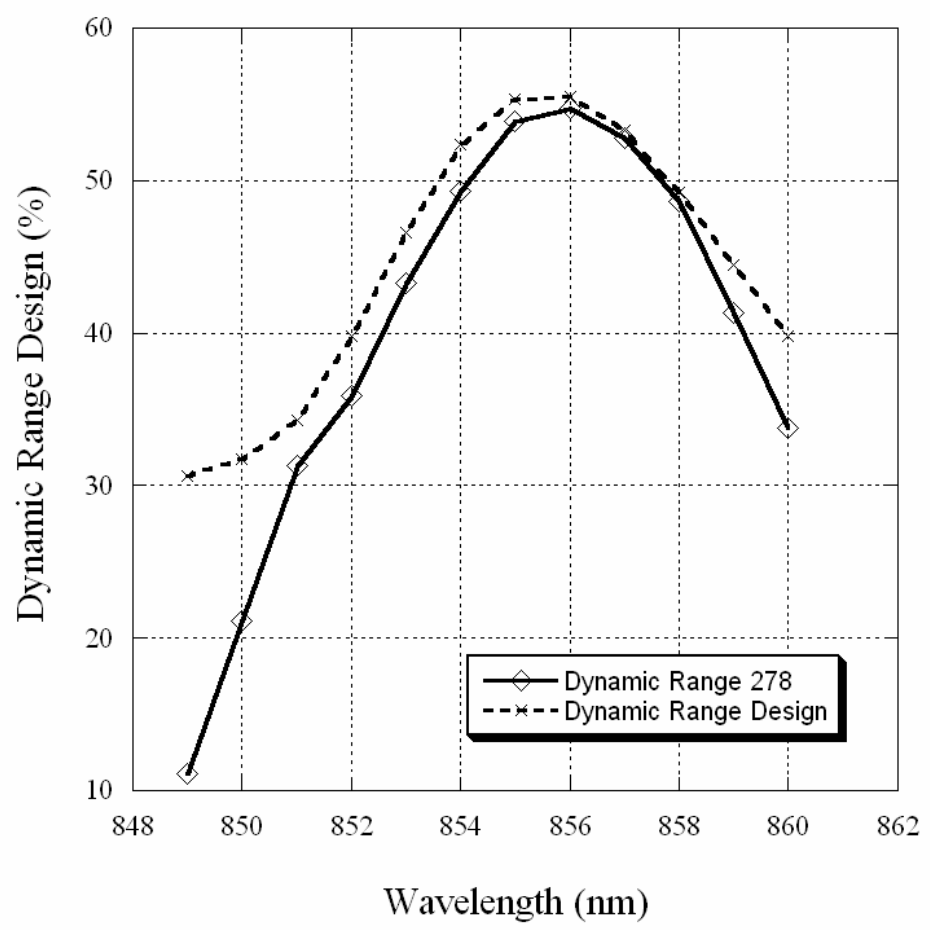

Figure 6.10: The dynamic range of the simulated subtractor is presented as a function of wavelength, calculated using the design and experimental data from wafer 278.

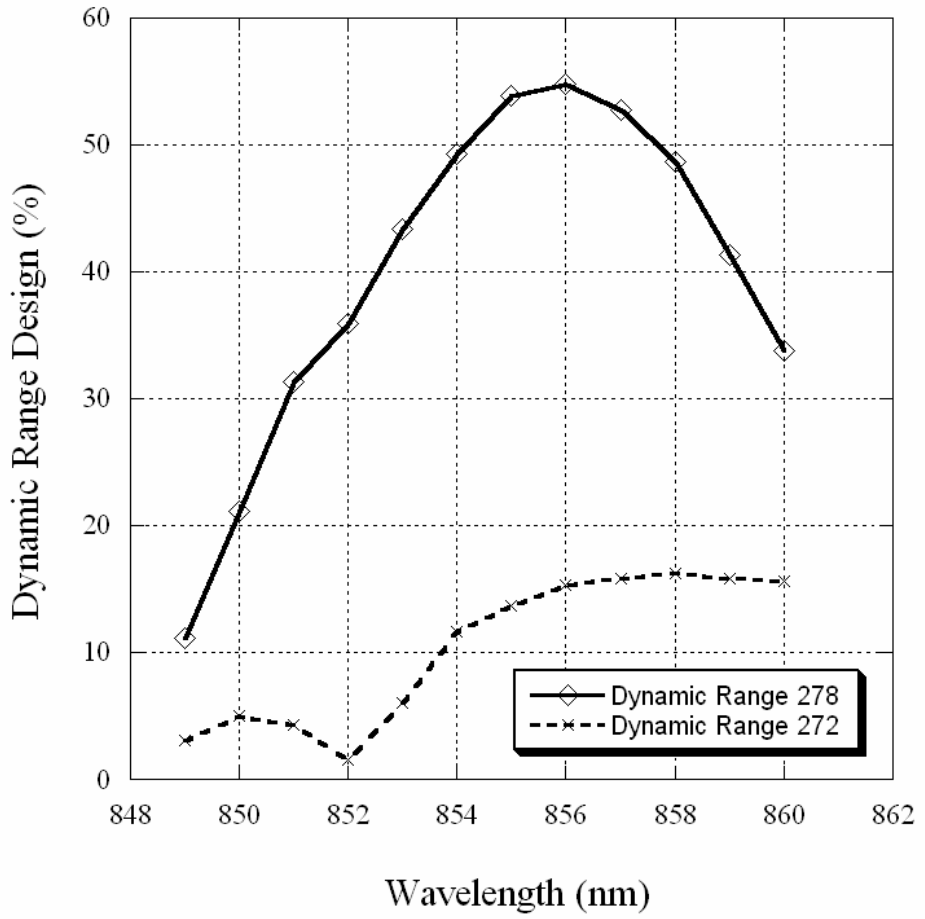

Figure 6.11: The dynamic range of the simulated subtractor is presented as a function of wavelength calculated using experimental reflectivity and responsivity data from wafers 278 and 272. The effect of the Fabry-Perot resonance is demonstrated as 278 has the resonance at 857 nm, while wafer 272 has the resonance at 830 nm.

6.11. Wafer 272 has the Fabry-Perot resonance positioned at 830 nm, which has minimal effect on the subtractor operation at the wavelengths considered. However, wafer 278 has the Fabry-Perot positioned at 857 nm, and a much larger dynamic range is achievable. Thus Fig. 6.11 demonstrates that the Fabry-Perot resonance significantly enhances the dynamic range of an optical SEED subtractor.

6.1.2 Comparator

The operation of the comparator was described in detail in Chapter 3 using chip 436. However, due to the absence of a Bragg reflector in these devices, it was not

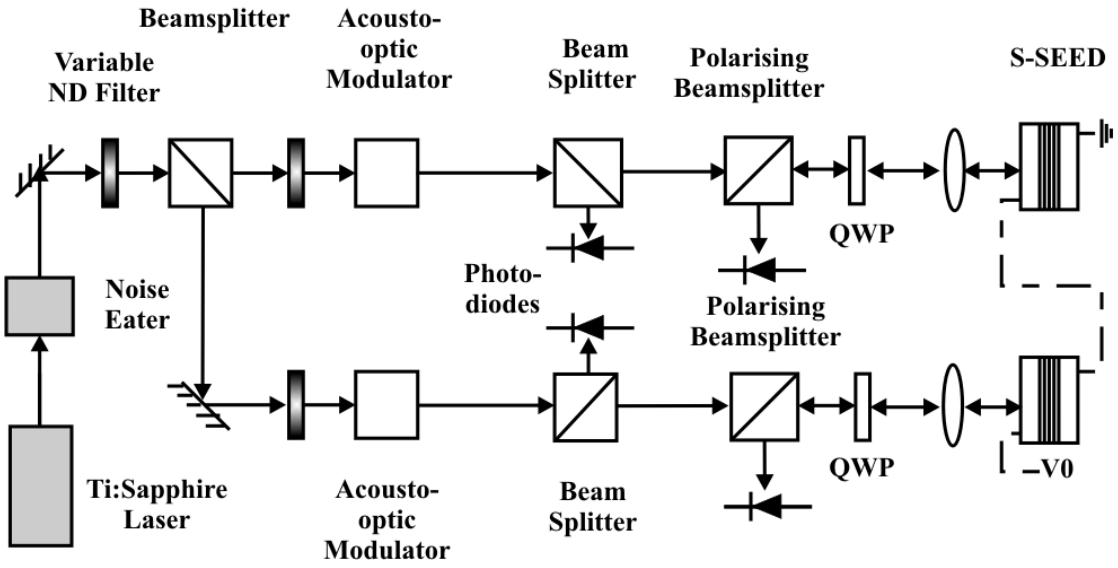

Figure 6.12: Experimental setup for measurement of output contrast from an S-SEED.

demonstrated with an optical output. Therefore, to verify the expected performance in the A/D application, we repeat the clocked comparator switching experiment using devices from wafer 278 in this section.

To reiterate, the clocked comparator switching experiment consists of the application of optical pulses to set the S-SEED into a high or low state, followed by higher power clock pulses to read out the S-SEED state. As distinct from the set pulses, the clock pulses applied to each SEED are ideally equal in power. This technique provides time sequential gain[36], which occurs when the power applied for the read-out pulses is greater than the input set pulses. The ratio of the power output from each SEED during the application of the clock pulse gives the contrast ratio.

The experimental setup is given in Fig. 6.12. The setup is the same as that employed in Chapter 3, Fig. 3.14, except for the addition of a polarising beam splitter and quarter waveplate in each beam to enable measurement of the reflected light.

As our devices were grown on a conducting N-type substrate, to simplify the N-contact of the device, all the diodes on a wafer had a common cathode. Therefore, to construct an S-SEED we required two separate pieces of wafer to allow two devices

to be placed electrically in series. Unfortunately, on the separate pieces of wafer 278 that we had available, we were unable to find two identical working devices. The consequences of using two devices with different peak responsivities, reflectivities and resonance positions were that unequal clock powers (P_{clock1} and P_{clock2}) were required for the read-out pulses. This requires modification to the definition of contrast ratio

$$CR = \frac{Q_H/P_{clock1}}{Q_L/P_{clock2}}. \tag{6.18}$$

The simulated hysteresis curve for the unequal devices is given in Fig. 6.13 and is centred at $P_{in}/P_{fixed} = 1.34$, owing to different peak responsivities of the two devices.

Nevertheless, with the correct choice of input powers, the comparator operation was successfully demonstrated. The simulation and calibrated measured optical output are compared in Fig. 6.14 (a) for parameters $\lambda = 847\,\text{nm}$, $V_0 = -8.5\,\text{V}$, $P_{low} = 37\,\mu\text{W}$, $P_{high} = 116\,\mu\text{W}$, $P_{fixed} = 53\,\mu\text{W}$, $P_{clock1} = 214\,\mu\text{W}$ and $P_{clock2} = 157\,\mu\text{W}$ that produced a large output contrast and avoided device heating and saturation. As was the case in Chapter 3, agreement is observed, within the predicted error, between the simulation and experiment. Importantly, there is significant contrast between the two labelled output clock states. Also, the concept of time sequential gain is demonstrated, which is simply that the output (clocked) states are a higher power than the set states. The quantisation error seen in the measurement on the oscilloscope is due to large voltages produced by the photodiode used to measure the power. For comparison to the results in Chapter 3, the output voltage is presented in Fig. 6.14 (b).

A simulation of the unequal devices used in the experiment was performed to calculate the optimum contrast ratio, by varying the voltage (V_0) and wavelength, with the constraint that the voltage could not exceed $-8.5\,\text{V}$. This was compared in Fig. 6.15 to the optimum contrast ratio calculated using equal devices in the simulation. Due to the use of equal clock powers, Fig. 6.15 shows that the achievable contrast using equal devices is reduced compared to the case with unequal devices. The calculated contrast shown in Fig. 6.15 is relatively low, compared to values

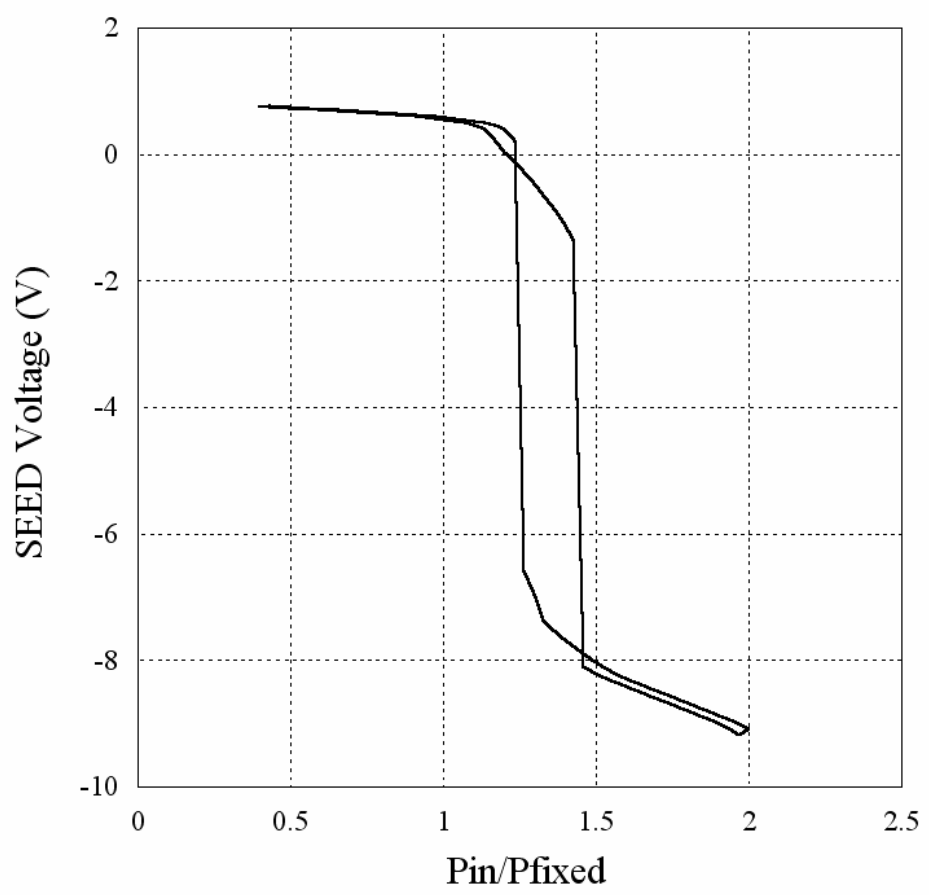

Figure 6.13: Simulated hysteresis curve for an S-SEED constructed from two unequal devices on wafer 278. The curve plots the voltage of one SEED as a function of the ratio of the input power to each SEED at 850nm.

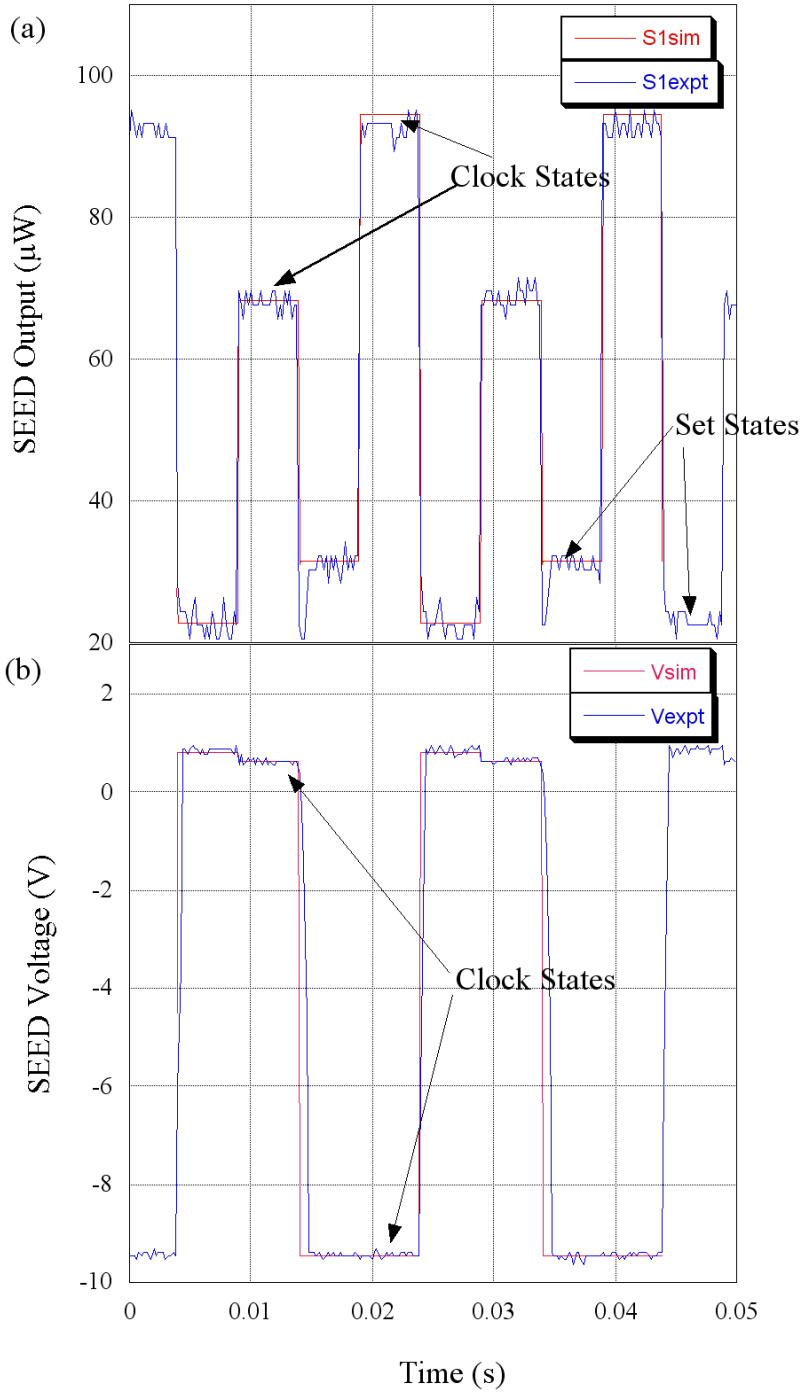

Figure 6.14: Comparison of the simulated (red) and measured (blue) results for the time sequantial gain experiment. Optical output is given in part (a) and voltage output in part (b). The parameters were $\lambda = 847\,\text{nm}$, $V_0 = -8.5\,\text{V}$, $P_{low} = 37\,\mu\text{W}$, $P_{high} = 116\,\mu\text{W}$, $P_{fixed} = 53\,\mu\text{W}$, $P_{clock1} = 214\,\mu\text{W}$ and $P_{clock2} = 157\,\mu\text{W}$. The mean absolte percentage error between simulation and experiment in part (a) was 5.0%, which is within the 2.2% simulation error and 2.9% experimental error (combined 5.1%) due to unnormalised laser noise. The error between simulation and experiment in part (b) was 0.5%. The improvement is due to reduced laser and oscilloscope quantisation noise.

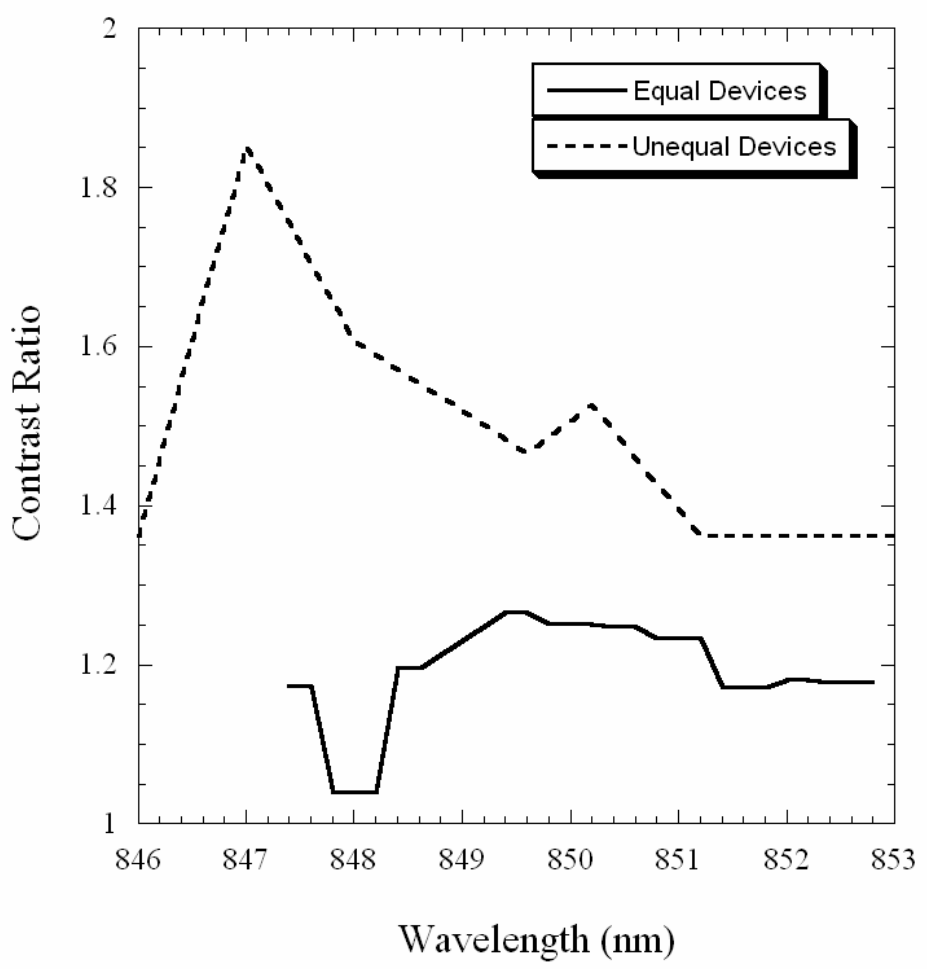

Figure 6.15: Calculated contrast ratio with optimum V_0, for devices used in the comparator experiment of Fig. 6.14 (dashed) and for identical devices in the S-SEED (solid).

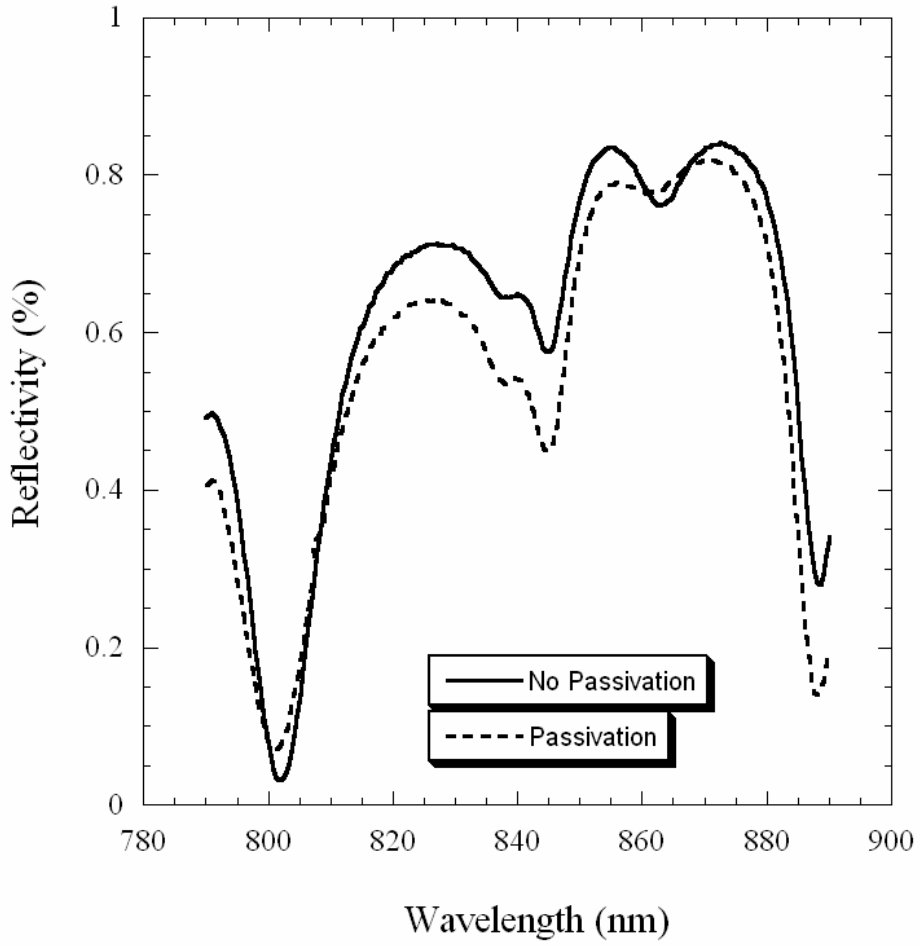

Figure 6.16: Reflectivity of different portions of a device window with SiO_2 passivation (dashed), and without (solid).

greater than 10 achieved in similar device structures[73]. Part of the reason for the low contrast ratio is due to a reduction in depth of the Fabry-Perot resonance, caused by a SiO_2 passivation layer, that was not completely removed from the device window during fabrication. The effect of the SiO_2 passivation layer is to reduce the reflectivity of the air/semiconductor interface, reducing the Finesse of the Fabry-Perot. The effect on device reflectivity is demonstrated in Fig. 6.16. The device used in Fig. 6.16 had passivation in the centre of the active area, but not on the edge. This allowed measurement of device reflectivity with and without SiO_2 passivation by focusing the laser to a small spot, and positioning the spot in the centre or on the edge of the device's active area. This device was not used in the comparator experiment as it had high dark current.

Greater contrast ratio can be achieved by co-locating the Fabry-Perot resonance and the zero field heavy-hole exciton peak[73], at the expense of subtractor dynamic range. Alternatively, the addition of extra quantum wells may be used to increase absorption, without adversely affecting subtractor performance. With greater absorption, the matched cavity condition (5.35) is approached, reducing the minimum reflectivity and increasing contrast.

To summarise the results presented in this chapter thus far,

- Optical subtraction has been experimentally demonstrated
- The conditions necessary to idealise subtraction have been derived and experimentally verified
- All optical switching has been experimentally demonstrated and agreement achieved with simulated results.

6.1.3 Optical Clock

As discussed in the introduction, the availability of clocks with timing jitter that are at least an order of magnitude lower than that achievable with electronic components is one of the main motivations for considering a photonic A/D. Timing jitter of less than 100 fs has routinely been reported [77] using modelocked fibre lasers at multi-GHz repetition rates, and values as low as 16 fs have been achieved [3]. Semiconductor diode lasers have been mode-locked using both active modulation of the gain at the cavity round-trip time, and by passive means using a saturable absorber. Another clock source called a coupled optoelectronic[78] oscillator has been proposed that uses a semiconductor optical amplifier or a colliding pulse modelocked laser[79] to achieve ultra low jitter values. This technique has the potential advantage of achieving lower jitter than actively locked semiconductor lasers, while still being compatible with integration into a small package[78]. Further, the use of semiconductor optical amplifiers[80] or colliding pulse modelocked lasers[81] allow the clock source to operate at around 850 nm.

6.1.4 Gain and Delay

Optical gain is required to idealise the subtractor and overcome losses. The most appropriate way of providing gain for our application is with a semiconductor optical amplifier (SOA). It can be manufactured from the same material system as the SEEDs, it is of similar dimensions and the gain is controlled by the supplied current. A SOA can be formed by the operation of a Fabry-Perot laser diode below oscillation threshold, and this type of device is termed a Fabry-Perot amplifier (FPA). Alternatively, high quality anti-reflection coatings can be applied to both facets of a laser diode to form a travelling wave amplifier (TWA). A TWA acts as a single pass amplifier with superior gain bandwidth and signal gain compared to a Fabry-Perot amplifier [82]. Examples of demonstrated SOAs based upon the $GaAs/AlGaAs$ material system are given in the literature for an FPA[83] and a TWA[80].

The delay is the simplest component to implement, as it consists of a length of waveguide or free space in which light propagates. The fabrication of the precise delay length (d) is important for successful operation of the oversampled quantiser. For propagation in a medium of refractive index n, d is given by

$$d = \frac{t_d\ c}{n}, \tag{6.19}$$

where c is the velocity of light in vacuum and t_d is the required time delay. For example, a sigma-delta quantiser loop operating at a clock frequency of 50 GHz requires a delay element of one clock period, or $t_d = 2 \times 10^{-11} s$. This corresponds to a length in $GaAs$ of 1.67 mm, which is a practical length to fabricate in a photonic integrated circuit.

To summarise, the individual operation of the comparator and subtractor has been demonstrated experimentally and simulations of each component have agreed with expectation. In addition, the clock, gain and delay have been considered. Thus each of the five elements required for the sigma-delta and error diffusion quantiser architectures have been shown to demonstrate the requisite properties. The following sections consider the task of integrating the components.

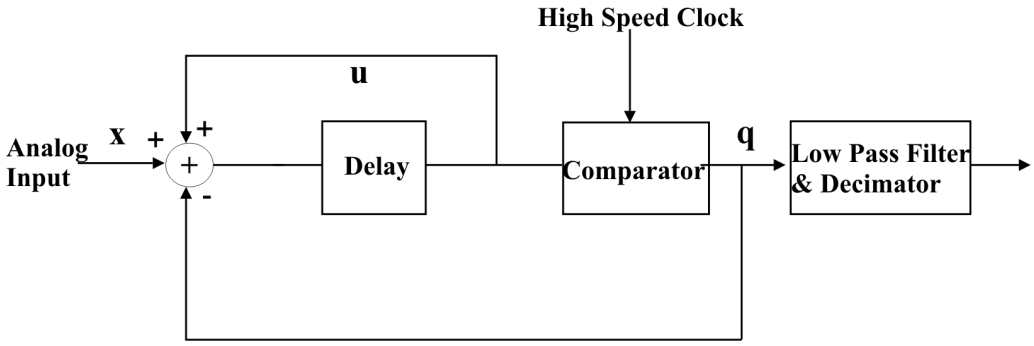

Figure 6.17: Schematic of the sigma-delta quantiser architecture.

6.2 Architecture

Until now, the sigma-delta architecture of Fig. 6.17 has been considered superior for a photonic implementation, compared to the error diffusion design, as it requires one less subtraction node. In this section, the question of which architecture is superior will be revisited by considering the subtractor dynamic range required for each design. Additionally an optical layout of the quantiser will be proposed and its implementation considered.

To determine the limits of the subtractor performance, we define the subtraction ratio for each subtractor as

$$subtraction\ ratio(q_n) = \left| \frac{\text{negative } input}{\text{positive } input} \right| \tag{6.20}$$

We also repeat the constraints that unipolar operation implies for the error diffusion, of Fig. 6.18, and sigma-delta architectures, which were described in Chapter 4, Section 4.2.1 for the specific cases of $q_n = Q_L$ and $q_n = Q_H$. Using (4.16) and (4.31) and the comparator characteristic, of Fig. 6.19 the limits for $u_n,\ x$ and e_n are

$$\begin{aligned} P_{\theta L} &\leq u_n \leq Q_H - Q_L + P_{\theta H} \ if\ q_n = Q_H \\ Q_L - Q_H + P_{\theta L} &\leq u_n \leq P_{\theta H} \qquad if\ q_n = Q_L \qquad (6.21) \\ Q_L &\leq x \leq Q_H \qquad (6.22) \\ Q_L - P_{\theta H} &\leq e_n \leq Q_H - P_{\theta L}, \qquad (6.23) \end{aligned}$$

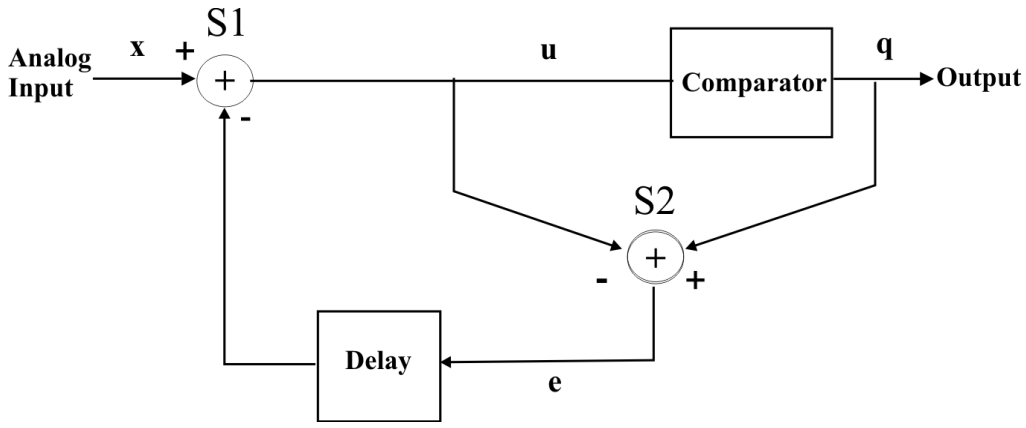

Figure 6.18: Schematic of the error diffusion quantiser architecture.

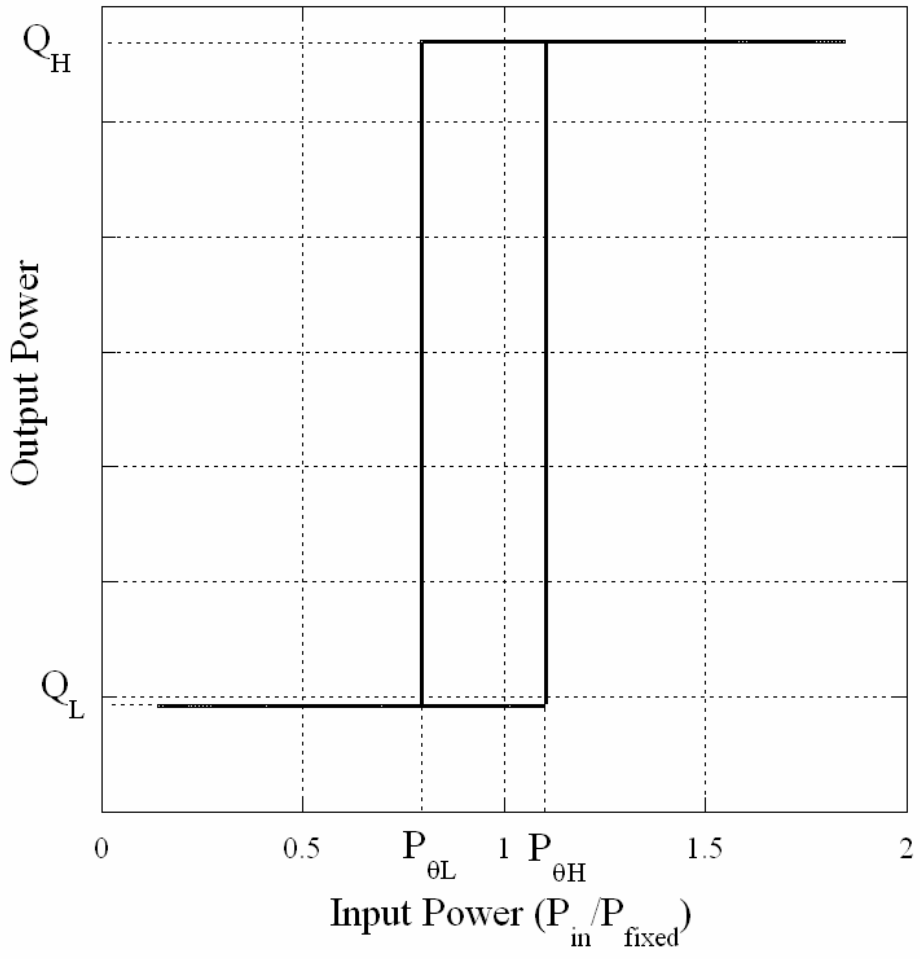

Figure 6.19: Schematic of an optical comparator with hysteresis. The output levels are labelled Q_H and Q_L, while the limits of the hysteresis region are labelled $P_{\theta H}$ and $P_{\theta L}$.

where constraint (6.23) is only applicable to the error diffusion architecture.

First consider the error diffusion architecture governed by

$$u_n = x_n - e_{n-1} \tag{6.24}$$

$$e_n = q_n - u_n. \tag{6.25}$$

The subtraction ratio of the node labelled S1 in Fig. 6.18, which can be written as

$$subtraction\ ratio = \frac{e_{n-1}}{x}. \tag{6.26}$$

Using (6.22) and (6.23) the extrema are

$$subtraction\ ratio_{\max} = \frac{Q_H - P_{\theta L}}{Q_L} \tag{6.27}$$

$$subtraction\ ratio_{\min} = \frac{Q_L - P_{\theta H}}{Q_H}. \tag{6.28}$$

The required dynamic range of the subtractor node S1 can be calculated from the difference of (6.27) and (6.28) to yield

$$dynamic\ range = \frac{Q_H^2 - Q_L^2 - Q_H P_{\theta L} + Q_L P_{\theta H}}{Q_H Q_L}. \tag{6.29}$$

For the second error diffusion subtractor, labelled S2, the subtraction ratio is

$$subtraction\ ratio = \frac{u_n}{q_n}. \tag{6.30}$$

For this subtractor, we must consider the minimum and maximum values of the subtraction ratio for the case when $q_n = Q_H$ and $q_n = Q_L$. Using (6.21) and (6.21),

we can write the extrema as

$$\begin{aligned} \textit{subtraction ratio}_{\max}(Q_H) &= \frac{Q_H - Q_L + P_{\theta H}}{Q_H} \\ \textit{subtraction ratio}_{\max}(Q_L) &= \frac{P_{\theta H}}{Q_L} \qquad (6.31) \\ \textit{subtraction ratio}_{\min}(Q_H) &= \frac{P_{\theta L}}{Q_H} \qquad (6.32) \\ \textit{subtraction ratio}_{\min}(Q_L) &= \frac{Q_L - Q_H + P_{\theta L}}{Q_L}. \qquad (6.33) \end{aligned}$$

In Appendix A (6.31) and (6.33) are shown to be the greatest extrema. Therefore, the required dynamic range of subtractor S2 is

$$\textit{dynamic range} = \frac{Q_H(Q_H - P_{\theta L}) + Q_L(P_{\theta H} - Q_L)}{Q_H\ Q_L}. \qquad (6.34)$$

To derive the required subtraction limits for the sigma-delta of Fig. 6.17, defined by

$$u_n = x_n - q_{n-1} + u_{n-1}, \qquad (6.35)$$

we write the subtraction ratio as

$$\textit{subtraction ratio} = \frac{q_n}{x_{n+1} + u_n}. \qquad (6.36)$$

Again both cases of $q_n = Q_H$ and $q_n = Q_L$ need to be considered. Therefore, using (6.21), (6.21) and (6.22), the extrema are

$$\begin{aligned} \textit{subtraction ratio}_{\max}(Q_H) &= \frac{Q_H}{Q_L + P_{\theta L}} \\ \textit{subtraction ratio}_{\max}(Q_L) &= \frac{Q_L}{Q_L + Q_L - Q_H + P_{\theta L}} \qquad (6.37) \\ \textit{subtraction ratio}_{\min}(Q_H) &= \frac{Q_H}{Q_H + Q_H - Q_L + P_{\theta H}} \qquad (6.38) \\ \textit{subtraction ratio}_{\min}(Q_L) &= \frac{Q_L}{Q_H + P_{\theta H}}. \qquad (6.39) \end{aligned}$$

Finally, as shown in Appendix A, (6.37) and (6.39) are the greatest extrema, and they are used to calculate the required dynamic range required for the subtractor in

the sigma-delta architecture as

$$dynamic\ range = \frac{Q_H^2 - Q_L^2 + Q_H P_{\theta H} - Q_L P_{\theta L}}{(Q_H + P_{\theta H})(Q_L + P_{\theta L})}. \tag{6.40}$$

To determine which architecture requires the greatest subtractor performance, the difference between the dynamic range of the sigma-delta and first error diffusion subtractor is simplified in Appendix A and demonstrated to be negative. Therefore (6.40) $<$ (6.29), proving that the sigma-delta architecture has a less arduous requirement of subtractor performance and is therefore the preferred architecture.

One further constraint to consider is the allowable contrast ratio that maintains unipolarity. Dividing both sides of the unipolar constraint that applies to both architectures, (4.16) by Q_L gives

$$\frac{Q_H}{Q_L} - 1 \leq \frac{P_{\theta L}}{Q_L}. \tag{6.41}$$

Since the contrast ratio (CR) of the comparator output is defined as

$$CR = \frac{Q_H}{Q_L}, \tag{6.42}$$

(6.41) leads to the constraint that

$$CR \leq 1 + \frac{P_{\theta L}}{Q_L}. \tag{6.43}$$

In the case of the error diffusion, the second unipolarity constraint ($Q_L \geq P_{\theta L}$) limits the contrast ratio of (6.43) to a maximum of two. However, in the case of the sigma-delta, contrast ratios greater than two are allowed.

In summary, the first-order sigma-delta architecture has been demonstrated to require one less subtractor, and hence less SEEDs. It also has a reduced subtraction requirement and a greater allowable comparator contrast ratio, when compared to the error diffusion architecture. Therefore, the sigma-delta is easier to implement in a photonic technology. Henceforth we will only consider the sigma-delta.

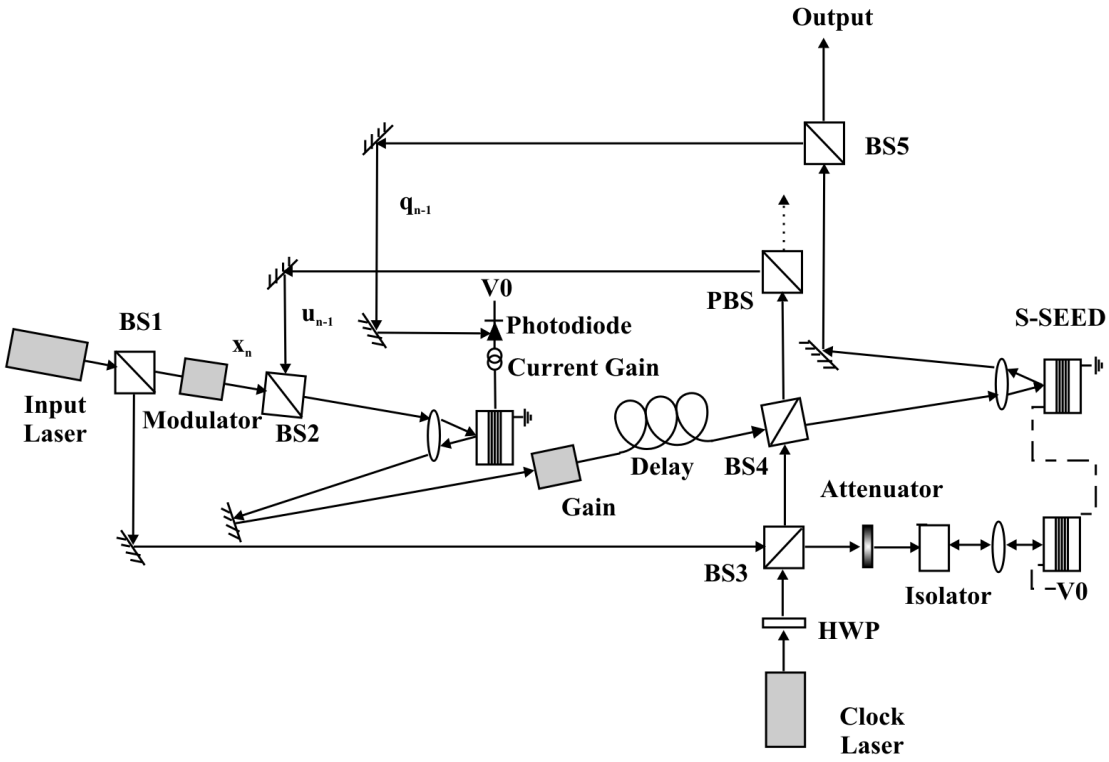

Figure 6.20: Proposed implementation of the Sigma Delta architecture in free space photonics.

6.2.1 Implementation

A proposed photonic implementation of the sigma-delta architecture is given in Fig. 6.20. The description of the layout starts with the laser diode (input laser) that provides the fixed input for the S-SEED comparator and together with a modulator generates the input signal x_n. The beam representing x_n is combined with u_{n-1} at beamsplitter BS2 and input onto the SEED forming the subtractor. The output of the SEED is increased by the optical gain, which is set to idealise the subtractor, as discussed in Section 6.1.1, and overcome the loss of BS4 and BS2. A delay and BS4 are used to provide u_{n-1}. A separate diode laser (clock laser) provides the clock input to the comparator through BS3. Utilising the time sequential gain feature of the comparator, the power of the clock laser is set such that after the losses of BS4 and BS5, the correct clock power to maintain unipolarity reaches the photodiode. The output of the quantiser is given by the transmitted beam at BS5, while the reflected beam passes through a delay to provide q_{n-1} and complete the loop.

A free space laboratory implementation of a photonic sigma-delta, as shown in Fig. 6.20, is an important step in verifying the architecture's suitability for this technology and for establishing device and architecture design criteria. Nevertheless, to realise short path lengths and operating speeds greater than current state-of-the-art electronic A/Ds, and to produce an A/D in a small package at reasonable cost, the photonic sigma-delta requires implementation in a photonic integrated circuit technology. Current appropriate technologies available are monolithic integration on a single wafer or hybridisation on a separate waveguide structure[84]. Much of the current photonic integrated circuit research is directed at the telecommunications market, where wavelengths around $1.55\,\mu$m are predominantly used on Si or InP substrates. Therefore, it would be advantageous to use the knowledge already gained in current photonic integrated circuit applications. This would necessitate the use of MQW devices operating at $1.55\,\mu$m using materials such as InGaAsP on InP substrates, such as those demonstrated in [85], [86], [87]. A further differing design requirement for integrated devices is that the light is required to propagate parallel to the plane of the quantum wells and the devices become polarisation dependent[86], [87], as opposed to the normal propagation used in our devices which is polarisation insensitive. The light can then be coupled out of the device via evanescent coupling[88], or at the edge of the device in either the monolithic construction or flip-chip packaged hybrid case[89]. An example of a monolithically integrated waveguide, MQW modulator and SOA is given in [90]. Propagation of the light parallel to the quantum well layers gives greater device design flexibility, as the absorption is determined by the length of the device and not by the number of quantum wells or a Fabry-Perot resonance.

As the photonic sigma-delta architecture is appropriate for any photonic system that has a comparator and a subtractor available, the free-space demonstration of the photonic sigma-delta, and simulations thereof, using normal incidence SEEDs built in the GaAs/AlGaAs material system, demonstrates the concept that can be translated into a higher operating frequency waveguide system built on InP.

6.3 Results

In the previous sections individual experimental and simulated operations of the subtractor and comparator have been demonstrated. Furthermore, the constraints upon the architecture were calculated and an optical layout was designed. This section details the integration of the individual models into one simulation of the sigma-delta architecture, that solves the differential equation describing the equivalent circuits of the subtractor and comparator, for each cycle of the quantiser loop. Experimental data is used for the device responsivity, capacitance, reflectivity and dark current. The output of the simulation is then used to calculate the performance of the sigma-delta quantiser from the power spectrum, as described in Chapter 3.

To choose a wavelength for which the comparator and subtractor would simultaneously operate, Fig. 6.15 and Fig. 6.10 were used to select 849 nm. The following parameters were found using many trial simulations to maintain unipolarity of the sigma-delta quantiser simulation: $P_{fixed} = 60\,\mu\text{W}$, $P_{clock} = 200\,\mu\text{W}$, $V_0(comparator) = -9\,\text{V}$, $V_0(subtractor) = -8\,\text{V}$, $G_1 = 1.18$, $G_2 = 1.15$, $\lambda = 849\,\text{nm}$, $fs = 1000\,\text{Hz}$, $f_0 = 1\,\text{Hz}$, oversampling ratio= 100. The above parameters resulted in the following characteristic values: $Q_H = 83.6\,\mu\text{W}$, $Q_L = 78.5\,\mu\text{W}$, $P_{\theta H} = 63.2\,\mu\text{W}$, $P_{\theta L} = 58.0\,\mu\text{W}$, $max\ subtraction = 61.2\%$, $min\ subtraction = 53.5\%$, contrast ratio= 1.065. A simulation of the sigma-delta was performed for 6000 clock cycles, with an input sine wave, centred at $(Q_H + Q_L)/2$, varying in amplitude from 0 to $(Q_H - Q_L)/2$. Indicative output from the simulation is presented in Fig. 6.21. A portion of the unprocessed quantiser output is shown in red, while the results of low-pass filtering one point from the centre of each output clock cycle are shown in blue, demonstrating the convergence of the processed output to the input sine wave. Plotted in Fig. 6.22 is the power spectrum of the unprocessed output, which is used to calculate the signal to quantisation noise ratio (SQNR) as described in Section 4.1.1. Part (a) plots the spectrum up to half the sampling frequency, while part (b) has a reduced scale to highlight the input signal. The resultant SQNR performance of the sigma-delta simulation, as a function of input amplitude is given in Fig. 6.23. In addition, the SQNR of the sigma-delta quantiser with an ideal comparator and

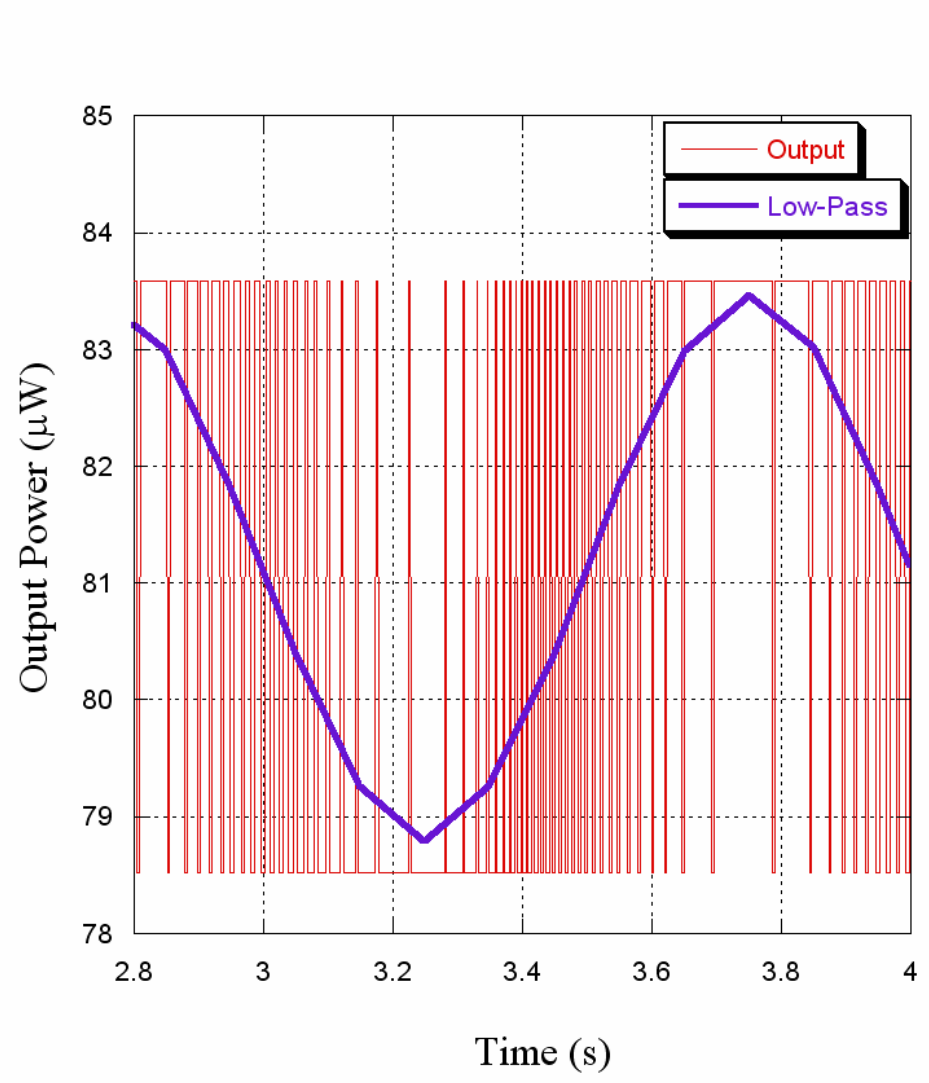

Figure 6.21: Output of the 1-bit sigma-delta quantiser simulation is shown in red. Overlayed in blue is the result of low-pass filtering.

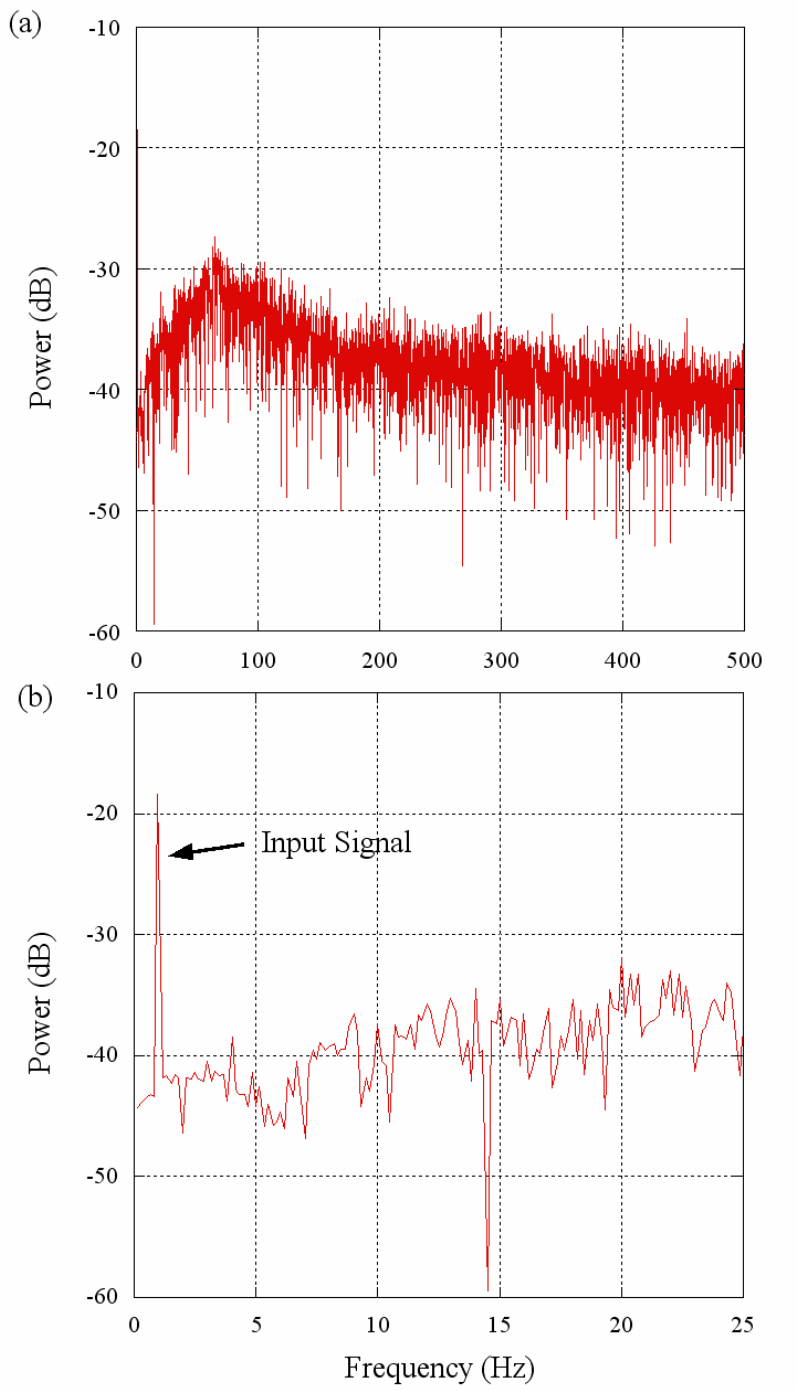

Figure 6.22: Power spectrum of the unprocessed sigma-delta output. Part (a) plots the spectrum up to $f_s/2$, while part (b) has a reduced scale to highlight the input signal (labelled).

subtractor, using the parameters given above is plotted in Fig. 6.23. The A/D resolution in bits, is given by the well known expression[8]

$$bits = \frac{SQNR - 1.76}{6.02}. \tag{6.44}$$

Thus the peak SQNR of Fig. 6.23 corresponds to a resolution of 7.93 bits.

Even though the SQNR of the sigma-delta simulation approached that of the ideal case, demonstrating that a realistic subtractor provides sufficient linearity, the input range of 5.1 μW is too small to be practically useful. The input range is limited by the low contrast ratio, which in turn is a result of the requirement to have one device design that operates as a comparator and subtractor at a single wavelength. If a hybrid fabrication process is considered, as opposed to a monolithic one, then the freedom to use different wafer growths for the comparator and subtractor is allowed.

To simulate the performance of a hybrid packaged sigma-delta using an optimally designed comparator and subtractor, temperature tuning was employed to modify the characteristics of wafer 278. Altering the temperature of the device changes the bandgap of the semiconductor and also changes the length of the resonant cavity. The bandgap of $GaAs$ changes with temperature according to the empirical relation[67]

$$E_g(eV) = 1.519 - \frac{5.408 \times 10^{-4} T^2}{T + 204}. \tag{6.45}$$

Therefore, the shift in exciton position per degree change in temperature (in nm/K) is

$$\frac{dE_g}{dT} = \frac{3.422 \times 10^6 (274.3 + 0.6723T)T}{(-3000 + T)^2 (191.0 + T)^2}. \tag{6.46}$$

The change in the optical cavity is now considered, but due to insufficient data the variation of refractive index with temperature is neglected. Only the linear thermal

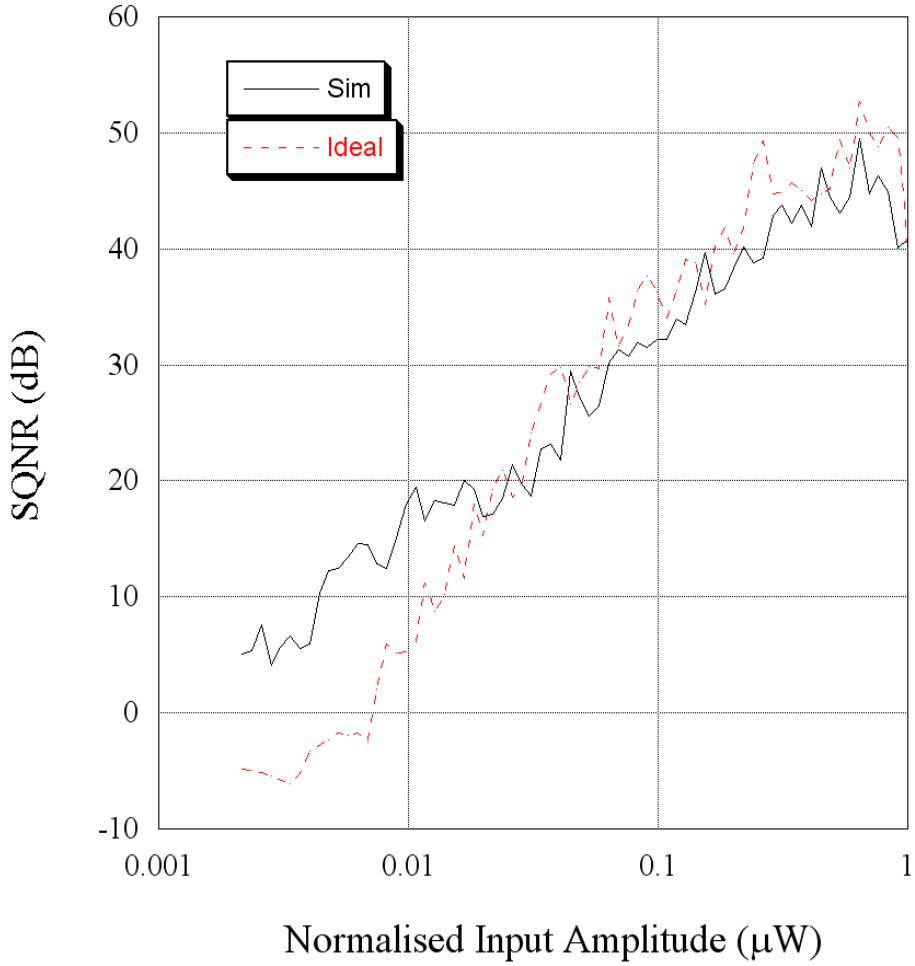

Figure 6.23: Signal-to-quantisation noise-ratio (SQNR) as a function of input amplitude for the photonic sigma-delta quantiser with identical devices used for the subtractor and comparator. Idealised and experimental data based simulations are compared.

expansion coefficient is used, and for $GaAs$ it is given by[67] in $10^{-6}/K$

$$\alpha(T) = 4.24 + 5.82 \times 10^{-3}T - 2.82 \times 10^{-6}T^2 \; for \; 200 < T < 1000K \tag{6.47}$$

where α is defined as

$$\alpha(T) = \frac{\Delta L}{L}\frac{1}{\Delta T} \tag{6.48}$$

and L is the initial length of the material. Using the simulation of the Fabry-Perot cavity described in the previous chapter, the unit length change in the Fabry-Perot resonance is found to be $0.00265\,\mathrm{nm}/10^{-6}$. Thus, the Fabry-Perot resonance shift with temperature (in nm/K) is given by

$$1.12 \times 10^{-2} + 1.54 \times 10^{-5}T - 7.47 \times 10^{-9}T^2 \; for \; 200 < T < 1000K. \tag{6.49}$$

If we now consider an example where the temperature is increased 50 degrees from a starting temperature of $300K$, the redshift in the exciton (6.46) is 13.9 nm and the redshift in the resonance (6.49) is 0.75 nm. Hence temperature variation of the device can be used to move the position of the exciton with negligible effect on the location of the Fabry-Perot resonance. This can have a significant impact on the device characteristics. An experimental demonstration of this is presented in Fig. 6.24, for a plot of reflectivity versus wavelength. As the temperature is increased by $60°C$, the heavy-hole exciton red-shifts approximately 17 nm, while the resonantly enhanced absorption peak (reflectivity minimum) created by the Fabry-Perot only moves 4 nm.

The optimum comparator design is one that has the heavy-hole exciton and Fabry-Perot resonance coincident for zero applied bias at the operating wavelength [73]. For wafer 278 this was achieved by increasing the temperature to move the exciton and Fabry-Perot resonance to a longer operating wavelength, as shown in the reflectivity plot of Fig. 6.25 for a temperature of $80°C$. The contrast ratio was simulated using experimental data for temperatures from $40 - 80°C$. The results

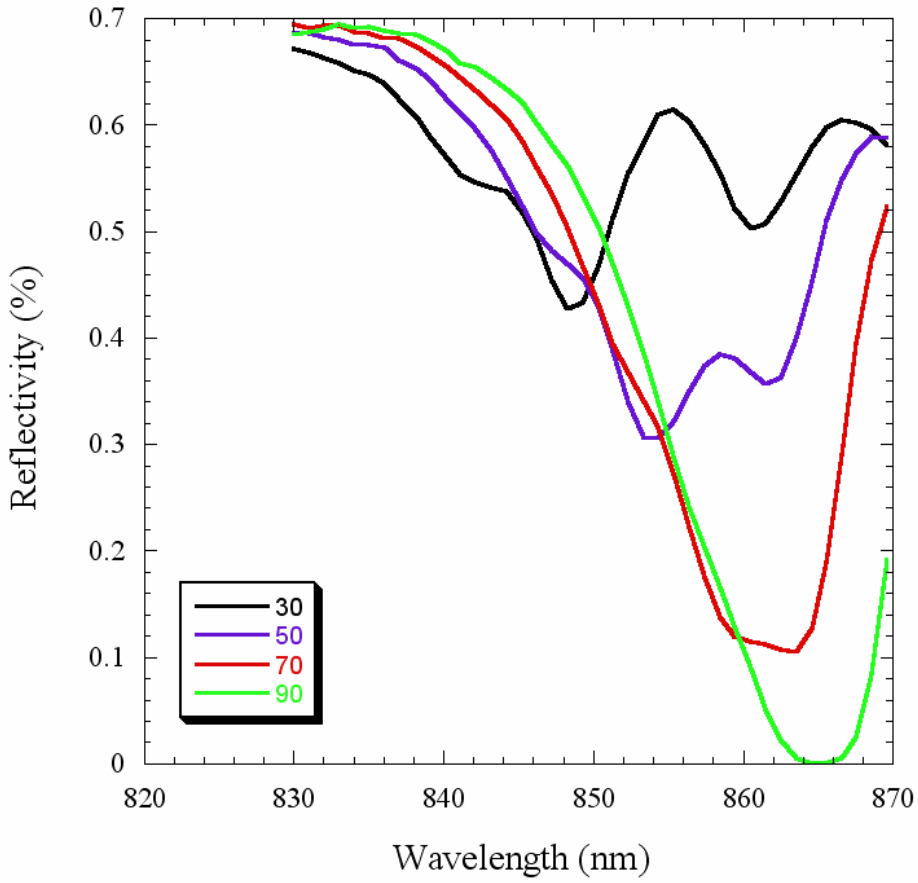

Figure 6.24: Reflectivity as a function of wavelength for device temperatures of 30°, 50°, 70° and 90°C. The heavy-hole exciton is observed to shift approximately 17nm, while the resonantly enhanced absorption peak created by the Fabry-Perot only shifts 4nm as the temperature increases by 60°C.

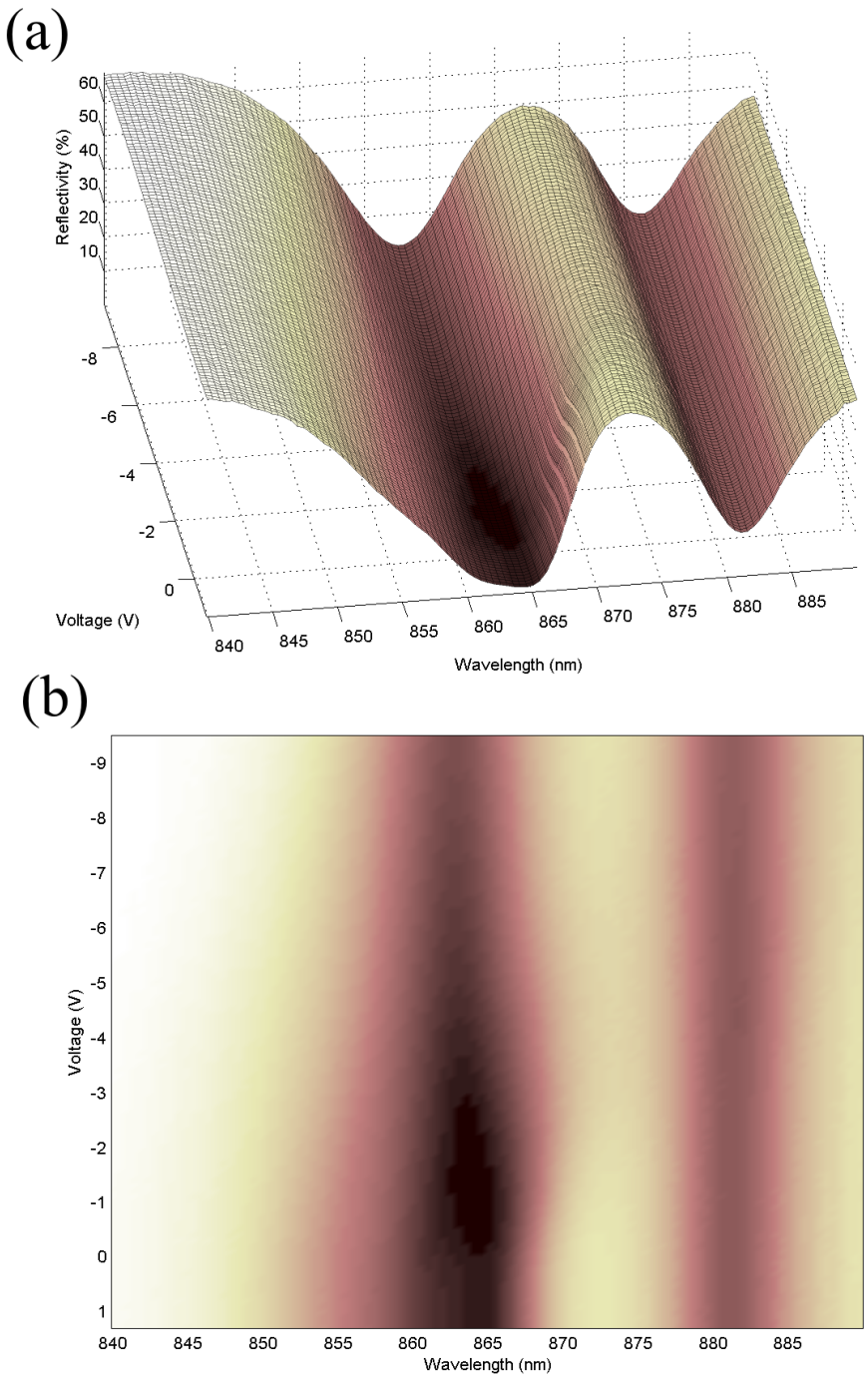

Figure 6.25: (a) Measured reflectivity as a function of wavelength and voltage for the a device on wafer 278 at $80°C$. (b) Projection (a) onto the x-y plane to elucidate the position of the features. The plots demonstrate that the reflectivity minimum occurs near $0V$ applied bias, which is optimum for the comparator operation.

are presented in Fig. 6.26 (a) and demonstrate that significantly greater contrast ratio is achievable at $80°C$, than at room temperature.

The optimum design for a subtractor is one where the operating wavelength is at the position of the Fabry-Perot resonance, and the exciton and Fabry-Perot peaks are brought into coincidence at the maximum operating voltage [73]. Achieving the maximum subtractor dynamic range was the main design goal for wafer 278. However, with a longer operating wavelength caused by the temperature tuning of the comparator, it was also necessary to temperature tune the subtractor. The simulated subtractor dynamic range for temperatures of $40 - 70°C$ is given in Fig. 6.26 (b) and the experimental reflectivity plot for the operating temperature of $40°C$ that achieves the peak dynamic range is given in Fig. 6.27.

With the option to choose a much higher contrast ratio than was the case for the simulation using equal devices, the architectural limit on contrast ratio of 2.28 imposed by (6.43) was reached. With the aid of Fig. 6.26 (a) and Fig. 6.26 (b) a contrast ratio of 1.86 was selected at an operating wavelength of 860 nm, which also maximised the subtractor dynamic range. To maintain unipolarity, the following parameters were used in a simulation of the sigma-delta quantiser : $P_{fixed} = 40\,\mu\text{W}$, $P_{clock} = 400\,\mu\text{W}$, $V_0(comparator) = -5\,\text{V}$, $V_0(subtractor) = -9\,\text{V}$, $G_1 = 1.05$, $G_2 = 1.72$, $\lambda = 860\,\text{nm}$, $fs = 1000\,\text{Hz}$, $f_0 = 1\,\text{Hz}$, oversampling ratio= 100. The above parameters resulted in the following characteristic values: $Q_H = 52.3\,\mu\text{W}$, $Q_L = 28.1\,\mu\text{W}$, $P_{\theta H} = 44\,\mu\text{W}$, $P_{\theta L} = 36\,\mu\text{W}$, $max\ subtraction = 81.6\%$, $min\ subtraction = 29.2\%$ and gave the SQNR performance as a function of input amplitude of Fig. 6.28. Figure 6.28 demonstrates agreement between the simulations based on ideal and experimentally based devices and a peak resolution of 8.71 bits, which is better than the results achieved for identical devices, while also allowing a larger input range. This result compares favorably with the peak theoretical value from (4.37) of 9.6 bits, as the simulated result is limited by hysteresis. Hence, there is scope to achieve improved SQNR by selecting parameters that minimise hysteresis, or implementing switching schemes that reset the S-SEED to a known state each clock cycle[15], negating the effect of hysteresis. More generally, SQNR performance could be improved by increasing the oversampling ratio, or implementing higher order ar-

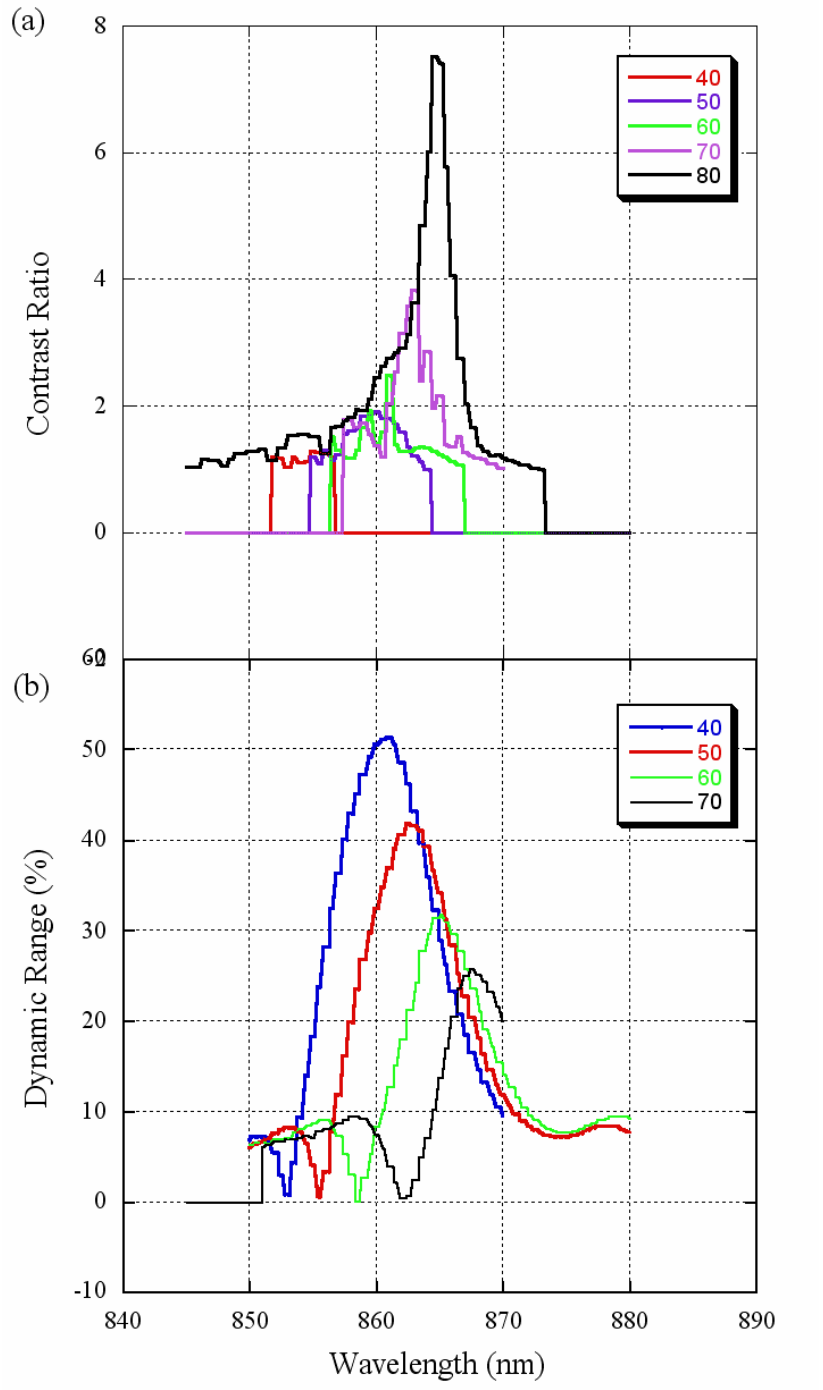

Figure 6.26: (a) Simulated contrast ratio for wafer 278 at temperatures from $40 - 80°C$. (b) Simulated dynamic range for wafer 278 at temperatures from $40 - 70°C$.

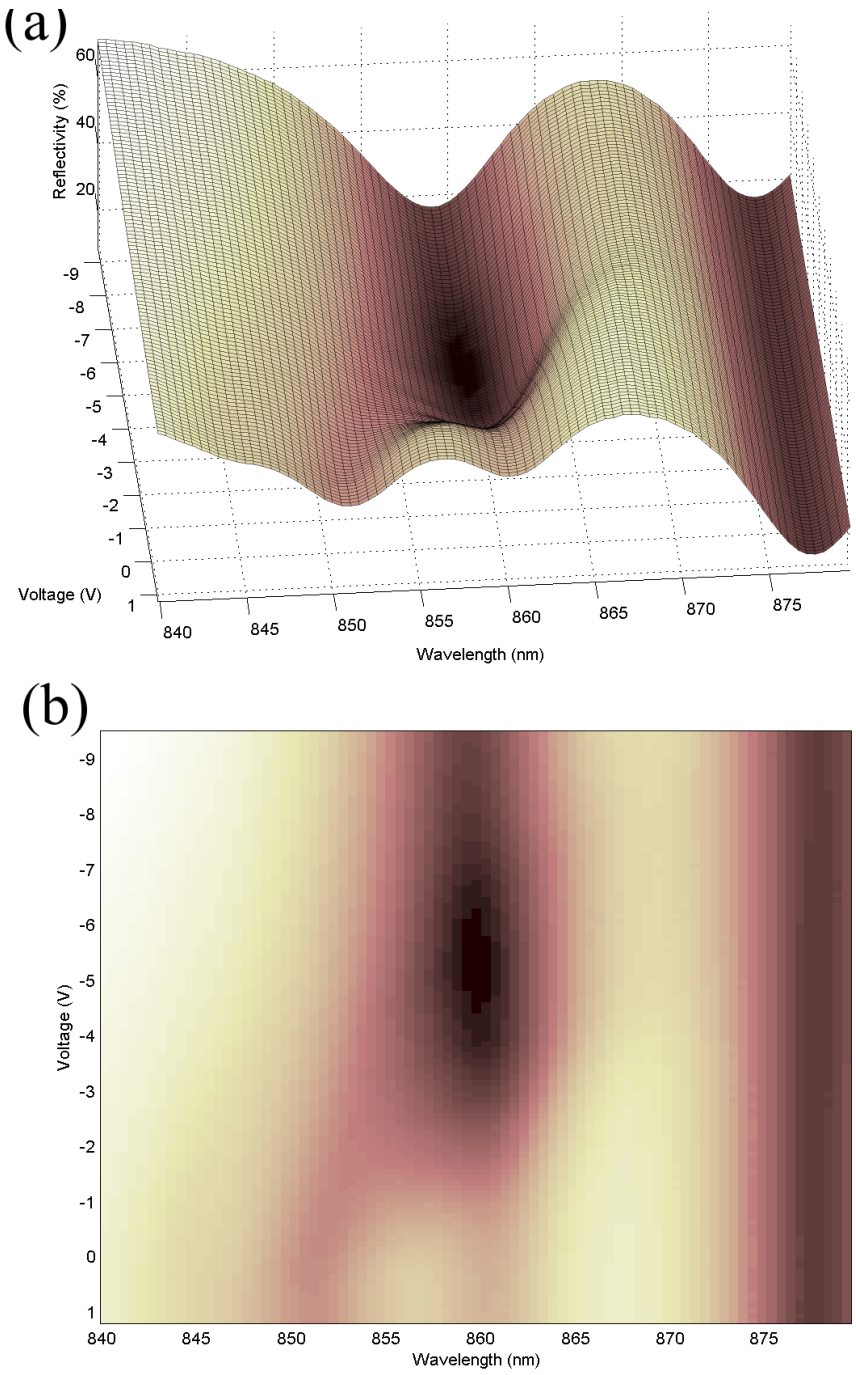

Figure 6.27: (a) Measured reflectivity as a function of wavelength and voltage for the a device on wafer 278 at $40°C$. (b) Projection (a) onto the x-y plane to elucidate the position of the features. The plots demonstrate that the reflectivity minimum occurs at a high applied bias for the operating wavelength ($\sim$860 nm), which is optimum for subtractor operation.

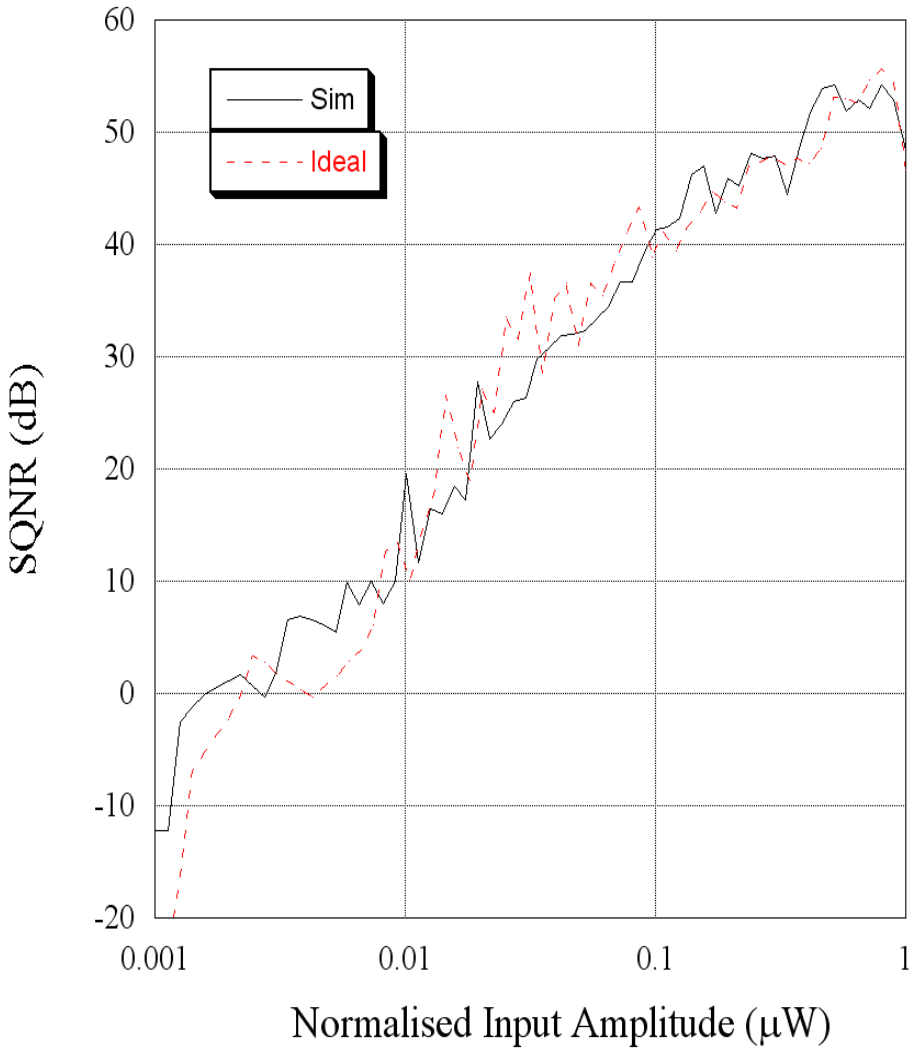

Figure 6.28: Signal-to-quantisation noise-ratio (SQNR) as a function of input amplitude for the photonic sigma-delta quantiser with separately optimised subtractor and comparator. Ideal and experimental based simulations are compared.

chitectures.

6.3.1 Operating Frequency Scaling

The results presented above use an S-SEED comparator operating at a clock speed of 1 kHz. The slow speed is a result of the large area devices, and hence large capacitance (∼100 pF per device). As a guide for the switching time (Δt), the linearisation of the differential equation for the S-SEED's equivalent circuit yields[36]

$$\Delta t = \frac{C_{tot} V_0}{\overline{S}(|P_{in2} - P_{in1}|)}. \tag{6.50}$$

Where C_{tot} is the total capacitance, $\overline{S}$ is the average responsivity and P_{in1} and P_{in2} are the input powers of the two devices in an S-SEED. Equation (6.50) demonstrates that the switching time is proportional to the total S-SEED capacitance and applied voltage, and it is inversely proportional to the difference in applied powers. Therefore, to achieve very low switching times, SEEDs should be fabricated with as small an area as possible. A switching time of 6 ps was demonstrated[27] for an S-SEED consisting of devices with a 27 μm diameter and 1 μm thick intrinsic region, giving a capacitance of 0.07 pF. In addition to the low capacitance, the following factors aided in achieving the reported short switching time: a small applied voltage of 1 V was required for switching, a 0.92 W peak power pulsed laser was used, low resistance contacts were fabricated and shallow quantum wells with thin barriers were used to minimise the carrier sweep out time[91].

In determining the switching time, the RC time constant dominates the time constant for transport of carriers out of the intrinsic region for devices with shallow quantum wells[27]. Therefore, it is realistic to scale the performance of the simulation by reducing the capacitance to a value as small as possible (*eg.* 23fF[44]) and reducing the applied bias to ~ 1 V. Furthermore, as shown in (6.50), increasing the applied power also reduces the switching time. We may increase the continuous wave power to approximately 30 mW, and still avoid exciton saturation[92]. Applying the above scalings to (6.50) yields an operating clock frequency of ~ 4 GHz.

To test the sigma-delta performance with an increase in operation speed due to

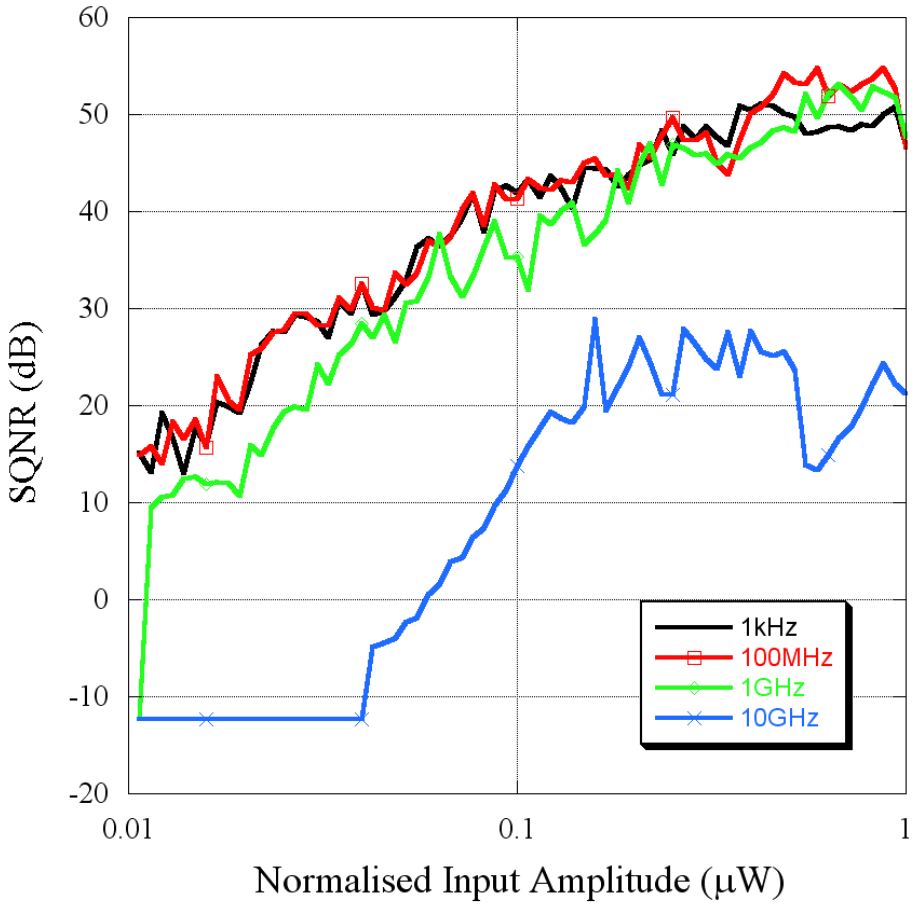

Figure 6.29: Simulated sigma-delta SQNR performance as a function of input amplitude for clock frequencies of 1 kHz, 100 MHz, 1 GHz and 10 GHz.

the application of these scalings, the numerical simulation was repeated using the following parameters: $P_{fixed} = 3\,\text{mW}$, $P_{clock} = 30\,\text{mW}$, $V_0(comparator) = -5\,\text{V}$, $V_0(subtractor) = -9\,\text{V}$, $G_1 = 1.05$, $G_2 = 1.72$, $\lambda = 860\,\text{nm}$, $C_{tot} = 20\text{fF}$, oversampling ratio= 100 $Q_H = 3.92\,\text{mW}$, $Q_L = 2.11\,\text{mW}$, $P_{\theta H} = 3.3\,\text{mW}$, $P_{\theta L} = 2.7\,\text{mW}$. The SQNR was calculated for clock frequencies of 1 kHz, 100 MHz, 1 GHz and 10 GHz with input frequencies 1 Hz, 1 MHz, 10 MHz and 100 MHz respectively. The results are presented in Fig. 6.29, which demonstrates that the sigma-delta performance with the scaled parameters does not deteriorate at clock frequencies up to 1 GHz, but is unacceptable at a frequency of 10 GHz. This is consistent with the approximation of (6.50) that with the substitution of the simulation parameters, predicts 10 GHz as the maximum switching frequency. The effect of device series

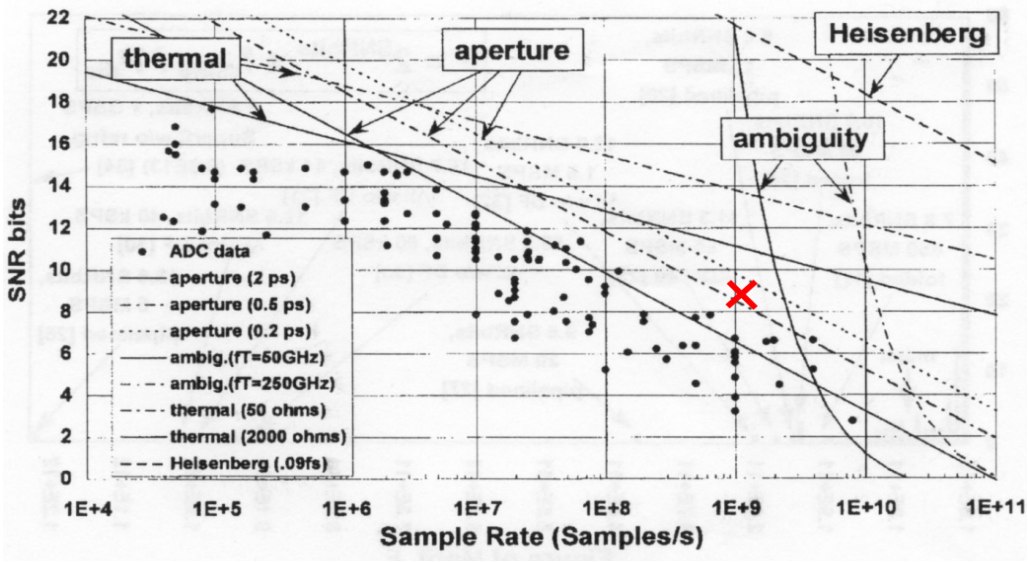

Figure 6.30: A/D performance resolution limitation due to thermal noise, aperture uncertainty (clock jitter) and comparator ambiguity, from [1]. The performance of a potential photonic sigma-delta is marked with a red cross.

resistance is included in the dark current in (6.50), but it is not included as an independent parameter in the numerical simulation as we were unable to measure contact resistance for the contact on the substrate. However, series resistance can have a significant impact on high speed performance, and a reduction in the resistance could yield a further increase in the sigma-delta operating speed. The upper limit on switching speed would likely be 6 ps, or 166 GHz, demonstrated in [27], giving an upper limit on performance of 8.71 bits at 1.6 GHz for a first-order photonic sigma-delta at an oversampling ratio of 100. Such a device would appear at the position shown with the cross in Fig. 6.30 on the A/D performance limitation diagram. This would be an improvement on the devices appearing on Fig. 6.30, with potential for further improvement with higher order architectures and greater oversampling ratios.

6.4 Summary and Future Work

As the photonic sigma-delta has been established to be feasible, the extension of Fig. 6.20 to a benchtop demonstration is planned for future work. However, we do not

have access to fabrication facilities to enable us to achieve the goal of constructing a sigma-delta photonic integrated circuit. To develop a photonic integrated sigma-delta, research would need to be undertaken to design and fabricate waveguides and waveguide compatible MQW devices, integrate these devices with lasers and amplifiers, and integrate the photonics with high speed electronics to perform decimation and filtering.

With respect to the architecture, future work is planned to investigate a differential photonic sigma-delta[43]. The differential architecture offers several important advantages over the unipolar version, at the expense of an increase in the number required MQW devices. Specifically, the advantages of the differential architecture are that it allows quantisation of negative inputs, as the input is encoded as the difference between two optical powers. The input dynamic range is doubled due to the differential encoding and the addition of an extra parameter controlling the subtractor operation[60] eases the constraints upon simultaneous operation of the subtractor and comparator. These additions promise to make the photonic sigma-delta more attractive for real world application. Likewise, higher order sigma-delta architectures[8], [10] need to be investigated to improve the SQNR for a given oversampling ratio and demonstrate a performance advantage over electronic A/Ds. For higher order architectures the unipolar constraints and the comparison between error diffusion and sigma-delta designs would need to be revisited. With the performance improvements expected from a higher order differential implementation, photonics may provide a real alternative to the evolutionary progress of electronics in the development of A/Ds.

In summary, the **operation of a SEED based comparator and subtractor** have been **demonstrated experimentally**, and the technique to idealise the subtractor has been determined. The conditions required to operate photonic sigma-delta and error diffusion quantiser architectures were developed, and **the sigma-delta was found to have important advantages for an optical implementation**. Two alternative integrated implementations were proposed and the performances were simulated. A peak SQNR of 54.2dB was calculated for 100 times oversampling. Finally, an argument for scaling of the conversion frequency to 1.6 GHz

was given, and plans for improved architectures were presented.

Chapter 7

Summary and Conclusions

High-speed, high resolution analog-to-digital conversion is important to many applications. One specific defence application is the direct digitisation of the RF carrier, but this has yet to be achieved. This thesis examines optical A/D conversion techniques, to demonstrate their feasibility and determine expected performance. However, the work was somewhat constrained by available technology and resources.

After reviewing various optical A/D techniques, the oversampled A/D employing SEEDs was selected as the most appropriate architecture for an optical implementation, since it allows speed to be traded for resolution, is simple in design and only requires a single bit comparator. The analysis of the optical A/Ds proceeded with the development of a numerical model in Chapter 3, based upon the equivalent circuit of a SEED. To make the model as accurate as possible, experimentally derived data for responsivity, measured as a function of wavelength and voltage, capacitance and dark current were used as input into the simulation. The accuracy was verified by the agreement between simulation and experiment for a clocked switching experiment. To demonstrate the utility of our approach, the simulation was used to find the SEED parameters of input power, wavelength and voltage where critical slowing down and tri-stability would occur. These phenomena were observed experimentally and agreement between experimental and simulated results was shown.

In Chapter 4 the simplest oversampling technique, pulse code modulation (PCM), was studied. The parameters necessary to maintain unipolar operation were derived and the architecture was simulated by two different methods. In the first method,

the numerical model developed in Chapter 3 was used to directly solve the differential equation governing the S-SEED switching. This was compared to an ideal static comparator with the same SEED transfer function, to determine an upper limit of the PCM performance. A peak signal-to-quantisation-noise ratio of 44dB was achieved for the PCM quantiser, with agreement demonstrated between the two simulations. However, hysteresis in the comparator incurred a large performance penalty, of up to 22dB. The PCM technique was demonstrated experimentally, with agreement between simulation and experiment shown for the dynamic behaviour of the comparator. However, excess noise induced by the experimental apparatus restricted the experiment from achieving the predicted SQNR performance. The PCM architecture was subsequently extended by adding negative feedback to create first-order sigma-delta and error diffusion architectures, as originally proposed by Shoop[4], [5], [6], but assuming an ideal subtractor. Unipolar constraints for both architectures were derived that included the effect of hysteresis, and did not require the addition of optical bias signals as used by Shoop[4], [5], [6]. The sigma-delta architecture was shown to have the least restrictive unipolar constraints. Performance simulations of the sigma-delta were performed, again for the ideal static and experimental data based numerical model. For both cases an ideal subtractor was assumed. A peak SQNR of 50dB was obtained, and significantly, hysteresis caused a far smaller performance penalty than the PCM case.

Chapter 5 detailed the development of a Fabry-Perot microcavity multiple quantum well (MQW) device. This was required in order to access an optical output, since the devices used in the previous chapters did not have an inbuilt mirror to provide such an output. The development proceeded with analysis of a Bragg mirror and construction of a device model using experimental absorption data. The model enabled accurate positioning of the Fabry-Perot resonance, which creates a dip in reflectivity in the output spectrum. The results of the device model were compared to a numerical simulation package and agreement was observed. Using the model, the design was optimised to enable the device to perform subtraction and comparison functions at the same wavelength. The optimum design was achieved with the Fabry-Perot resonance positioned at a wavelength 8 nm longer than the heavy-hole

exciton peak. After three MOCVD growth iterations, the design goal was achieved.

In Chapter 6 the results of the proceeding chapters culminated in the demonstration of the sigma-delta performance simulation. The simulation of Chapter 4 was extended by the inclusion of a realistic subtractor. The optical subtraction function was demonstrated using the devices designed in Chapter 5. However, to achieve optical subtraction with the degree of accuracy demanded by the sigma-delta, it was established that gain on the input photodiode and output of the MQW device was required. Electrical gain on the photodiode was demonstrated experimentally. Clocked switching was also demonstrated experimentally and the gain, delay and clock components were shown to be compatible with integration. The required subtraction ratios and subtractor dynamic range for the sigma-delta and error diffusion architectures were derived. In comparison to the first order error diffusion architecture, the first order sigma-delta design was shown to have the advantages that it requires less subtractor dynamic range and also has one less subtractor node. Therefore, based on the analysis performed, the sigma-delta is more suitable for an optical implementation than the error diffusion. However, it is possible that other factors that have not been considered in this thesis, such as component non-idealities[93], may alter this conclusion. An optical layout of the sigma-delta was proposed and its performance simulated, achieving a peak SQNR of 49dB for an oversampling ratio of 100. However, the input range was limited by low contrast ratio, caused by the requirement of using the same device design for the comparator and subtractor. If a hybrid fabrication process were considered, different devices could be used for each function. Different device designs were simulated by temperature tuning the MQW devices, allowing separate optimisation of subtractor dynamic range and comparator contrast ratio. The sigma-delta simulation using an increased contrast ratio achieved a peak SQNR of 54dB at an oversampling ratio of 100 times.

This work has demonstrated the feasibility of an all optical first-order sigma-delta quantiser. The upper limit on the performance was found to be 8.71 bits at 1.6 GHz for 100 times oversampling. However, to take full advantage of optical sampling, and achieve quantiser resolutions significantly better than electronics, more complex architectures are required. One possibility is a higher order sigma-delta[10].

As a result of our work, we have demonstrated all the components necessary to build such a design in the optical domain. However, while significant improvements in A/D performance using this technology are possible, their realisation would require considerable research effort in developing the necessary photonic integration technology.

7.1 Contributions

As a result of this work, the following contributions have been made to the field:

- A dynamic simulation of S-SEED switching based upon experimental data was developed that included the effect of critical slowing down. The simulation was shown to have a higher degree of accuracy than had previously been demonstrated. Further, critical slowing down was demonstrated for the first time in the switching of an S-SEED.

  -B. A. Clare, K. A. Corbett, K. J. Grant, P. Atanackovic, W Marwood, J. Munch, "Investigation of Critical Slowing Down in a Bistable S-SEED", *IEEE Journal of Lightwave Technology*, vol. 21, pp. 2883-2890, 2003.

- A photonic oversampled PCM quantiser was demonstrated experimentally and via simulation. Unipolar constraints, including hysteresis, for PCM, first-order error diffusion and sigma-delta architectures were derived. The first-order architectures were far more tolerant of comparator hysteresis than PCM.

  -B. A. Clare, K. A. Corbett, K. J. Grant, A. Massie, J. Munch, W Marwood, "Photonic A/Ds Employing S-SEED Comparators", *Proceedings of SPIE Conference on Photonics: Design, Technology and Packaging,* vol. 5277, pp. 42-53, 2004.

  -B.A. Clare, K.A. Corbett, K.J. Grant, A. Massie, J. Munch, W. Marwood, "Oversampled photonic A/D converters using self-electro-optic effect devices", *Conference on Lasers and Electro-Optics, 2004. (CLEO).* Volume 1, 16-21 May 2004 Page(s):2 pp. vol.1

- A microcavity MQW device to optimise subtractor and comparator operation at the same operational wavelength was designed.

- A method to achieve accurate optical subtraction using a SEED and photodiode was developed. The subtraction requirements for the error diffusion and sigma-delta architectures were derived, and the sigma-delta was shown have important advantages for a first order optical implementation. The sigma-delta was simulated using the experimental data based model, achieving a peak SQNR of 49dB for a system using a single device design for subtraction and comparison functions, and 54dB for a system using separately optimised components. The results demonstrated the feasibility of an optical implementation of a first-order sigma-delta quantiser.

  -B. A. Clare, K. A. Corbett, and K. J. Grant, "Performance of a photonic oversampled sigma-delta quantiser", *Proc. SPIE Int. Soc. Opt. Eng.* 5814, 248 (2005).

Appendix A

Proofs of Subtractor Constraints

In this appendix we seek to formally prove that the subtractor's dynamic range requirement in the sigma-delta quantiser is less than that for the error diffusion. However, it must first be shown that the chosen extrema for the subtractor, labelled S2, in the error diffusion and the subtractor sigma-delta are the correct choices.

Due to our use of optical signals and the requirement for unipolarity, we have the following constraints:

$$\begin{aligned} Q_H &> 0,\ Q_L > 0,\ P_{\theta H} > 0,\ P_{\theta L} > 0 \\ Q_H &> Q_L && \text{(A.1)} \\ P_{\theta H} &\geq P_{\theta L} && \text{(A.2)} \\ Q_L &\geq P_{\theta H}\ (only\ for\ the\ error\ diffusion) && \text{(A.3)} \\ P_{\theta L} &\geq Q_H - Q_L. && \text{(A.4)} \end{aligned}$$

Note that we require all the parameters in (A.1) to be strictly positive to ensure switching of the comparator. That is, if $P_{\theta L} = 0$ then there will be no unipolar input less than $P_{\theta L}$ to switch the comparator into the low state Q_L.

We first seek to prove that

$$\frac{Q_H - Q_L + P_{\theta H}}{Q_H} \geq \frac{P_{\theta H}}{Q_L}, \qquad \text{(A.5)}$$

as was asserted in Chapter 6, Section 6.2 for the upper bound of the subtractor labelled S2 in the error diffusion architecture. Consider

$$\frac{Q_H - Q_L + P_{\theta H}}{Q_H} - \frac{P_{\theta H}}{Q_L}. \tag{A.6}$$

This simplifies to

$$\frac{(P_{\theta H} - Q_L)(Q_L - Q_H)}{Q_H Q_L} \geq 0 \tag{A.7}$$

since both terms in the numerator of (A.7) are negative, via constraints (A.3) and (A.1) and the denominator is positive via (A.1). Proving (A.5).

The next problem seeks identifies the lower bound of the subtraction ratio, and prove that

$$\frac{Q_L - Q_H + P_{\theta L}}{Q_L} < \frac{P_{\theta L}}{Q_H}. \tag{A.8}$$

Consider

$$\frac{Q_L - Q_H + P_{\theta L}}{Q_L} - \frac{P_{\theta L}}{Q_H}, \tag{A.9}$$

which simplifies to

$$\frac{(P_{\theta L} - Q_H)(Q_H - Q_L)}{Q_H Q_L} < 0,$$

since the numerator is negative as $P_{\theta L} \leq P_{\theta H} \leq Q_L < Q_H$ and $Q_H > Q_L$, while the denominator is positive from (A.1). Thus proving (A.8).

We now consider the bounds of the subtractor dynamic range of the sigma-delta architecture and are required to first prove, from Chapter 6, Section 6.2:

$$\frac{Q_H}{Q_L + P_{\theta L}} > \frac{Q_L}{Q_L + Q_L - Q_H + P_{\theta L}}. \tag{A.10}$$

Consider

$$\frac{Q_H}{Q_L + P_{\theta L}} - \frac{Q_L}{2Q_L - Q_H + P_{\theta L}}, \tag{A.11}$$

which simplifies to

$$\frac{(Q_H - Q_L)(P_{\theta L} + Q_L - Q_H)}{(P_{\theta L} + Q_L)(P_{\theta L} + 2Q_L - Q_H)}. \tag{A.12}$$

Since the terms $(Q_H - Q_L)$ and $(P_{\theta L} + Q_L)$ are positive, via (A.1) and (A.1), respectively, we are left to consider

$$\begin{aligned} & \frac{(P_{\theta L} + Q_L - Q_H)}{(P_{\theta L} + 2Q_L - Q_H)} \\ \geq \; & \frac{2P_{\theta L}}{(P_{\theta L} + 2Q_L - Q_H)} \end{aligned} \tag{A.13}$$

using (A.4)

$$> \frac{2P_{\theta L}}{(P_{\theta L} + 2Q_L - Q_L)} \tag{A.14}$$

using $-1/Q_H > -1/Q_L$, from (A.1). Therefore

$$\frac{2P_{\theta L}}{(P_{\theta L} + Q_L)} > 0$$

from (A.1), thus proving (A.10).

The final bound to prove is

$$\frac{Q_L}{Q_H + P_{\theta H}} < \frac{Q_H}{Q_H + Q_H - Q_L + P_{\theta H}}. \tag{A.15}$$

Consider

$$\frac{Q_L}{Q_H + P_{\theta H}} - \frac{Q_H}{2Q_H - Q_L + P_{\theta H}}, \tag{A.16}$$

which simplifies to

$$-\frac{(Q_H - Q_L)(P_{\theta H} + Q_H - Q_L)}{(P_{\theta H} + Q_H)(P_{\theta H} + 2Q_H - Q_L)} < 0,$$

since all the bracketed terms are positive, via (A.1) and (A.1). Thus proving (A.15).

Having verified the subtractor extrema, it is left to prove that the dynamic range of the sigma-delta subtractor is less than the dynamic range required from a subtractor in the error diffusion. That is,

$$\frac{Q_H^2 - Q_L^2 + Q_H P_{\theta H} - Q_L P_{\theta L}}{(Q_H + P_{\theta H})(Q_L + P_{\theta L})} < \frac{Q_H(Q_H - P_{\theta L}) + Q_L(P_{\theta H} - Q_L)}{Q_H\ Q_L}. \tag{A.17}$$

Start by considering

$$\frac{Q_H^2 - Q_L^2 + Q_H P_{\theta H} - Q_L P_{\theta L}}{(Q_H + P_{\theta H})(Q_L + P_{\theta L})} - \frac{Q_H(Q_H - P_{\theta L}) + Q_L(P_{\theta H} - Q_L)}{Q_H\ Q_L}, \tag{A.18}$$

which simplifies to

$$\frac{Q_H P_{\theta L}(P_{\theta L} - Q_H)(Q_H + P_{\theta H}) + Q_L P_{\theta L}(Q_H^2 - P_{\theta H}^2)}{Q_H\ Q_L(Q_H + P_{\theta H})(Q_L + P_{\theta L})}$$
$$\frac{-Q_L^2 P_{\theta H}(Q_H + P_{\theta H} - P_{\theta L}) + Q_L^3 P_{\theta H}}{Q_H\ Q_L(Q_H + P_{\theta H})(Q_L + P_{\theta L})}.$$

Since the denominator of (A.19) is positive, via (A.1), we only need to consider the numerator. Consider the first two terms in the numerator of (A.19). That is,

$$Q_H P_{\theta L}(P_{\theta L} - Q_H)(Q_H + P_{\theta H}) + Q_L P_{\theta L}(Q_H^2 - P_{\theta H}^2) \tag{A.19}$$
$$< \quad Q_H P_{\theta L}(P_{\theta L} - Q_H)(Q_H + P_{\theta H}) + Q_H P_{\theta L}(Q_H^2 - P_{\theta H}^2) \tag{A.20}$$

using (A.1)

$$= \quad (P_{\theta L} - Q_H)(Q_H + P_{\theta H}) + Q_H^2 - P_{\theta H}^2 \tag{A.21}$$
$$= \quad P_{\theta L} P_{\theta H} + P_{\theta L} Q_H - Q_H P_{\theta H} - P_{\theta H}^2 \tag{A.22}$$
$$= \quad (P_{\theta L} - P_{\theta H})(P_{\theta H} + Q_H) \leq 0 \tag{A.23}$$

as $P_{\theta L} - P_{\theta H} \leq 0$ and $P_{\theta H} + Q_H > 0$. Therefore (A.19)< 0. Now consider the second pair of terms in (A.19). That is,

$$
\begin{aligned}
& -Q_L^2 P_{\theta H}(Q_H + P_{\theta H} - P_{\theta L}) + Q_L^3 P_{\theta H} && \text{(A.24)} \\
= \; & -Q_H Q_L^2 P_{\theta H} - Q_L^2 P_{\theta H}^2 + Q_L^2 P_{\theta H} P_{\theta L} + Q_L^3 P_{\theta H} && \text{(A.25)} \\
< \; & -Q_L^3 P_{\theta H} - Q_L^2 P_{\theta H}^2 + Q_L^2 P_{\theta H} P_{\theta L} + Q_L^3 P_{\theta H} && \text{(A.26)}
\end{aligned}
$$

using $-Q_H < -Q_L$,

$$\leq Q_L^2 P_{\theta H}^2 - Q_L^2 P_{\theta H}^2 = 0,$$

using (A.2). Therefore (A.24)< 0, and combined with (A.19)< 0 proves that

$$
\begin{aligned}
& \frac{Q_H P_{\theta L}(P_{\theta L} - Q_H)(Q_H + P_{\theta H}) + Q_L P_{\theta L}(Q_H^2 - P_{\theta H}^2)}{Q_H \; Q_L(Q_H + P_{\theta H})(Q_L + P_{\theta L})} \\
& \frac{-Q_L^2 P_{\theta H}(Q_H + P_{\theta H} - P_{\theta L}) + Q_L^3 P_{\theta H}}{Q_H \; Q_L(Q_H + P_{\theta H})(Q_L + P_{\theta L})} < 0.
\end{aligned}
\qquad \text{(A.27)}
$$

Thus the dynamic range of the sigma-delta subtractor is less than the dynamic range required from a subtractor in the error diffusion architecture.

The proof of convergence of the two level output to the analogue input for an error diffusion quantiser is reproduced from [23] below.

Let

$$\overline{q}_i = \frac{1}{i+1} \sum_{j=0}^{i} q_j. \qquad \text{(A.28)}$$

The value for $q(i)$ for the error diffusion architecture is given by

$$q_i = x_i + [e_i - e_{i-1}]. \qquad \text{(A.29)}$$

Therefore,

$$\overline{q}_i - x = \frac{1}{i+1}[e_i - x + q_0 - e_0], \qquad \text{(A.30)}$$

which approaches zero as i approaches infinity since e_i is bounded. So, for slowly varying x, a number of q_i values can be averaged to approximate x.

Appendix B

Publications

B.1 Publications

Attached are the following journal and conference publications (in chronological order) that resulted from work presented in this thesis:

- B. A. Clare, J. Munch, K. A. Corbett, K. J. Grant, P. Atanackovic, W. Marwood, "FEASIBILITY OF PHOTONIC SIGMA-DELTA ANALOG-TO-DIGITAL CONVERSION", *Proc. Aust. Inst. Phys. Conf.,* 2002.

- B.A. Clare, K.A. Corbett, K.J. Grant, P.B. Atanackovic, W. Marwood, J. Munch, "Investigation of critical slowing down in a bistable S-SEED", *Journal of Lightwave Technology*, Volume 21, Issue 11, Nov. 2003 Page(s):2883 - 2890

- B. A. Clare, K. A. Corbett, K. J. Grant, A. Massie, J. Munch and W. Marwood, "Photonic A/Ds employing S-SEED comparators", *Proc. SPIE Int. Soc. Opt. Eng.* 5277, 42 (2004)

- B.A. Clare, K.A. Corbett, K.J. Grant, A. Massle, J. Munch, W. Marwood, "Oversampled photonic A/D converters using self-electro-optic effect devices", *Conference on Lasers and Electro-Optics, 2004. (CLEO).* Volume 1, 16-21 May 2004 Page(s):2 pp. vol.1

- B. A. Clare, K. A. Corbett, and K. J. Grant, "Performance of a photonic oversampled sigma-delta quantiser", *Proc. SPIE Int. Soc. Opt. Eng.* 5814,

248 (2005).

B. A. Clare, J. Munch, K. A. Corbett, K. J. Grant, P. Atanackovic, W. Marwood, ”Feasibility of photonic sigma-delta analog-todigital conversion”, Proc. Aust. Inst. Phys. Conf., 2002.

B.A. Clare, K.A. Corbett, K.J. Grant, P.B. Atanackovic, W. Marwood, J. Munch,"Investigation of critical slowing down in a bistable S-SEED", Journal of Lightwave Technology, Volume 21, Issue 11, Nov. 2003 Page(s):2883 - 2890

B. A. Clare, K. A. Corbett, K. J. Grant, A. Massie, J. Munch and W. Marwood, ”Photonic A/Ds employing S-SEED comparators”, Proc. SPIE Int. Soc. Opt. Eng. 5277, 42 (2004)

B.A. Clare, K.A. Corbett, K.J. Grant, A. Massle, J. Munch, W. Marwood, ”Oversampled photonic A/D converters using self-electro-optic effect devices”, Conference on Lasers and Electro-Optics, 2004. (CLEO). Volume 1, 16-21 May 2004 Page(s):2 pp. vol.1

Appendix C

Table of Wafers Used

Wafer Label	Supplier	MBE or MOCVD	Heavy-Hole Peak (nm)	Fabry-Perot Peak (nm)	Used in Chapter	Comment
436	Stanford	MBE	843	NA	3,4,5	No optical out
239	ANU	MOCVD	845	835	5	first design
272	ANU	MOCVD	848	<830	5	calibration
278	ANU	MOCVD	847	857	5,6	successful

The first devices used in this thesis (436) were supplied from Stanford University by Petar Atanackovic, working at the time for DSTO. This wafer was grown by MBE, with the structure shown in C.1. As the GaAs substrate absorbs light at the operating wavelength of the devices ($\sim 850\,\mathrm{nm}$), wafer 436 did not provide an optical output. Nevertheless, these devices enabled us to demonstrate S-SEED switching, develop the numerical simulation and they served as the basis for the modelling of devices with an optical output.

By the time the structure for devices with an optical output was designed, we no longer had access to the Stanford facility. However, we did have access to Australia's leading III-V facility, namely the EME group at ANU. Wafers 239, 272 and 278 were grown by MOCVD at ANU with a microcavity design to provide an optical output. The wafer structure is given in Fig. C.2. To fabricate devices, the mask shown in Fig. C.3 was used. The top half of the mask was used for metalisation of the top p-doped contact, and the bottom half of the mask was used for the mesa etch to the n-doped layer. Using an n-doped substrate, electrical contact to the n-doped region

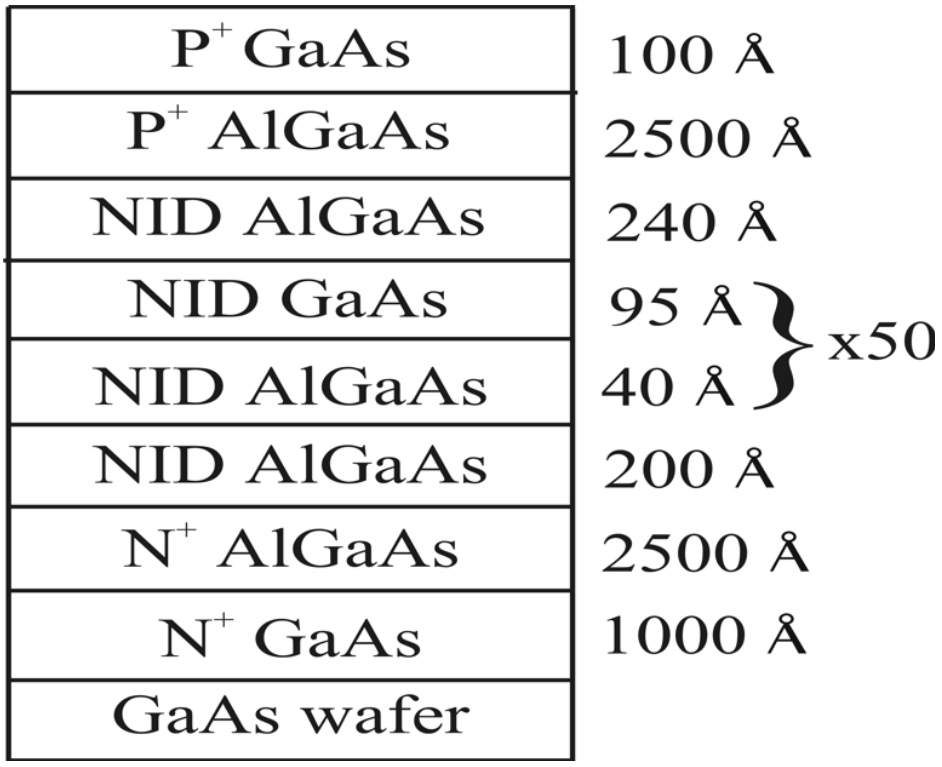

Figure C.1: Growth structure of wafer 436.

was made on the underside of the substrate. The device was constructed in this fashion to simplify fabrication, but it made it difficult to obtain accurate contact resistance measurements for the whole device.

A photograph of fabricated devices from wafer 278 is given in Fig. C.4.

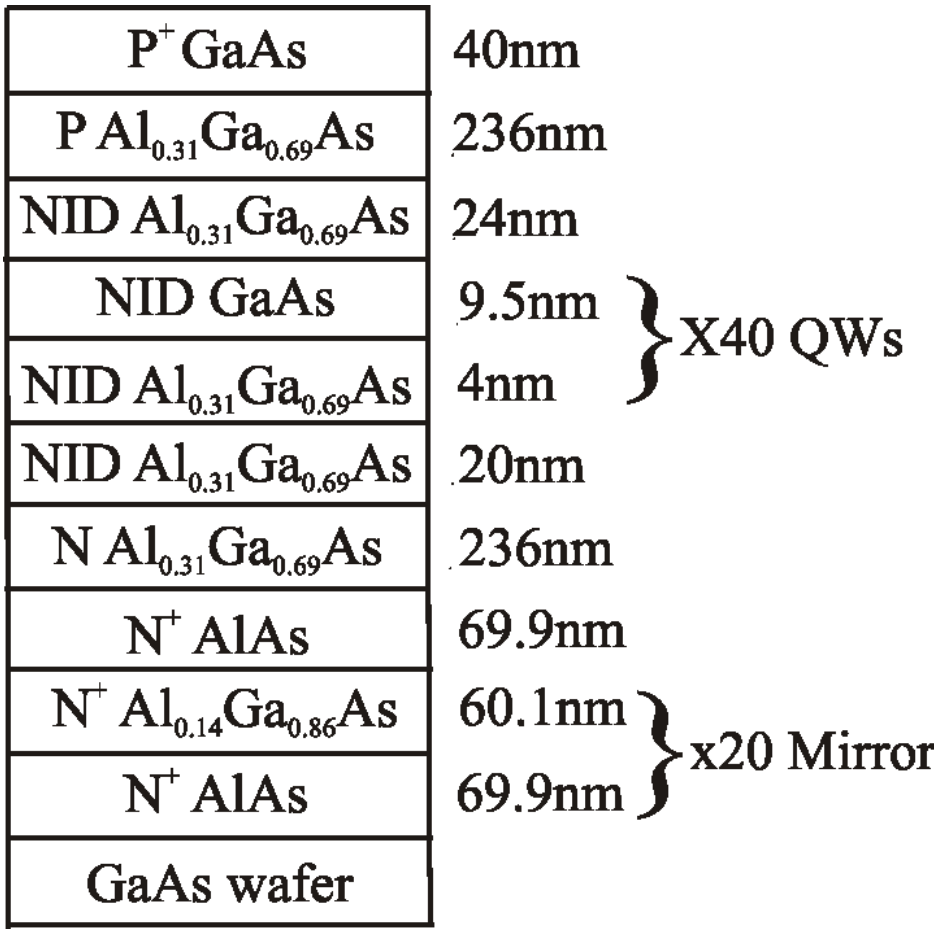

Figure C.2: General structure of the MOCVD grown wafers 239, 272 and 278. Only the doped *AlGaAs* layers changed between the three different growths to adjust the Fabry-Perot resonance position.

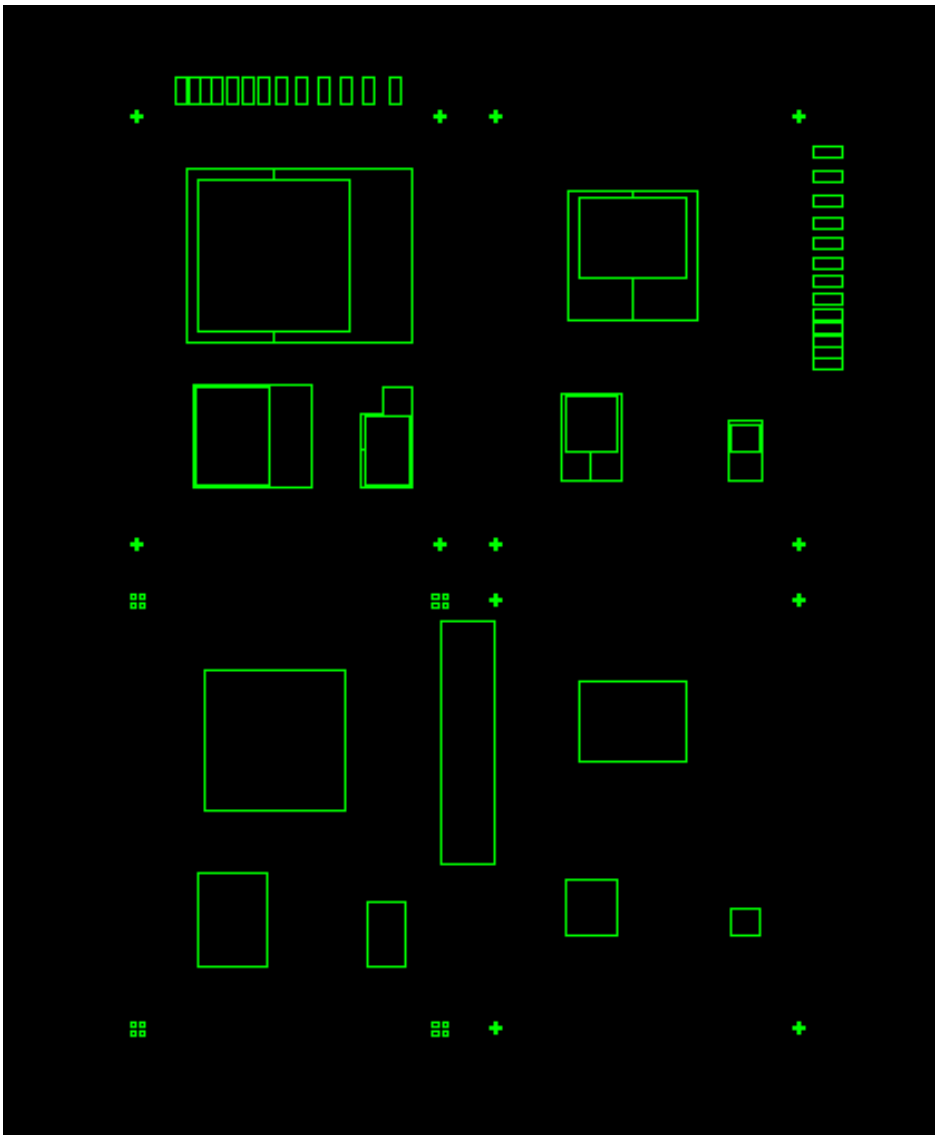

Figure C.3: Mask design for fabrication of devices at ANU. The top half of the mask is for metalisation of the top p-doped contact. The bottom half of the mask is for the mesa etch to the n-doped layer.

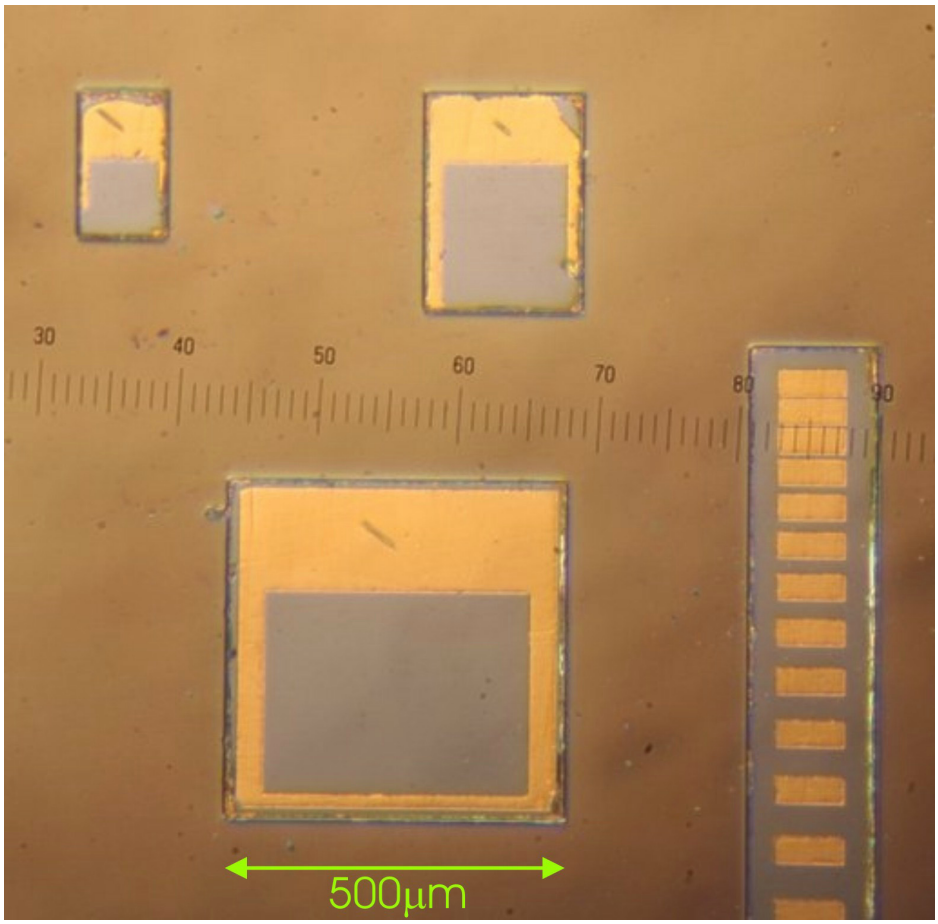

Figure C.4: Photograph of fabricated devices from wafer 278.

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