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# Software-Centric and Interaction-Oriented System-on-Chip Verification

by

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A thesis submitted for the
degree of Doctor of Philosophy

in

School of Electrical and Electronic Engineering

Faculty of Engineering, Computer and Mathematical Sciences

March 2009

# Declaration of Authorship

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# *Abstract*

As the complexity of very-large-scale-integrated-circuits (VLSI) soars, the complexity of verifying them increases even faster. *Design verification* becomes the biggest bottleneck in VLSI design, consuming around 70% of the effort and time in a typical design cycle. The problem is even more severe as the system-on-chip (SoC) design paradigm is gaining popularity.

Unfortunately, the development in verification techniques has not kept up with the growth of the design capability, and is being left further behind in the SoC era. In recent years, a new generation of hardware-modelling-languages alongside the best practices to use them have emerged and evolved in an attempt to productively build an intelligent stimulation-observation environment referred to as the *test-bench*. Ironically, as test-benches are becoming more powerful and sophisticated under these best practices known as *verification methodologies*, the overall verification approaches today are still officially described as *ad hoc and experimental* and are in great need of a methodological breakthrough.

Our research was carried out to seek the desirable methodological breakthrough, and this thesis presents the research outcome: a novel and holistic methodology that brings an opportunity to address the SoC verification problems. Furthermore, our methodology is a solution completely independent of the underlying simulation technologies; therefore, it could extend its applicability into future VLSI designs.

Our methodology presents two ideas. (a) We propose that system-level verification should resort to the *SoC-native languages* rather than the test-bench construction languages; the software native to the SoC should take more critical responsibilities than the test-benches. (b) We challenge the fundamental assumption that "objects-under-test" and "tests" are distinct entities; instead, they should be understood as *one* type of entities – the *interactions*; interactions, together with the *interference between interactions*, i.e., the parallelism and resource-competitions, should be treated as the focus in system-level verification.

The above two ideas, namely, *software-centric* verification and *interaction-oriented* verification have yielded practical techniques. This thesis elaborates on these techniques, including the *transfer-resource-graph* based test-generation method targeting the parallelism, the coverage measures of the concurrency completeness using Petri-nets, the automation of the test-programs which can execute smartly in an *event-driven* manner, and a software observation mechanism that gives insights into the system-level behaviours.

# *Acknowledgements*

I thank my supervisors Prof. Cheng-Chew Lim and Prof. Michael Liebelt. They provided me with this research position, and they are the co-authors of my research publications. I am grateful to their advice and feedback during the development of this thesis. Cheng-Chew's help comes in all forms, including the resources he guarantees, the meetings he organises, the peer review he performs and the presentations he rehearses.

I would like to extend special thanks to Mr. Adriel Cheng, who has kindly opened his source codes in the SALVEM (Software Application Level Verification Methodology) approach to me. These codes have guided me to learn new programming languages, new tools and new technologies, and more importantly, I was able to understand the nature of software-based verification from them. It is these codes that have invited me to form my own idea. In addition, the Nios SoC used in my research was generated for the SALVEM project. I appreciate many scintillating talks with Adriel about SoC verification.

I would also like to thank Mr. Kiet To for interesting conversations on more general topics about typical computer structures.

This research work is supported by Australian Research Council Linkage Project (LP0454838). And the Australian Postgraduate Award (Industry) allows me to concentrate on the research.

Finally, I must thank my wife Hongqi Wu, who has given me energy and support throughout the research.

# Contents

# List of Figures

# List of Tables

# Abbreviations

| | |
|---|---|
| **ALU** | **A**rithmatic **L**ogic **U**nit |
| **BDD** | **B**inary **D**ecision **D**iagram |
| **BFM** | **B**us **F**uctional **M**odel |
| **CTL** | **C**omputation **T**ree **L**ogic |
| **DMA** | **D**irect **M**emory **A**ccess |
| **DUT** | **D**esign **U**nder **T**est |
| **EDA** | **E**lectronics **D**esign **A**utomation |
| **FPGA** | **F**ield **P**rogrammable **G**ate **A**rray |
| **FSM** | **F**inite **S**tate **M**achine |
| **HDL** | **H**ardware **D**escription **L**anguage |
| **HVL** | **H**ardware **V**erification **L**anguage |
| **HW** | **H**ard**w**are |
| **IC** | **I**ntegrated **C**ircuit |
| **ISR** | **I**nterrupt **S**ervice **R**outine |
| **OOP** | **O**bject **O**riented **P**rogramming |
| **OS** | **O**perating **S**ystem |
| **RISC** | **R**educed **I**nstruction **S**et **C**omputer |
| **RTL, RT-Level** | **R**egister **T**ransfer **L**evel |
| **SoC** | **S**ystem **o**n **C**hip |
| **SW** | **S**oft**w**are |
| **TB** | **T**est-**B**ench |
| **TLM** | **T**ransaction **L**evel **M**odel(ling) |

| | |
|---|---|
| **TP** | **T**est-**P**rogram |
| **UART** | **U**niversal **A**synchronous **R**eceiver and Transmitter |
| **VLSI** | **V**ery **L**arge **S**cale **I**ntegration |

*Dedicated to my girls: Hongqi, Jingyi and Grace.*