High-Performance RFID Systems

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BY

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Declaration of Originality

I declare that this thesis does not incorporate without acknowledgment any material previously submitted for a degree or diploma in any university; and that to the best of my knowledge it does not contain any material previously published or written by any other person except where due reference is made in the text.

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10 January 2006

I give consent to this copy of my thesis, when deposited in the University Libraries, being available for photocopying and loan.

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Abstract

In this thesis, I present and analyze two of the most fundamental constraints of Radio Frequency Identification Systems (RFID), power rectification and signaling. These two issues play an important role in the continuing development of RFID systems.

A passive RFID tag draws power from the RF field created by an RFID reader and uses it to energize its circuitry. It does this by rectification of the reader's radiated RF field using rectifying circuitry. The power then available to the tag is dependent upon both the available field strength and the efficiency of the rectification process. One option for increasing the operating range of an RFID system without increasing the reader's field strength is to increase the efficiency of the tag's rectification structure. A major component of any rectification circuit is a diode type device and so, the first part of the thesis focuses on the design and implementation of a novel high efficiency Schottky Barrier Diode (SBD) on a standard CMOS process. The forward voltage drop of the SBD diode was investigated and analytic equations formulated considering the Schottky barrier drift region resistance and the contributions from the p^+ guard-grid. A design procedure to minimize the drift region resistance for any blocking voltage was derived. The fundamental trade-off between the forward voltage and leakage current in the novel SBD concept was determined.

Based on the critical review of the Schottky diodes fabricated in the first part, new structures of novel SBD were designed to address most of the open issues related to its reverse break-down voltage and series resistance. Detailed analysis of the important design parameters of the novel Schottky barrier diode were performed using HSPICE with the parameter set used in the calibration process. The novel structure was also compared to an alternative fabrication approach, specifically, a NMOS and PMOS gate-cross-connected bridge. The comparison shows that the novel structure provides a 10% higher

figure of merit for power rectification.

In the later part of the thesis, an analysis of circuit advantages enabled by the novel SBD is given. The circuit simulation showed that by utilizing the novel SBD the operating frequency of the circuit can be increased to the UHF region while maintaining approximately the same power efficiency as that achievable when using a discrete Schottky diode. This leads to the possibility of dramatic improvements in size, weight and cost of the RFID transponder circuits.

Signaling also plays an important role in the development of RFID systems. The choice of signaling methods and protocols determines not only the spectrum bandwidth usage, but also the data throughput. Also with constantly changing standards and regulations, it is important to be able to characterize and optimize these issues.

Therefore the second part of this dissertation presents the design, implementation and evaluation of a novel RFID data logging reader architecture based on software radio concepts. The system is designed to overcome the many challenges and exploit the advantages of performing real-time signal processing and data logging in an RFID environment. The proposed concept has a unique multi-band RFID tag reader platform and has been designed to read tags conforming to the Electronic Product Code (EPC) specifications in both the HF and UHF frequency bands. The hardware architecture consists of a general purpose analogue front end up/down-converter for each band, followed by a software radio based architecture allowing easy adaptation to new frequencies and protocols if required.

The last chapter presents the results of investigations conducted to determine the ability of the proposed reader architecture to communicate with tags in typical channel noise and environmental conditions present in an

RFID operational environment. Studies of the effects of reader interference in multi-reader environments and the development of an anti-collision protocol signaling to address and mitigate those effects are also presented.

Publications

1. Behnam Jamali, Peter H. Cole "Design and Optimization of Schottky Diodes on Standard CMOS process", Proceedings of SPIE International Symposium in Smart Structures, Devices, and Systems II, Sydney, Dec 2004.

2. Behnam Jamali "Brief comparison of different rfid rectifier structure", Auto-ID Lab, Zurich, Sept 2004, http://autoidlab.eleceng.adelaide.edu.au/

3. Behnam Jamali "Software Based Data Logging Reader", Frontline Conference & Expo, Chicago, Sept 2004, http://www.frontlineexpo.com/

4. Peter Cole, Behnam Jamali, Damith Ranasinghe "Coupling Relations in RFID Systems", Auto-ID Lab, Adelaide, Jun 2002, http://autoidlab.eleceng.adelaide.edu.au/Tutorial/

5. Peter Cole, Damith Ranasinghe, Behnam Jamali "Coupling Relations in RFID Systems II: Practical Performance Measurements", Auto-ID Lab, Adelaide, Jun 2003.

6. B. Jamali, D. C. Ranasinghe, P. H. Cole , "Analysis of UHF RFID CMOS rectifier structures and input impedance characteristics", SPIE International, Microelectronics: Design, Technology, and Packaging II, In proceeding

7. B. Jamali, D. C. Ranasinghe, P. H. Cole , "Design and optimisation of power rectifiers for passive RFID systems in monolithic CMOS", SPIE International, Microelectronics: Design, Technology, and Packaging II, In proceeding

8. Ranasinghe D., Jamali B., Lim D., Devadas S., Zhu Z. and Cole P.H. "Low-cost and efficient physical random number generator based on race conditions", in Smart Structures, Devices, and Systems II, S. F. Al-Sarawi, Editor, Proceedings of SPIE International Symposium MSN, & MSS, Vol. 5649, Sydney, Australia, 1215 December 2004.

9. Daihyun Lim, Damith C. Ranasingheb, Srinivas Devadas, Behnam Jamali, Derek Abbott, Peter H. Cole "Exploiting metastability and thermal noise to build a re-configurable hardware random number generator" Proc. of SPIE Vol. 5844 (SPIE, Bellingham, WA, 2005)

10. D. Hall, D. Ranasinghe, Behnam Jamali, P. H. Cole "Turn-on circuits based on standard CMOS technology for active RFID labels" Proceedings of SPIE International Symposium, Proc. SPIE Vol. 5837, p. 310-320, VLSI Circuits and Systems II.

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Chapter 1

Introduction

This dissertation is about improving the performance of RFID systems. The work done has been partitioned into two main parts. The first part identifies the critical issues in developing high performance RFID systems and goes on to describe those aspects that become the focus of this work. It then proceeds to describe the design, fabrication and usage of a power efficient Schottky Barrier Diode (SBD) on a standard CMOS process. The second part describes design and construction of a software based data logging reader and its use in implementing, monitoring and evaluating recent RFID communication protocols.

The purpose of this first chapter is to present an introduction to Radio Frequency Identification Systems (RFID), the motivation and the outline of the work done in this dissertation.

1.1 Introduction to RFID

RFID is a relatively new technology, first appearing in tracking and access applications during the 1980s [1] or even 1940s[1]. These wireless systems allow for non-contact reading of data from electronic labels by electromagnetic signals, and consequently are effective in manufacturing and other hostile environments where bar code labels could not survive. RFID tags can be read in challenging circumstances when there is no physical contact or direct line of sight [2] [3]. RFID has established itself in a wide range of markets including livestock identification and automated vehicle identification systems because of its ability to track moving objects. RFID technology is becoming a primary player in automated data collection, identification and analysis systems worldwide [4].

RFID, its application, standardization and innovation are constantly changing. It is a new and complex technology, and there are many features of this technology that are not well known and understood by the general public, or by many practitioners.

Wider reading range, larger memory capacity and faster signal processing and data communications are a few of the areas which need development.

It is very unlikely that RFID will replace traditional bar code systems [5, 6], because even with the cost reduction in fabricating CMOS chips, RF tags will never be as cost effective as bar code labels. However, RFID will continue to grow in areas where bar code or other optical technologies are not effective. This will be especially true when improved solutions to RFID problems can be devised.

[1]Many authors date RFID to 1940's when World War II pilots signaled home radars by dipping their wings. These dips produced modulation on the reflected radar signals.

The standardization of tags will further add to their uptake as equipment from different manufacturers can be used interchangeably [7].

The strong revival, during the past few years, of research and applications in the RFID region is attributed to the advance of new technology, and innovations in the context within which RFID can be used. The evolution of new requirements for reading range and communication links and the superiority of RFID over optical bar code systems for penetration of dust, smoke and other adverse environments, has generated much interest in both commercial and military applications [8] [9]. The improved technology includes better read range, faster communication links, higher capacities, multiple tag reading algorithms and better sensitivities. Of particular importance is the development of the Auto-ID Center concepts discussed in Section 1.1.5.

1.1.1 Reading Range

The reading range of a tag is essentially determined by:

- The power available at the reader to communicate with the tag, which is limited by electromagnetic regulations which restrict the amount of power that a reader can transmit.
- The amount of the power available within the tag to respond.
- The environmental conditions and structures. These become more significant at higher frequency.
- The way that the power is deployed within the tag circuitry.

As the shape and orientation of the transmitter antenna determines the shape of the electromagnetic field created around it, the read range will be

influenced by the orientation of the tag antenna in relation to the interrogating electromagnetic field. The issues are different at different frequencies, as we may be operating at some frequencies in the near field and in the far field at other frequencies [10].

Another important factor is the strength of the field as the tag moves farther from the reader antenna. In free space, in the near field, the strength (power) of the field reduces in inverse proportion to the sixth power of the distance from the antenna. In free space, in the far field, the strength (power) of the field reduces in inverse proportion to the second power of the distance from the antenna.

Although it is possible to choose a high power level to achieve a long read range, it is not possible to exercise complete freedom of choice [11]. There are legislative constraints on power levels emitted from the reader antenna [12]. This makes the near field quite interesting [13], as it provides energy storage with minimum amount of electromagnetic radiation, which always occurs and needs to be minimized. There is also the issue that high transmitted power automatically generates high receiver noise into the receiver circuit of the reader, due to their homo-dyne receiver architecture [14]. Thus, techniques to deal with such noise need to be developed.

1.1.2 Data Transfer Rate

The data transfer rate depends mostly on the frequency bandwidth. Generally speaking, the higher the bandwidth the higher the transfer rate. It should also be mentioned that transferring data to and from the tag requires a finite amount of time. This can be an important consideration in applications where a tag is passing swiftly through an interrogation zone. The considerations which limit data transfer rate in the interrogator to label di-

rection are those of electromagnetic compatibility regulations [11] [12]. The principal consideration which limits data transfer rate in the label to interrogator direction is the employment of a coding methodology which is robust in the face of interfering signals which may be generated by other users of the spectrum.

1.1.3 The Reader

The readers or interrogators can differ quite considerably in complexity, depending on the type of tags being used and the functionality expected from them [15]. Their main purpose is to communicate with the tags and retrieve information contained within them. The functions performed by the interrogator may include signal conditioning, error checking and correcting, collision detection, sending commands to the tags in the field and processing the reply. In an environment where multiple tags are present, the amount of processing a reader must do is much more. Contention management is a vital issue, and a variety of techniques have been developed to improve the process of batch reading [16].

Because RFID systems generate and radiate electromagnetic waves, they are justifiably classified as radio systems. The function of other radio services must under no circumstances be disrupted or impaired by the operation of RFID systems. The need to exercise care with regard to other radio services significantly restricts the range of suitable operating frequencies available to an RFID system. For this reason, it is usually only possible to use frequency ranges that have been reserved specifically for industrial, scientific or medical applications or for short range devices. These are the frequencies classified worldwide as ISM frequency ranges (Industrial-Scientific-Medical) that can also be used for RFID applications.

Low-frequency (30 KHz to 500 KHz) RFID systems have short reading ranges and lower system costs. They are most commonly used in security access, asset tracking, and animal identification applications. High-frequency (850 MHz to 950 MHz and 2.4 GHz to 2.5 GHz) systems, offering long read ranges (greater than 90 feet) and high reading speeds, are used for such applications as railroad car tracking and automated toll collection. However, the higher performance of high-frequency RFID systems incurs higher system costs.

Many companies manufacture RFID readers among them, Alien Technology, AWID, Matrics and SAMSys are market leaders. All of these readers are designed to read tags based on the Class 1 Electronic Product Code specification [107].

Most of the readers are set up with one or more external circular polarized antenna and they differ in performance (which includes read distance, read rates and performance on a variety of products and in real-world conditions), connectivity (how easy it is to add the reader to an RFID network), control (the ability to tune antennas, sequence the antennas and control the power output) and total cost of ownership.

1.1.4 Standardization

The proliferation of incompatible RFID standards is provoking much debate among RFID developers. All major RFID vendors offer proprietary systems, which operate on different protocols. The current state of RFID standards are highly variable across the world and between competing standard making bodies. This lack of system inter-changeability has severely crippled RFID industry growth. However a number of organizations, influenced in a variety of ways [7], have been working to address, and hopefully bring about, some

commonality among competing RFID systems. One of them will be discussed further in the next section.

Just as standardization enabled the tremendous growth and widespread use of barcodes, cooperation among RFID manufacturers will be necessary for promoting the technology development and refinements that will enable the broad based application growth.

1.1.5 The Auto-ID Center Concepts

In 1999 researchers at Massachusetts Institute of Technology (MIT) established an Auto-ID Center, and developed the concepts of Electronic Product Code, the Object Naming Service, and the Physical Markup language [4] [7]. These concepts have been enthusiastically embraced by the RFID user community, (even if not the vendor community) for automatic identification. These concepts are substantially in harmony with the views of this author as to how the RFID technology should be developed, and my work is therefore of such a nature as to enhance the utility and applicability of those concepts.

1.2 Problem Statement

The literature review from Section 1.1.1 to 1.1.5 highlights, in general, which elements are of importance. A major conclusion which emanated from this review is that there exists difficulties with the current RFID systems that may need to be addressed:

- Electromagnetic propagation losses and polarization mismatch between the label and the interrogator. This can result in a significant reduction of power transfer across the electromagnetic link. For this reason the

study and development of an efficient power rectifier circuit is imperative [17] [18] [19].

- Inefficient label antennas. Label antennas need to be small, for such antennas it is difficult to keep the loss resistance within the antenna and the matching network small compared with the radiation resistance. Also, it is difficult to achieve adequate bandwidth with small antennas to meet the operational needs required for different UHF frequencies in different jurisdictions [20] [21].

- Transmitter power constraints, which are limited by both radio frequency licensing authorities and human exposure to RF fields [11] [12].

- The behavior of CMOS circuits at variable, unpredictable and low supply voltages, such as can be extracted by rectifying the interrogation signal, needs further exploration and optimization [29] [30].

- Transistor noise, which shows itself as variation in amplitude and phase of the RF signal. These variations are due to thermal noise, shot noise and flicker noise. These phenomena decrease the spectral purity of the transmitted signal, and increase the error rate of the overall system [25] [26] [27] [28].

- Detecting signals in a crowded and noisy channel requires lots of signal processing. Software Radio based RFID readers can be implemented to handle complex signal processing tasks [15] [103] [104].

- Reader proliferation causes reader-to-reader interference, resulting in probability of ghost reads that emphasize the need for reader networking [22].

- Work needs to be done to bring harmony into the currently diverse standards for communications and reading algorithms [23] [24].

Current developments in RFID technology continue to yield larger memory capacities, wider reading ranges, the capability to read multiple tags present in the interrogation field and faster processing of information. For more information about the development and standards of RFID systems, readers are referred to the following references [34], [12], [35], [36], [11].

Although considerable progress has been made over the past few years in the understanding of the aforementioned intriguing properties, many of them have remain unresolved.

1.3 Approach

The major part of this thesis is spent on the development of specialized CMOS circuits which function correctly under the small, unreliable and highly variable power supplies that can be extracted from the interrogation field of an RFID system. In this dissertation, a number of the issues presented in Section 1.2 are highlighted and discussed.

The principal purpose of this work is to extend the bandwidth of the sampling circuits so that future generations of the RFID systems can operate at high frequencies and higher fractional bandwidth. The first important improvement needed was to increase the RC cutoff frequency of the Schottky diodes that were used in power rectification circuits. By changing the doping concentration profiles of the diode and scaling down their geometries, a substantial improvement in circuit speed can be achieved. But, a problem with standard CMOS process is that we have no control over the doping concentration, so only the latter option, geometry, can be optimized. By using these techniques we managed to reduce parasitics, reduce loss and increase efficiency from 9% to almost 20%.

The other outcome of this work was the development of a turn-on circuit. A turn-on circuit is an interrogation field sensing circuitry which allows the battery to be connected to an active transponder (battery powered) only when communication is needed, thus lengthening the life of the battery.

Another outcome of this work was the development of an RF detector circuit for sensing a burst of high power microwave signal, even a nanosecond long. This kind of RF pulse can produce a shock that indiscriminetly disrupts and destroys unprotected CMOS circuits and devices.

Another aspect of the work is establishing, by the construction of experimental non-integrated prototypes prior to making a major commitment to IC fabrication, the practical feasibility of the fast multiple reading methodology referred to above.

Software Radio is a new technology where signal processing software is implemented on general purpose hardware platforms. Another aspect of this work is the implementation of a Software based Data Logging RFID reader, from here on referred to as SDLR. This approach can be used to solve many of the issues that traditional RFID readers face today. It can be used to enhance and accelerate the development of RFID wireless communication protocols.

As in RFID, signal processing tasks involve hard real-time constrains, the SDLR (with its built-in dedicated and powerful Digital Signal Processor) was used to perform low level tasks such as FFT, filtering, waveform shaping, etc. The results were then passed to a host PC for further study and analysis. Some of the analysis performed and documented in this work are RFID Communication Protocol Optimization, Baseband Recovery Timing Measurements, Read Range versus Frequency measurements and Reader Collisions Protocol Development.

Another focus of the work is the development of new multiple label reading and collision detection algorithms that will allow hundreds of labels to be read in a second. The design approach here is firstly to make use of advanced electromagnetic theorems which suggest a particular collision detection mechanism, and secondly to keep the label structure as simple as possible, at the expense of adding complexity to the interrogator.

The other outcome developed during this research was development of circuits for detection of signaling pulses and for stable time reference generation.

Experimental work was also carried out on labels with a kernel of state storage elements for temporary, unpowered, preservation of key data supporting the multiple read algorithm described below. Experimental work on extremely low power synchronous counter circuits for time reference generation were also studied.

Also under investigation are interrogator signaling methods that employ a combination of amplitude and phase modulation to improve signaling reliability, while still adhering to EMC regulations. Different but successful approaches for both HF and UHF systems are developed.

1.4 Organization

The first chapter of this dissertation, this chapter, offers an insight into the motivation and a brief overview of the thesis topics. The state of the art technology and how it can be improved as a result of this research is presented. The goals which are finally achieved are mentioned in this chapter as well.

The rest of the chapters are separated into two parts. The first part is concerned with optimization and application of Schottky Barrier diodes on a standard CMOS process. The second part of this work deals with the optimization and implementation of a software based data logging reader and its applications in reader-to-reader and tag-to-reader protocol development. These two parts are outlined in more details in the following two sections:

There are also several appendices in which the work of the candidate is recorded.

1.4.1 Part One

Part one is divided into eight chapters. Chapter 2 begins with introduction to various theoretical and experimental techniques used for the characterization of planar Schottky diodes using a standard CMOS process. It is then followed by the compilation of important material and model parameters of the novel SBD.

Chapter 3 explains the detailed implementation of the diode environment. Most of the concepts and implementation know-how are documented here. Some sample IP cores for the novel Schottky Diode have been implemented and their performance is elaborated in Chapter 4. Previous work had shown that the designed diodes suffer from low breakdown voltage. In chapter 5 methods have been suggested to overcome these shortcomings and simulation results are presented.

The next three chapters emphasize the system advantages gained from the implementation of SBD in an RFID transponder. The first case describes the use of the novel SBD in a turn-on circuit. The second case, analyzes and simulates its use in an RF detector circuit. Lastly, a comprehensive analysis

of a charge pump circuit based on the novel SBD is presented.

1.4.2 Part Two

Chapter 9 reviews the technology background of SDLR and provides a basic system definition, while chapter 10 deals with the implementation issues. Chapter 11 deals with two cases where SDLR was used to investigate and improve the development process of particular aspects of RFID systems. The first scenario is about optimization of small antennas designed for objects with metallic surfaces and the second section is dedicated to the development of an anti-collision protocol for RFID readers in high density area.

The status of this thesis and possible future works are described in Chapter 12. Also, included in that chapter is a statement of my contributions to knowledge. The appendix gives additional background information on the system development. Finally, the derivations of some of the equations which appear in the main body of the thesis are relegated to the appendices.

1.4.3 Appendices

In appendix A, we describe aspects of semiconductor theory relevant to the thesis and introduce the concept of Schottky diodes and their electrical activity. Further, an introduction to semiconductor theory, which forms the foundation for the interpretation of the Schottky diode property measurements, is given.

Appendix B lists the Matlab source codes of the scripts used in this dissertation. Appendix C lists the SPICE parameters, values of some important Physical constants, formulae derivations and sample calculations.

The basic research has been carried out in HSPICE. The VHDL implementation of the reader's decoder algorithm is based on the results obtained from the MATLAB simulations. Mentor Graphics FPGA Advantage for Xilinx Spartan II FPGA has been used for the hardware implementation. All the signal processing algorithm are written in the C++ programming language and have been complied into machine code using Code Composer Studio from Texas Instruments.

1.5 A Note On Units

Although Standard International (SI) units have been defined for a long time, the literature describing semiconductor theory frequently make uses of units of cm or angstrom units for length, and units of $[cm]^{-3}$ for carrier concentration. In some equations this usage does not matter, as inappropriate units may sometimes form dimensionless ratios. In other cases serious errors may occur if one inserts numerical values not in SI units into one part of a formula for which it is traditional to use SI units in other parts of the equation.

We take the view that in a scholarly work SI units should prevail and we have adopted them throughout this thesis. We offer the caution that the reader who may extract numerical data from the literature should first check the units in which the data is offered and convert them into SI units before using them in the equations provided here.

Part I

Chapter 2

Novel Schottky Barrier Diode on Standard CMOS

The purpose of this chapter is to describe a layout design which can be used to implement a novel Schottky diode on a standard CMOS process. Thus, the design can be directly implemented into a standard CMOS process without adding costly extra process steps or mask layers.

2.1 Introduction

Fast switching speed and low forward voltage drop are favorable characteristics of Schottky diodes. These properties of Schottky diodes are primarily determined by majority carrier phenomena, while minority carriers determine those properties for pn junction diodes. Due to their excellent high frequency performance, Schottky diodes have been widely used in power detection and microwave circuits [60]. They are often fabricated by depositing metals such as titanium on n-type or p-type semiconductor materials such as GaAs or SiC [61].

In order to increase high frequency performance and decrease the power loss in rectifier circuits, it is important to integrate Schottky diodes into a modern CMOS process. But a process that can integrate Schottky diodes on CMOS are not widely available as they require extra mask layers and processing steps to be implemented.

Clever techniques exist to build Schottky diodes but they are fabricated with special processes which are not available in a full-scale standard CMOS fabrication facility [54]. Others require post processing of the CMOS chip using Focused Ion Beam (FIB) to build the Schottky diode after CMOS chip has been fabricated. Although the results might be promising, again it does not apply to RFID as the price of tags would increase dramatically if it were to add any extra process steps, such as FIB. It is also worth mentioning that, FIB is a very lengthy process and it takes a long time, up to two hours, to implement a Schottky diode on a pre-fabricated CMOS chip.

Therefore this work is quite unique in that no publications were found on building a power rectifier circuit for RFID transponders using Schottky diodes on a Standard CMOS process.

2.2 Planar SBD on Standard CMOS Process

In designing a Schottky diode for RFID systems, both non-linearity of the capacitance and the RC cut-off frequency of the diode are of primary concern. A brief discussion of the diode fabrication is necessary at the outset because parasitics of the diode are functions of its geometry and physical implementation.

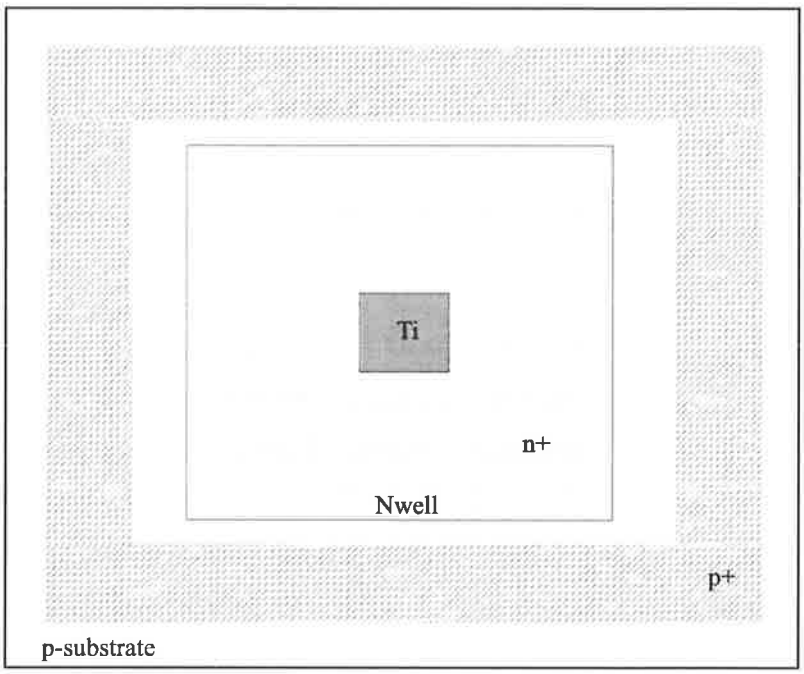
Implementing diodes on a standard CMOS process is designed specifically for ease of integration into circuits where the devices must be heavily packed and fabricated as a monolithic system. Figure 2.1 shows a cross-sectional view of the proposed novel Schottky Barrier diode that was fabricated for this project. It consists of a Schottky contact to an n-well active region and ohmic contacts to a heavily doped n+ layer. With this diode geometry the layout is compact and the extrinsic parasitic effects are minimized. That is an important factor for high frequency operation of the circuit.

Figure 2.2 shows a cross-sectional view and the schematic of the Schottky diode and its associated equivalent circuit elements. The Schottky contact has width of W, the length of the diode into the plane of the page is L and the separation between Schottky contact and ohmic contact is D. The capacitance of the Schottky diode, C, as given in Equation 2.1, is from the depleted space charge region with depth, d, where d is a function of applied reverse bias and is given by:

$$C = \frac{\epsilon W L}{d} \tag{2.1}$$

$$d = \sqrt{\frac{2\epsilon}{qN_d}\left(V_{bi} - V_{bias} - \frac{kT}{q}\right)} \tag{2.2}$$

The derivation of the above equations are given in the appendix A. The



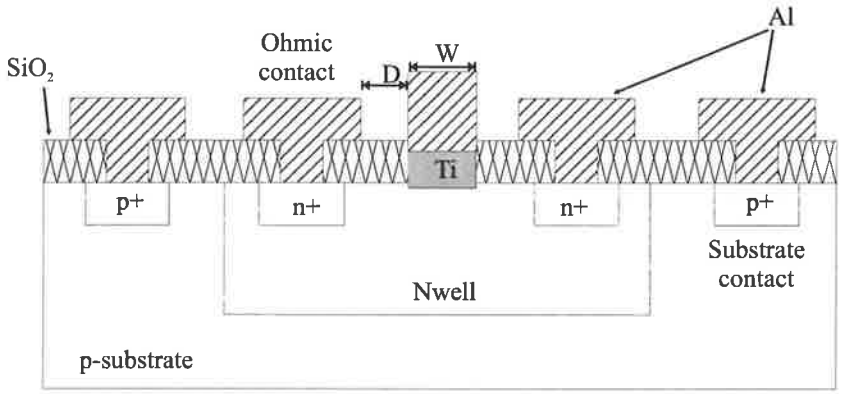


Figure 2.1: Top and Cross sectional view of a planar Schottky Barrier Diode.

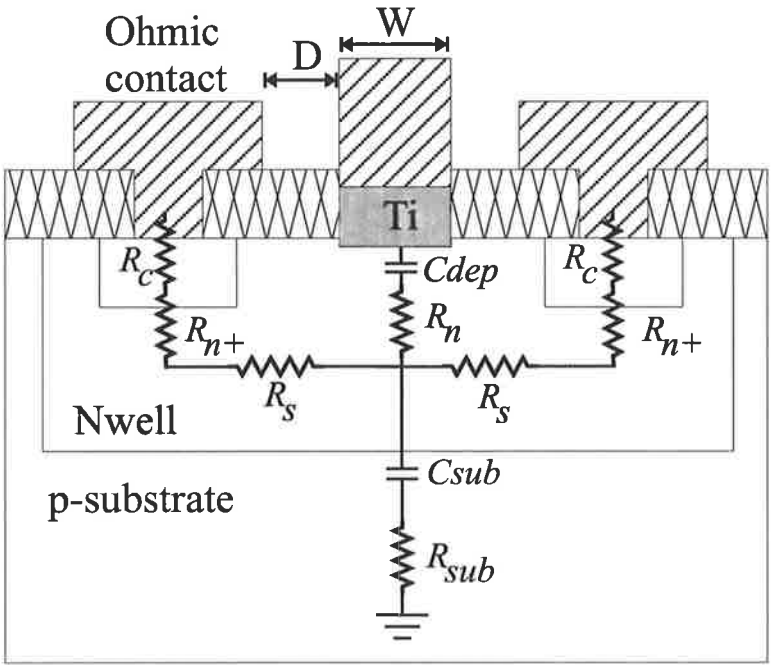


Figure 2.2: Equivalent circuit of Schottky diode, illustrating the various components of the series resistance.

sum resistance in series with this capacitance, R_{sum}, can be modeled as the sum of four components. The first element, R_n, is the n-well vertical resistance through the un-depleted portion of the n-well layer, where, the amount of un-depleted material is a function of bias. A 0 V bias is used as a conservative value because this resistance will be at its largest value, that is given by:

$$R_n = \rho_n \cdot \frac{T_{undep}}{WL} \tag{2.3}$$

where ρ_n is the resistivity of the n-well material and T_{undep} is the thickness of the un-depleted region at $0V$ bias. Because this is a sheet resistance, it is an area term and so its value is inversely proportional to $W \cdot L$. The second component of the resistance is the spreading resistance, R_s, that accounts

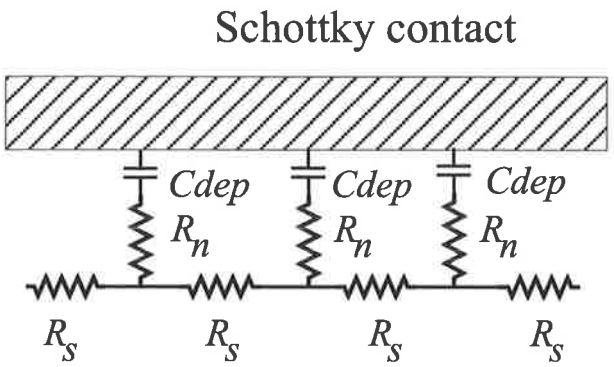


Figure 2.3: Diagram, illustrating the distribution nature of the resistance and capacitance of the Schottky contact [53].

for the spreading of the current flow under and around the Schottky contact into the n-well region. The value of R_s is given by:

$$R_s = \frac{1}{3} \cdot \frac{W}{4} \cdot \frac{1}{L} \cdot \frac{\rho_n}{T_n} \tag{2.4}$$

where ρ_n is the resistivity of the n-well material and T_n is thickness of the n-well layer. A factor of $W/4$ comes from the fact that the current travel only half the contact's width as it spreads out to either side, and that these resistances are in parallel. Another additional factor of $1/3$ arises from the distributed nature of the spreading resistance and capacitance under the contact, which is analogous to the spreading resistance in the base of a bipolar junction transistor or the distributed resistance of the gate finger of a MESFET (Figure 2.3) [68].

The third component, R_{n+}, comes from the resistance of the $n+$ contact region due to the separation between the n-well and ohmic contacts:

$$R_{n+} = \frac{1}{4}\left(\rho_{n+} \cdot \frac{D}{L \cdot T_{n+}}\right) \tag{2.5}$$

and again the factor of 1/4 arises because there are four of them in parallel. The final component of the series resistance, R_c, is from the ohmic contacts:

$$R_c = \frac{1}{4L}\sqrt{\rho_{cont} \cdot \frac{\rho_{n+}}{T_{n+}}} \tag{2.6}$$

where ρ_{cont} is the specific contact resistivity. Because R_s, R_N, and R_c are inversely proportional to L and the capacitance is directly proportional to $W \cdot L$, decreasing W and increasing L to maintain a constant diode area reduces R_{sum} in proportion to C and consequently increases the cut-off frequency of the diode,f_{cls}, which is defined using the large signal capacitance of the diode:

$$f_{cls} = 1/(2\pi C_{ls} R_s) \tag{2.7}$$

This is analogous to the design of the base-emitter junction of a bipolar transistor where the dominant resistance is the base resistance, which is also a periphery dependent term, so by decreasing the emitter strip width, the $R_{base}C_{eb}$ time constant is reduced.

Equation 2.7 for the diode cut-off frequency is valid at low frequencies, but neglects several high frequency phenomenon that adversely affect the series resistance of the diode. The following discussion of these effects is taken directly from the work by Champlin and Eisenstein [66] and also includes their references to original work. Dickens [69] was the first to treat this problem in the context of a Schottky diode and showed that the high-frequency extension of the spreading resistance is an impedance Z that for circular geometries given by:

$$Z = \frac{1}{2\pi\sigma a}\arctan(b/a) + \frac{(1+j)}{2\pi\sigma\delta}\ln(b/a) \tag{2.8}$$

where b and a are the radii of the substrate and contact, respectively, σ is the dc conductivity of the semiconductor and δ is the skin depth given by:

$$\delta = \sqrt{\frac{2}{\omega\mu_0\sigma}} \tag{2.9}$$

in which μ_0 is the magnetic permeability of free space.

Equation 2.8 is based on two assumptions that are not generally valid for semiconductors in the sub-millimeter wave region. They are

$$\omega \ll \omega_{dr} = \frac{\sigma}{\epsilon} \tag{2.10}$$

where ω_{dr} is the dielectric relaxation angular frequency and

$$\omega \ll \omega_{\text{scat}} = \frac{q}{m_e^*\mu_e} \tag{2.11}$$

where ω_{scat} is the scattering frequency, m_e^* is the effective mass of the electrons and μ_e is the mobility of the electrons. Making assumption 2.10 is tantamount to ignoring the displacement current and is the usual assumption that leads to 2.9. Assumption 2.11 is equivalent to ignoring the inertial mass behavior of the carriers in their response to an applied electric field [70].

Both assumptions can be removed from 2.8 by replacing the DC conductivity σ with the complex quantity

$$\sigma' + j\omega\epsilon = \sigma\{\frac{1}{1+j(\omega/\omega_{\text{scat}})} + j(\omega/\omega_d)\} \tag{2.12}$$

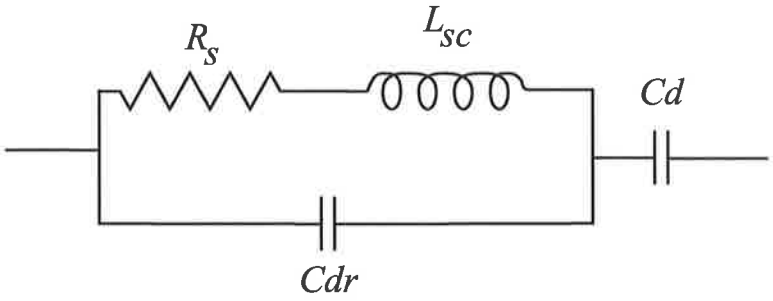


Figure 2.4: Equivalent circuit model of a Schottky diode that includes the effects of the displacement capacitance.

and by replacing $(1+j)/\sigma$ with the actual propagation constant of the semiconductor material:

$$\begin{aligned} \gamma &= \sqrt{j\omega\mu_0}\sqrt{\sigma' + j\omega\epsilon} \\ &= \frac{(1+j)}{\delta}\{\frac{1}{1+j(\omega/\omega_{\text{scat}})} + j(\omega/\omega_d)\}^{1/2} \end{aligned} \tag{2.13}$$

Substituting 2.12 and 2.13 into 2.8 and assuming $(b/a) \gg 1$ leads to $Z = Z_s + Z_0$ where Z_s is the complex bulk-spreading impedance given by:

$$Z_s = \frac{1}{4\sigma a}\{\frac{1}{1+j(\omega/\omega_{\text{scat}})} + j(\omega/\omega_d)\}^{-1} \tag{2.14}$$

and Z_0 is the complex skin-effect impedance. With a buried N_+ layer (underneath the ohmic contacts) doped as heavily as possible, $N_D \approx 5 \times 10^{18}$ cm^{-3} and $\rho_{N+} = 7.5\ \Omega \cdot \mu$m, the skin depth at 1 THz is 1.4μm. Since the layer is only 1.0μm thick, the current crowding effect will be negligible in the frequency range of interest (UHF), and Z_0 can be neglected.

An equivalent circuit model including Z_s is shown in Figure 2.4. These

high frequency effects can be modeled by adding two elements to the equivalent circuit model: a displacement capacitance $C_{\text{dis}} = 1/R_s\omega_{dr}$ and an inertial inductance $L_{\text{scat}} = R_s/\omega_{\text{scat}}$. The parallel $L_{\text{scat}}C_{\text{dis}}$ circuit is resonant at the plasma angular frequency given by:

$$\omega_{pl} = 2\pi f_{pl} = \frac{1}{\sqrt{C_{\text{dis}}L_{\text{scat}}}} = \sqrt{\omega_{dr}\omega_{\text{scat}}} \tag{2.15}$$

For the diodes used in this work, the n-well active region was doped at a level of $N_D = 1.0 \times 10^{17}$ cm^{-3}, for which $f_p = 3.0$ THz. Because the operating frequencies of the circuits are well below these, the use of the simple RC model to calculate f_{cls} as a figure of merit is valid.

Other factors, though, limit how far W can be effectively reduced. As W approaches dimensions similar to the n-well layer thickness, the lateral extent of the depletion region around the edges becomes significant, and effectively increases the area of the diode, a problem that has been solved analytically by others [71]. The real problem is that as the depletion depth increases under reverse bias, the lateral depletion region becomes proportionately larger, flattening out the C-V curve. This effect can be eliminated by using a self-aligned guard-ring to remove the n-well layer not directly under the Schottky contact, so there is no material remaining to become laterally depleted.

2.3 Models and Parameters of the SBD

Numerical device modeling and simulation are essential for analyzing and developing semiconductor devices. They help a design engineer, not only to gain an increased understanding of the device operation, but also they provide the ability to predict electrical characteristics, behavior and parameter effects that influence the device behaviour. With this knowledge and

abilities the designer can design a better structure, estimate the device performance, perform worst case analysis and optimize device parameters to yield an optimized device performance.

As in any device simulator, any quantative, or qualitative simulation of a device, relies heavily on the device models and their parameter values. Although many device models with their default parameters are available in many commercial simulators, some of their parameters do not provide realistic characteristics of the semiconductor materials. As for the SBD developed in this work, there is no model available that takes into account all the parameters affecting its performance.

Therefore, it is important to develop a model for the SBD fabricated on a standard CMOS process. In developing a model the following were the main purposes taken into consideration:

- To define the electrical circuit equivalent of the SBD structure to enable improved analysis of circuit performance.
- To define the magnitude and location of relevant parasitic electric elements to enable prediction of performance effects.
- To manipulate parasitic elements to obtain improved or enhanced circuit performance.
- It shall consist of conventional lumped circuit elements.
- It should accurately re-produce the diode IV characteristics and S parameters.
- It shall be compatible with the commonly used simulation tools.

The aim of this section is to analyze the applicability of CMOS material parameters from the literature and measurements, and implement them into

SPICE program as a way to calibrate the simulation process with the real device characteristics.

2.3.1 Simplified Model

Figure 2.5 shows a simplified model developed for the Schottky diode fabricated on a standard CMOS process. Data collected with measurement tools in the later phase of this work, was used to develop and refine this model. The refining process was done through iterative data collection and analysis and comparing expected results with actual data.

In this figure L_i and L_o are the anode and cathode series wire inductance respectively. C_i and C_o are the input and output capacitance. C_f is the equivalent capacitance of the interdigitating fingers of anode and cathode. R_i and R_o are the anode and cathode parasitic n-well resistance to the substrate (or Gnd). D_{pn} models the parasitic n-well to p-substrate pn junction diode.

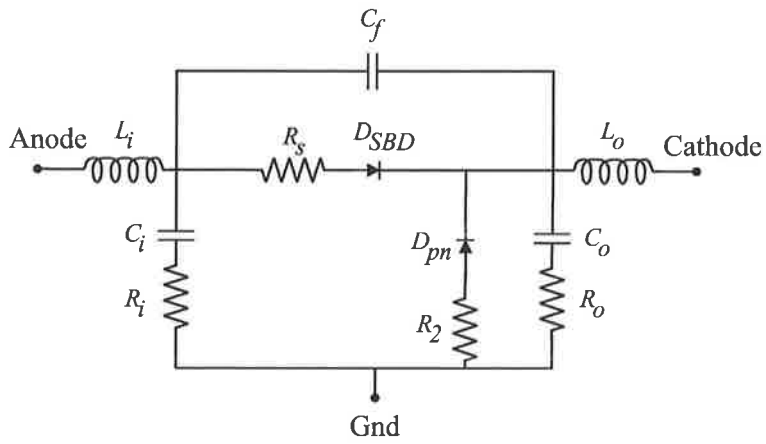


Figure 2.5: Equivalent circuit model of a Schottky Diode on standard CMOS process.

Its characteristics can be obtained from the Spice model file supplied by the foundry. R_2 is the n-well vertical resistance just above the D_{pn} diode.

2.4 Simulations

This section describes the study of simulation of Schottky Barrier diodes built on standard CMOS process. Atlas is a two-dimentional device simulator which solves numerically the following basic semiconductor device equations:

$$\epsilon \nabla^2 \psi = -q(p - n + N_D^+ - N_A^-) - \rho_s \tag{2.16}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla J_n - U_n \tag{2.17}$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \nabla J_p - U_p \tag{2.18}$$

$$J_n = q\mu_n n \nabla \phi_n \tag{2.19}$$

$$J_p = -q\mu_p p \nabla \phi_p \tag{2.20}$$

where

ϵ	is the dielectric permittivity
ψ	is the electrostatic potential
n, p	are electron and hole concentrations
N_D^+, N_A^-	are the ionized donor and acceptor impurity concentrations
ρ_s	is the surface charge density
J_n, J_p	are vectors of the electron and hole current density
U_n, U_p	are the electron and hole net recombination rate.
μ_n, μ_p	are the electron and hole mobilities
ϕ_n, ϕ_p	are the electron and hole quasi-Fermi levels.

The method used for the simulation is based on the quantum mechanic equations, as above, using finite element method to discretise these equations on a simulation grid. This descretization process yields a set of coupled non-linear algebraic equations which represent a number of grid points, for the

unknown potentials and free-carrier concentrations. This set of non-linear algebraic equations must be solved using non-linear iteration methods such as Newton's or Gummel's methods. Regardless of which iteration method is used, the solution must be carried out over the entire grid until a self-consistant potential (ψ), and carrier concentrations (p, n) are obtained. Once this is done, it is possible to determine the quasi-Fermi level (ϕ) and the hole and electron currents (J_p, J_n) from Equation 2.16 to Equation 2.20.

2.4.1 SBD characteristics

Athena, a two-dimensional device simulation program, was used to determine the characteristic parameters of the proposed SBD. Two-dimensional impurity profile was generated using the parameters extracted from the material available in Athena. Figure 2.6 shows a cross-sectional view of the test SBD generated with Athena. Figure 2.7 shows the plot of I-V characteristics of the SBD device designed with Athena.

The junction capacitance of the SBD was simulated using Atlas. The simulation results are shown in Figure 2.8. Calculations and simulations of the breakdown voltage, critical field and depletion width as a function of doping performance can be used as a useful guide in designing any silicon based device, assuming a defect free bulk material. However, in a real device, tunneling may take place before avalanche breakdown at high doping levels. Normally breakdown occurs at the edges of the space charge region. Figure 2.9 shows the results of simulation of the breakdown voltage.

The scripts used for the above simulations are presented in the appendix C.

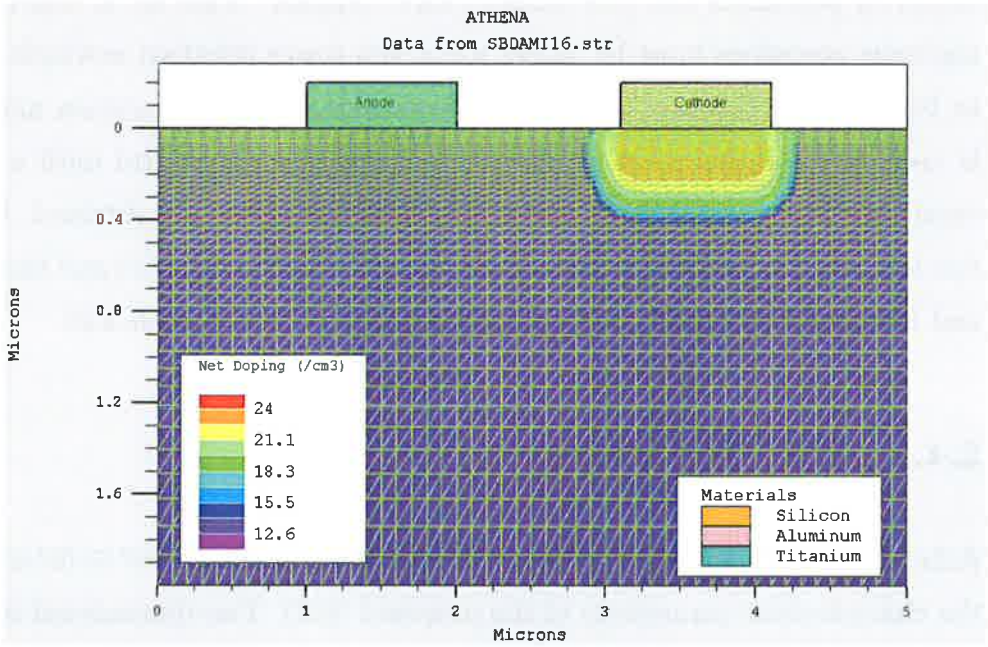


Figure 2.6: A SBD structure generated with Athena.

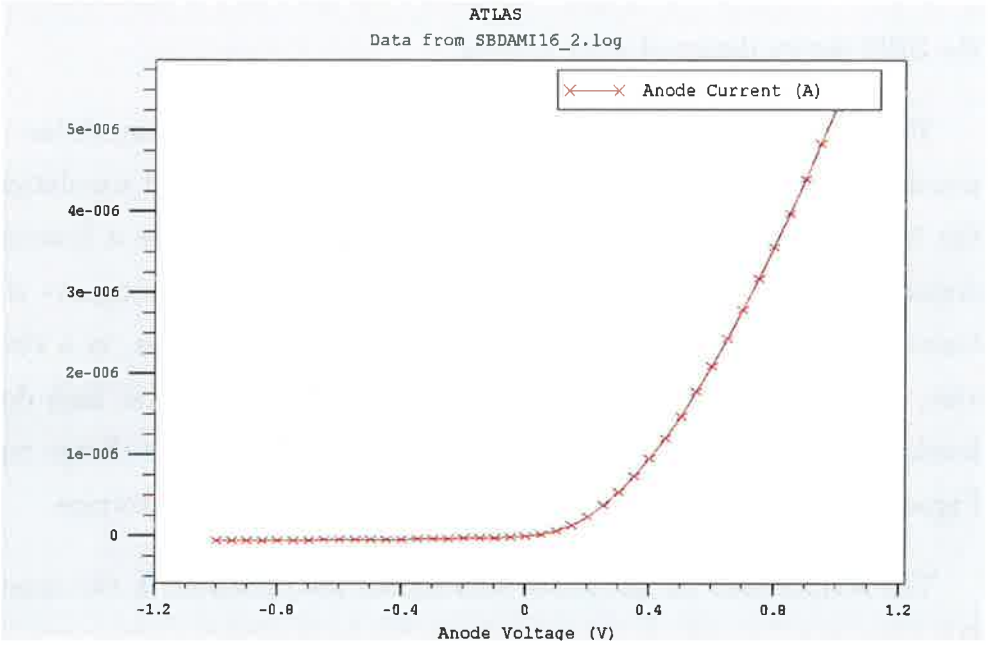


Figure 2.7: Simulated I-V curve characteristics of the above SBD generated with Atlas.

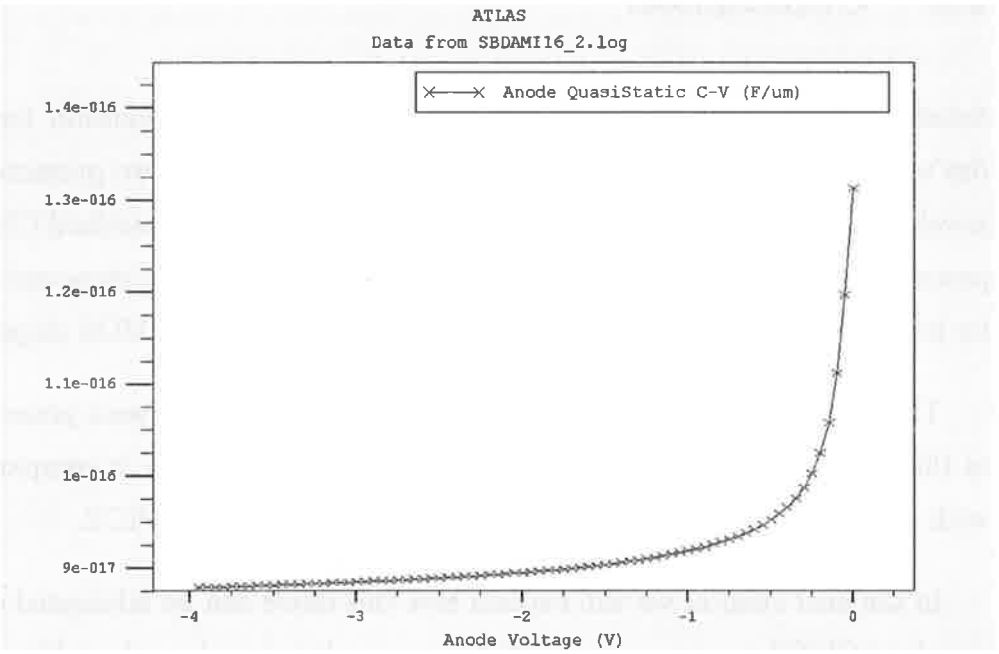


Figure 2.8: Simulated C-V curve of the SBD, generated with Atlas.

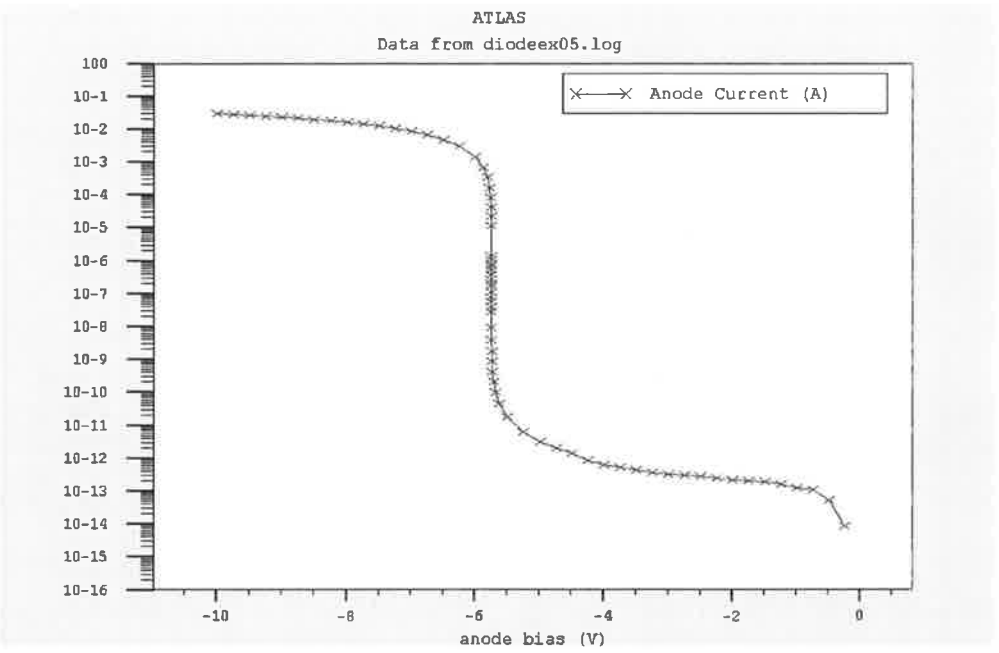


Figure 2.9: Simulated I-V curve of breakdown voltage of the SBD generated with Atlas.

2.5 Conclusion

Schottky diodes provide a high-performance, cost-effective solution for today's circuit designs for RFID applications. In this chapter we presented a novel Schottky diode structure that can be constructed on a standard CMOS process. This SBD diode does not need any special processing steps and can be integrated monolithically with existing circuits built for CMOS chips.

Theoretical analysis and characterization of this SBD has been presented in this chapter. A model has been derived for this diode that is compatible with existing standard electrical simulation tools such as HSPICE.

In the next chapter we will explain how this diode can be fabricated on a standard CMOS process, using CMOS layout editing tools such as Virtuoso from Cadence.

Chapter 3

Fabrication Process of Novel SBD

A brief discussion of the diode fabrication is warranted at the outset because the parasitics of the diode are a function of its geometry and physical implementation. This novel Schottky diode is designed specifically for ease of integration into circuits where the device must be densely packed. As such this chapter concentrates on the fabrication process, its limitations and the ways to get around those limitations.

3.1 Introduction

This chapter provides the proposed process steps in fabricating a novel SBD structure on a standard CMOS process. Detailed study of process parameters and its effects related to the fabrication of the SBD has been carried out and led to successful SBD device results. Consequently, the process steps for the fabrication of self-aligned novel SBD are proposed according to these confirmed process parameters.

3.2 Layout of the Schottky Diode

The first step in fabrication process is to create a layout of the design using Cadence Virtuoso or other layout design tools such as Magic. A layout describes the masks from which the design will be fabricated. The layers in the layout describe the physical characteristics of the device and have more details than a schematic.

There are two types of layout design: Full-Custom and Automated. Full-Custom layout is when the user physically draws all of the layers for the individual transistors, resistors, diodes, etc. This is a very tedious process, but it usually results in a compact design when compared to the automated process. The automated process, on the other hand, is done by instantiating standard cells (reusing basic blocks) and usually takes more area but layout is much faster.

As Schottky contacts are not used in the design of standard CMOS circuits, they are not present in CMOS computer aided design (CAD) tools. The ability to implement these diodes through standard CMOS process was established by modifying the design rules provided by the foundry. This led

to a series of design rule violations and as such would not be supported by the foundry.

The first test chip was designed using MAGIC, a public domain layout editor tool which was used to layout the structure of the Schottky diode. A completed design file must be sent to a foundry for fabrication in a standard file format, called Caltech Intermediate Form (CIF). After the design completion, the output CIF file was edited manually and p^+ layer was removed so that metal1 will make direct contact with n-well. The remaining CIF layers at the junction point are CAA, CA and CMF, which correspond to *sc_active*, *active_contact* and *metal1*. This allows the metal layer to connect directly to the n-well as opposed to a highly doped semiconductor as is typical with conventional well and substrate ohmic contact.

In order to simplify the process, two new layout blocks were defined. We call them *sbd-active* and *sbd-contact*. The *sbd-active* consists of the CIF layer CAA which is an active area with no hidden wells or implants associated with it. The *sbd-contact* consists of the design layers sbd-active, active contact and metal1, which correspond to CIF layers CAA, CCA and CMF, respectively.

The diodes were fabricated using the Charted Semiconductor 0.35 μm process to the dimensions provided in Table 3.1, and were subjected to an extensive set of tests. The results from this fabrication were satisfactory. In this run two types of Schottky diodes were designed; n-type and p-type. N-type SBD diodes were made by depositing metal directly on top of the n-well layer. The results were promising and showed a working Schottky barrier diode can be built using this technique. Although the forward voltage drop is slightly more than what was expected, the Schottky diode implemented produced contacts that had rectifying properties which can be characterized by an ideal diode equation. As for p-type SBD, metal on p-well was used. p-type diodes did not show any sign of rectification due to the almost equal

work functions of the p-substrate and the aluminum, thus no difference in potential between the semiconductor and the metal, and no barrier existed. In fact, p-well and metal1, aluminum, formed an ohmic contact.

3.2.1 Layout Steps

The second chip was designed using a layout editor called Virtuoso from Cadence. The steps taken in the Virtuoso layout design to build a Schottky diode are summarized in the following steps:

Draw the N-Well

1. Select the n-well layer from the Layer Selection Window (LSW).
2. Select the Create → Rectangle (or choose the Rectangle icon from the side toolbar).
3. Using the mouse, draw the n-well on the cell-view to be 6.8 long by 4.9 μm wide.

Draw the N+ diffusion

1. Select the N+Diff layer from the LSW window
2. Select the Create → Rectangle (or choose the Rectangle icon from the side toolbar).
3. Using the mouse, draw the N+Diff on the cell-view to be 3.8 long by 1.2 wide. The N+Diff should be placed within the n-well. (the Edit→move command can be used to move the layer)

Draw the Metal1 Contacts

1. Select the Contact-dg layer from the LSW window
2. Select the Create → Rectangle (or choose the Rectangle icon from the side toolbar).
3. Using the mouse, draw the Contact on the cell-view to be of minimum size. The Contacts placed within the N+Diff region will form an ohmic contact to the n-well. Any Contact placed outside the N+Diff, but inside the n-well forms a Schottky contact. It is better to place ohmic contacts such that they surround the Schottky contacts like a ring.

Draw the Metal1

1. Select the Metal-1 layer from the LSW window
2. Select the Create → Rectangle (or choose the Rectangle icon from the side toolbar).
3. Using the mouse, draw the Metal layer on the Contacts. Metal-1 layer is used to connect ohmic and Schottky contacts to the appropriate GSG pads.

The final result should look some thing like the diagram shown in Figure 3.1. The design procedure mentioned above is only suitable for NEC technology. Layout structure for any other fabrication method are similar to the above steps but not necessarily the same. There is also some fine tuning that needs to be done, depending on different manufacturer's rules.

A few publications have reported failure in designing Schottky diodes on standard CMOS process [64]. It is crucial to follow the fabrication process

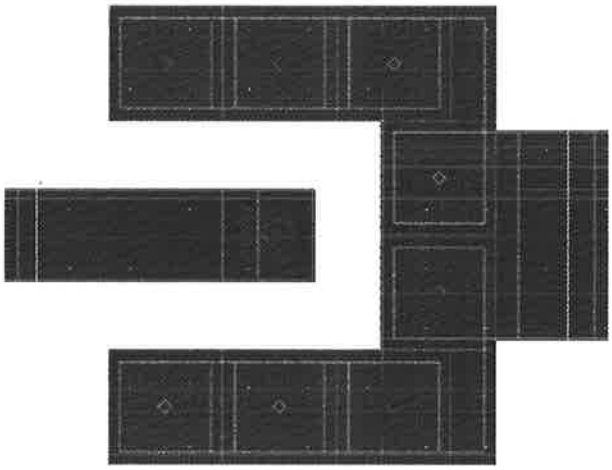


Figure 3.1: CAD layout of the Schottky diode

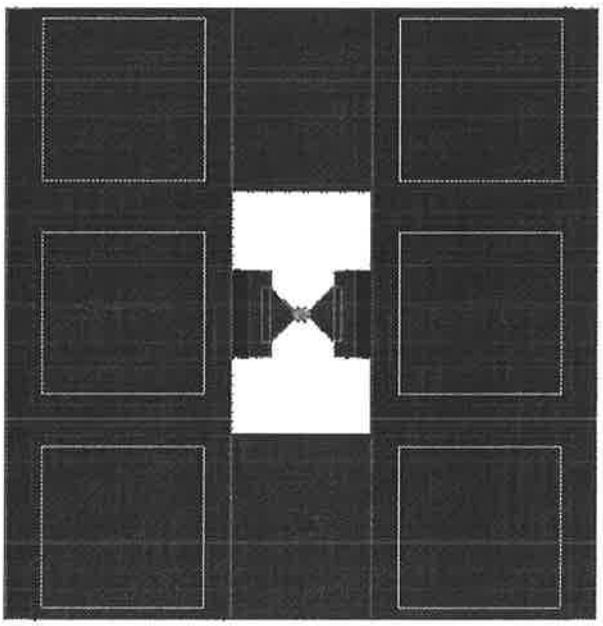


Figure 3.2: CAD layout of the Schottky diode, including the guard ring around it and the GSG probe pads.

steps and to visualize them mentally. In order to build a working SBD it is essential to make sure that an active layer is placed on top of the Schottky contact area. Failure to do so, results in an open circuit or an incomplete contact as depicted in Figure 3.3. Omitting to put an active layer, will result in the field oxide growing on and around the contact area. During the later process step, where the contacts are made, the thinness of thick oxide layer is too deep for the chemical dissolvent to etch away a hole all the way down to the n-well area. The result would be an incomplete contact.

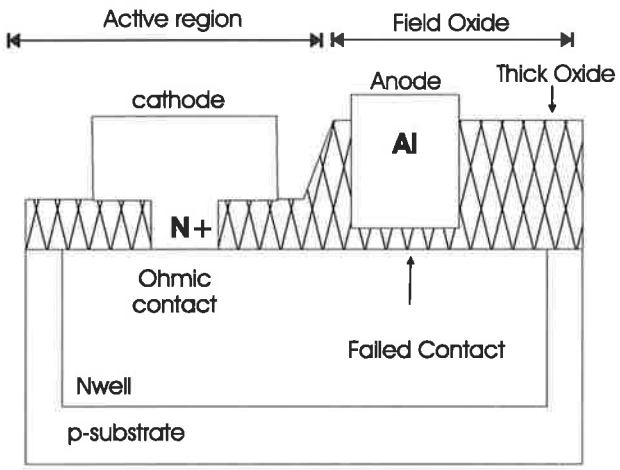


Figure 3.3: Layout cross-sectional view of badly designed Schottky diode.

3.3 Fabrication

The development of CMOS technology was driven mainly by digital circuits. However, recently, CMOS has been used extensively in the analog circuit design. The reason being the low cost of fabrication and the ability to integrate both analog and digital circuits monolithically on the same silicon chip, which improves the overall performance and reliability, while at the

same time reducing the cost of packaging. Currently circuit designers are exploring emerging pure CMOS approaches, integrating not only digital and analog blocks but also radio frequency (RF) circuits on the same chip.

As in a standard CMOS process, we have no control over doping concentration and the type of the material used, the only parameter that can be controlled is the size of the junction. In order to get a high efficiency rectifier, it is essential to have Schottky diodes with high saturation current I_s, which results in low forward voltage drop, low junction capacitance C_j, small series resistance R_s, and also low parasitic capacitance to substrate C_{sub}. A large junction Schottky diode results in a large saturation current and small series resistance, but also large junction and substrate capacitance. Those large capacitances would dominate the diode characteristics, so the optimum junction size of the diode needs to be found. For comparison, Table 3.1, shows the different Schottky junction sizes that were implemented.

From the discussion in the previous chapters we know that the series resistance of the n-well is relatively high. This manifests itself as the series resistance of the Schottky diode. This was compensated by interdigitating the fingers of the ohmic and Schottky contacts. The distance between the ohmic and Schottky contacts was also reduced to the minimum allowable by the CMOS design rule-set. This technique increased the perimeter of the contact while keeping its area to minimum, so in effect, not only does it decrease the junction capacitance but also it reduces the series resistance. Interdigitating also greatly reduces the distance from anode to cathode, mitigating the likelihood of electrons being swept down to the substrate. Figure 3.2 shows a layout view of the Schottky diode including the guard ring around it and the GSG probe pads.

Table 3.1: Prototyped Schottky diode junction sizes.

No	Area (pm^2)	Perimeter (μm)	Fingers	W × L (μm)
SD1	0.23	1.92	1	0.48 × 0.48
SD2 [1]	0.23	1.92	1	0.48 × 0.48
SD3	1.4976	7.20	1	0.48 × 3.12
SD4 [2]	16.128	72.90	6	0.48 × 5.6
SD5	14.4	60.96	1	0.48 × 0.30

3.3.1 Geometry

Several devices of different contact size and geometry were laid out and fabricated in the first fabrication stage. Table 3.1 shows the different Schottky junction sizes that were implemented. The following sub-sections explain each one of these designs in more detail.

Donut Junction

The simplest way to improve the performance of SBD is to surround the Schottky barrier junction with ohmic contacts as shown in Figure 3.4. This surrounding ohmic contact would also act as a guard ring, trapping all electrons wandering from the metal into the n-well. It still keeps the junction area to its minimum size, while at the same time decreasing the series resistance by forming a network of parallel connected resistors.

[1]The SD1 and SD2 have same junction area, but SD1 anode and cathode are connected by metal1 while the anode of SD2 is connected out by metal2. That would make the cathode contacts to surround the junction.

[2]Extra-long junction dimension Schottky Diode is fabricated to verify our understanding over the dimension effects.

This would lower the junction impedance by at least a factor of five. HSPICE can be used to analyze and predict the junction impedance. An HSPICE net list must contain lumped resistors and capacitors placed in series and parallel. After simulation, HSPICE is able to provide us with a total equivalent impedance value.

Multi-finger Junction

Another contemplated (and proven to be even better) design geometry can be achieved by interdigitating the contacts. In this configuration each type of contact is surrounded by the opposite contact type. In this constellation, the design is more compatible with the CMOS design rule-sets, which is an advantage over the donut shape design. Multi-finger designs have larger junction area compared with the donut type, which would increase the junction capacitance. That is not an attractive property for UHF applications. Figure 3.5 shows a typical comb shaped Schottky diode structure.

3.4 Pad Design Considerations

Coplanar GHz probes have only been available in the 1980s, and have significantly advanced wafer probing capabilities. Successful GHz probing requires that consideration be given to layout and design before design completion and mask fabrication. Failure to observe specific layout requirements can result in the inability to test the devices with GHz probes.

There are specific mechanical and electrical layout rules that must be followed. These rules will assure that the fabricated device can be successfully probed. It is important to note that what we really measure is what is connected to the probe tips. This includes parasitics and parasitics associated

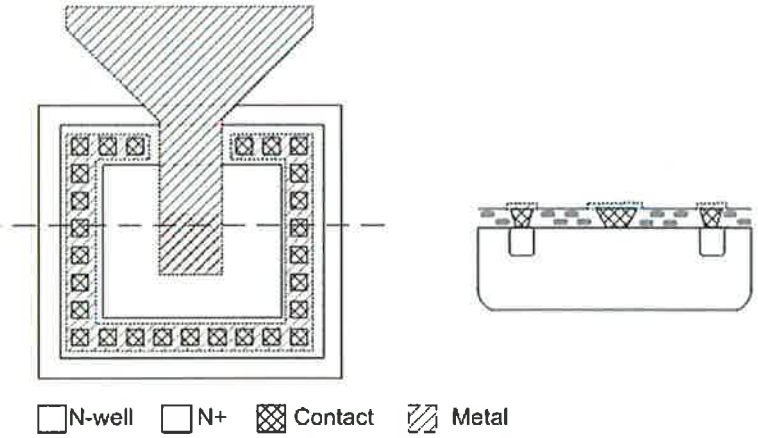


Figure 3.4: Top and Cross-section view of the Donut shaped Schottky diode on standard CMOS process.

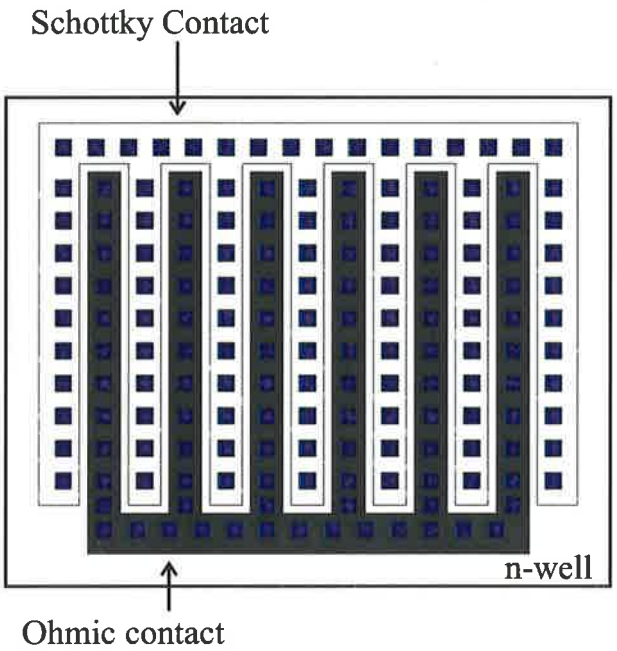


Figure 3.5: Top view of multi-finger Schottky contact diode.

with the interconnects from pads to other devices on the substrate. In order to measure a device independent of the pad effects, it is useful to make the pads as small as possible, so their effects would be negligible or can be easily subtracted from the measured data. When using a network analyzer we will be measuring everything past the end of the probe tips, unless we use special calibration or correction techniques. A detailed de-embedding procedure is covered in the next chapter.

Different pad structures were designed, some with guard-rings and some without. The use of a guard-ring does not effect pad spacing. Our general recommendation is that pads must be 100 μm x 100 μm with a pitch of 170 μm (allows for pad edge to pad edge spacing of 70 μm). Smaller pads and tighter pitches are possible but not without considering the exact location of the package cavity pins, angle of wire to the pins and the length of the wires.

The fabrication process used for this project supports two metal layers. The pad structure constitutes the top most metal layer, which in this case is metal2. As such a layer of metal1 was extended in every direction underneath the signal pad to prevent peripheral fringe capacitance to the substrate.

Ground shielding under the signal pad has several benefits in RF probing. One benefit is that coupling between the probe ports will be minimized compared to the unshielded pad structures since the signal pad is isolated from the substrate. This coupling technique becomes important especially in a CMOS technology with a low substrate resistivity. Another benefit is that the process of de-embedding the pad parasitics becomes simpler because its equivalent circuit is purely capacitive with a high quality factor. This structure is shown in Figure 3.6. Yet another benefit for a shielded probe pad is better noise characterization of devices because substrate coupling through the signal pad is minimized.

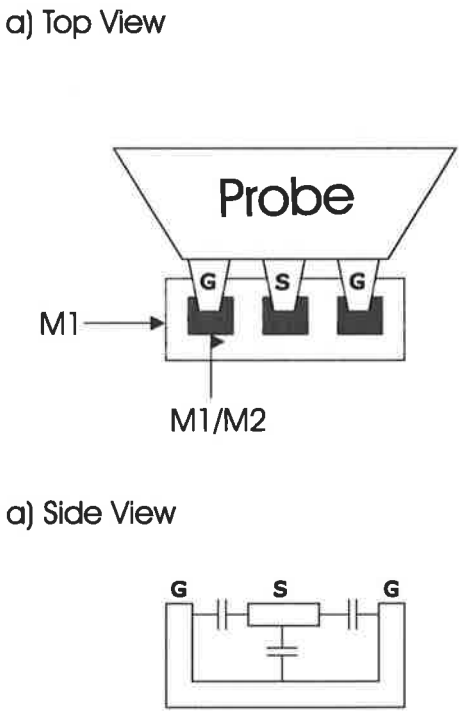


Figure 3.6: a)One-port GSG top view of the ground shielded probe pad layout. b)Side view of the layout.

3.5 Implementations

Our basic approach here is to divide our attention into two major categories. One is the geometry and the other is the optional fabrication process capability. The second choice is not easy and we decided to leave it for the second phase of fabrication. During the first fabrication phase we only tried to optimize and work on the geometry and theory of the Schottky diodes on standard CMOS process.

The first design was aimed for the AMI 1.5 μm process. The area of the metal-semiconductor contact was set to the minimum process feature size, 1.6 μm square. The n-well ohmic contact ring was placed as close as possible

to the Schottky contact. This would minimize the series resistance of the diode. In order to be able to bias the diode and also guard the diode from the rest of the circuit, a guard ring was placed around it. The guard ring is made of p-substrate contact.

A better isolation from the surrounding circuit can be achieved by negative biasing the substrate of the diode. Each diode on the die is connected to the outside world by three testing pads of size 100 μm x 100 μm. The presence of these testing pads adds a significant amount of capacitance to the measurement of the diode characteristics, which would not be present in a working device. This chip was delivered and subsequent testing carried out by midyear 2002.

During the second phase of the research, since enough confidence was gained about the validity of the designed SBD, it was decided to make use of Intellectual Property (IP) produced. Therefore, commercial companies were contacted to obtain bids for the design and construction of the Schottky diode, in return they would have access to the IP developed. Shanghai's HUAHUNG-NEC Pty Ltd was the first company to accept our offer. Therefore the design work began in early 2004. The fabricated chip was delivered to us by the end of 2004.

3.6 Conclusion

For this project we have developed a novel Schottky diode on a standard CMOS process. For circuit development this device has been modeled. To build this kind of diode there is no need for additional process steps. Both types of diode, n-type and p-type devices are available.

Schottky diodes are not part of standard CMOS process; as such there is

no model for them in EDA CAD tools. This makes the design of the novel SBD more tricky as the automated DRC tools fail to recognize the errors that might be present in the novel SBD design. All the error checking needs to be done manually, which is very tedious and itself prone to human errors. A proposed solution to this problem is to modify the files where the DRC program reads its input rules. By doing that we can add new rules to the list of the existing rules and make it legitimate to build novel Schottky diode on a standard CMOS process.

The main controllable parameter in the design of this type of Schottky diode is the area of the contact region. The other parameters such as doping concentration and work function of the metal and electron affinity of the semiconductor are determined by the CMOS foundry process. As such the nature of this type of Schottky diode is not controllable as effectively as it should be and in fact may vary substantially from one process to another. From previous chapters, it is clear that, in order to decrease the junction capacitance, we need to decrease the junction area. Also, it has been learned that decreasing the junction area would increase the diode's series resistance. So, considering the planar structure of the CMOS circuits, it seems appropriate to fabricate Schottky diodes of different geometry and employ very exhaustive testing techniques to characterize them.

Chapter 4

Measurements and Characterization of SBD

After the circuits had been fabricated, a number of measurements were made to characterize them. The first diagnostics were on the test SBD diodes. Some of these diodes were not connected to the rest of the circuit but instead had microwave probe pads on each end. Detailed measurement methods and characterization of DC and AC performance of these SBD diodes are covered in this chapter.

4.1 Introduction

Diodes can operate under two conditions: forward bias and reverse bias. In this section the fabricated Schottky diodes were examined under these two conditions and such characteristics as their built in voltage, junction capacitance, doping concentration and breakdown voltage were measured and characterized. Techniques such as current versus voltage plots and capacitance versus voltage plots were used during these measurements.

Diodes on which these measurements were carried out, were connected to Ground-Signal-Ground (GSG) pads that were configured to be used with microwave probes. That would allow both DC and AC measurements to be conducted on the device without the need to remove the probes, that would save both pads and probes from wearing out or being damaged.

The test structures on the test chip were laid out in such a pattern to include several different diode geometry sizes, some with just a minimum sized diode and some with a multi-finger configuration.

Current versus voltage curves were measured in both forward and reverse bias conditions. That would give a complete DC characteristics of the diodes. Capacitance versus voltage curves were used in order to check the doping profile in the diode N-well region. By comparing the measured CV data of a large diode with that predicted using Equation 2.2, the exact value of doping characteristics can be determined.

4.2 DC Characteristics

The first measurements done on the diodes were usually DC voltage-current measurements. That would reveal their forward voltage drop (V_j), emission

coefficient (N), reverse saturation current(I_s) and series resistance (R_s).

An effective and straight-forward method for linear curve fitting is the regression analysis method. The goal of this analysis is to determine the values of parameters for a function that causes the function to best fit a set of data observations that were collected. The more observations collected the more accurate the estimate of the parameters will be. To do this we have to solve the equation below for parameters m and b:

$$y = m * x + b \tag{4.1}$$

The diode equation, given by Equation 4.2, is a non-linear one and as such it can only be solved numerically. The way around this is to transform this non-linear equation to a linear one. A diode has an exponential function, so the transform that we need is a logarithmic conversion to linear range, for which a linear regression analysis can be used. From there we can work out the slope and the y-intercept of the line of best fit. A simple diode model at DC is depicted in Figure 4.1. This model consists of an ideal diode D, representing the non-linear characteristics and a series resistance R_s, which accounts for high current effects.

Figure 4.1: DC diode model

The basic diode equation describing the ideal diode current voltage relationship is given by:

$$i_d = I_s(e^{\frac{V_d}{NV_T}} - 1) \tag{4.2}$$

In this equation V_d and i_d are the diode voltage and current respectively. V_T is the thermal voltage that is given by:

$$V_T = \frac{kT}{q} \tag{4.3}$$

where, k is the Boltzmann's constant, T is the absolute temperature and q is the magnitude of an electron charge. At room temperature V_T has a value of almost $26mV$.

Applying the logarithmic conversion yields the following approximation:

$$ln(i_d) = ln(I_s) + \frac{V_d}{NV_T} \tag{4.4}$$

$$= ln(I_s) + \frac{1}{NV_T}V_d \tag{4.5}$$

which is an equation of the same format as Equation 4.1. In order to interpret this linearly we have to substitute:

$$y = ln(i_d) \tag{4.6}$$

$$b = ln(I_s) \tag{4.7}$$

$$m = \frac{1}{NV_T} \tag{4.8}$$

$$x = V_d \tag{4.9}$$

After the logarithmic conversion of the measured values of i_d and V_d, they are introduced into the regression equations of Section C.1.1.

From there we obtain the y-intercept b and the slope m of the linear

regression function. Solving Equation 4.7 for I_s and Equation 4.8 for N, we are able to calculate these two parameters from b and m as follows:

$$I_s = e^b \tag{4.10}$$

$$N = \frac{1}{mV_T} \tag{4.11}$$

A script for Matlab was developed to optimize and perform this tedious task automatically. The script is named `regression_rs.m` and is listed in Appendix B.

4.2.1 Validity of the method

The method described above is valid only in the range of measured data, where the assumptions are true. This means the above equations are valid for $V_d > 0$, where the noise level in the measured data is low, i.e. where the bias is larger than 0.2V [65]. The other assumption made is that the diode current must not be dominated by *recombination effects*, the weaker slope at low bias voltage, but it must be below *high-current effects*, thus there are no ohmic effects, or the famous knee-effects, in the half-logarithmic diode characteristic curves, as depicted in Figure 4.2.

4.2.2 Measuring R_s

After the parameters I_s and N are extracted from the collected data, the value of R_s can be found. This can be done by using the two highest points:

$$R_s = \frac{V_d(n) - V_d(n-1)}{I_d(n) - I_d(n-1)} \tag{4.12}$$

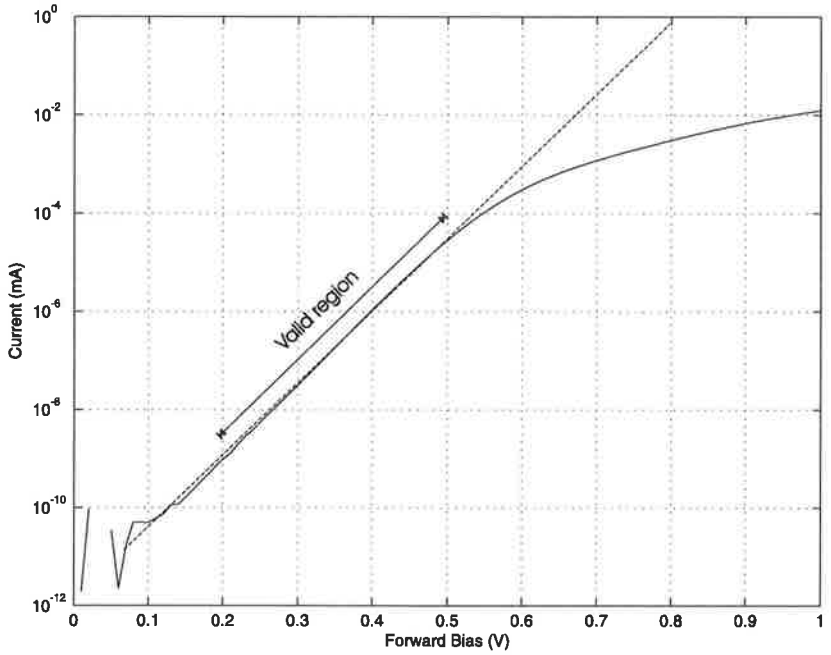


Figure 4.2: Valid region of IV curve for use in the DC characterization.

Another method that can be used to determine the ohmic part of a diode characteristic is to consider the voltage drop between the ideal diode characteristics and its shift due to the ohmic effect. This can be accomplished by choosing a point from the measured data where the ohmic effects are more pronounced, say $V_d(n)$ and $I_d(n)$, and then calculating the voltage using the ideal diode equation for that particular data point $I_d(n)$. The difference between the two voltages can be divided by its corresponding current to finally give the value of R_s. This method is illustrated in Figure 4.5. The prerequisite for a good R_s extraction is to make sure that the decline for high bias voltage is clearly visible in the extraction range.

The forward bias DC characteristics were measured for all of the fabricated diodes. The minimum size diode has a much higher series resistance compared with other configurations. The multi-finger configuration exhibits much lower series resistance as we would expect from its geometry. The

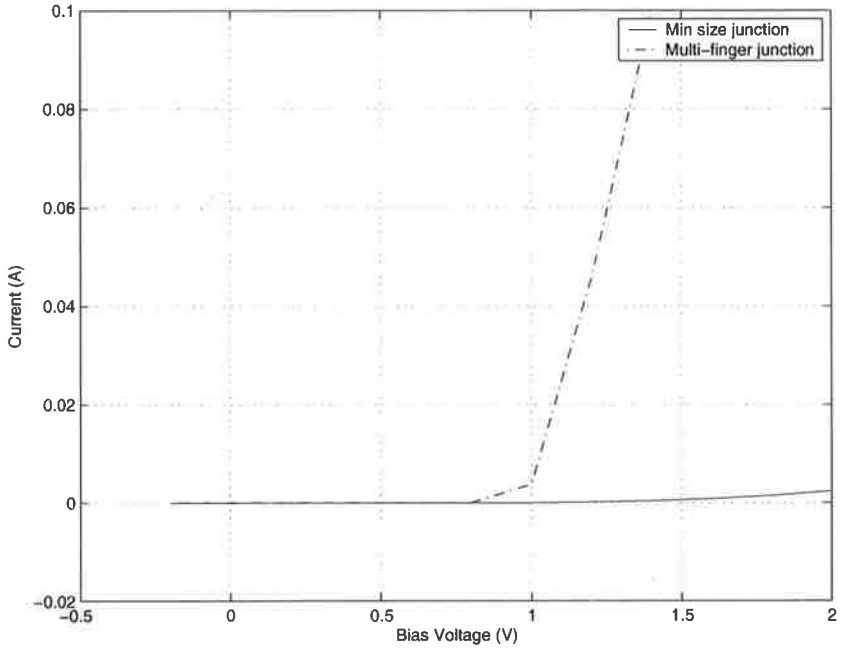


Figure 4.3: Forward I-V curve of SBD1 of size $0.48\mu m \times 3.12\mu m$ in comparison with SBD4, which has a six-finger junction of finger size $0.48\mu m \times 5.6\mu m$.

measured data for two extreme cases are plotted in Figure 4.3. The Matlab scripts used to do the regression analysis are presented in Appendix B.

4.2.3 Reverse Bias Region

The reverse breakdown voltage, V_{br}, was determined by measuring the I-V curves of diodes under negative bias conditions. These measurements for two diodes, one with minimum feature size and the other with multi-finger configuration, are compared in Figure 4.6.

There are two types of breakdown that occur in diodes. The first is the Zener breakdown which happens at low voltage, say below five volts. The second type of breakdown is called Avalanche breakdown, which happens at higher voltages, for example above 10 volts.

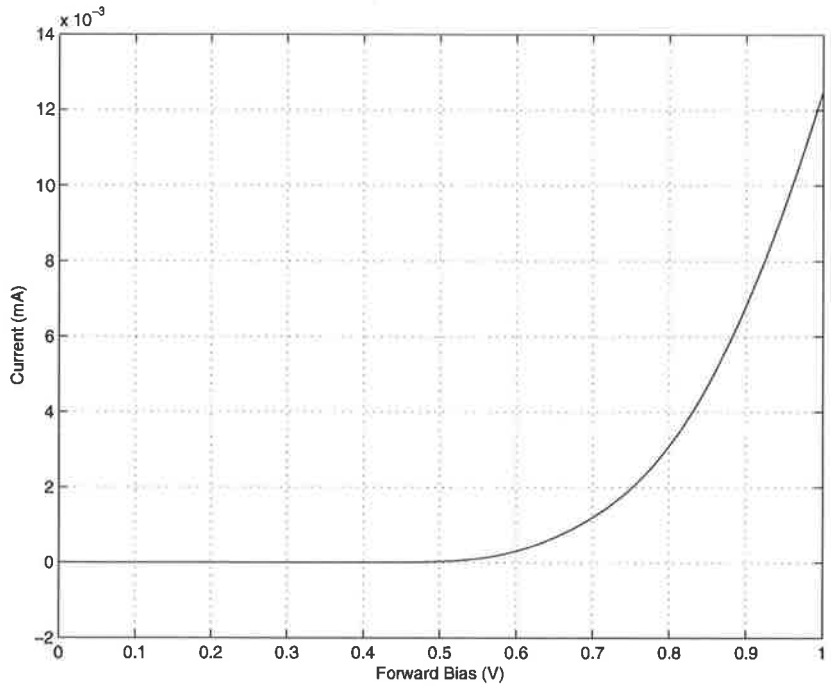


Figure 4.4: Forward I-V curve of SBD4 of size $0.48\mu m \times 5.60\mu m$ plotted with current on a linear scale.

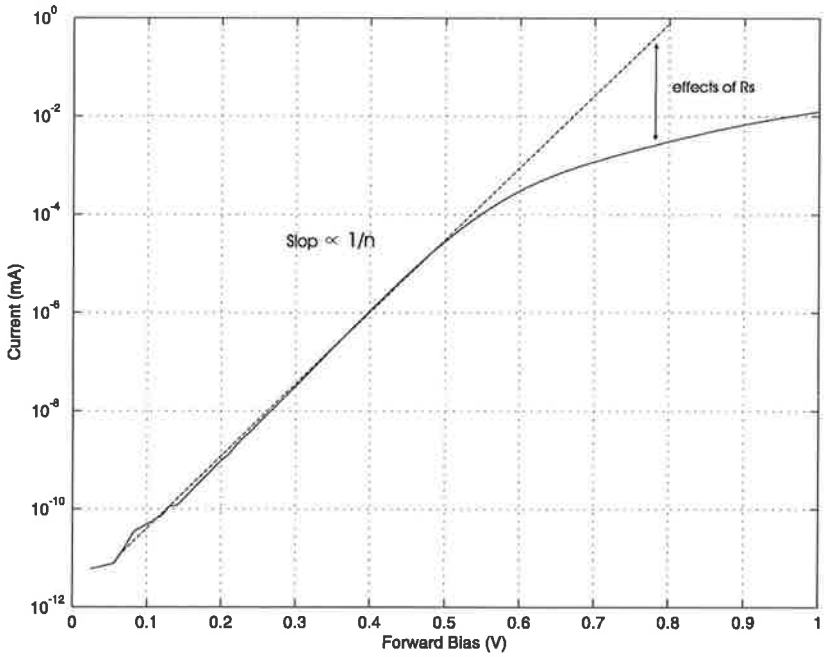


Figure 4.5: Forward I-V curve of SBD4 of size $0.48\mu m \times 5.60\mu m$ plotted with current on a logarithmic scale.

There are two parameters that need to be measured: BV, the break down voltage and IBV, the current at the breakdown voltage. The typical measured values for these parameters are; $BV = 25V$ and $IBV = 9mA$.

Note that BV is recorded as a positive value although on a typical characteristic curve the value of the breakdown voltage is negative. These parameters were measured by doing DC analysis. The source voltage was swept from -30 to 0 volts on a Keithly 236 Source Measurement Unit and the results were plotted in Figure 4.6.

As it is evident form the plots the designed SBDs have some shortcoming in their breakdown voltage. There exists several methods to tackle this problem which are covered in more details in the next chapter.

4.2.4 Temperature Dependencies

"Zener" and "Avalanche" breakdown are terms often used interchangeably, with the former more common. Both refer to breakdown of a diode under reverse bias. Avalanche breakdown occurs in lightly doped junctions, where the depletion region is comparatively long. The doping density controls the breakdown voltage. The temperature coefficient of the avalanche mechanism is positive. That is, as the temperature increases, so does the reverse breakdown voltage. The magnitude of temperature coefficient also increases with increasing breakdown voltage. For example the temperature coefficient of a 8.2V diode is in the range of 3 to 6 mV/K, while the temperature coefficient of an 18V diode is in the range of 12 to 18 mV/K.

Zener breakdown occurs in heavily doped junctions. The heavy doping makes the depletion region extremely narrow. So, the carriers cannot accelerate enough to cause ionization. With the thin depletion region, however,

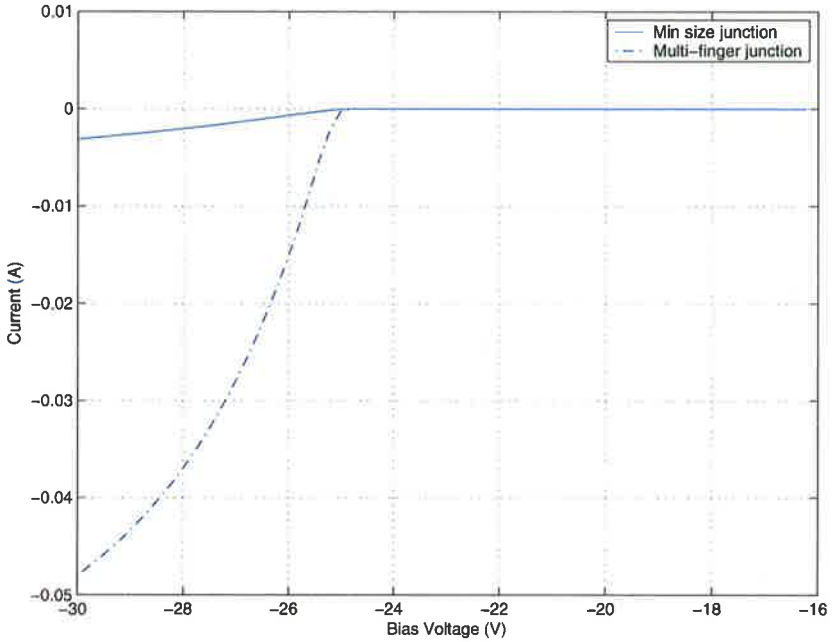


Figure 4.6: DC Reverse breakdown measurement of SBD1 of size $0.48\mu m \times 3.12\mu m$ in comparison with SBD4, which has a multi-finger junction of size $0.48\mu m \times 5.6\mu m$.

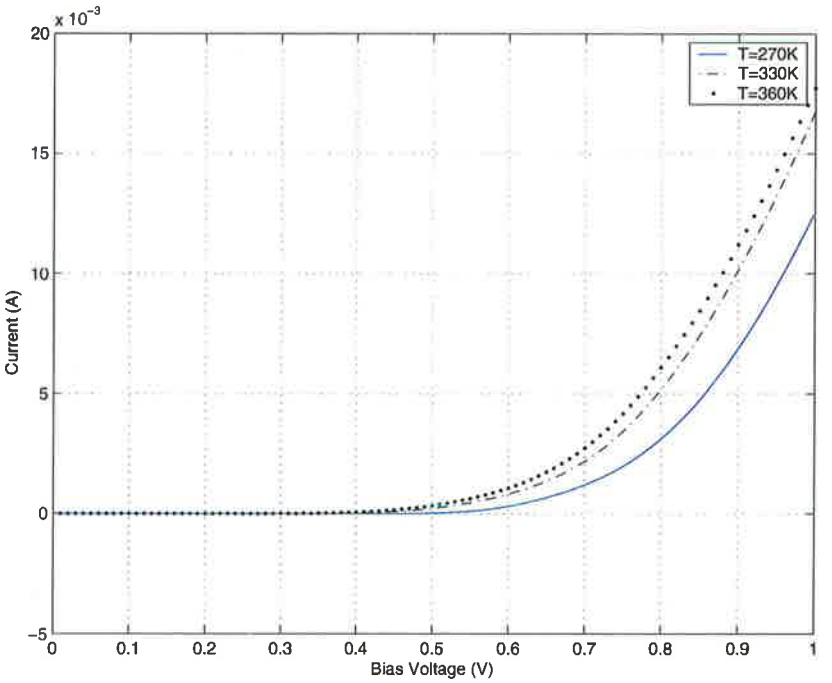


Figure 4.7: Comparison of I-V curve at three different temperatures.

quantum mechanical tunneling through the layer occurs causing current to flow. The temperature coefficient of the Zener mechanism is negative. Therefore the breakdown voltage of a particular diode decreases as its temperature increases.

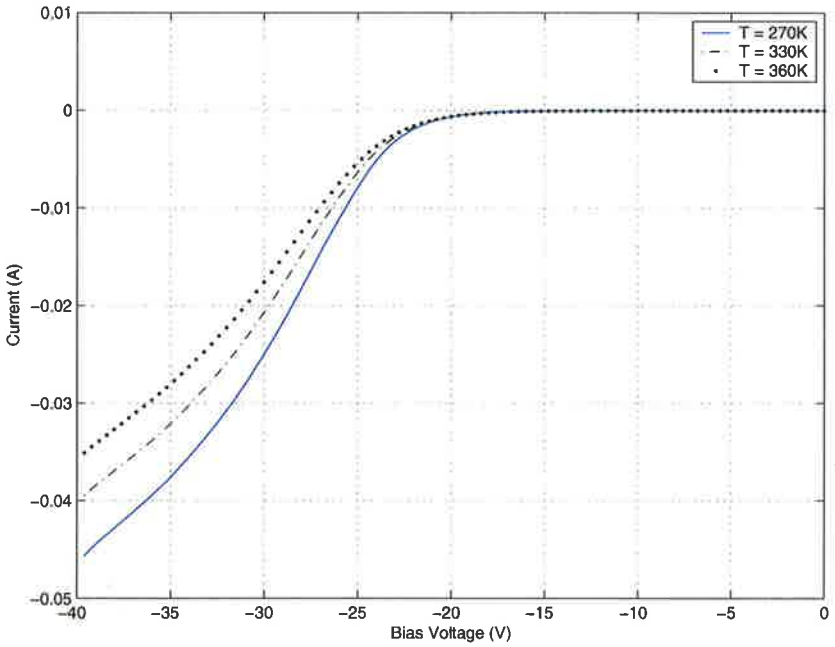


Figure 4.8: Comparison of breakdown voltage at three different temperature.

In any diode either or both of these mechanism may be present. At low doping level and high voltage the Avalanche mechanism dominates, while at heavily doped junction and lower voltage the Zener mechanism dominates.

As such, the next experiment performed on the SBD was to test the devices at different temperatures. Since a temperature increase causes the SBD to shift its characteristics I-V curve in the positive direction, then, its breakdown method is due to tunneling. This phenomena is depicted in Figure 4.7 and Figure 4.8. For avalanche, an increase in random kinetic energy

of individual carriers would make it more difficult for free carriers to descend down the potential energy ramp crossing the depletion region due to their increases ability to travel to different parts of their source semiconductor.

4.2.5 Instruments Used

A Keithley 236 Source Measuring Unit (SMU) was configured to measure the diodes' characteristics. Using this instrument reduced the effort required to aquire data and characterize the device performance. The Keithley 236 has a noise floor as low as 0.4 femtoamp peak-to-peak, which makes it very suitable for measuring low leakage current of a diode. A PC computer equipped with a PCI GPIP card was used to drive the SMU. It is capable of rapidly executing a whole series (100 or so) of measurements without tying up the external data bus and remote computer.

The diodes were connected to the Keithley 236 SMU between In/Out Hi and In/Out Low. Then the SMU was programmed to sweep voltage and measure the current or to sweep current and measure the voltage. The sweep of the voltage was done in the reverse bias region of the diodes to determine the leakage current at a known voltage. Next, a sweep of current was done in the forward bias region to limit the power in the device to a safe level.

The effect of incident light and the temperature on the device was studied by generating a family of I-V curves for different levels of these variables. The remote sense connections of the SMU were not used as there was not much current flowing through the connecting leads.

Table 4.1: Prototyped Schottky Diodes DC Measurement Results

No	Size μm	I_s	N	Rs	Description
sbd1_iv.txt	0.48×0.48	5.65×10^{-10}	3.89	343K	Minimum size rectangular
sbd2_iv.txt	0.48×0.48	3.41×10^{-10}	3.63	248K	Minimum size circular
sbd3_iv.txt	0.48×3.12	1.31×10^{-11}	2.01	599	Long junction, rectangular
sbd4_iv.txt	0.48×5.60	8.21×10^{-12}	1.76	55.6	Long junction, 6 fingers
sbd5_iv.txt	0.48×30.00	7.58×10^{-12}	1.77	62.9	Extra long junction

4.2.6 Summary

The series resistances of the fabricated diodes were measured and tabulated. The SBD of minimum size has a very high series resistance while the one with multi-finger configuration shows minimum series resistance. So, interdigitating the design would help to lower the series resistance, although doing so has other adverse effects on the operation of the diode, which will be discussed in a future section.

The linear region of the I-V curve on the logarithmic scale will have a slope that is inversely proportional to the emission coefficient, so from two points in this region the value of I_s and N can be determined. The diodes typically had an emission coefficient of N = 2 and a reverse saturation current density of $1.3 \times 10^{-11} A/cm^2$ as summarized in Table 4.1 .

These measurements led to a very important discovery that minimum size diodes had extremely large values of R_s. It was almost five times what was predicted. This is illustrated in the previous graphs. This phenomenon can be attributed to the lateral straggle of ions during the ion implementation process. The material along the mask edge is damaged by the ions that scatter in the horizontal direction. When this damaged material becomes a

significant portion of the total diode length, the series resistance of the diode is greatly increased.

To quantify the impact of this traverse straggle, a few test structures were designed. Diodes of varying length were defined by the implant mask and by plotting the measured resistance as a function of the mask width (as shown in Figure 4.9) the effective width of each diode was determined. From the results it was concluded that the effect was worse for small diodes as shown in Table 4.1. It was found that *the diodes with minimum length suffer from severe degradation of series resistance.*

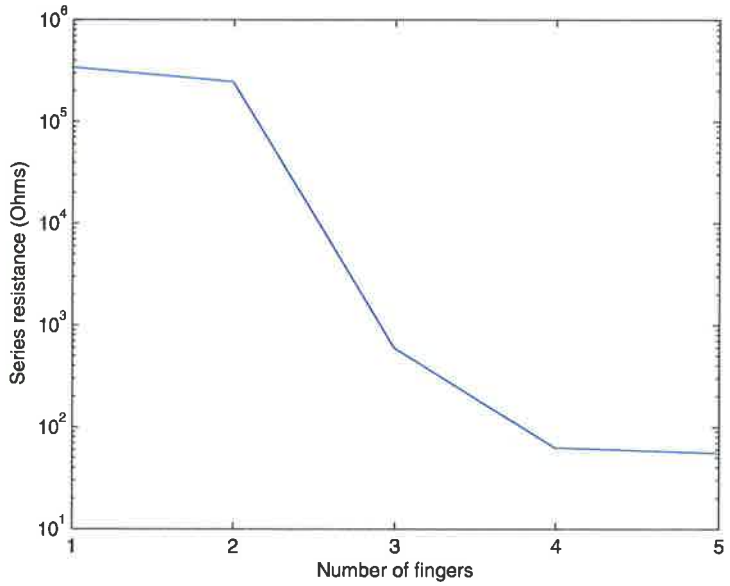


Figure 4.9: Measured resistance as a function of the mask width.

4.3 Microwave Measurements

Microwave data was obtained by measuring the s-parameters of diodes from 500 MHz to 2 GHz. As the cut-off frequencies of the diodes were so high, there were two critical steps required in order to accurately extract values for the junction capacitance and the series resistance. First of all because the series resistance of the diode is small, the measured s-parameters were very close to the edge of the Smith chart. Thus a very accurate calibration was needed because even a small amount of ripple would make the diode appear to have gain. Secondly the capacitance of the pads used to connect the probes were comparable to the intrinsic capacitance of the diodes being measured, so the data for the diodes has to be carefully de-embedded from the effects of the pads.

The most common method of calibration used for microwave devices is the open-short-load-through (OSLT) method. In this method three different standards are measured on each of the two ports. A precise 50 Ω load and a short circuit are measured and then the probe is raised in the air to make the open circuit measurement. If two port calibration is required the probes are connected to a very short through line. The problem with this method is that when measuring the open circuit we raise the probes and as air has lower dielectric constant than the substrate (and hence a lower capacitance), so a negative capacitance is defined for that measurement. This problem was overcome by using an open circuit pad on the substrate. Another problem that sometimes arises as a result of non accurate measurement is that the reflection coefficient of a device goes outside the Smith chart.

A second calibration method that can be used is the line-reflect-line (LRL) method. This method does not suffer from the drawbacks for the OSLT method. In LRL calibration, two transmission lines of lengths differing by

a quarter of a wavelength are measured, followed by a measurement of a high reflection standard. Because the value of the reflection standard does not have to be precisely defined, this method does not require the same approximation as made for OSLT. The drawback of this method is that the lines need to be exactly 50 Ω at all frequencies, which means that the calibration degrades at high frequencies, because dispersion effects alter the line impedance. The second problem with this method is that the lowest frequency that can be measured is limited by the longest length of line used as standard, typically giving a low frequency limit of about 2 GHz.

The third commonly used technique is the line-reflect-match (LRM) method that was developed by Cascade Microtech [57]. This is a hybrid of the two earlier techniques that overcome the shortcomings of each method. In this method a very short line, 1 ps electrical length, is measured for the through standard, so it will not have dispersion problems. The reflection standard is the same as for the LRL method in that it must be a high reflection but does not have to be precisely defined. The third calibration measurement is to terminate both probes in precise 50 Ω loads that are mathematically treated as infinite delay lines. This eliminates both dispersion problem and the lower frequency limit suffered using the LRL method.

4.3.1 De-embedding parasitics

At low frequencies, the electrical characteristics and small signal performance of an electronic device can be identified by measuring its corresponding voltage and/or current. From there its related quantities such as impedance and admittance can be found. At high frequencies however, voltage and current are difficult to measure as the signal must be treated as a traveling electromagnetic wave. Therefore the characteristics of passive components at high frequencies need dedicated high frequency measurement instruments. Special

attention must be paid to minimize the measurement errors.

Aluminum is a commonly used metal for silicon integrated circuits. Some processes are migrating to copper. Aluminum forms the least expensive and simplest pad metal. Devices with Aluminum and Copper pads are much more difficult to accurately probe than the ones with gold pads. But gold has the tendency to contaminate silicon. As such any measurement that is sensitive to a series resistance will be affected by pad contact resistance.

This section describes the high frequency on-wafer measurement methods and equivalent high frequency modeling methods for on-chip Schottky diodes. The first section describes the high frequency measurement methods and the second section describes equivalent circuit modeling methods in details.

4.3.2 High frequency on-wafer measurement methods

Electronic devices can be represented by a network of circuit model parameters. The models are usually in forms of two-port networks as shown in Figure 4.11 [39]. It can be expressed in terms of Impedance, Z-parameters or admittance, Y-parameters. Parameters of a two port network can be represented by the well-known set of equations given in Section C.1.2.

Since voltage and current can be measured easily at low frequencies using a multimeter or an oscilloscope, these quantities are widely used in low frequency measurements. At high frequencies, however, those measurements are done in terms of their scattering parameters (s-parameters). The scattering parameters are fixed properties of the (linear) circuit which describe how the energy couples between each pair of ports or transmission lines connected to the circuit. Equations below are linear equations describing a two-port network, where a_1 and a_2 are the incident electromagnetic waves and b_1 and

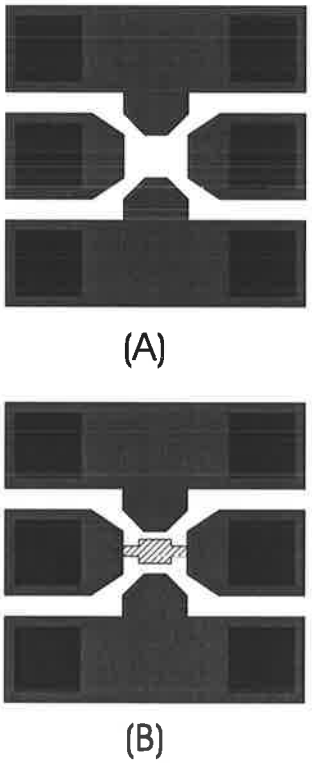


Figure 4.10: (A) Empty pads (PAD), (B) Pads with a Schottky diode, device under test (DUT).

b_2 are the reflected electromagnetic waves. The s_{11} and s_{22} are the input and output reflection coefficients and s_{12} and s_{21} are forward and reverse transmission coefficient. The respective equations are provided in Section C.1.3.

In order to perform high frequency characterization of an on-chip Schottky diode, on-wafer s-parameter measurements must be employed. This method is desirable because it mitigates the effects of wires, off-wafer fixtures and other parasitics. The on-wafer probe pads and transmission line ground planes can be directly implemented on the substrate along with the on-chip Schottky diode. Since the presence of probe pads and the ground

Figure 4.11: Diagram of two-port networks for s-parameters

planes next to the Schottky diode can add some parasitics into the measurement results, de-embedding of these parasitics is a crucial step in order to obtain valid results.

The exclusion of parasitic effects of pads and wiring can be done by fabricating dummy devices consisting only of probe pads and ground planes on the substrate near the Schottky diodes under the test. By measuring the s-parameters of both DUT and PAD, and subtracting the admittance of the PAD from that of the DUT, accurate measurements for the Schottky diode can be obtained.

Typically the test setup consists of a vector network analyzer, a s-parameter test set and a frequency sweeper. Figure 4.12 shows an example of such a setup consisting of an Agilent 8510C vector network analyzer, a HP8340B frequency synthesizer and HP8515A s-parameter test unit. The ground-signal-ground (GSG) pads used were 40A-GSG-200-P from Cascade Industries.

The first step in doing measurements is to calibrate the system using high frequency calibration standards. In this work the CS-5 impedance standard substrate with open-short-load-through (OSLT) calibration kit was used as shown in Figure 4.13. That allows for removal of all parasitics in the cables and the connectors and also sets the reference plane at the probe tips.

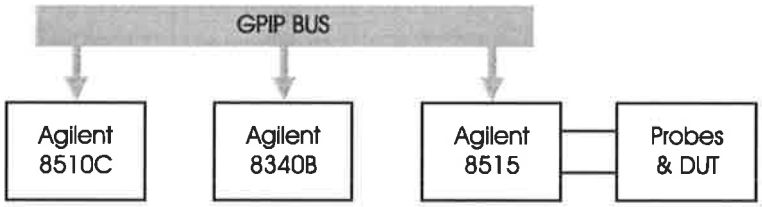


Figure 4.12: Measurement setup consisting of an Agilent 8510C Vector Network Analyzer, HP8340B Frequency Synthesizer, HP8515A s-parameter Test Unit and High frequency probes form Cascade Industries.

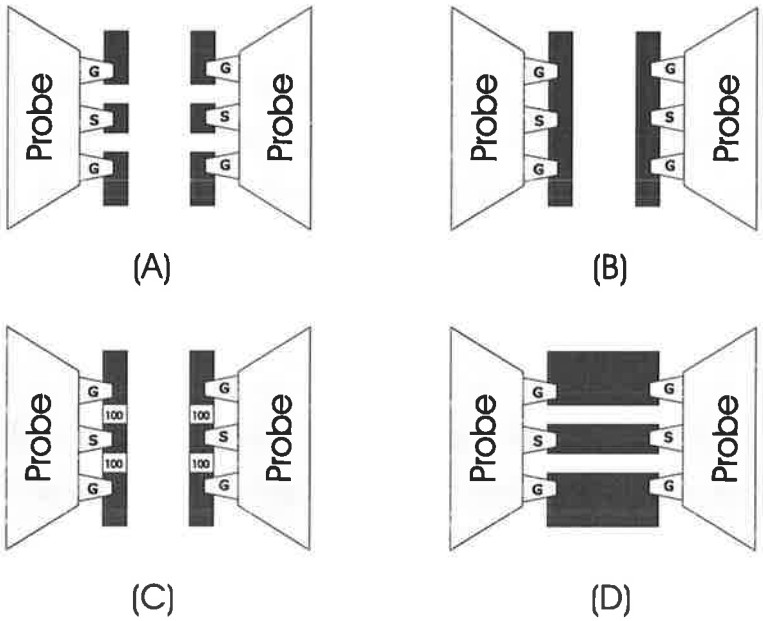


Figure 4.13: Open-Short-Load-Thru Calibration procedures of the on-wafer probes. (A) Open, (B) Short, (C) 50Ω load, (D) Thru.

The s-parameters measured by the HP instruments are automatically stored in a text file in CITIFILE standard format. A Matlab script was used to convert the produced files into the widely used Touchstone format. The Matlab computer program citi2touch.m is shown in the Appendix B. Once the pad and DUT s-parameter data are obtained, the admittance of pads must be subtracted from the DUT data so that one can have accurate data for DUT without the parasitic effects.

One convienient method to do the de-embedding is by converting the s-parameter matrices of the DUT and the pad into Y-parameter matrices and then subtracting the Y-parameter of the pad from those of the DUT [39]. The s-parameter of both Schottky diodes (DUT) and that of probe pads are converted into Y-parameters (admittance) using equations for two port networks.

$$y_{11} = \frac{1}{Z_0}\frac{(1-s_{11})(1+s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.13}$$

$$y_{12} = \frac{1}{Z_0}\frac{-2s_{12}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.14}$$

$$y_{21} = \frac{1}{Z_0}\frac{-2s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.15}$$

$$y_{22} = \frac{1}{Z_0}\frac{(1+s_{11})(1-s_{22})+s_{12}s_{21}}{(1+s_{11})(1+s_{22})-s_{12}s_{21}} \tag{4.16}$$

Where $Z_0 = 50\ \Omega$ and $Y_0 = 0.02$ S are characteristic impedance and admittance of the system respectively.

$$\begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{\text{De-embedded}} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{\text{Schottky}} - \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}_{\text{PAD only}} \tag{4.17}$$

In order to obtain the Y-parameters of the Schottky diode only, the Y-

parameters of the probe pads were subtracted from the diode with probe pads using the equations below. These de-embedded Y-parameters include only the effect of the Schottky diode. Modeling of the Schottky diode is discussed in the next section. The de-embedded s-parameters can be converted back from Y-parameters using the equations below.

$$s_{11} = \frac{(1 - y_{11}Z_0)(1 + y_{22}Z_0) + y_{12}y_{21}Z_0^2}{(1 + y_{11}Z_0)(1 + y_{22}Z_0) - y_{12}y_{21}Z_0^2} \tag{4.18}$$

$$s_{12} = \frac{-2y_{12}Z_0}{(1 + y_{11}Z_0)(1 + y_{22}Z_0) - y_{12}y_{21}Z_0^2} \tag{4.19}$$

$$s_{21} = \frac{-2y_{21}Z_0}{(1 + y_{11}Z_0)(1 + y_{22}Z_0) - y_{12}y_{21}Z_0^2} \tag{4.20}$$

$$s_{22} = \frac{(1 + y_{11}Z_0)(1 - y_{22}Z_0) + y_{12}y_{21}Z_0^2}{(1 + y_{11}Z_0)(1 + y_{22}Z_0) - y_{12}y_{21}Z_0^2} \tag{4.21}$$

The Matlab program de-embed.m, as shown in Appendix B, converts s-parameters of DUT and pad into Y-parameters, subtracts admittances of pad from those of DUT and converts the resulting Y-parameters back into de-embedded s-parameters to be used as the correct measurement data in circuit modeling.

4.3.3 The diode model generation

A diode model is to be developed such that it is compatible with the standard simulation softwares. Agilent parameter extraction software, IC-CAP, was used for this purpose. Using this software the intrinsic Si Schottky diode elements were modeled, excluding parasitic resistances, using the de-embedding techniques as covered in the previous chapter. There are parasitic resistance

of the RF probes and cable that contribute to losses. Figure 4.14 displays the procedure how to generate the Root-diode model using the IC-CAP program.

The first step is to measure RF port parasitic series resistances using short pattern on an impedance standard substrates. For a two port network configuration, it measures series resistance at each port and then subtract that from the diode measurements made later on. The procedure also includes the extraction of the parasitic inductances. The de-embedding process allows the intrinsic Root-diode to be model constructed with much higher accuracy. After model extraction the program performs a comparison of the diode simulation based on the extracted model with the measurement data. The program then re-calculates the s-parameters and iterates the steps mentioned here until the discrepancy satisfies the user defined criteria. The end result is the Root-diode model.

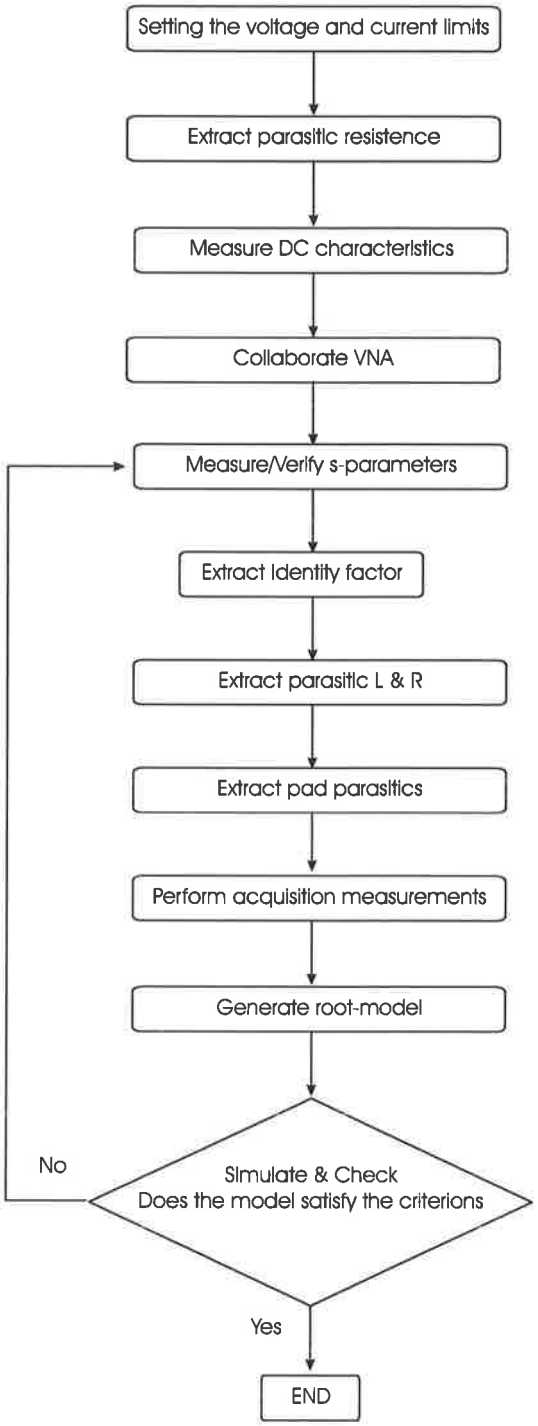


Figure 4.14: Procedures to generate Root diode model using Agilent IC-CAP software.

4.3.4 High Frequency Measurement Results

After accurately calibrating the network analyzer, the second step when making the microwave measurements was to account for the effects of the pads that were used to contact the diodes. This was done by first measuring the pads when they were open circuited and then shorting them together across where the device under test would be. In the first case only the capacitance should be measured, so the imaginary part of the input admittance should be a straight line as a function of frequency and have a slope equal to the capacitance. The data for the open standard is shown in Figure 4.17, where the linear fit from 500 MHz to 2 GHz corresponds to $C_{pad} = 14pF$.

The inductances of the pads was determined by taking the measurement data from the short standard and subtracting the capacitance determined from the open standard. The remaining part should look purely inductive since the resistance is negligible. So the imaginary part of the impedance is linear with frequency and have a slope equal to the inductance as shown in Figure 4.16.

The parameters of the diode under the test were de-embedded from the pads by subtracting the capacitance and inductance determined from the two standards, as shown in the equivalent circuit in Figure 4.17. Near the edge of the Smith chart, all the circles of constant resistance are extremely close together, so it is very difficult to identify a small R_s. This can be seen in Figure 4.18 where the measured diode impedance is barely distinguishable from the edge of the Smith chart. This again emphasises the importance of having an extremely good calibration technique.

In order to extract the parameters of the diode it is instructive to consider the admittance of the device instead of its impedance.

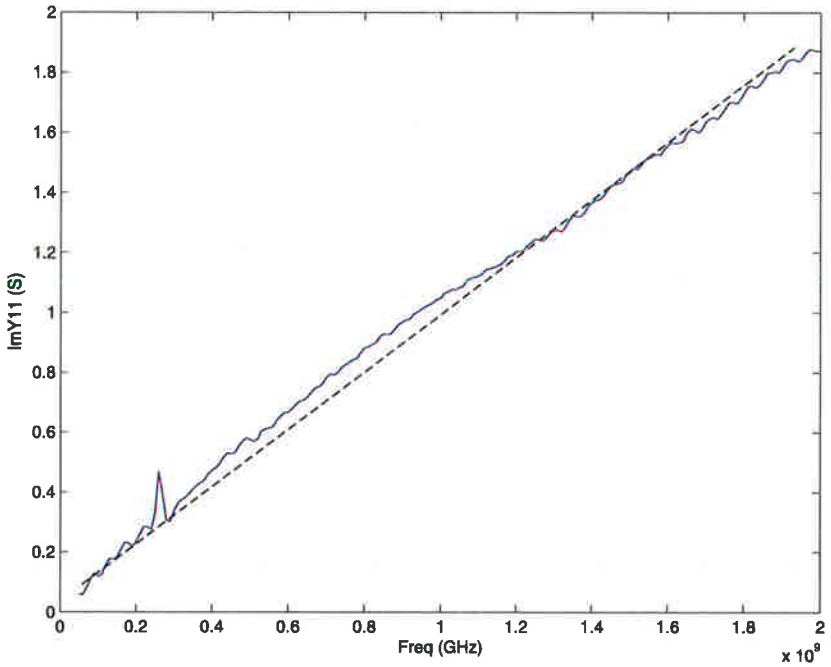


Figure 4.15: The capacitance of the pads is determined by fitting a straight line to the imaginary part of the input admittance.

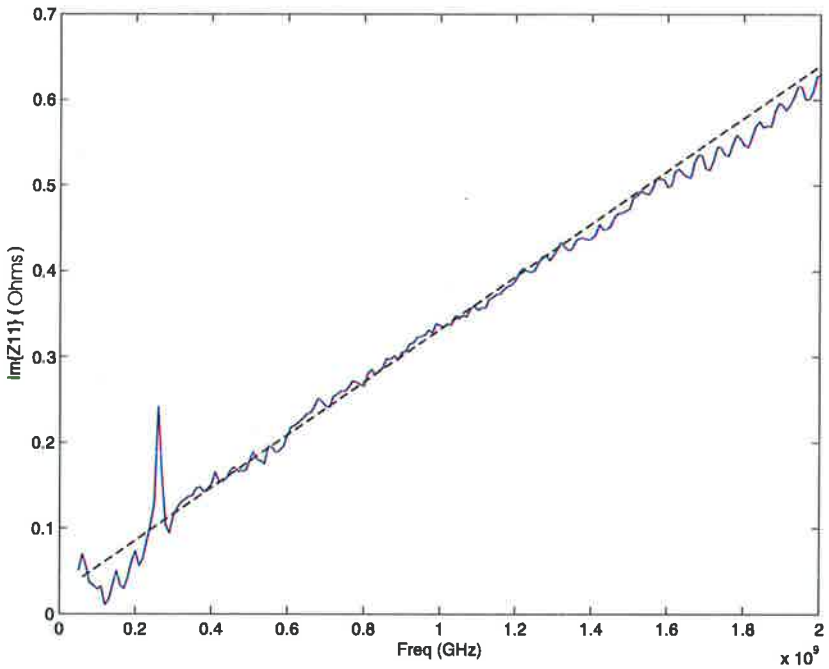


Figure 4.16: The inductance of the pads is determined by fitting a straight line to the imaginary part of the input impedance.

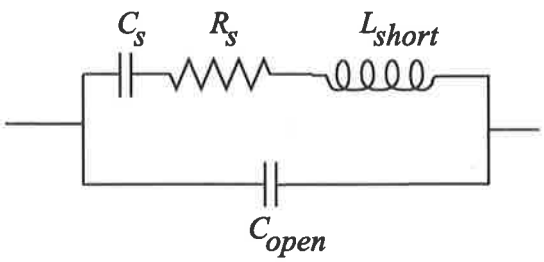


Figure 4.17: Circuit model used to de-embed the diode under test from the pads' parasitics.

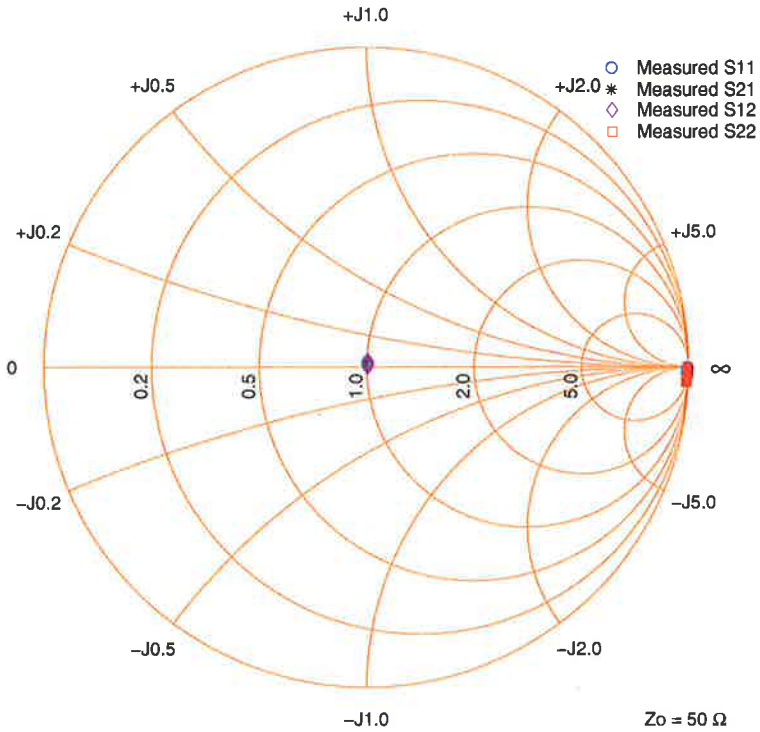


Figure 4.18: Smith Chart showing de-embedded data for SBD4 at 0V bias.

$$Y = \frac{\omega^2 C^2 R_s}{1+\omega^2 C^2 R_s^2} + \frac{j\omega C}{1+\omega^2 C^2 R_s^2} \tag{4.22}$$

At angulary frequencies $\omega << 1/CR_s$, this reduces to:

$$Y = \omega^2 C^2 R_s + j\omega C \tag{4.23}$$

The capacitance is now easily determined as the imaginary part of the admittance, it is linear with frequency and has a slope of C. The real benefit in examining the admittance instead of impedance comes when determining R_s. The conductance of the diode at frequencies well below f_c is directly proportional to the diode area, so examining the real part of the admittance provides a reliable extraction of R_s. By knowing the diode capacitance accurately R_s can be determined by fitting a curve to the measured conductance.

Figure 4.18 shows the de-embedded measured capacitance of SBD4 diode of a size 0.48 $\mu m \times 5.6$ μm at 0 V bias. The extracted capacitance of 900 fF is very close to the theoretical value of 820 fF calculated for that diode. The measurements were made on this diode because it was the test diode that had the largest area.

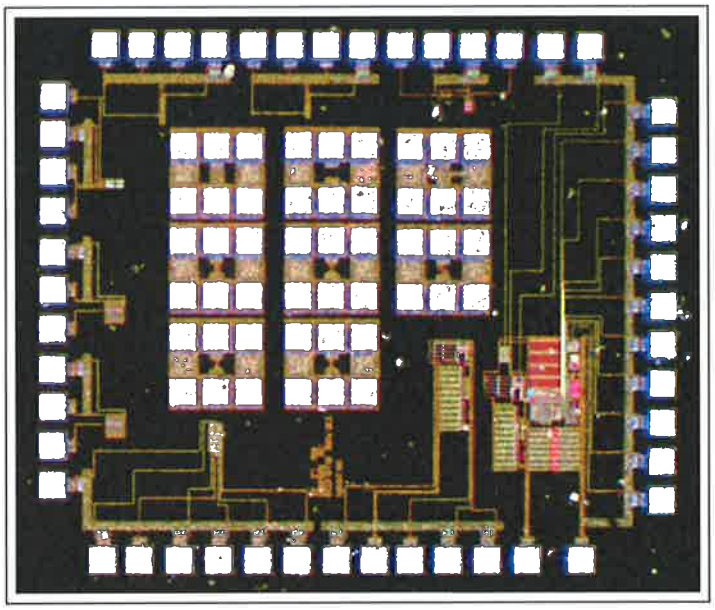


Figure 4.19: Photomicrograph of the test chip.

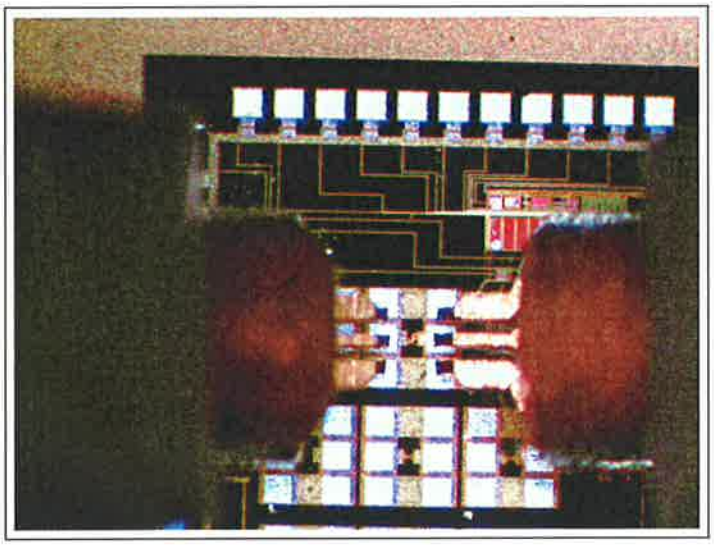


Figure 4.20: Photograph showing microwave probes during the testing of SBD diodes.

4.4 AC Characteristics

The high frequency behavior of a semiconductor diode can be modeled by its space-charge capacitance and diffusion capacitance. The space-charge or junction capacitance due to the dipole in the transition region and the charge storage capacitance or diffusion capacitance arising from the lagging behind of voltage as current changes, due to charge storage effect. Both of these capacitances are important and they must be considered when designing a diode for use with a time varying signal. The junction capacitance is dominant under reverse bias conditions. The diffusion capacitance is dominant at forward bias, and that is what determines the diode's charge storage time delay. The space-charge capacitance can be measured using an LCR meter. The diffusion capacitance can be measured using a Network-Analyzer [75].

No measurements of AC characteristics were performed on packaged chips. As it is known that packaging parasitic elements preclude the obtaining of good results for the AC characteristics of the actual diodes, all the reports and measurements were made on the wafer with appropriate RF probes.

4.4.1 Junction Capacitance

In this section we cover measurement and modeling of space-charge capacitance. The parameters we need to extract are C_{j0}, V_j and m. The behavior of a space charge capacitor is given by:

$$C_s = \frac{C_{j0}}{(1 - \frac{V_D}{V_j})^m} \tag{4.24}$$

A more detailed equation is given below:

$$C_s = \frac{C_{j0}}{(1-F_c)^{(1+m)}} * [1 - F_c * (1+m) + m * \frac{V_D}{V_j}] \tag{4.25}$$

Where C_{j0} is the space charge capacitance at zero volts, V_j is the built in potential, m is the junction exponential factor, which determines the slope of the C-V curve. For an abrupt junction it has a value of 1/2 and for linear graded junction it is 1/3. F_c is the forward capacitance switching coefficient and has a default value of 1/2.

We follow the same procedure as described for DC measurements, by converting Equation 4.24 to logarithmic form:

$$ln(C_s) = \ln(C_{j0}) - m * \ln(1 - \frac{V_D}{V_j}) \tag{4.26}$$

This equation can be interpreted as a linear function such that:

$$y = b + m * x \tag{4.27}$$

Where:

$$y = \ln(C_s) \tag{4.28}$$

$$b = \ln(C_{j0}) \tag{4.29}$$

$$m = m \tag{4.30}$$

$$x = \ln(1 - \frac{V_D}{V_j}) \tag{4.31}$$

The collected data for C_s and V_D were converted to logarithmic values according to Equation 4.28 and Equation 4.31 respectively. Since the parameter V_j has a physical meaning, it must be set to a range from 0.2 to 1 V. Therefore we select 0.2 V as a starting value for V_j. These two arrays of values are then introduced into a regression analysis program as y_i and x_i.

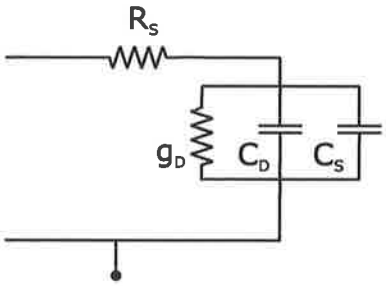


Figure 4.21: High Frequency Model of a Diode.

This regression analysis program is written in Matlab. For more information about this program please refer to Appendix B. A linear curve is fitted to this cloud of measured data. The value of the y-intercept b and the slope m for the actual value of V_j can now be retrieved. These two values are the best choice for the given V_j. Then this procedure was repeated with an incremented value for V_j. Each time we obtain different values of b and m, and the regression coefficient r^2 is different from earlier results as well. The regression line fitted better for some values of V_j. Eventually the best regression coefficient was found and the iteration loop was stopped. The final value for b, m are the optimum values corresponding to optimum V_j.

In practice there is always an overlay of this capacitance with parasitic capacitance due to packaging and bond pads. These parasitics needed to be de-embedded and eliminated from the measurements, otherwise we might have ended up with values that have no physical meaning. This is specially true for V_j and m.

Figure 4.21 shows the small signal equivalent circuit of the diode at high frequencies. The ideal diode in this figure has been replaced by a small signal conductance g_D, where g_D is in fact, the slope to DC diode characteristics at the operating point.

For this section there were two choices of measuring equipments that can

Table 4.2: Prototyped Schottky Diodes C_j Measurement Results

No	Size μm	V_j(V)	C_j(fF)	Description
sbd1_iv.txt	0.48×0.48	0.484	10	Minimum size rectangular
sbd2_iv.txt	0.48×0.48	0.485	13	Minimum size circular
sbd3_iv.txt	0.48×3.12	0.561	900	Long junction, rectangular
sbd3_iv.txt	0.48×5.60	0.626	850	Long junction, 6 fingers
sbd3_iv.txt	0.48×30.00	0.612	890	Extra Long junction

be used. An LCR meter or a Vector Network Analyzer (VNA) with ability to apply DC bias to a device. Since there was no appropriate LCR meter at our disposal, we chose the harder method which was using a VNA. An HP 8510C VNA was set up with an HP 8515A s-Parameter Test Set. A step mode frequency sweep was performed with an IF averaging of 64. All test interfaces were 3.5 mm coaxial. After calibration, the VNA internal settings were stored on disk for further processing.

As for calibration, the system was LRM calibrated using the method explained in Section 4.3. The measured values of C_s and V_d, were collected and used to calculate the diode parameters as explained in aforementioned text. The results of the measurements are tabulated in Table 4.2:

Another method that can be used [38] to determine a junction built in potential is as following. From Chapter 2, we have:

$$C = qN_d \frac{dx_n}{dV_R} = \left[\frac{q\epsilon_s N_d}{2(V_j + V_R)}\right]^{1/2} \tag{4.32}$$

where C is the capacitance per unit area. If we square the reciprocal of Equation 4.32, we obtain

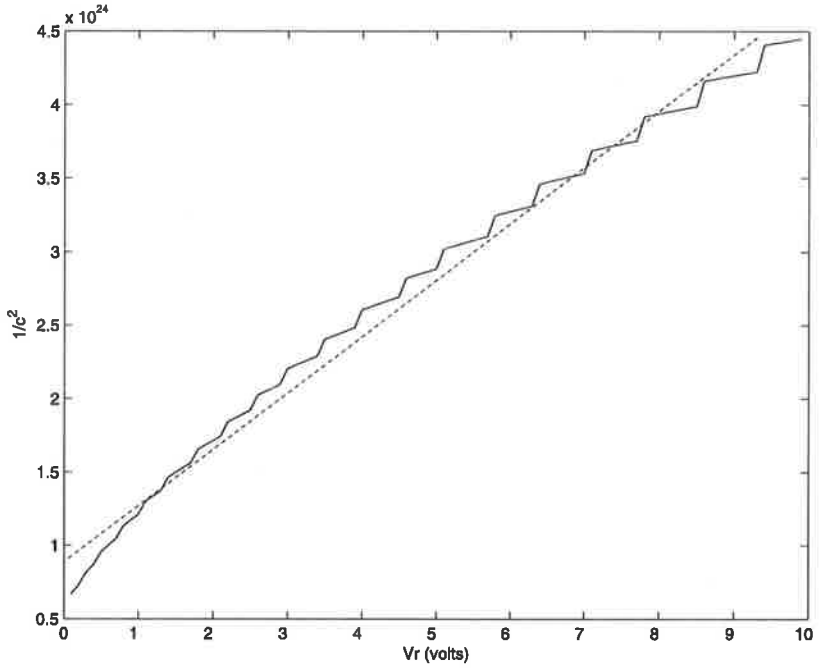


Figure 4.22: $1/C^2$ versus V_R for SBD4 Schottky Barrier Diode.

$$\left(\frac{1}{C}\right)^2 = \frac{2(V_j + V_R)}{q\epsilon_s N_d} \tag{4.33}$$

We can use Equation 4.33 to obtain, to a first approximation, the built in potential barrier V_j by finding the intercept of the curve on the y-axis. The slope of the curve from the Equation 4.33 also yields the semiconductor doping concentration N_d. We define the above slope as χ.

$$\chi = \frac{d(1/C^2)}{dV_R} \approx \frac{\delta(1/C^2)}{\delta V_R} = \frac{2}{q\epsilon_s N_d} \tag{4.34}$$

This value is in fact the slope of the aforementioned plot and can be obtained from the plot graphically, therefore:

$$N_d = \frac{2}{q\epsilon_s \chi} \tag{4.35}$$

$$\phi_n = \frac{kT}{q} ln\left(\frac{N_c}{N_d}\right) \tag{4.36}$$

$$\phi_{Bn} = V_j + \phi_n \tag{4.37}$$

and that gives us the value of ϕ_{Bn} or barrier height.

4.4.2 Diffusion Capacitance

Junction capacitance, dominates the reactance of a diode under reverse bias conditions. In forward bias conditions, however, the charge-storage capacitance C_s, becomes dominant. This in fact is the most important factor in signal rectification as it can be a serious limitation for forward performance of a diode in switching applications. To calculate the capacitance due to charge storage effects, let us assume that our diode has a junction of type p^+n and it is forward biased with a steady current I, then

$$C_s = \frac{dQ_p}{dV} \tag{4.38}$$

Where:

$$Q_p = I\tau_p \tag{4.39}$$

$$= qA\Delta p_n L_p \tag{4.40}$$

$$= qAL_p p_n e^{qV/kT} \tag{4.41}$$

The capacitance due to small changes in this stored charge is

$$C_s = \frac{q^2}{kT} AL_p p_n e^{qV/kT} \tag{4.42}$$

$$= \frac{q}{kT} I\tau_p \tag{4.43}$$

Similarly we can determine the AC conductance by allowing small changes in the current:

$$g_D = \frac{dI_D}{dV_D} \tag{4.44}$$

$$= \frac{qAL_p p_n}{\tau_p} \frac{d}{dV}(e^{qV/kT}) \tag{4.45}$$

$$= \frac{q}{kT} I \tag{4.46}$$

Thus the AC conductance of current is

$$i(t) = G_s v(t) + C_s \frac{dv(t)}{dt} \tag{4.47}$$

Therefore:

$$C_s = G_s \tau_p \tag{4.48}$$

Now, we can generalize the above equation and write it in a form that includes both holes and electrons current in the diode, as

$$g_D = \frac{dI_D}{dV_D} \tag{4.49}$$

$$= \frac{I_s}{NV_T}(\exp \frac{V_D}{NV_T} - 1) \tag{4.50}$$

For simplicity the term -1 in the above equation can be ignored. The value of C_s was measured using a network analyzer. This was a one-port (reflection) measurement. It gave the S_{11} curve. The value of C_D measured using this method is the sum of the diffusion capacitance and the junction capacitance, the reason being that the diode is biased at zero volts by default. In order to measure the diffusion capacitance only, we needed to apply some bias to the network analyzer instrument. That was achieved by connecting a DC supply to the back of the network analyzer. The auxiliary applied bias was varied from -3 to +1 volts.

For parameter extraction of charge storage lifetime, τ, we interpret the S_{11} curve as the diode impedance:

$$s_{11} = \frac{r - 50}{r + 50} \tag{4.51}$$

therefore:

$$r = 50 * \frac{1 + s_{11}}{1 - s_{11}} \tag{4.52}$$

As we configure the circuit such that the diode is working in forward bias, C_j can be neglected in comparison with C_s. Therefore:

$$r = R_s + \frac{1}{g_D + j2\pi f C_D} \tag{4.53}$$

The above equation can be solved for C_D. The S_{11} curve was obtained using a network analyzer. The curve looked like a circle for low frequencies but it deviated for higher frequencies, the reason being parasitics, such as bond wires, packaging, etc. The complex r was calculated using Equation 4.52. From there using the following equation we managed to get the internal complex conductivity of the diode.

$$g = \frac{1}{r - R_S} = g_D + j2\pi f C_D \tag{4.54}$$

Where C_D can be calculated using its imaginary part:

$$C_D = \frac{\Im g}{2\pi f} \tag{4.55}$$

And finally the value of τ can be calculated by

$$\tau = C_D / g_D \tag{4.56}$$

The final value of τ was obtained using the regression analysis technique. This required using a range of data points rather than a single data point. Doing that we ended up with an array of $\tau(f)$. We plotted this array against the frequency f and fitted a line to the range where the plotted τ array was linear. The mean of the y-value of this linear region gives the value of the parameter of τ.

A diode does show recombination effects at low forward bias voltages. This shows up as a lower slope on a semi-log scale plot. In order to cover this effect, the diode model is replaced by a sub-circuit, consisting of a diode for the recombination effect and another diode in parallel to the first one for the upper voltage area and a resistance in series with both diodes.

No measurements or further discussion of Diffusion capacitance are made because it is not a relevant parameter for the performance of a Schottky Barrier diode, where majority carriers form the conduction mechanism.

4.4.3 Reverse Recovery Time

Reverse Recovery Time, T_{rr}, is the transition from conduction to open circuit when the bias is reversed. Figure 4.23 shows what happens when the diode bias is switched from forward to reverse. At the switch time, the current reverses and stays at a constant level for a period of time called the storage time (t_s). During this time the diode acts essentially as a short circuit. Then the current decreases to the reverse leakage current value. This latter time is called the transition time. The sum of the storage and transition times is the reverse recovery time. This delay time is an important figure of merit for evaluating diodes for switching applications. It is usually desirable that the T_{rr} be small compared with switching times required. The critical parameter determining T_{rr} is the carrier lifetime (τ_p for example for p^+n junction). Since the recombination rate determines the speed with which excess holes can disappear from the n region. In fact the exact analysis of the problem of Figure 4.23 leads to the result:

$$T_{rr} = \tau_p[erf^-1(\frac{I_f}{I_f + I_r})]^2 \tag{4.57}$$

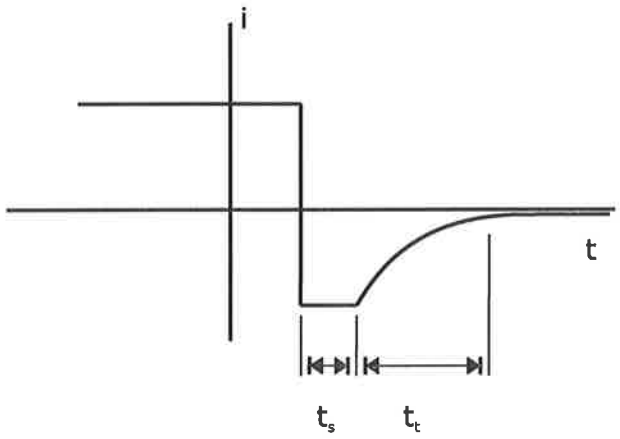


Figure 4.23: Illustration of the Reverse Recovery Time for a Diode.

4.5 Efficiency

Power Conversion Efficiency (PCE), can be used as a performance index of rectifier circuits. It is defined as:

$$\eta = P_{out}/P_{in} \tag{4.58}$$

where, P_{out} is the DC output power and P_{in} is the input RF power. The power dissipation in a rectifier needs to be considered in the different modes of operation. During the negative cycle of the input signal, the rectifier is in its blocking state. The losses in the blocking state can be expressed as

$$P_R = I_R \times V_R \times D \tag{4.59}$$

where I_R is the reverse leakage current in the diode, V_R is the reverse voltage across the diode, and D is the duty cycle. During the positive portion of the input signal, the diode turns on and the energy is transferred to the output. The diode now starts conducting and the power dissipated in the diode is

$$P_F = I_F \times V_F \times (1 - D) \tag{4.60}$$

where I_F is the forward current in the diode and V_F is the forward voltage drop across the diode. At the end of this cycle the diode turns off and enters the blocking state. The power dissipation during the transition from the conduction to the blocking state is given by

$$P_{rec} = V_{RRM} \times I_{RRM} 0.5 f t_b \tag{4.61}$$

Where I_{RRM} is the peak reverse recovery current, V_{RRM} is the peak reverse voltage, and f is the switching frequency. Figure 4.24 shows the circuit diagram of the test circuit used for simulation.

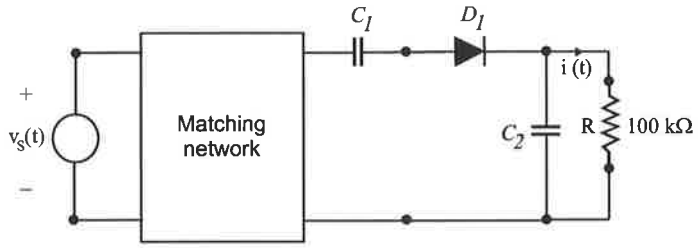


Figure 4.24: Test circuit to measure PCM for Schottky diode.

In order to simplify the simulation procedure and save time in computation, the matching network and resonant circuit are omitted. Star-HSPICE was used to run the simulations. For power calculations, Star-HSPICE computes dissipated or stored power in each passive element (R, L, C), and source (V, I, G, E, F, and H) by multiplying the voltage across an element and its corresponding branch current. However, for semiconductor devices, Star-HSPICE calculates only the dissipated power. The power stored in the device junction or parasitic capacitances is excluded from the device power computation. Equations for calculating the power dissipated in a diode is shown in the following;

$$P_d = V_{pp} \cdot (I_d + I_{cap}) + V_{pn} \cdot I_d \tag{4.62}$$

where

P_d is the power dissipated in diode.

I_d is the DC component of the diode current.

I_{cap} is the capacitive component of the diode current.

V_{pn} is the voltage across the junction.

V_{pp} is the voltage across the series resistance RS.

The keyword `measure power` can be used in a SPICE file to trigger power computation by HSPICE. This keyword has other optional switches such as average, RMS, min and max. The average (AVE), RMS, MIN, MAX, and peak-to-peak (PP) measurement modes report functions of the output variable rather than the analysis value. Average calculates the area under the output variable divided by the periods of interest. RMS takes the square root of the area under the output variable square divided by the period of interest. MIN reports the minimum value of the output function over the specified interval. MAX reports the maximum value of the output function over the specified interval. PP (peak-to-peak) reports the maximum value minus the minimum value over the specified interval. Integral provides the integral of an output variable over a specified period.

During the first phase of this work, simulation tools were used to calculate the PCE of different rectifier structures. This work has been documented and formated into a workshop paper titled "Brief comparison of different rectifier structures" [32]. In the next stage when SBD chips were fabricated, practical measurements were conducted on them to compare the results with the simulations.

It was concluded that the PCM of a diode depends on the operating frequency, the load and the input voltage level. At low frequencies such as the HF region, it is more economical to build the rectifier from NMOS and PMOS gate cross-connected bridge. At UHF, Schottky diodes are more efficient. At the input voltage level of 2V, the PCM reaches 20% efficiency.

4.5.1 Summary

After the diodes had been fabricated, a number of different test measurements were carried out on the wafers to characterize the SBD diodes. The first measurements were to characterize the DC parameters. After being satisfied with the results, the next step was to determine the AC or microwave parameters. High frequency parameter extraction was improved by using GSG pads. Details of these measurements are covered thoroughly in this chapter. The lack of detail for results of experiments performed on packaged samples resulted from the fact that they are known to give results that have unpredictable errors.

It was found from the analysis of the results that this type of diode has low junction capacitance and performs quite well at UHF. The series resistance is high, but it can be reduced by using a multi-finger configuration. Although multi-finger configuration increases the diode capacitance, it still satisfies the operational needs at UHF.

For each diode several different experimental methods were used and the results were compared. At the final stage the extracted parameters were substituted into the diode equation and a SPICE simulation was used to confirm the derivations. Where the product of diode's series resistance and its junction capacitance is a relevant performance parameter, the multi-finger configuration gives the best results.

4.6 Conclusion

For a diode modeling, the measurement of the DC performance with respect to its input and output characteristics as well as its transfer function was done first, followed by the so-called C-V modeling, i.e. the characterization

of the depletion capacitance at high frequencies. Finally, the s-parameters of the diode as well as of the dummy devices (contact pad capacitances and inductances) are measured. The dummy devices consist of an OPEN dummy (representing the contact pads and the open connection lines to the device-under-test [i.e. everything except the device]), a SHORT (the device is replaced by a metal plane, thus shorting both ports to ground at the location of the device), and a THRU (the device is replaced by a strip-line between port1 and port2 of the network analyzer).

After the de-embedding process has been verified (by modeling the THRU dummy device for example), the s-parameters of the inner device-under-test are de-embedded (OPEN and SHORT dummy de-embedding) and the device modeling can be applied.

The model parameters are then extracted and fine-tuned for each sketched step bottom-up. For the DC case, it is the non-linear model parameters, for the CV the junction capacitance parameters and for the s-parameters the transit time, and also the parasitics which are only visible at UHF.

By critically evaluating the capabilities and requirements of Schottky diode performance, it was concluded that a functional Schottky diode implemented using standard CMOS processes was possible. This implementation is not as efficient and robust as a state-of-the-art discreet Schottky diode, but it is less costly by eliminating the special fabrication processing steps required. It also decreases the total time to manufacture the system.

Chapter 5

Improving the SBD's Characteristics

In this chapter recent improvements in SBD design are presented. Previous work had shown (in Section 4.2.3) that the designed SBD had some shortcoming in its breakdown voltage. To overcome this limiting factor, a set of design procedures based on a Junction Barrier Schottky diode is extended to this work. An increase in breakdown voltage is demonstrated through simulations. Several other advantages over existing design are also presented and analyzed.

5.1 Introduction

The most important parameters when quantifying a rectifier diode are forward voltage drop (V_f), on-resistance in the drift region (R_s), which accommodates the specified blocking voltage, reverse breakdown or blocking voltage (V_b) and the junction capacitance (C_j). All of these parameters are of substantial importance and must be taken into account seriously.

So far two chips have been fabricated and tested. Although the results were satisfactory, it still is possible to make further improvements to the design. This chapter is devoted to the analysis of the extent to which these parameters (within the context of the overall physical possibility) can be improved. So we start by studying each of these characteristic parameters even more thoroughly and try to optimize them to the highest level possible.

For a rectifier, the static on-state losses can be expressed in term of V_f and R_s. The barrier voltage for Schottky diode is lower compared with pn junction diode, since it is determined by the metal-semiconductor barrier height instead of p^+n junction barrier. The pn junction diode's on-resistance is a function of blocking voltage, current density and carrier lifetime in the base, while for Schottky diode it is a linear function of forward voltage drop. On the other hand, the on resistance is lower for pn junction diode since its forward current is conductively modulated.

For the total diode resistance, the contact resistance and substrate resistance must also be accounted for. CMOS Silicon wafers (substrates) are normally 300 μm thick and have a sheet resistance of about 100 mΩ/sq. The sheet resistance for n-well, however, is in order of 500 to 1 kΩ/sq [45]. They would contribute substantially to the overall voltage drop.

5.2 Breakdown Voltage

The reverse breakdown voltage of a Schottky barrier diode fabricated using the technique mentioned in this dissertation is lower than that of a p^+n junction diode with the same n-well doping level. This is due to high electrostatic field at the edge of the metal-semiconductor contact and it is similar to the curvature effect in a pn junctions. This phenomenon is depicted in Figure 5.1.

The high electrostatic field at the periphery, which causes this premature breakdown voltage, can be removed by extending the metal layer over the thin oxide surrounding the contact, as illustrated in Figure 5.2. This also extends the reverse breakdown voltage by increasing the length of the depletion region and lowering the high electrostatic fringing field. For this to have any effects, the oxide should be thin, about 90 nm. This method is a viable solution which needs further study and consideration.

Another method for increasing the breakdown voltage of the Schottky barrier diode is to use a mesa structure. This method does not increase the capacitance of the structure and is compatible with planar technology, but not with the standard CMOS process. The mesa is required to be surrounded by thermally grown oxide on all sides. This reduces the peripheral fringing field, resulting in a higher breakdown voltage. The structure of a mesa Schottky barrier diode is shown in Figure 5.3. This method would be the optimum method to make Schottky barrier diodes, but unfortunately is not compatible with the standard CMOS process, as it calls for extra etching steps which are not available under the standard CMOS fabrication process.

Yet, another method that can be used to increase the breakdown voltage is using a p^+ guard ring surrounding the metal contact, as shown in Figure 5.4. This method introduces a p^+n junction in parallel with the Schottky barrier

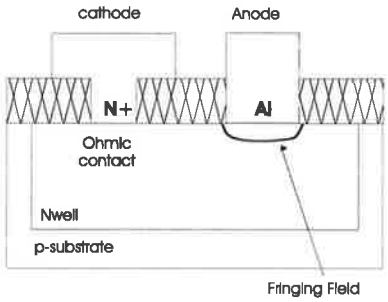


Figure 5.1: High electrostatic field at the periphery.

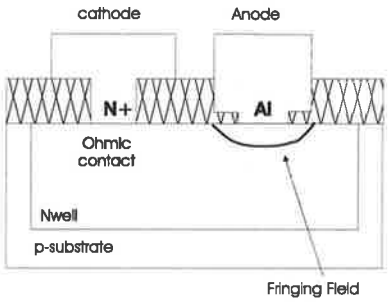


Figure 5.2: Cross-sectional view of Schottky Barrier Diode With Extended metal overlap.

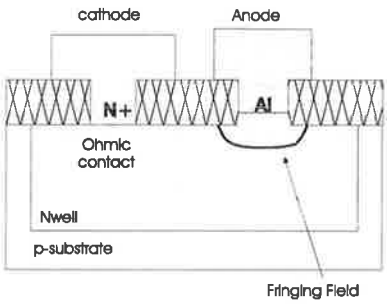


Figure 5.3: With mesa junction structure.

Reverse breakdown voltage of Schottky diode.

contact, resulting in an increase in total junction capacitance of the diode. The combined structure has a higher breakdown voltage but at the cost of reducing its switching speed. However, this method can be implemented in CMOS and it is a viable design to consider.

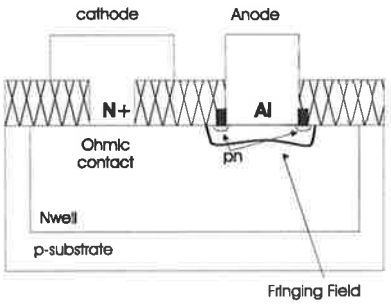


Figure 5.4: With p^+ guard ring.

5.3 SBD with p^+ guard-ring

A performance comparison of the three structures mentioned in the previous section was carried out. The results indicate that the SBD with p^+ guard-ring (hereinafter referred to as Junction Barrier Schottky diode, JBSD) has the most attractive properties. Thus, in this section we will do more analysis of its characteristics and performance.

5.3.1 Drift region resistance of JBSD

The drift region resistance,R_s, of the JBSD, if we neglect the contact and the substrate resistances for now, is determined by the n-well layer thickness (t_n), doping concentration (N_d) and electron mobility (μ_n) according to Equation 5.14. This in fact is derived from Equation A.6.

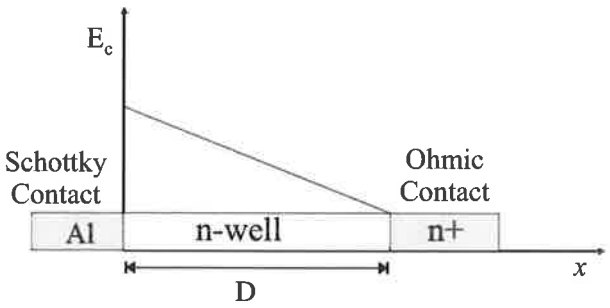


Figure 5.5: Electric field distribution for a JBSD junction, where D is the depletion width and E_c is the electric field strength.

$$R_s = \frac{t_n}{q\mu_n N_d} \tag{5.1}$$

where q is the electron charge. In an ideal non-punch through structure, the depletion width t_n, is equal to the physical distance, D, between the ohmic and Schottky contacts, at the diode's breakdown voltage. From Equation A.18, the reverse bias breakdown voltage is given by:

$$D = \sqrt{\frac{2\epsilon_s V_b}{qN_d}} \tag{5.2}$$

By re-arranging the above equation, the reverse bias voltage as a function of junction width can be expressed as:

$$V_b = \frac{qN_d D^2}{2\epsilon_s} \tag{5.3}$$

where, ϵ_s, is the permittivity of the depletion layer material.

Therefore the depletion width, D, at the breakdown voltage can be expressed in terms of the critical electric field at the junction and doping concentration as in Equation 5.5. A simple electrostatic field distribution for a

JBSD junction is shown in Figure 5.5.

$$D = \frac{\epsilon_s E_c}{qN_d} \tag{5.4}$$

$$= \frac{2V_b}{E_c} \tag{5.5}$$

the critical electric field E_c has a doping dependency according to Equation 5.6, which is experimentally determined by Konstantinov [67] for a particular process (in SI units).

$$E_c = \frac{2.49 \cdot 10^6}{1 - \frac{1}{4} log(\frac{N_d}{10^{22}})} \quad [\mathrm{V/m}] \tag{5.6}$$

Combining 5.4 and 5.5 gives the maximum blocking voltage for a given drift region doping as

$$V_b = \frac{\epsilon_s E_c^2}{2qN_d} \tag{5.7}$$

The drift region resistance in Equation 5.1 can be re-written in terms of Equation 5.4 and Equation 5.7 to obtain an expression in terms of the blocking voltage and critical electric field.

$$R_s = \frac{4V_b^2}{\epsilon_s \mu_n E_c^3} \tag{5.8}$$

This equation can be used as a figure of merit for rectifying diodes as it gives the on resistance of a JBSD for a particular blocking voltage. The on resistance of a Schottky diode, therefore, increases quadratically with blocking voltage. That is the reason why Schottky diodes have non-attractive on resistance for higher blocking voltages compared to pn junction diodes. It

also is important to note, that the electron mobility has a doping dependency and has to be taken into account when calculating the on-resistance as given by [62], for a particular process (in SI units):

$$\mu_n = \frac{97}{1 + (\frac{N_d}{1.945 \times 10^{23}})^{0.61}} \quad [m^2 V^{-1} s^{-1}] \tag{5.9}$$

5.3.2 Forward voltage drop

The forward voltage drop in JBSD is determined by thermionic emission theory [63]. The forward voltage drop is a function of temperature, Schottky barrier height and drift region resistance. The forward voltage drop V_f at a defined current density J_f is given by Equation 5.10[1].

$$V_f = \frac{nkT}{q} \ln\left(\frac{J_f}{A^* T^2}\right) + n\phi_B + R_s J_f \tag{5.10}$$

where

- n is the identity factor
- k is Boltzmann's constant
- q is the magnitude of electron charge
- T is the absolute temperature
- ϕ is the Schottky Barrier height
- J_f is the forward current density at V_f
- A^* is the Richardson's constant

During normal operation of JBSD, the forward current flows unipolar between the anode and cathode in channels between the p^+n junctions. Con-

[1]For more detailed description and derivation of the equations in this chapter please refer to appendix A.

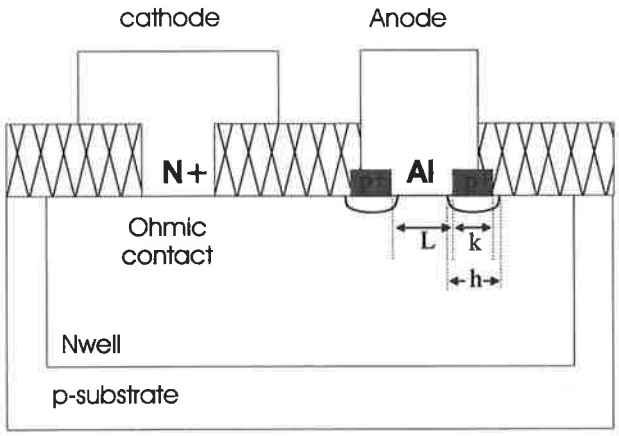


Figure 5.6: Showing the effects of p^+ guard-ring on the total voltage drop of JBSD.

sequently in normal operation conditions, the Schottky current dominates the overall forward current in the diode and the analysis can be based on thermionic emission theory of Schottky junction.

For the proposed JBSD, the relation between the forward voltage drop and current density is the same as given in Equation 5.10, however, the expression has to be modified to take into account the area taken up by the p^+ guard-ring structure, see Figure 5.6. The total current density over the metal contact J_{jsbd}, is therefore given by:

$$J_{jbsd} = \frac{\text{Schottky Contact Area}}{\text{Total Contact Area}} \cdot J_f \tag{5.11}$$

For the design proposed in Figure 5.6, Equation 5.11 can be written in terms of the p^+ grid spacing L, the grid width k and the junction depletion width from the p^+ regions, h:

$$J_{jsbd} = \frac{L - 2h}{L + k} \cdot J_f \tag{5.12}$$

Where, h can be calculated using Equation A.18. Therefore the area relation between the total area and the Schottky area is given by:

$$A_{jsbd} = \frac{L - 2h}{L + k} \cdot A_{total} \tag{5.13}$$

If a 45^o current spreading is assumed below the channel of the p^+ region, then the drift resistance, R_S, can be modified to take into account the effects of the guard-ring modulation. Also important to note that the electron mobility parallel to the c-axis is 20% higher than the mobility perpendicular to it [62]. A sufficiently good estimation for the analytical calculation can be made by assuming a 45^o current spreading. In that case, Equation 5.1 can be modified to accommodate the effects of guard ring as follows:

$$R_{s,jbsd} \simeq \frac{t_n - (x + k/2)}{q\mu_n N_d} \tag{5.14}$$

where x is the depth of the p^+ guard-ring. From there, the grid resistive contribution, R_g, from the channels and current spreading is given by:

$$R_g = \left(\frac{x + k/2}{q\mu_n N_d}\right)\left(\frac{L - 2h}{L + k}\right)\ln\left(\frac{L - 2h}{L + k}\right) \tag{5.15}$$

The total on-resistance of the diode is the sum of R_s and R_g:

$$R_{on} = R_{s,jbsd} + R_g \tag{5.16}$$

Now by modifying Equation 5.10 with Equation 5.12 and Equation 5.13 the forward voltage drop of the JBSD can be written as:

$$V_f = \frac{nkT}{q}\ln\left(\frac{L - 2h}{L + k} \cdot \frac{J_f}{A^* T^2}\right) + n\phi_B + R_{on}J_f \tag{5.17}$$

This equation can be used to calculate the forward voltage drop of JBSD diode at a given current density.

5.3.3 Temperature dependency

The on-resistance of doped silicon increases with temperature due to a decrease in mobility with increasing temperature as given for a particular process (in SI units) by the following equation [73];

$$\mu_n = \frac{97}{1 + (\frac{N_d}{1.945 \times 10^{23}})^{0.61}} \cdot (\frac{T}{300})^{-2.15} \quad [cm^2 V^{-1} s^{-1}] \tag{5.18}$$

In comparison with pn junction diodes this dependence is a disadvantage with respect to losses since pn junction diodes show a negative temperature coefficient for on-resistance.

5.3.4 Cut-off frequency

To increase the cut-off frequency, it is necessary to examine the key factors limiting the high frequency region operation. At this stage we go one step further in simplifying the Schottky diode equivalent circuit. What we end up with is shown in Figure 5.7, where R_n is a combination of series resistance in n-well, the series resistance of the $n+$ region and the ohmic contacts. G_j, is the junction conductance, C_s and C_d are the space charge and diffusion capacitances. We can see that a Schottky diode obeys the same rules as a pn junction diode. The junction capacitance, series resistance and junction resistance are given by:

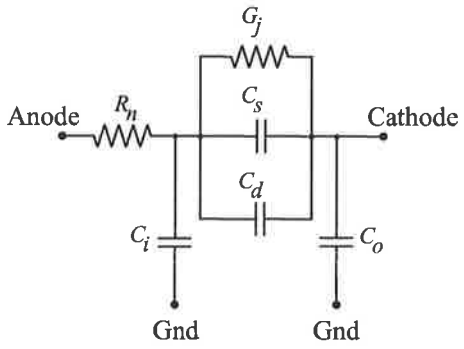


Figure 5.7: Small signal equivalent schematic of the JSBD for high frequency.

$$C_j = A\sqrt{\frac{\epsilon q N_d}{2(V_a + V_d)}} \tag{5.19}$$

$$\frac{1}{R_j} = \frac{dI_x}{dV_a} = AI_s\frac{q}{nkT}e^{\frac{qV_a}{nkT}} \tag{5.20}$$

$$R_s = R_n + R_{n+} = R_0/A + R_1/\sqrt{A} \tag{5.21}$$

where A is the area of the diode, N_d is the doping concentration, V_a is the applied voltage and V_d is the built in voltage. The series resistance includes the spreading resistance, which is due to the geometry and is proportional to $1/\sqrt{A}$ as has been discussed in chapter 2. From the above equations the cut-off frequency is given by:

$$f_c = \frac{1}{2\pi(R_s C_j)} \tag{5.22}$$

Therefore the frequency response of a Schottky diode is proportional to $1/\sqrt{A}$. Thus to get a good high frequency response it is necessary to decrease the contact area and the resistance in the lightly doped n-well. One way to reduce the resistance of the n-layer is to use silicon molecular epitaxy (Si-MBE) [72]. This process has been shown to reduce the n layer thickness to

$0.3\mu m$, which is very close to the depletion length of the Schottky diode. However, this process can not be done in the standard CMOS process, thus our only choice is to manipulate the geometry of the Schottky diode contact.

Chapter 6

UHF Rectifier based on SBD

A new organization of switched-capacitor charge pump circuits based on Dickson's voltage doubler structure is presented in this chapter. A charge pump takes a DC input voltage and outputs a doubled DC voltage. A simulator working in the QV realm was used for simplified circuit simulations and to estimate the number of charge pump stages required to achieve the desired voltage. In order to evaluate the efficiency and delivered power of the charge pump, a resistive load was attached to the circuit's output. A comparison of the proposed circuit with the current technology is presented in terms of the input threshold voltage, area requirements, voltage gain, and the output power level. The simulation results indicate that there is an optimum load for different charge pump configurations. Finally, design guidelines for the desired voltage and power levels are discussed.

6.1 Introduction

In contact-less RFID context, the DC power supply voltage is generated from the incident RF signal power by the means of a voltage rectifier. At HF ISM band, 13.56 MHz, it is more common to use diode connected transistors or a MOSFET bridge rectifier. The most common structure of the bridge rectifier consists of two nMOS and two pMOS FETs [88]. The output voltage of such a circuit, however, suffers from the voltage drop across the transistors because of the MOSFETs' threshold voltage. Therefore further away from the interrogator antenna, where the RF signal is weaker, this kind of rectifier might fail to operate properly.

Therefore, there is a need for a device that can operate from a lower input voltage level. The Schottky diodes developed in this dissertation satisfy these conditions. The voltage drop of a SBD is approximately 200 mV, at 10 μA, as was confirmed by experimental work. A new organization of these diodes can be used to deliver a high voltage to the chip from the weak input RF signal.

Although voltage multiplier circuits are widely used in CMOS, the description of the kind of circuit presented in this chapter has only been restricted to operating principles and a thorough and systematic treatment has not been presented. In this chapter, the voltage doubler realized with SBDs is thoroughly analyzed and a complete model is proposed. Its degradation features and its implication on tag circuitry endurance are studied and experimental results supporting the proposed method are presented.

6.2 Comparison of different rectifier structures

RFID designers, traditionally use MOS bridge rectifiers, as shown in Figure 6.1 [88]. Although these structures are well suited for low frequency, they perform inadequately at UHF. It worth mentioning that with advancement in CMOS circuits and availability of new submicron transistor feature sizes, it still is possible to build a UHF rectifier from MOSFETs. However, the turn-on threshold voltage of such a configuration is normally much higher ($\approx$ 300 mV) than that of a Schottky diode rectifier structure. Plots in Figure 6.2 shows a comparison of a Schottky diode rectifier with a MOS bridge configuration. As it is evident from the plot, the MOS bridge rectifier has a sluggish response to the input signal. The MOSFET models used for this simulation are derived from AMI submicron fabrication with feature size of 0.35 μm.

For a more comprehensive study of different rectifier topology please refer to the paper presented by the author *et al.* [78] at the Auto-ID workshop.

6.3 Voltage Doublers

A voltage doubler, also referred to as a charge-pump in the context of memory ICs, provides a voltage that is higher than the voltage of the power supply. In many applications such as EEPROMs, flash memory, filters, switched-capacitor transformers, etc, voltages higher than the power supplies are frequently required. The increased voltage levels in a charge pump are the result of transferring charge to a capacitive load. Its ability to provide voltage amplification makes it suitable as rectifier structure of tags' power supply

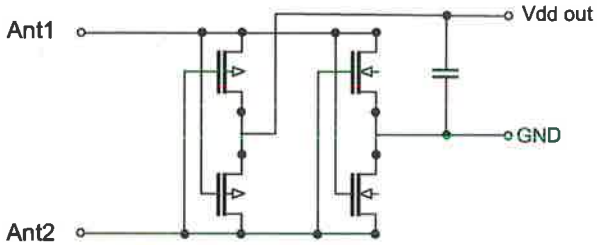


Figure 6.1: MOS bridge rectifyer network.

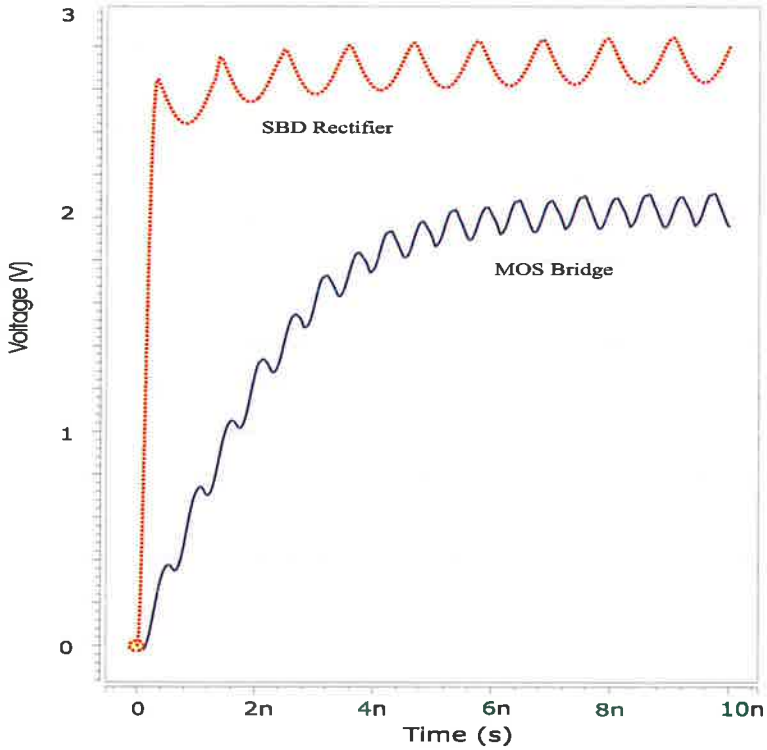


Figure 6.2: Comparison of the response time of a SBD diode with a MOS bridge rectifier cirucit.

circuitry, where the normal range of operating voltage is limited.

Charge pumps operate by switching on and off a large number of MOSFET switches which charge and discharge a large number of capacitances, transferring energy to the output load. A large amount of energy is lost whenever the load current is changed. For example, where there is no load, the circuit still operates but with 0% efficiency. Savings of switching energy can be achieved by regulating the switching frequency whenever a requirement for the load current changes. In addition, simulation and measurement results indicated a strong dependence of the output voltage on the load resistance [86].

In practical implementations, a number of issues related to parasitic capacitances, leakage resistances and the operating frequencies have to be considered. Power loss in a charge pump must be minimized both to protect the integrated circuit from overheating and to improve the power conversion efficiency. Most of the resistive power loss results from current through the diode. Dynamic power loss occurs as a result of switching charge pump capacitors. Diodes with a large junction area have smaller series resistance, minimizing the resistive power loss. This, however, results in larger junction capacitance that increases dynamic power loss and also limits the operating frequency of the charge pump.

6.3.1 Current techniques in CMOS

In Figure 6.3(a), a charge-pump circuit that uses diodes as the charge transfer device is shown. It is based on the Dickson's design. The output voltage of a diode charge pump is given by [80]:

$$V_{out} = (V_{dd} - V_t) \times N \tag{6.1}$$

where V_t is voltage drop in the diode and N is the number of stages. The term $(V_{dd} - V_t)$, may be called the voltage gain per unit stage and its output voltage linearly increases as the number of stage increases. Because forming independent diodes in the same substrate is very unwieldy and the voltage drop across the diode is not scalable, the conventional charge pump proposed by Dickson [81] uses the diode-connected MOSFET as the charge transfer device in place of the diode.

In the Dickson charge-pump circuit as shown in Figure 6.3(b), as the voltage of each stage increases by the charge pumping, the threshold voltage of the diode-connected MOSFET increases due to the body effect. The voltage gain $V_{dd} - V_t$ decreases and the output voltage becomes lower than the value obtained by the diode charge pump. Therefore, the output voltage of the Dickson charge pump cannot be a linear function of the number of stages and its efficiency decreases as the number of stage increases.

Several attempts have been made to alleviate the loss problem in the Dickson's design [82], but they must use a very complex timing scheme or backward control which may have a risk of reverse current even with auxiliary MOSFETs [88]. Use of floating devices [83] to eliminate body effects has also been reported, but the resulting charge-pump may generate substrate current by floating the device.

Witters and Geroeseneken [85] provided a detailed analysis of a Dickson multiplier built in VLSI technology with diodes realized by nMOS transistors. They considered effects of threshold voltage and leakage current. Most of the charge pump applications require a two-phase clock. A high-efficiency charge pump can be constructed using cross-coupled voltage doubler consisting of

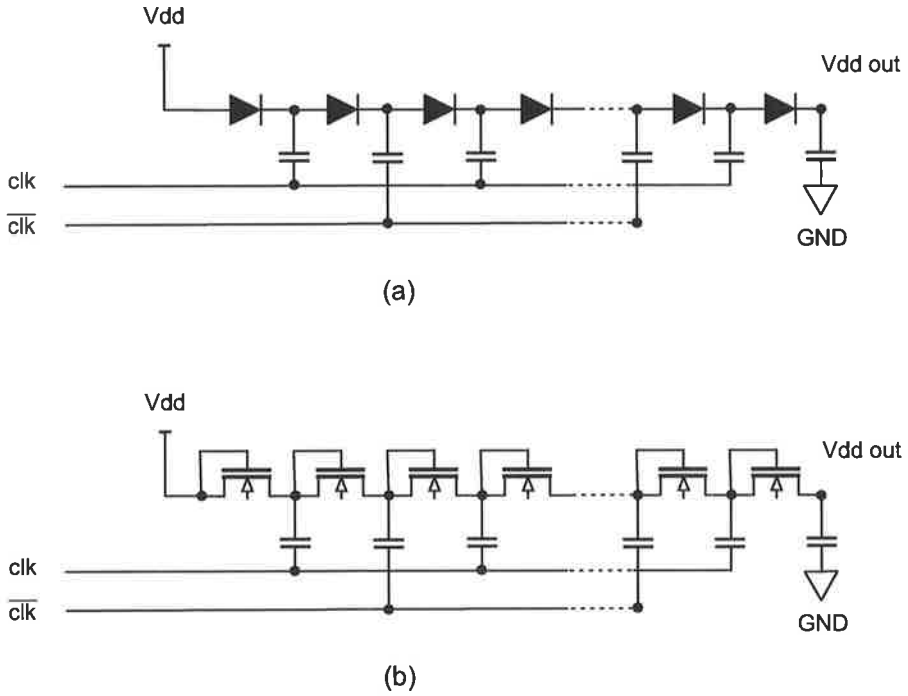


Figure 6.3: Functional Diagram of (a)diode and (b)Dickson charge-pump.

four power nMOS, four power pMOS [79]. But all of the above require auxiliary circuits or power transistors and capacitors that occupy a large area.

6.3.2 A New Approach

A bridge rectifier based on the SBD diodes cannot be used in a CMOS circuit, because when the input voltage swings to its negative value, it drives the cathode of the SBD diode into the negative region. That condition will make the n-well at lower voltage with respect to the p-substrate. In such a scenario, the parasitic diode D2, as shown in Figure 2.5, becomes forward biased, causing a large amount of current to flow from n-well to the substrate. This phenomena is similar in analogy to the latch-up condition of an inverter

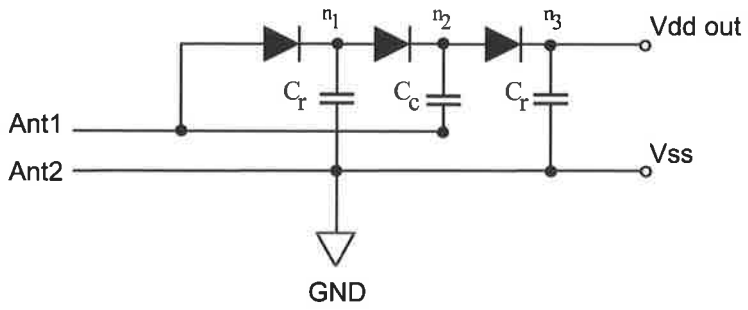


Figure 6.4: A new rectifier/multiplier topology using the SBD, based on Dickson's design.

in a CMOS circuit.

In Figure 6.4 a new approach based on Dickson's voltage multiplier design is proposed. In this circuit diodes are Silicon-Titanium Schottky diodes, developed in this dissertation. These SBD diodes have low series resistance of less than 500 Ω and low Schottky junction capacitance of approximately 500 fF. The schematic shown in Figure 6.4 is a simplified one and does not show the capacitances that anode and cathode of the SBD makes to the ground or substrate. However, these capacitances are included in the diode model for simulation. For this configuration to operate the antenna needs a DC connection through it.

These diodes are connected to the antenna pins by poly-poly capacitors. From RF point of view, assuming that the C_r and C_c have low impedance, the junction capacitance of these diodes are connected in parallel. For DC, however, they are connected in series to allow a DC current to flow from V_{dd} to V_{ss}.

For a short explanation of its operation assume that the Ant2 is connected to the ground and the Ant1 is connected to a sinusoidal voltage source of amplitude V_{in}, furthermore assume that the pump starts with all the capac-

itors depleted of any charge. In phase I, the voltage doubler starts by rising Ant1 from zero to $+V_{in}$. Capacitor C_r is charged to voltage $V_{in} - V_d$, where V_d is the voltage drop across the diode and C_c is assumed to have no charge. In phase II, the input voltage will swing to $-V_{in}$. The voltage across C_c is now $V_{in} + (V_{in} - 2V_d)$. Subsequently when the pump goes back to phase I, the voltage at node n_2 now rises to V_{in} plus the voltage access C_c and the charge stored by C_c is now shared with C_r at node n_3 and the final output voltage at node n_3 is equal to $2V_{in} - 3V_d$. Thus the charge sharing allows the output voltage to grow to a level higher than the input voltage.

In Figure 6.5 a multi-stage charge pump of the above configuration is depicted. A detailed analysis can be performed to show that the voltage generated at the output of this circuit to a good approximation is given by:

$$V_{dd} = (V_i - V_d) + nV_\Phi - (n+1)V_d - nV_l \tag{6.2}$$

where

- V_i is the RF input signal amplitude.
- V_d is the voltage drop across the diode.
- V_Φ is the voltage swing at a node due to capacitive coupling with the input signal.
- n is the number of stages.

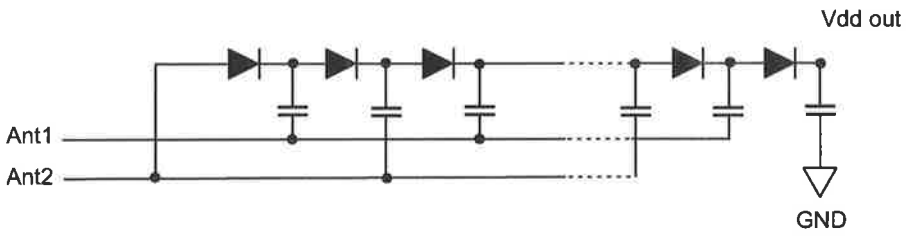


Figure 6.5: A multi-stage multiplier schematic based on the SBD.

V_l is the voltage drop due to the output current.

In the above equation, the voltage swing, V_Φ, can be calculated in terms of the reservoir capacitor, C_r, coupling capacitor C_c and parasitic capacitor (due to interconnect wires), C_s:

$$V_\Phi = V_i \left(\frac{C_r}{C_r + C_c + C_s} \right) \tag{6.3}$$

Figure 6.6 shows the output voltage of a two stage charge pump as the output current is increased. As can be observed from the plot, the voltage drop, V_l, is directly proportional to output current, I_o, and inversely proportional to operation frequency, f and the total node capacitances, $C_r+C_c+C_s$, therefore:

$$V_l \propto \frac{I_o}{f \cdot (C_r + C_c + C_s)} \tag{6.4}$$

This is only true assuming T $\ll$ RC, ie. the load time constant is much much less than the charging time constant.

Figure 6.7 shows the input-output relation of a single stage voltage multiplier circuit. It consists of three diodes and three capacitances. As expected, the output voltage is almost twice the input.

An n-stage cascade of the above design will produce almost $V_i \times n$ V output voltage. By choosing an appropriate number of stages, any voltage can be reached. However, this is only valid for negligible current draw. As soon as there is output current, there is also an AC current through the capacitors, resulting in a voltage drop and a lower input voltage for subsequent

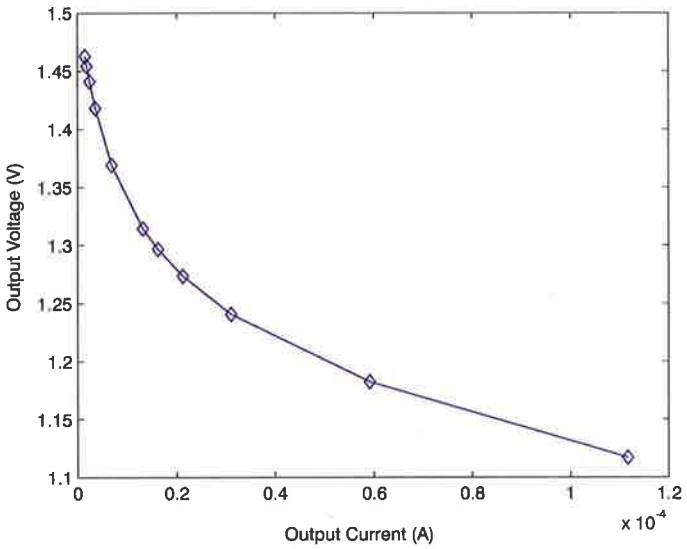


Figure 6.6: Plot of the output voltage as a function of the output current.

stages. In fact, numbers much higher than, say, 10 or 20, are not sensible in practice.

Plot of the empirical data shows that the output voltage drop, V_l, is a cubic function of the number of stages n. Using least-square curve fitting technique and statistical analysis, one can find the coefficients of a polynomial, $p(n)$, of degree 3, that fits the empirical data. In the above case Matlab was used to simplify this process. The Equation 6.4 can now be rewritten as:

$$V_l = \frac{I_o}{f(C_r + C_c + C_s)} \left(\frac{2}{3}n^3 + \frac{1}{2}n^2 - \frac{1}{6}n \right) \tag{6.5}$$

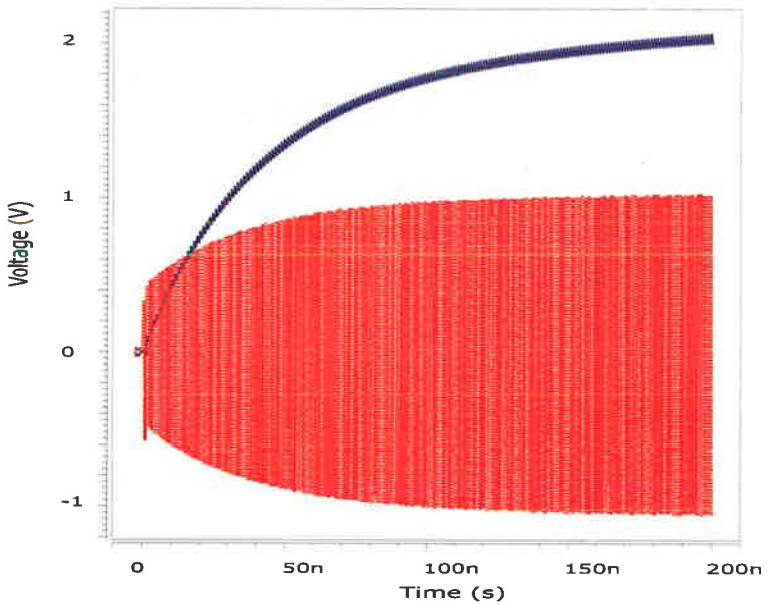


Figure 6.7: Plot of input and ouput of a single stage voltage multiplier cirucit.

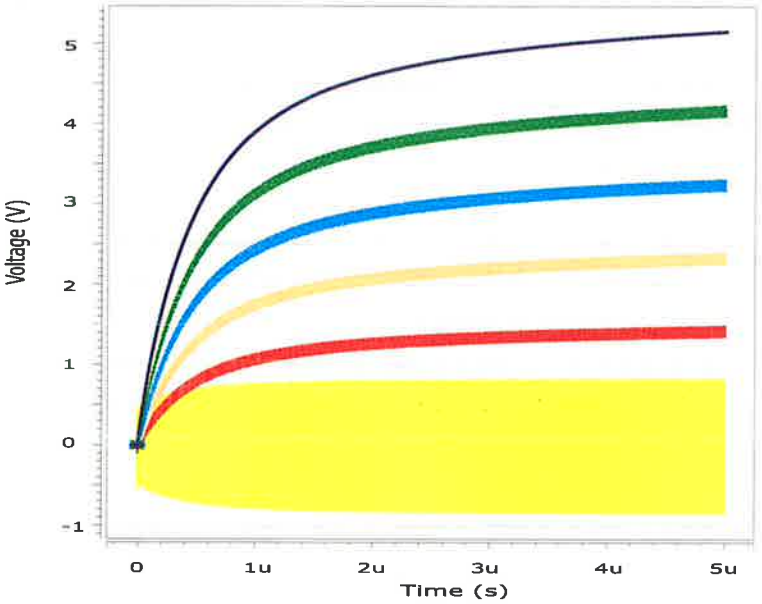


Figure 6.8: Plot of comparison of output voltage versus input from 1 to 5-stage case.

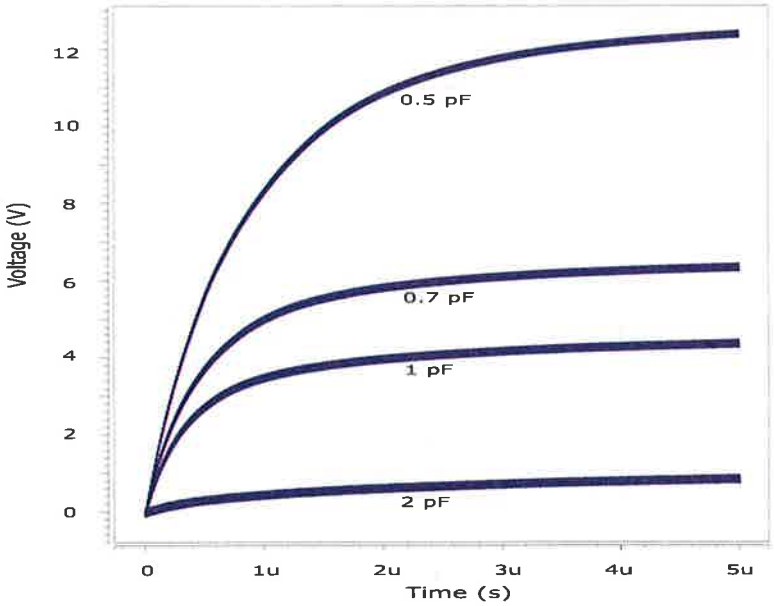


Figure 6.9: Plot of effects of junction capacitance on the output voltage.

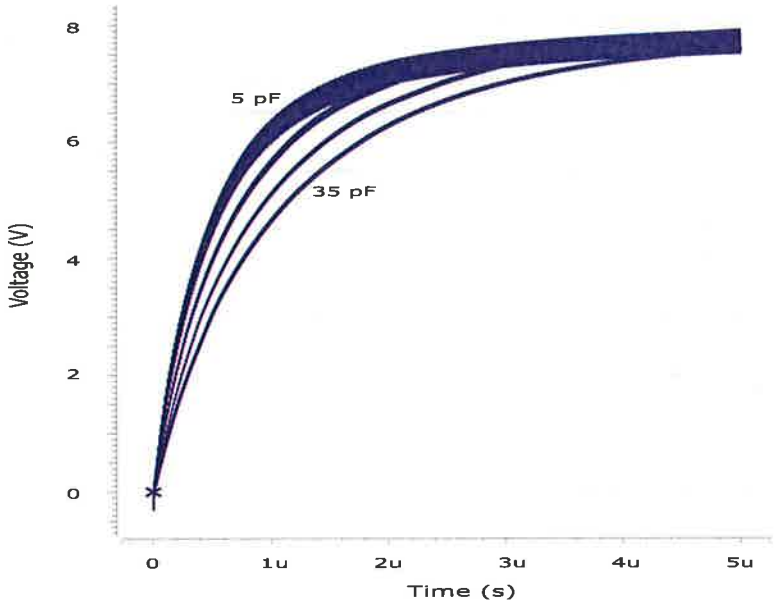


Figure 6.10: Plot of effects of C_c & C_r on the output voltage.

6.3.3 Optimization analysis

Effects of C_c & C_r on V_o

These capacitors work as a charge transfer device. They get charged during the negative cycle of the input and transfer their charge to the output during the positive cycle of the input RF signal. Therefore a small value would decrease the time required to transfer the charge from one stage to the next. A large value on the other hand, would increase the RC time constant and would act as a low pass filter to the input signal. Thus, they cannot have an arbitrary size. Figure 6.10 shows the effect of these capacitors on the output voltage of the charge pump.

For these capacitors, it is important to have small parasitic resistance, R_s and capacitance, C_{sub}. However C_{sub} is proportional to the desired capacitance C_c & C_s, because a capacitor value is proportional to its area. Since a certain amount of coupling is needed, the value of C_c & C_s cannot be made arbitrarily small and in fact neither can C_{sub}. The best way to minimize C_{sub} is to build the capacitors (lateral capacitors) formed by multi-finger top metal layer configuration or making use of the capacitance between the top two metal layers. To minimize R_s, large aspect ratio or multifinger capacitors can be used. Also, using top metal layer would minimize the amount of charge lost to the substrate.

The capacitors designed for this project were laid out using multi-finger configuration with the minimum distance allowed, according to the design rules, between the fingers. The value of these capacitors were chosen such that it would dominate the capacitance of the n-well to substrate, which has a value of almost 0.3 pF, acording to AMI process specifications.

6.3.4 Input impedance

The effectiveness of communication between the RFID reader and a tag can be increazed by maximizing the power transfer from the antenna to the rectifier structure. It can be shown mathematically that a source will deliver its maximum power to the load when the impedance of the load is a complex conjugate of the impedance of the source. This is achieved through impedance matching.

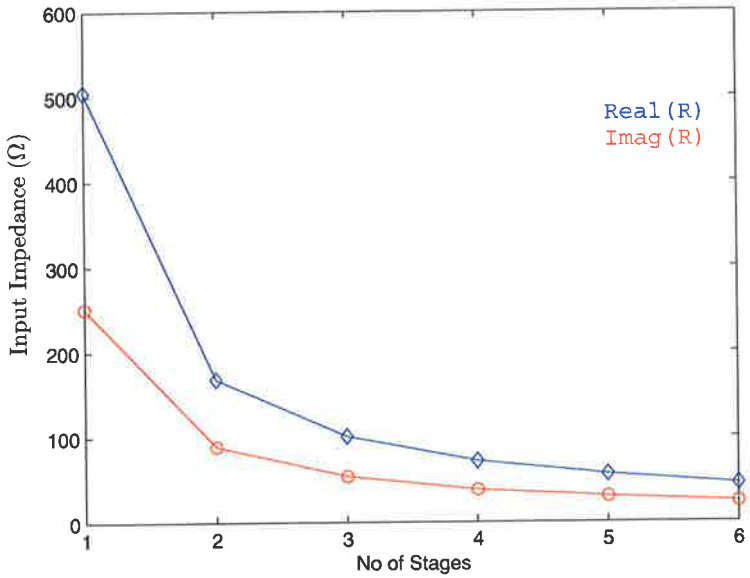


Figure 6.11: Plot of input impedance vs. number of stages.

The plot in Figure 6.11 shows the input impedance of the charge pump versus its number of stages. As it is evident from the plot, the higher the number of stages the lower the input impedance will be, therefore, in practice there is a limit to how far one can introduce more stages.

Table 6.1 shows the measurement results performed on two RFID chips from two different manufacturers. The Open port measurement was performed to help with the de-embedding of the results.

To have high efficiency, it is important to have diodes with small junction capacitance (Figure 6.9), large saturation current, I_s, resulting in low voltage drop, small series resistance, to minimize the loss in the diode and small parasitic capacitances to the substrate.

Large area SBDs have a larger saturation current, smaller series resistance, but also large junction and parasitic capacitances, which may dominate the power loss. Therefore, an optimum size of the SBD needs to be found.

6.4 Voltage regulator

A control method must be used to regulate the input voltage to the chip to achieve the desired operating conditions. The optimum performance of the converter is obtained through a compromise of achieving the correct output voltage and using as little power as possible. A linear technique can be used to control the output voltage. A bandgap based reference voltage can be compared to the output voltage and used to control the regulator feedback loop [84].

Figure 6.12 shows a shunt voltage regulator used in our RFID tag chip front-end. This circuit uses the ratio of the output voltage to a bandgap reference voltage to control the gate voltage of the load transistor M_7. This

Table 6.1: Measured chip impedance on May 26, 2005

Chip Manufacturer	**Input Impedance Ω**
Alien C1G2	$24 - j63.2\ \Omega$
TagSys 6408	$15 - j174\ \Omega$
OpenPort	$6 - j358\ \Omega$

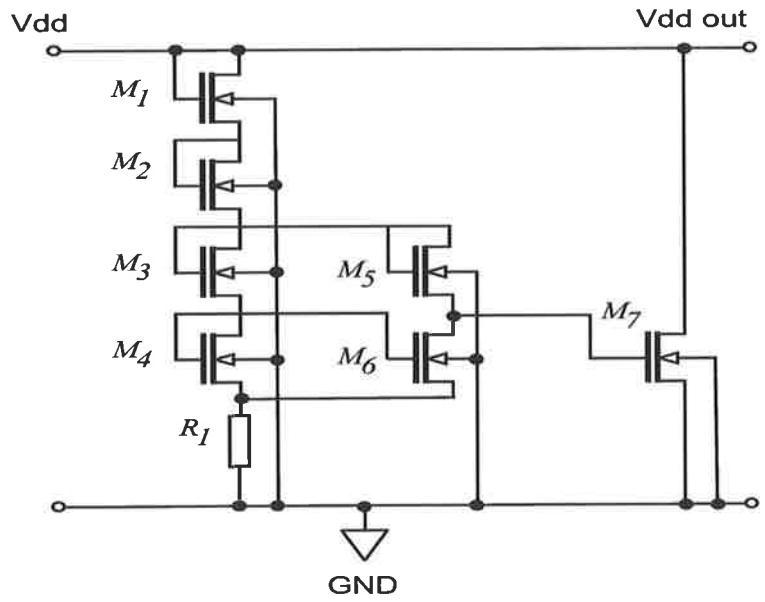


Figure 6.12: Circuit schematic of shunt regulator.

transistor has a comparatively large size and works in its saturation region, acting as a variable load. It would drain more current from the source, if the output voltage of the regulator goes above a certain level [90].

6.5 Conclusion

In this chapter the circuits of voltage doublers are analyzed and an analytical method was used to show that the charge transfer produces the expected growth in voltage level. The computer simulation results of the proposed charge pump based on the novel SBD are also presented in this chapter. Design considerations of the proposed charge pump are included and trade offs between power, frequency and voltage level are addressed. An optimum load termination is discussed using a resistive model. The input impedance to this circuit is mainly determined by the junction and substrate capacitance of the SBD diodes.

The SBD based charge pumps are good to serve as the power supplies for RFID transponders, with the result that a smaller package, cheaper price and ease of manufacturing for modern RFID systems are achieved.

Chapter 7

Turn-On Circuits

The evolution of RFID Systems has led to the development of a class hierarchy in which the battery powered labels are a set of higher class labels referred to as active labels. The battery powering an active transponder must last for an acceptable time, so the electronics of the label must have very low current consumption in order to prolong the life of the battery. However due to circuit complexity or the desired operating range the electronics may drain the battery more rapidly than desired, but use of a turn-on circuit allows the battery to be connected only when communication is needed, thus lengthening the life of the battery.

Two solutions available for the development of a turn-on circuit use resonance in a label rectification circuit to provide a high sensitivity result. This chapter presents: the results of experiments conducted to evaluate resonance in a label rectification circuit, and the designs of fully integrable turn-on circuits. The tests conducted show a successful practical implementation of the turn-on circuit designs.

7.1 Introduction

RFID has two basic tag types, Active and Passive. Active tags use a battery for power to transfer data to and from the reader. These tags are generally more expensive and physically larger than passive tags. Active tags' main advantage is longer transmission distances between the tag and the reader. Their disadvantages include battery maintenance and price.

To make the best use of the battery supplied and get the maximum battery lifetime it is imperative to turn the power on only when a tag is in the interrogation field. Therefore, an interrogation field sensing circuit is required to allow the battery to be connected to the transponder only when communication is needed, thus lengthening the life of the battery. Such circuits are referred to as turn-on circuits.

To achieve optimum performance, the power supply circuit of a system requires a considerable amount of supplementary circuitry. It requires circuits to protect it from harsh conditions, ensure that it switches in the most efficient possible way and also feeds back information of the power state back to control logic. The need for these features makes the design of the power stage a complex task. Within the RFID area comes another significant objective and that is to protect the tag circuitry from a burst of destructive electromagnetic waves.

Therefore there is a need for an intelligent power supply circuit. This is required for safe, reliable and efficient operation of a tag. The power supply circuit needs to be optimized for switching speed to reduce losses. It is required to protect the surrounding components from excessive voltage, current and temperature. It must also be able capable of interfacing with logic-level systems, allowing transfer of information: both control information passed from the controller to the power stage and status information from

the power stage back to the controller.

The idea of turn-on circuits for active tags is of considerable importance to the proliferation of RFID technology. As such, this chapter of the thesis is dedicated to development and improvement of turn-on circuit topologies. One such technique is based on detection circuits that uses electromagnetic energy conversion using MEMS devices [76]. Another method, which is described in detail here, involves rectifying the incident electromagnetic wave and using that signal to trigger a microelectronic switch to power up the circuit.

7.2 Circuit Topologies

There are two types of active tags. An active backscattering tag will modulate the powering carrier to establish a communication link with the reader. It has the same architecture as that of a passive RFID tag, except it uses a battery to power up the logic circuit of the tag, rather than relying on the power supplied by the interrogation carrier signal. The other type of active tag uses an independent source of power to generate a reply to a reader. It uses the on-board battery to power the logic circuit of the tag and to generate and transmit a reply signal. It works on the same principles as a radio transceiver. Irrespective of the type of active tag, a turn-on circuit is an essential component of the tag circuitry.

As the turn-on circuit is permanently powered from the battery, its current drain must be low with respect to the self discharge current of the battery. The circuit must be compatible with standard CMOS process, allowing easy incorporation into existing transponder design. The turn-on circuit must have trimmable sensitivity to account for process variations and

different sensitivities. Its sensitivity must exhibit minimum change with temperature allowing it to operate seamlessly over a wide range of temperatures.

There exist two options for a turn-on circuit. One would be a rectifier circuit that produces a voltage of the order of 1V that can be used to turn-on a switch transistor from fully off to fully on. The other method can make use of a rectifier circuit that produces a DC voltage of the order of a few millivolts, that when amplified and then compared with an internal reference voltage, can trigger a transistor switch from fully off to fully on. Both types of turn-on circuits are explored in [77]. That work is summarized and extended somewhat in this chapters by the author and coworkers.

7.2.1 Implementation

A label antenna, which in this application is preferably inductive, and the rectifying circuit that is intended to produce a rectifying voltage used for circuit turn-on, can be modeled as indicated in Figure 7.1. Here R_r represents the antenna radiation resistance, L_1 represents the antenna reactance, C_1 represents the reactance of the diode capacitance, C_2 is the reservoir capacitor that also serves as an RF low-pass filter, R_L represents the ohmic loss in the diode junction, and R_a is the ohmic loss contribution from the antenna.

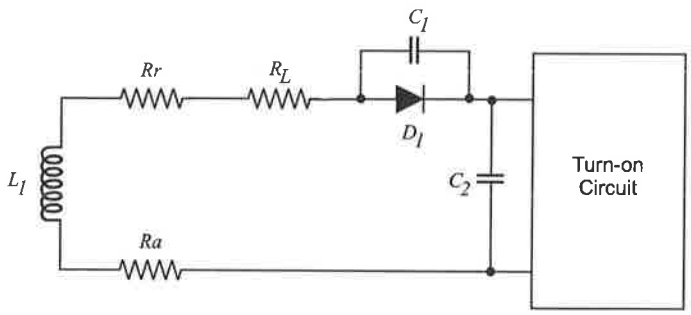


Figure 7.1: Label resonant rectifier circuit.

The antenna ohmic losses can be ignored since the antenna construction in a good design can be a slot antenna containing a significant amount of copper. In addition, the series combination of the impedances due to C_1 and C_2 is approximately equivalent to that provided by the diode junction capacitance. The reservoir capacitor has a relatively large capacitance of the order of 100pF. It is assumed that no DC power is removed from the diode. By shaping the antenna and its connection points appropriately, it is evident, that an impedance match between R_r and R_L can be achieved.

The turn-on circuit appearing in Figure 7.1 could vary from a single transistor consuming no power in its off state to a low power consumption threshold detection circuit.

The experiments performed here utilized the Hewlett Packard 5082-2835 Schottky diodes to evaluate the feasibility of a resonant rectifier. A surface mount version of the same diodes are also available as HSMS-2820. These are good candidates for the application due to the range of its capacitance (1pF - 0.5pF) and low cost.

As this experiment was conducted at high frequency using a network analyzer to deliver RF power to the circuit and also to measure the return loss, a tunable matching network was required. This was achieved by an adjustable trimmer capacitor in series with stray inductance of the capacitor connec-

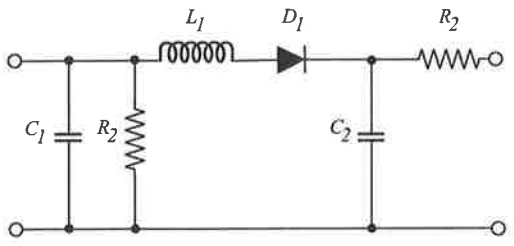


Figure 7.2: Schottky diode rectification circuit.

tions. Measuring the output voltage from the reserviour capacitor requires adequate filtering and shielding to remove all the unwanted RF signal from the output and to mitigate the radiation from the circuit output connections. A schematic of the diode rectification voltage measurement circuit is provided in Figure 7.2.

The function of R_2 is to provide a DC return path for the case where no such path is present in the source. The function of R_3, which can have a high value, is to assist in isolating the RF element of the circuit from the external DC voltage measuring elements. C_2 is the reserviour capacitor of the rectifier and L_1 and C_1 are the impedance matching elements, and also fulfill the function of resonating the diode junction capacitance.

It was established that the quality factor of the diode resonance was 130. With the circuit in Figure 7.2, it was established that with the input power of -46.2 dBW a voltage of 1 V can be obtained but with considerable detuning, or with an input power of -76 dBW a voltage of 10 mV could be obtained with very little detuning.

The proposed turn-on circuit in Figure 7.3 is an adequate and cost effective design that can be used for a backscattering active tag. It can be integrated onto a digital CMOS process including the Schottky diode that

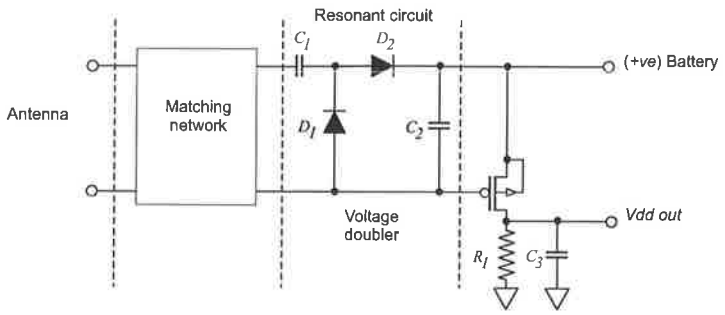


Figure 7.3: Turn-on circuit implementation.

has been developed in this dissertation.

In this proposal, a p-channel FET was used as a switch to control the power to the main circuitry. This circuit utilizes a voltage doubler, consisting of two diodes. The power generated and amplified by the diodes can be utilized to turn the pFET from off state to on.

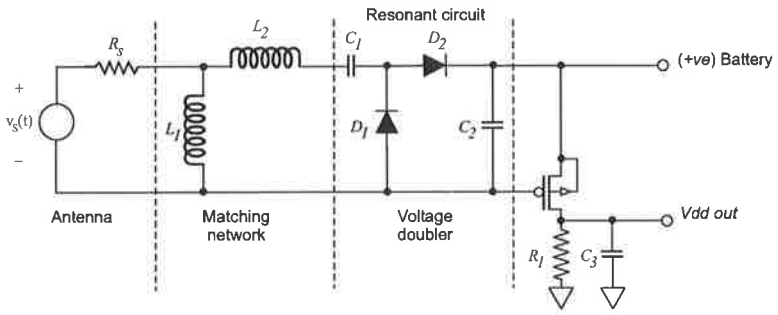


Figure 7.4: Turn-on circuit implementation used with Hspice simulation tools.

A Hspice implementation of the turn-on circuit is given in Figure 7.4. In this circuit, the antenna is modeled as a voltage source with an source impedance of 50 Ω. A matching network consisting of inductors and capacitors is used to match the circuit to the source voltage. Simulation results in Figure 7.5 indicates the resonance frequency of the circuit as a whole. Figure 7.6 shows simulation results that confirm that the turn-on circuit performs adequately at the minimum power of -12.5 dBW. This result may be compared with the practical results performed previously with HP Schottky diodes. However, the simulation results indicate a much higher power requirement to generate the required turn-on voltage, but there is the benefit that with the lower Q that occurs with this circuit, the de-tuning effect is effectively absent.

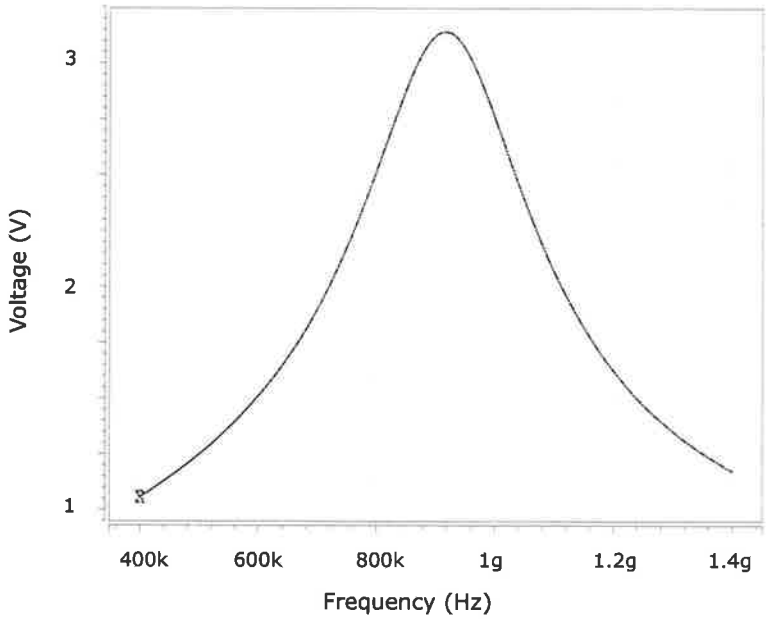


Figure 7.5: Frequency response (AC) analysis of the Turn-on circuit.

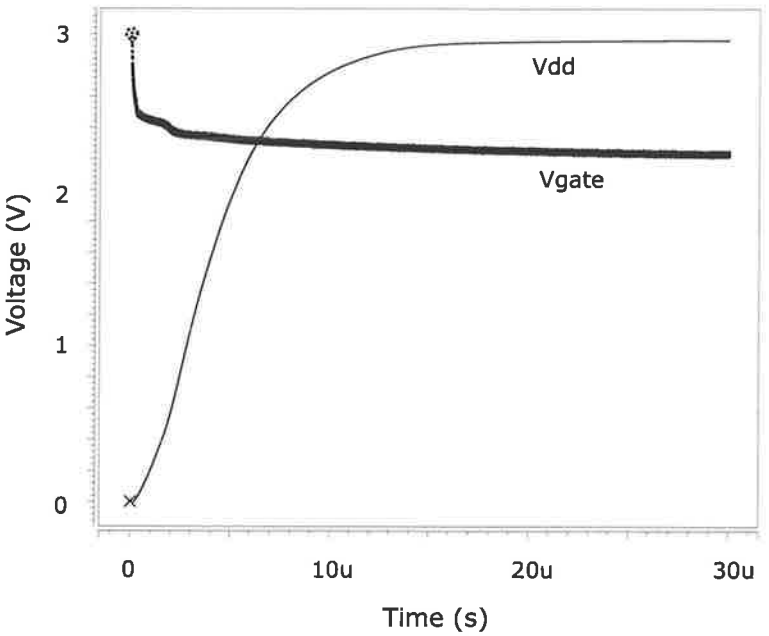


Figure 7.6: Transient response of the Turn-on circuit.

7.2.2 Power Requirements

The minimum UHF frequency input power required, with the proposed turn-on circuit employing the Schottky diodes of our first fabrication run, to obtain a DC output of 1 volt from the circuit was measured to be -12.5 dBW.

For favorably oriented antennas, a reader with antenna gain of 6 dB and output power of 1W, (as is allowed under the US regulations) and a tag antenna of gain 1.5, analytical calculation, using standard far field antenna formulae, gives a range of 10 m at which the turn-on circuit will start operating.

Alternatively, another turn-on circuit configuration can be built [77]. This circuit still exploits the diode resonance, but compares a small DC voltage developed across the diode with an internal reference voltage of a comparator circuit. The output can activate a switch when the rectified voltage exceeds the predefined internal value. In order for this low power turn-on circuit to be useful, the current drain of the MOSFET switch in its "off" state must be low with respect to the self discharge current of the battery. Unlike the previous turn-on circuit topology this design is triggered by a small DC voltage, rectified and amplified by diode resonance where the minimum value will be dictated by rectified RF noise.

Simulation work was conducted and proved that a minimum RF power of -65.3 dBW is required at resonance to obtain a 5 mV DC output from the reservoir capacitor. Again, using analytical calculation as mentioned above, with the same configuration of antennas, a range of 117 m is achievable. Such a long operation range makes this turn-on circuit suitable for independent reply generating active labels.

7.3 Conclusion

A turn-on circuit can be triggered by a small DC voltage, rectified from an RF interrogation field. The sensitivity must be set such that it must not be triggered by RF noise. The type of Schottky diode covered in this thesis can be used for the rectifying circuit. The self resonant frequency of the SBD discussed before in Chapter 4 and embedded in the circuit of Figure 7.4 was designed to be about 1 GHz.

For a turn-on circuit to be useful, its quiescent or stand-by current must be small compared with the self discharge current of the battery used as power source. Therefore a stable low current reference circuit is an essential component.

The concepts mentioned in this chapter were tested and used to design, analyze and simulate two turn-on circuit topologies using the fabricated SBD, while the results of the measurement studies of commercial discrete Schottky diodes were used to further optimize and fabricate a low power turn-on circuit.

The circuits employing the fabricated SBD presented in this chapter can be fabricated on a standard one poly, single metal CMOS process, allowing easy incorporation into existing transponder designs. The low power turn-on circuit has trimmable sensitivity to allow for process variations or different sensitivities. The circuit's sensitivity exhibits minimal change with temperature, allowing the trimming to be set at room temperature at the wafer testing stage. The low power turn-on circuit is triggered by a small DC voltage, rectified from an RF signal, the selected minimum value being dictated by RF noise. Simulation results show that the practical realization of the above concept in active labels is a possibility.

Chapter 8

Power Detector

In the modern world of increasing miniaturization, electronic devices are getting smaller and smaller with more transistors packed into a smaller area. Continual scaling of devices into the deep-submicrometer regime has resulted in the need for studying the effects of electromagnetic signal fed to sub-micron transistors.

Electromagnetic radiation received by a tag antenna may lead to high internal electric fields and oxide layer breakdown, where subsequent discharge energy melts silicon and a short circuit is formed. A weaker radiation may result in long term degradation such as shift in gate threshold voltage, drift in characteristics with time, increased gate or power leakages, loss of transconductance and reduced latch-up immunity.

In this chapter we start with a brief survey of different power detection techniques and then will focus on methods of measuring input signal strength at chip level. Knowing this enables a designer to employ strategies to mitigate the destructive effects of excessive input signals more rapidly.

8.1 Introduction

Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometers, but today's integrated circuits are incorporating MOSFETs with channel lengths of 0.13 μm. Until the late 1990s, this size reduction resulted in great improvement to MOSFET operation with no deleterious consequences. Historically, the difficulties with decreasing the size of MOSFET have been associated with the semiconductor fabrication process.

Aggressive scaling of the thickness of the gate insulator in CMOS transistors has caused the quality and reliability of ultrathin dielectrics to assume greater importance. It is found that there is high chance of dielectric wear out and breakdown in the ultrathin SiO_2 based gate dielectric [91].

These small MOSFET transistors are increasingly vulnerable to malfunction due to excessive input signals. Anything in excess of tens of volts can punch through the gate oxide of a CMOS circuit, effectively destroying the device. The damaging RF radiation can be accidental or from natural sources such as lightning. In some cases it can be intentional, produced by high power microwave weapons [92].

High electric fields can cause leakage current in gate oxide. The smaller the transistors are, the less energy is required to overload and destroy them. This current can be considered a nuisance parasitic and cause reliability problems by damaging the gate oxide and leading to long term wear out and even to oxide breakdown. That would cause the device to fail days, hours or even minutes after the incident.

The importance of this work is the incorporation of RF detectors on chip. That would allow a direct analog microwave level power measurement to be

implemented on a single chip along with the rest of the circuit. Integrating detectors with amplifiers allows non-invasive on-chip measurements.

8.2 Motivations

This work allows the study of the fundamentals of how RF pulses can disrupt RFID chips. It can also be used to study these effects on basic logic such as gates, latches, etc. The intention is to inject an interfering signal at different power levels and examine the circuit behavior. Collecting enough data enables the detection of weaknesses and vulnerabilities of modern CMOS integrated circuits.

Ultra short wave length radiation (X-ray, cosmic, alpha particles) could generate hole-electron pairs in both well and substrate regions, triggering pnpn latch paths. Also, Electrostatic Discharge (ESD) spark can trigger latchup. A charge pulse normally enters an input pad to be clamped by the ESD protection circuit which will inject minority carries into substrate or well. This can trigger a parasitic pnpn path.

The stress-induced parameter shifts are gradual, and the degradation is predictable on the basis of experimental data and physical models. The impact on device design therefore involves an engineering tradeoff between short-term and long-term performance. Oxide breakdown, on the other hand, is a sudden discontinuous increase in conductance, often accompanied by increased current noise. Breakdown is generally understood to be the result of a gradual and predictable buildup of defects such as electron traps in the oxide, but the precise point at which breakdown occurs is statistically distributed so that only statistical averages can be predicted [93].

In spite of the popularity and economic superiority of CMOS the lossy

nature of the silicon substrate has made the implementation of analog microwave circuits on standard CMOS relatively slow going. As the operating frequency of the circuits continues to increase, the undesirable effects of the silicon substrate dominate its performance and they become more and more apparent.

The results of our work here help to determine how to make circuits more immune to some unwanted RF pulses.

8.3 On-chip RF Detection

A burst of high power microwave signal, even nanoseconds long, can produce a shock that indiscriminately disrupts and destroys unprotected CMOS circuits and devices. The destructiveness depends on the strength of the microwave source and its distance from a device and any antenna coupling mechanism. At what level a destructive microwave signal penetrates a device and reaches a vulnerable CMOS chip is of interest to RFID users.

This has been the motivation to build an on-chip RF detector which can be used to measure RF power at the chip level. Knowing the RF signal level at the circuit level, enables one to employ strategies to mitigate its destructive effects. Within the RFID context, the detector can be used to monitor the strength of the interrogating signal and report it back to the reader. This can be useful in studying the environmental effects on the signal propagation path and the strength of the reader's signal. That can be achieved by placing RFID tags equipped with RF detector circuits in various locations and recording the output RF power reported by them.

8.4 Circuit Design

In this section the most popular techniques and methods used for measuring RF power are discussed. The principal uncertainty and error mechanisms are studied. For power measurements, thermistors, thermocouples, and diodes are typically used. Since diodes are the main focus of this dissertation, we only briefly cover thermistors and thermocouples. The reasons that thermal detectors, thermistors and thermocouples, are not pursued in detail in this work is that these devices cannot be built on a standard CMOS fabrication process and using discrete components are not economical for RFID and generally do not have response time small enough for our purpose here.

8.4.1 Thermistor

Thermistors employ temperature sensitive semiconductor material that have a negative temperature coefficient of resistance, i.e. as temperature increases, resistance decreases. Thermistors are still the sensors of choice for power transfer standards because of their DC power substitution capability. Thermistor characteristics of resistance vs. power are highly non-linear, and vary considerably from one thermistor to the next [94].

Power bridges are used for regulating and monitoring power sensing thermistors. The Wheatstone bridge, as shown in Figure 8.1, is the most common type of bridge used for RF detection. Once RF power is injected to the thermistor, the resistance of it becomes lower, that alters the voltage difference between the node A and B. A differential amplifier detects and amplifies the voltage difference. The Wheatstone bridge is kept in balance by automatically varying the DC voltage V_{ref}, which drives that bridge. By measuring the output of a differential amplifier, the injected power level can be known.

A typical thermistor power detector operates in range of -20 dBm to +10 dBm.

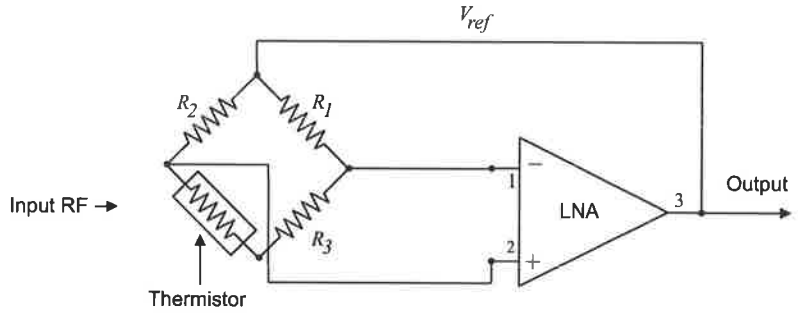


Figure 8.1: Simplified diagram of a thermistor power meter.

8.4.2 Thermocouple

Thermocouples are among the easiest temperature sensors to use for RF and microwave power sensing. They are based on the fact that dissimilar metals generate a voltage between them that is dependant upon to the temperature at their junction. The output voltage is small and non-linear, thus, the Seebeck coefficient is necessary to characterize the specific thermocouple being used. They are better than thermistors because they exhibit higher sensitivity as they have lower thermal time constant compared with thermistors but are more fragile.

Both thermistors and thermocouples feature an inherent square-law detection characteristics, and since they are heat based, they are true averaging detectors.

Various types of thermocouple power detectors on silicon or other substrate materials have been suggested [95] [96], but they all need extra process steps if they were to be implemented on CMOS process.

8.4.3 Diodes

Rectifying diodes have long been used as detectors and for relative power measurements at microwave frequencies. It was the low-barrier Schottky diode technology which made it possible to construct diodes with metal-semiconductor junctions for microwave frequencies that were very rugged and consistent from diode to diode. These diodes, introduced as power sensors in 1974, were able to detect and measure power as low as -100 dBW at frequencies up to 18 GHz [94]. Thus, diode technologies have captured the bulk of these applications because of their increased sensitivities, wider dynamic ranges, and higher power capabilities.

In this section we briefly review some of the diode properties that apply to microwave RF detection. The Schottky barrier diode has small junction capacitance, as such, it has extremely high impedance at low signal levels. An RF signal in the range of -20 dBm from a 50 Ω source is required to overcome the built-in voltage drop of the SBDs, which is almost 300 mV. An alternative technique would be to bias the SBD to 300 mV and is a usable approach if the detected output can be AC coupled. That eliminates the noise and drift introduced by the bias voltage.

AC coupling also improves the minimum power that can be measured by a biased diode which is limited by the drift and noise introduced by the bias current.

The general diode equation, $i = I_s(e^{qV/NKT} - 1)$, can be written as a power series to better analyze the rectifying action,

$$I = I_s \left\{ \frac{(\frac{qV}{nkT})^1}{1!} + \frac{(\frac{qV}{nkT})^2}{2!} + \frac{(\frac{qV}{nkT})^3}{3!} + \cdots \right\} \tag{8.1}$$

In Equation 8.1, the second and other even-order terms of this series provide the rectification because negative voltage input becomes positive component in this series. The second order term is the most significant in a small signal operation and DC output, as it is proportional to the square of power level. The diode is then said to be operating in the square law region.

If the input signal becomes larger, the third term and higher order terms become significant and the series resistance is not ignorable, the diode is no longer in the square law operation region and moves into the quasi-square law or transition region. For inputs even higher it moves into the linear region where the output voltage is proportional to the input voltage. A typical Schottky diode has the square law region of between -70 dBm to -20 dBm, the transition region of between -20 dBm to 0 dBm, and the linear region of above 0 dBm, all in a 50 Ω matching system. The square law region can be extended up to 20 dBm by using an attenuator [94].

Diodes that are highly stable with time and temperature are best suitable for power detection. Combining that with data correction and compensation techniques, can extend the operating range of the detector to 100 dB.

Maximum RF power would be delivered to the diode efficiently when the input impedance of the detector circuit is matched to the output impedance

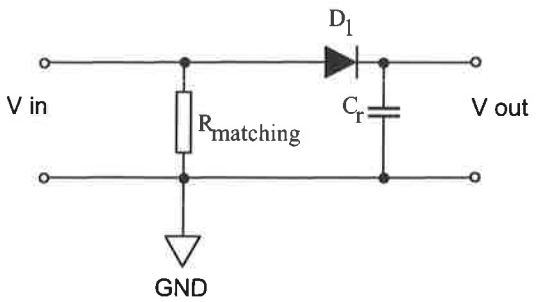


Figure 8.2: A simplified diagram of a diode detector with matching resistor.

of the source. Therefore depending on the type of the antenna used, a preferably lossless matching network must be implemented to set the detector's input termination impedance.

The input resistance of a diode is a strong function of temperature, which means the diode sensitivity and the reflection coefficient are also strong function of temperature. A diode with large resistance would decrease the sensitivity and diodes with low resistance have high saturation current. Therefore a compromise between good sensitivity to small signals and good temperature performance needs to be determined empirically. Diodes with high saturation current can be implemented with larger junction area as described in the earlier chapters.

Another issue we need to discuss here is that the antenna's impedance is fixed while the impedance of a diode is dependant on power level. Therefore even though the antenna might be matched to the detector circuit at a particular power level, it is unmatched as the power level is changed. As result the power fed to the diode varies as the diode resistance is changed.

The plot in Figure 8.2 shows a simplified diagram of a diode detector with matching resistor. It is often installed in laboratory coaxial detectors so they achieve a 50 Ω input impedance but a great sacrifices in sensitivity is made as most of the input power goes to the resistor, not the diode.

8.4.4 Implementation

The Figure 8.3 gives the basic circuit of the RF detector contributed from this study. It provides both RF power and die temperature measurements. Within the RF detector block, a number of diodes, for example two, are used in a DC series configuration for improved performance. This allows better

signal detection and thermal effects as well as a wider dynamic range. Also, as the noise sources are uncorrelated, the detected noise output is doubled in power while the signal output is doubled in voltage.

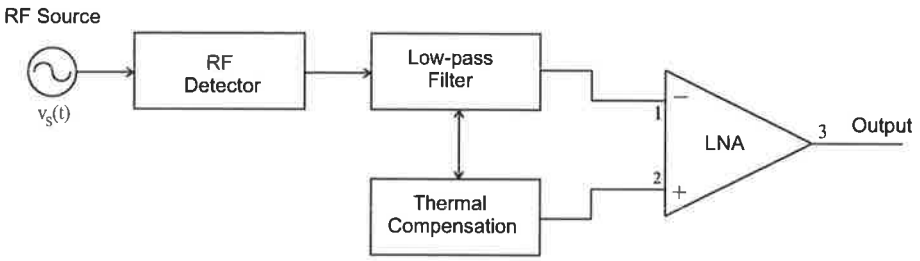


Figure 8.3: A block diagram of RF detector with temperature compensation.

In order to accurately measure the presence of signals with high peak-to-average ratio a dynamic range of 50 dB is often required. A single diode configuration is only capable of measuring the average power of low level signals and cannot satisfy this requirement. The approach here is to make use of a dual diode pair sensor and attenuators as proposed by Szente et. al. [97]. This topology has the advantage of always maintaining the sensing diodes within their square law operating region, therefore will respond properly to any kind of burst electromagnetic radiation as long as the sensor's correct range is selected. This approach can be refined even further by incorporating stacks of diodes in place of a single diode to extend the operation to higher power level at the expense of degrading sensitivity.

A series connection of n diodes results in a sensitivity degradation of $10\log(n)$ dB, while at the same time it increases the maximum power limit by $20\log(n)$ dB, yielding a net improvement in dynamic range of $10\log(n)$ dB compared to a single diode detector configuration.

This new configuration presented in Figure 8.4, is constructed from diodes of different geometry, with a small two diode stack pair for the low power path

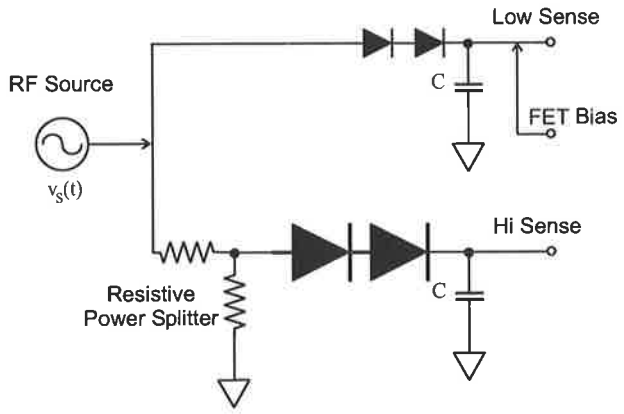


Figure 8.4: Schematic of multi-path RF detector.

and two large diodes for the high power path. A FET switch is connected to the cathode of the low power diodes to bias them to the off position when they are not in use. The decision to switch between low power and high power paths is made on the basis of the average power detected by the circuit. To avoid unnecessary switching a switching point hysteresis can be added, so that the two paths would have a few dB operation overlap.

As the real part of the diode impedance adds in determining rise time to the real part of the source impedance, the effects of finite load resistance can be estimated. Knowing the value of the reservoir capacitor (C in Figure 8.4), one could estimate the overall rise time accurately.

When the input signal is continuous (not pulsed), the circuit responds by putting out a steady-state DC voltage. When the input signal is not continuous, but pulses on and off instead, the circuit response time (the time it takes the output to change in response to a change at its input) is dominated by the RC time constant of the low pass output filter in Figure 8.3.

Setting the filter bandwidth very high will produce residual output ripple for low frequency input signals. It is also a known fact that the corner

frequency of the low pass output filter determines the circuits minimum input frequency. Therefore, when selecting such a corner frequency, the designer must consider the primary application of the detection. However, the circuit can be used to detect lower frequency inputs without any penalty as long as sufficient external low pass filtering is used.

The same power detector configuration can also be used in a circuit to detect a simple ASK signal from an interrogator. In such situation, the presence or absence of an RF burst conveys the 1s and 0s of digital information. It can also be used in such applications where the arrival time of the burst is the critical parameter to be measured.

8.4.5 Practical Issues

This design can be integrated into a CMOS chip at the power control stage. It can convert an RF signal coming from the reader into a DC signal to power up the tag. It can be based on an SBD. It must have two stages. one to provide signal detection while the other one to provide temperature information to a thermal compensation stage. A biasing stage can be used to suppress the detection diode voltage drop effects.

The main factors in here are the series resistance of the SBD and the diffusion capacitance. The diffusion capacitance of the SBD can be used as the reservoir capacitor, so in fact it becomes useful.

In the designed RF detector, the series resistance was reduced by interdigitating the fingers of the Schottky and ohmic contacts. The capacitor has been laid out in a manner to decrease charge lost to the substrate through the parasitic substrate capacitance. For added accuracy, an averaging circuit consisting of a resistor and a capacitor was added to isolate the Schottky

diode detector circuit from the measuring circuit. With these improvements in the design, the frequency and dynamic range of the Schottky diodes in the detector circuit was extended further into the GHz range.

In order to further improve the performance and reduce the unwanted noise and parasitics, the reservoir capacitor was coupled with the device on the same chip. That decreases the parasitic effects of having an external capacitor. As for the capacitor a regular layout design or poly-poly or metal-metal configuration was used, that would increase the distance from the substrate and mitigate the leakage caused by the charges that travel to the substrate.

8.4.6 Simulation

The plot of Figure 8.5 shows the output of the RF detector to an input signal of magnitude 400 mV peak value. As it is evident from the simulation plot, the circuit is able to respond to RF pulses as short as 100 ns at carrier frequency of 915 MHz. The rise and fall time of the output signal depends not only on the reservoir capacitor of the low pass filter but also on the junction capacitance of the diodes. Large diodes have large junction capacitances, but also have large saturation current which means lower voltage drop. The lower voltage drop accompanied with lower series resistance of large diodes makes them ideal choice for low power input bursts, but, they also are less sensitive to high frequency signals.

One issue with the current simple design is the discharging (roll-off) time constant. This problem can be compensated for by using an active load or a dynamic switch to increase the discharging current when reservoir capacitor is discharging, while still keeping the charging current small. That way we can increase the power detectors speed and linearity.

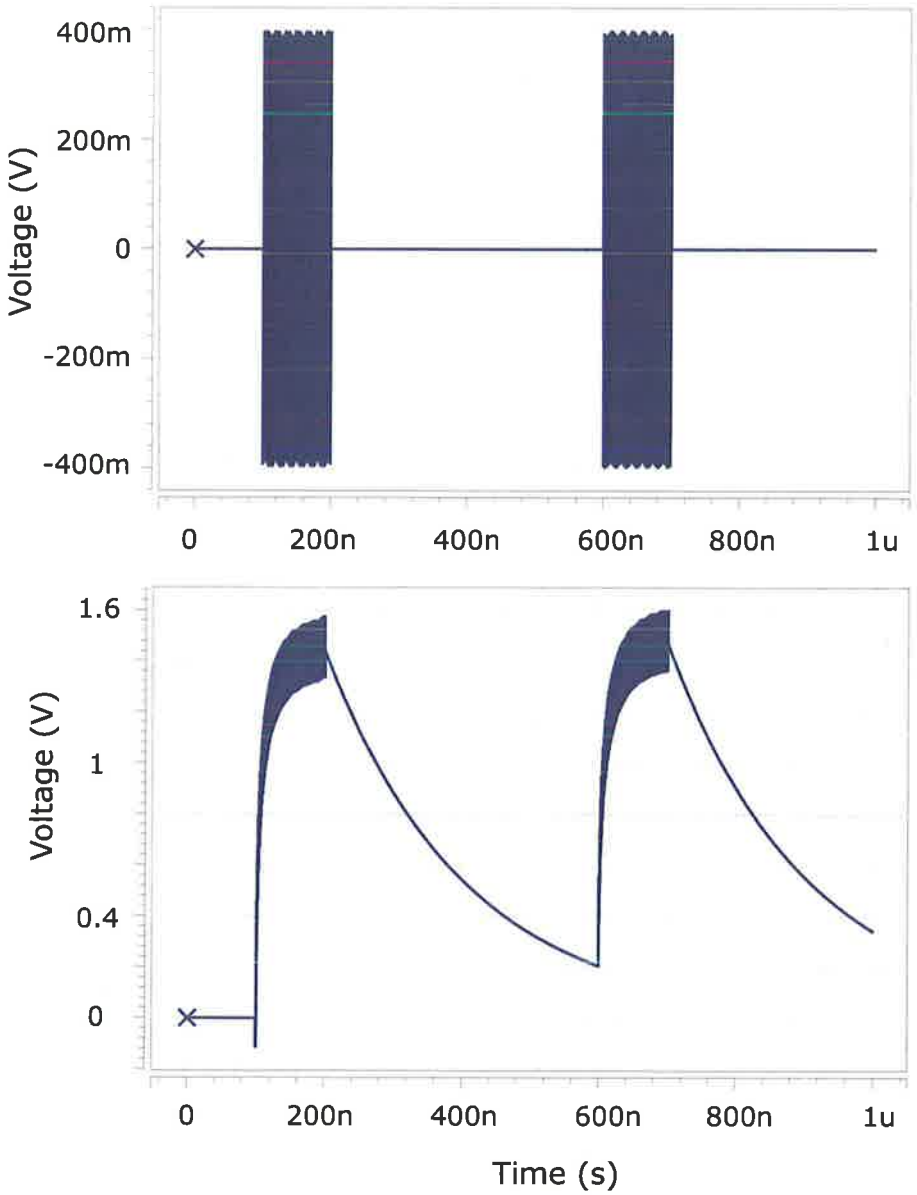


Figure 8.5: Simulation plot of the circuit's response to input RF bursts.

8.4.7 Conclusion

Modern electronic systems are increasingly vulnerable to malfunction due to incident electromagnetic radiation, particularly since many integrated circuits operate at lower and lower voltages.

The RF detector monitors the wanted and unwanted RF irradiation signals. This can sometimes be used to shut down the system if excess microwave energy is detected to protect the tag from damage caused by faulty readers or malicious attackers.

In this chapter we presented a new RF power detection circuit. The analysis and simulation performed on the circuit are also presented. Because of time and money constraints no fabrication has been attempted, as such only simulation results are quoted.

The protection can be provided by shunting the supply current by switching large transistors (for low series resistance) or by adding detuning capacitances to detune the circuit. But either of these cases involves switching large transistors which involves a large delay time-constant. Also considering the delay of the logic gates to be few nano-second each, this kind of on chip power detection technique can be seen to be more useful as power detection and measurement rather than protection device.

The RF detector circuit is able to provide both RF power and die temperature measurements. It takes its input from the available power of the antenna. The RF detector and the low pass filter provide a DC voltage depending on the input power level. Thermal compensation provides a DC voltage depending on the ambient temperature. As the detection system and the thermal compensation are based on the same topology, the DC output voltage will have the same temperature variation as thermal voltage. Con-

nected to a differential amplifier, the output will be a voltage directly linked to the RF input power.

The use of this RF detection technique allows the RF front-end designer to save chip area and to drastically suppress parasitic inductances as compared with external detection circuits.

Part II

Chapter 9

Software Data Logging Reader

Wireless communication is becoming softer and softer. This means that radios, terminals and networks are becoming reconfigurable and programmable. Software and cognitive radios are becoming one of the big trends in this field. Although these concepts have been studied for decades, a lot of challenges remain to make this vision a reality. In this work we are studying several aspects of a software based RFID reader, including experimentation, implementation and theoretical work.

9.1 Introduction

RFID systems are demanding more data, faster logging, and higher interrogation rates, so they require a powerful system that can manage information from a variety of sources, store the data, and transmit it reliably and continuously for long periods of time to other readers or a host PC. In addition, data logging is an extremely important part of RFID because it is the best method for determining what happens during the tag interrogation and to test software strategies and protocol efficiencies. In the near future, software will do much more than running a fancy Graphical User Interface (GUI). More and more of the functionality of traditional radio systems will be implemented in software.

Joseph Mitola [105] coined the term software radio as: "A software radio is a radio whose channel modulation waveforms are defined in software. That is, waveforms are generated as sampled digital signals, converted from digital to analog via a wideband DAC and then possibly upconverted from IF to RF. The receiver, similarly, employs a wideband Analog to Digital Converter (ADC) that captures all of the channels of the software radio node. The receiver then extracts, downconverts and demodulates the channel waveform using software on a general purpose processor."

9.2 Problem Statement

When one hears the litany of reliability and readability woes that plague RFID in the supply chain arena, it is possible to wonder if anyone is making any progress [99]. The problems with RFID range from non-functioning tags to environmental conditions, such as temperature, humidity and radio frequency interference, often from other readers. All these effects can render

tags unreadable. The challenge continues wherein a shipping and handling process, tags can be thrown out of alignment (detuned) so they don't receive the reader signal at their resonant frequency. And the list goes on. Average read rates are still under 80% [100]. Some of this is the result of tag failure but other important problems are incompatible tag and reader combinations as well as reader-to-reader interferance resulting in ghost tag reading [101].

Traditionally RFID systems have been designed with only a single reader scenario in mind. The increasing use of RFID in multiple industries and also increasing deployment of mobile RFID readers, results in situations where readers are to operate in close proximity of each other leading to interference which in turn may result in incorrect or slower operation.

The reader collision problem within an RFID network plays an important role in ubiquitous RFID implementation [102]. An anti-collision protocol needs to be developed for a mobile ad-hoc network of RFID readers. One of the challenges of RFID development is to make the tags as simple as possible even though doing so adds extra complexity to the reader. In a case where multiple readers try to read the same tag, the tag cannot select a particular reader to respond to. Therefore, passive tags, where the collision may take place, are not able to take part in the collision resolution. Reader-reader collision not only decreases throughput of tag identification, but also increases the bandwidth usage.

9.3 Solution

The Software Data Logging Reader, from here on refered to as SDLR, was developed to solve this interoperability problem. Traditional radios use hardware circuits, fixed at the time of manufacture, to perform the high-speed

signal processing tasks that convert back and forth between user data and the radio waveform. SDLR exploits advances in components such as digital signal processors and field-programmable gate arrays to make the hardware generic, and move all of the waveform-specific tasks into software. One SDLR device can support a variety of communications standards, just as one PC can run a variety of software applications. SDLR has a number of benefits in addition to improving interoperability.

Software Data Logging Reader has significant advantages over traditional RFID readers, that is why many Auto-ID labs are supporting its developments.

Desirable characteristics include:

1. Receive and transmit various modulation methods using a common set of hardware.
2. Alter functionality of the system by downloading and running new software.
3. The possibility of adaptively choosing an operating frequency and a mode best suited for prevailing conditions.
4. The opportunity to recognize and avoid interference with other RFID readers and communication devices in a high density reader environment.
5. Elimination of analog hardware and its cost, resulting in simplification of data logging reader architectures and improved performance.
6. The chance for new experimentation and development of new RFID protocols.
7. Support of multiple modulation formats.

8. The system can be simulated *Exactly.*

9. Flexible bandwidth selection and management.

10. The ability to dynamically join or leave an ad-hoc network formed by other readers in proximity.

11. The ability to transmit neighbour information to other readers or a server along with request to transmit.

12. The ability to scan the status of its neighbours and respond accordingly.

13. On collision with other readers, reducing its power level by a predefined factor.

While SDLR offers benefits as outlined above, a few obstacles remain to its universal acceptance. Those include:

1. The difficulty of writing software for various target systems,

2. The need for interfaces to digital signals and algorithms,

3. Poor dynamic range in some of the designs.

9.4 Novel Properties of SDLR

SDLR is capable of adjusting its software to suit the particular RFID environment in use. The following sections give an overview of two novel applications that can be used to demonstrate the advantages of integrating the software radio into an RFID reader.

9.4.1 Automatic Change of Modulation Scheme

A framework for changing modulation schemes on a per packet basis is given in a paper by Bose et al. [98]. In this case the modulation scheme is determined by a packet header that identifies the modulation scheme. With proper signal processing it is possible to determine the modulation scheme used at the transmitter [103]. A novel approach would be for an RFID reader to detect the modulation scheme of the incoming signal and then reconfigure its signal processing stack accordingly. This powerful feature can be used to provide flexibility to readers not only in a multi-tag environment but also in a high density reader environment. An FPGA device could dynamically load a new modulation scheme and become part of a new reader network without changing the hardware.

A layer in the communication stack can be used to act as a modulation detector and load the appropriate op-code into the FPGA device to demodulate the incoming signal. The modulation detection layer must perform analysis of the incoming signal to determine the modulation scheme used. This information can be added to attributes of the message block as it being passed to the next layer in the stack. The DSP, then, makes sure that the appropriate demodulation scheme is available to demodulate the incoming signal. If it does not have the appropriate demodulation scheme then, it raises an alarm, notifying the operator. Or alternatively it can send a request to the host computer asking for the latest demodulation scheme.

9.4.2 A Peer to Peer Component Sharing

Tuttlebee [104] describes Over-The-Air Reconfiguration (OTAR) for a software radio. Using this concept, a remote device can be reprogrammed by the transfer of new software into the device. Up to now hardware restric-

tions have meant that OTAR has only been used for one-off projects such as satellites.

Now, advances in hardware allows OTAR to be used in ad hoc networks. An ad hoc network can be a connected set of RFID readers without any centralized or hierarchical structure. In an ad hoc environment, readers might be communicating with tags using many different protocols, modulation schemes and location specific parameters. The ability of nodes to share information about network conditions would be of key importance to ensuring reliable communication is happening.

In such a situation, readers can go beyond just sharing information by sharing their network layer component as downloads. These network layers, for example, a new demodulation scheme, can also be downloaded from a central computer. In the absence of or unavailability of such a central computer system, this method can be used as a back up or alternative procedure in order to keep the system running. For example a reader installed in a new location, could contact its nearest operational reader using this scheme to download the most popular communication environment variables used in that area. These settings would include information such as available frequency allocation, bandwidth, average number of tags per unit of time, number of readers and their locations, noise conditions, etc. This information can be used to optimize communications. This scheme therefore can tremendously increase the flexibility of an RIFD system. Such functionality are not available currently in any RFID system.

9.5 Software vs. Hardware

A traditional radio receiver requires many analog components as shown in Figure 9.1. First the radio signal is received by the antenna and is then amplified by a LNA (Low Noise Amplifier). These parts are shared by all the radio channels [106]. After these components one receiver is required for each channel. The RF signal is down converted to baseband by a mixer and a local oscillator. At each stage analog filters are used to discriminate the signal outside the frequency band. The last step before the digitization is to decompose the signal into inphase and quadrature components. These signals are then converted in a narrow band ADC. In UHF, for example, FCC regulations limit the total bandwidth to 25 MHz while the channel bandwidth is about 500 KHz. A reader therefore can handle more than 50 channels.

If the ADC is moved closer to the antenna, more components can be shared for all channels and more of the signal processing can be done in software (Figure 9.2). This means that the hardware cost can be substantially reduced. An ideal software radio would consist of an antenna, one ADC that samples directly on the antenna signal, one DAC that generates the outgoing antenna signal in the tranceiver and a DSP (Digital Signal Processor). All

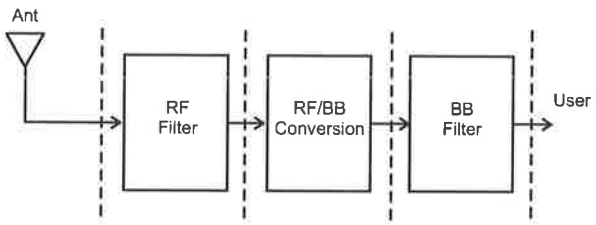


Figure 9.1: Simplified hardware chain of a traditional RFID reader.

the signal processing should then be done in software in the DSP. This ideal situation, however, is not feasible with today's technology.

There are other advantages with a software radio architecture, besides the hardware reduction. A software radio reader could be reconfigured without replacing any hardware. The same hardware could also be used for different systems, e.g., different tag generations and different classes, since all the signal processing is performed in software. The same software can be re-compiled for a different processor and can be run on different platforms such as in hand-held terminals. Instead of implementing several RFID receivers for different physical regions, one receiver could be used for all systems and different software packages could be used to switch between systems.

The requirements on the ADC in a software radio architecture are very high, as the signal received by the antenna for instance does fluctuate in amplitude by a large amount. When such a wide dynamic range signal is converted in the ADC the dynamic range must be high enough so that a weak tag reply can be separated from the harmonics and the strong carriers. The SNR (Signal to Noise Ratio) must also be high so that weak replies can be seen above the noise floor.

9.6 Contributions

The work on the SDLR (Software Data Logging Reader), makes the following contributions to the development of RFID systems and technology:

- The development of an open-source implementation of software based RFID data logging reader.
- The implementation of a proof-of-concept SDLR application using a

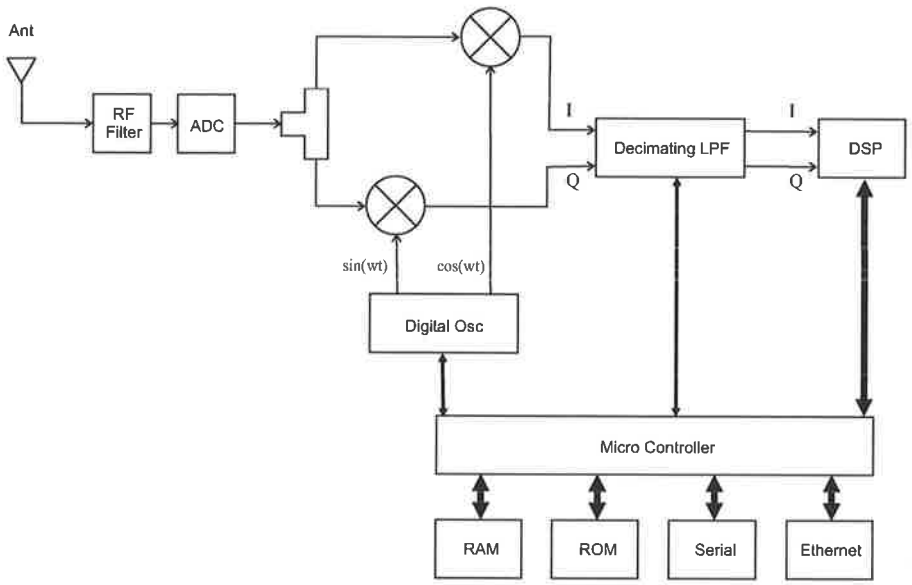


Figure 9.2: Simplified hardware and software chain of the SDLR receiver.

simple, low-cost, highly reconfigurable design, that can guide the further development of RFID systems.

- Reusable, open-source software components that can be used to build up SDLR compatible readers.

- Study, test, evaluate and validate Channel Estimation Algorithms and Link Level Adaptation Algorithms.

9.7 Conclusion

This chapter has demonstrated a flexible approach to implementation of a Software Radio based RFID data logging reader using dynamic communication schemes. This platform provides a powerful solution for rapidly building and testing new RFID communication systems and protocols and it forms a basis for developing highly flexible RFID readers.

The SDLR is an inexpensive and versatile solution to the collection of temporal and spatial field data for numerous research and educational endeavors. Defining an open architecture and implementing readers compatible with this architecture further enhances interoperability. It can be integrated with a large array of available sensors. In the next few chapters the experiments performed using this reader will be discussed. The full schematic, circuit board layout, firmware and host software will be published on the Auto-ID web site, so that other researchers can download sufficient information to construct their own SDLR.

Chapter 10

SDLR Architecture

RFID systems are demanding more data, faster logging, and higher interrogation rates, so they require a powerful system that can manage information from a variety of sources, store the data, and transmit it reliably and continuously for long periods of time to other readers or a host PC. In addition, data logging is an extremely important part of RFID because it is the best method for determining what happens during the tag interrogation and to test software strategies and protocol efficiencies.

Off the shelf RFID readers are not optimized for the data logging application. The purpose of this chapter is to describe a high speed RFID data logging reader. Developed for use in my research, the SDLR can be used to evaluate architecture, protocols and prototype hardware and software.

10.1 Introduction

Todays continuously changing technology in RFID brings the need to build futureproof RFID readers. If the functions that were formerly carried out by hardware can be performed by software, new functionality can be deployed easily by updating the software. With the existing stringent requirements of RFID spectrum, increasing traffic rates, and the need to adhere with the regulations on spectrum usage, this requires even more sophisticated signal processing algorithms that can only be implemented on a software based RFID reader system.

The software based RFID reader system will also allow the addition of new functionalities with a short time-to-market. The SDLR includes excellent multipath and antenna diversity performance, resulting in superb tag reading performance. User specific functions can be configured easily to the performance required for different environments, and only the software needs to be upgraded rather than a completely new hardware design. By integrating everything into software, fewer external components are required, which further reduces the cost. This allows innovative new features and a rapid development cycle.

The SDLR can be part of a large distributed and dynamic system in which each reader is responsible for the management of its own local population of tags that is changing dynamically. In such a system, the reader acts as a gateway between the low cost simple tags and a very sophisticated distributed information system which can interface to enterprise software applications.

The fundamental physics of antennas and radio frequency propagation properties at different frequencies causes devices operating at various bands to have different benefits and functionality tradeoffs. Therefore their use will remain a reality for a foreseeable future. The SDLR is designed around this

notion as a modular system and can support multiple frequency bands.

Furthermore, there is a need for flexibility in RFID design because the specifications are still changing, and even within a single specification, the tags can be asked to reply at different frequencies. For instance tags working within the EPC Global Generation 2 specifications can be asked to reply at a sub-carrier frequency ranging from 40 kHz up to 620 kHz. Therefore the reader must be able to be easily reconfigured to support frequency bands and protocols of different geographical regions and those that will become available in the future.

10.2 Hardware Design

This section concerns the design and development of the hardware for a data logging reader. The prototype instrument developed for this project is called Software Data Logging Reader (SDLR). It features a DragonBall network processor, which enables it to perform high-speed data processing. It runs on an Embedded Linux operating system and comes with a number of PC-like functions built in that enable it to run additional applications simultaneously. Additionally, it supports standard network protocols including DHCP, UDP/IP over Ethernet, 820.11x (Wi-Fi), HTTP and SNMP, and its superior network adaptability enables its software to be easily implemented from remote sites.

The general setup of the implemented SDLR transceiver is shown in Figure 10.1. In the following sections we discuss various considerations that led to its particular design. A detailed description of the overall system and its individual components are also given.

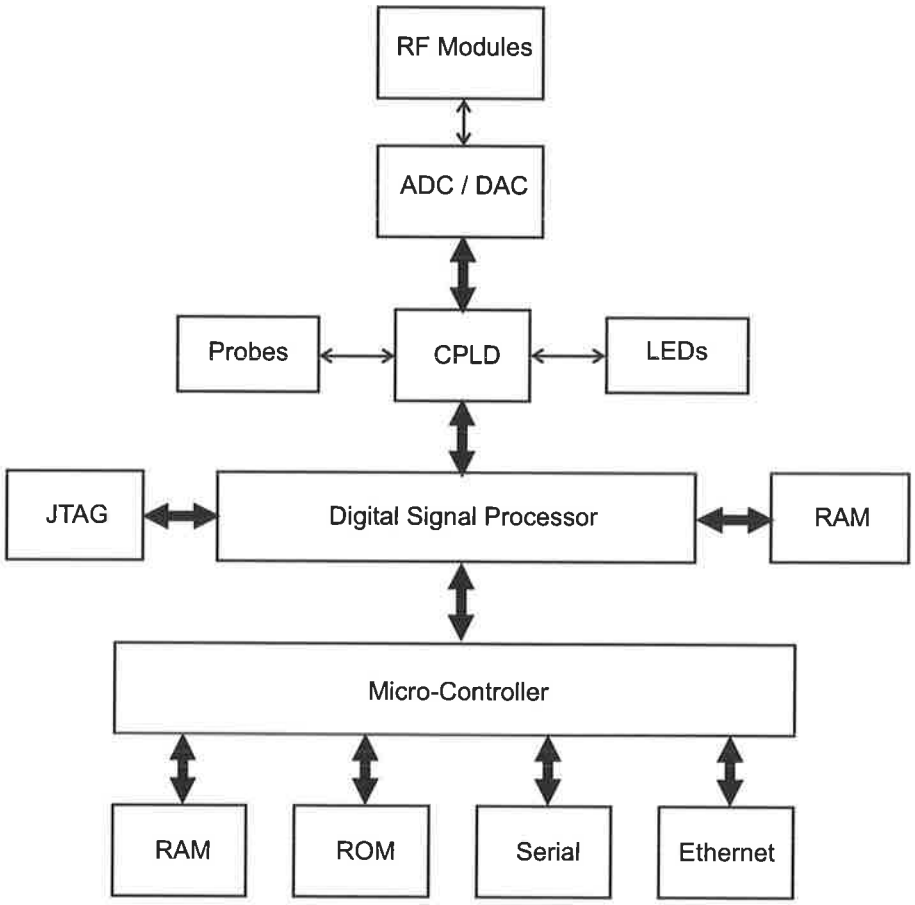


Figure 10.1: Simplified and abstract level hardware block diagram of SDLR.

10.2.1 Microcontroller

The microcontroller block is based on DragonBall, MC68EZ328 EZ Integrated Processor from Freescale Semiconductor. The MC68EZ328 core processor is identical to the MC68EC000 microprocessor and features full compatibility with the MC68000 as well. Running at 16 MHz it performs 2.7 MIPS. It also provides a UART, SPI, LCD controller, Timer/PWM, and parallel I/O.

The microcontroller runs on uCLinux, that is an operating system for a microcontroller without a Memory Management Unit (MMU). ucLinux is derived from the 2.0 Linux kernel. It is a multi-threaded real-time operating system for embedded applications. ucLinux is a mature, robust operating system that already supports a large number of devices, file-systems, and networking protocols. It gives the developers complete visibility of the source code. Bug fixes and new features are constantly being added, tested and refined by a large community of programmers and users.

The microcontroller block consists of an Ethernet controller, a UART Serial port, RAM and ROM. The system provides a boot strap mode function which allows system initialization as well as program/data download from ROM or via the UART (for debugging purposes). The microcontroller uses its parallel interface to communicate and load DSP firmware into the DSP chip. The microcontroller is responsible for high level tasks such as system management, self test, database maintenance and serving requests from the other readers or host PCs through TCP/IP network, while DSP handles low level computationally intensive processing tasks, such as FFT and filtering.

10.2.2 DSP

This system uses the TMS320VC5416-160 fixed-point, digital signal processor (DSP) chip from Texas Instruments, operating at 160 MHz. The chip includes 256 kB of RAM and 32 kB of ROM, which is used for both program and data storage. A 6 channel DMA, 16-bit HPI interface and 3 Multi-channel Asynchronous serial port are included. It operates with a core voltage of 1.6 Volts while the IO supply voltage is 3.3 V.

All the low level signal processing such as FFT, Filtering and waveform shaping are done within the DSP chip. It operates in "Microcontroller

Mode", allowing it to boot from the microcontroller board. It can be reset manually by power-cycling or through the software control of the microcontroller. At power up the DSP waits for the host microcontroller to upload the DSP firmware into its internal RAM through Host Port Interface (HPI). After the upload completes the DSP starts its boot cycle. More detail of the software architecture of the DSP sub-system is provided later in this chapter.

10.2.3 CPLD

The system used EPM3256A from Altera. This device is based on MAX 3000A family. It contains the electrically erasable programmable read-only memory (EEPROM), which provides instant-on capability and offers 256 macrocells. EPM3256A device supports in-system programmability (ISP) and can be easily reconfigured in the field. Each macrocell is individually configurable for either sequential or combinatorial logic operation.

This device is responsible for the interface between the DSP chip and other peripherals by converting and buffering the signals from ADC, DAC, PLL, etc to the Multi-channel Buffered Serial Ports (McBSP) format, that is acceptable by the DSP chip.

The CPLD has various internal registers, which are mapped to its IO pins. These IO pins are connected to PLL, LEDs and several other peripherals that can be controlled by software.

10.2.4 ADC

The system makes use of a ADS2807 high-speed, dual channel Analog-to-Digital Converter (ADC). The ADS2807 offer 12 bits of resolution at sample rates of up to 50 MHz. It is interfaced directly to the CPLD and it drives its

clock signal from the CPLD as well.

10.2.5 UHF Module

The UHF module is responsible for interfacing the DSP to the antenna. A simplified block diagram of this module is depicted in Figure 10.2, some blocks of this design may also be found in Figure 10.1. It operates at 902 MHz to 928 MHz UHF band and is compatible with FCC's part 15.247 rules. These rules specify that a maximum output power of 1 W may be exercised in a frequency hopping system with at least 50 channels. The maximum dwell time for each channel is set to 400 ms at any given frequency. The UHF band module is subject to PLL lock-time and the receiver circuit turn-around time limitations. The lock-time is the time that it takes the PLL to switch from one frequency to another for a given frequency change to a given frequency tolerance. In order to mitigate the effect of PLL lock-time, a two synthesizer design was chosen. This design allows the system to program the second PLL to a new frequency while the first one is still operating and then switching over to the second PLL when a frequency hop is required. This configuration prevents the dead-time during which the reader RF field would be off and no data can be transmitted. Also it reduces the risk of tags' brown-out (when the voltage temporarily drops below the operating voltage level and then recovers).

Oscillator

A PSN0930A Phase Locked Loop (PLL) from Z-Communications Inc. is used to generate the operating frequency. It is small hybrid circuit block based on a National Semiconductor LMX2316 PLL IC. This small module generates an output of 3 dBm with phase noise of -1000 dBc/Hz at 10 kHz bandwidth.

The output of the oscillator is bandpass filtered and then amplified by 10 dB. The amplifier output is then subjected to a ceramic filter with center frequency of 915 MHz to remove the strong harmonics and other unwanted spurious outputs. The output is then split into two parts, one is fed into the receiver chain and the other into the transmitter chain.

Transmit Chain

The transmit chain comprises a PSN0930A Phase Locked Loop, as local oscillator and frequency hopping. A 3-bit digitally controlled attenuator for RF output power level control, an RF power amplifier M57785 IC from Mitsubishi Semiconductors followed by a ceramic band-pass filter to suppress harmonics and spurious frequencies. The module is capable of delivering up to 4 W of RF at UHF band. The modulation is achieved by means of a mixer (MCL SBL-1Z) from mini-circuits. The modulating signal is generated using

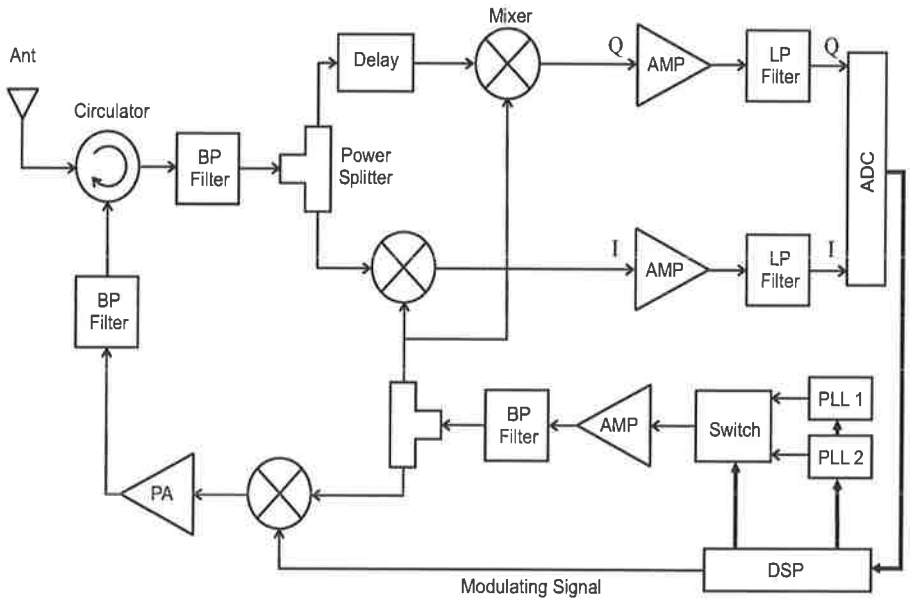


Figure 10.2: Simplified hardware chain of the UHF module.

a DAC, which receives its input from the DSP module.

Receive Chain

A three-port circulator (CN-6) from MECA Electronics Inc. is used to separate the transmitted signal from the weak tag reply. The tag reply is then filtered using a ceramic bandpass filter centered at 915 MHz. It then is split into two parts for I (In-phase) and Q (Quadrature) demodulation. The I and Q are then mixed with the local oscillator using Mini-Circuits double balanced mixers. The local oscillator signal for the Q channel is delayed by a quarter of wavelength to generate a 90 degree lag in the Q path.

The I and Q signals are then amplified and filtered by an anti-aliasing filter. The outputs are then amplitude limited and then applied to the ADC. Further signal conditioning and processing are performed digitally on the DSP.

10.3 Software Design

The system makes use of DSP-BIOS II from Texas Instrumnets. DSP/BIOS is a scalable real-time kernel, designed specifically for the TMS320C5000 and TMS320C6000 DSP platforms. DSP/BIOS is an integral part of the Code Composer Studio Development Tools from TI. The programing is done using Microsoft Visual Studio C++ and Texas Instrumnets' Code Composer Studio.

The heart of the SDLR is the C5000 DSP, which runs a TI DSP-BIOS II real-time kernel and controls the interface in addition to the specific transmit and receive functions. DSP/BIOS provides a convenient multi-tasking

capability through events, software as well as hardware interrupts, which operate at various levels of priority. Other functions such as tag management and communication to other readers or host PCs are performed in the microcontroller.

The DSP is required to receive commands from the microcontroller, and form packets of symbols, which are embedded into a flexible frame in order to be recognizable by a tag. The data is oversampled and pulse shaped before passing it on to the RF module. Thus, the aims of the DSP implemented in software comprise:

1. Initialization of interfaces and interrupts.
2. Initialization of CPLD, PLL, ADC and DAC. These are done via McBSP0.
3. Reception and transfer of data from/to the microcontroller. This is performed over the HPI interface.
4. Formation of tag command data frames.
5. Mapping from bytes to symbols. The bit stream is converted into amplitude modulated (AM) symbols, whereby here an AM mode is employed, although other modulation modes are possible.
6. Pulse shaping. The symbol stream is moderately oversampled by a factor of 2, which is required as a minimum by the subsequent mixer hardware, and filtered by a root raised cosine filter.
7. Passing data samples to the RF module. The oversampled and pulse shaped signal values are passed over to the DAC, and its output is connected to the mixer's input.
8. Reception of I and Q data from ADC. The Inphase and Quadrature signal values are received from the ADC via the McBSP0/CPLD. These

samples are oversampled by a factor of 4 compared to the symbol rate in order to permit sufficient resolution for timing synchronization.

Step 1 and 2 are performed at boot level, initialization of PLL, ADC and DAC needs to be done via McBSP0 after the CPLD is initialized and functional. Processing of both the transmitter and receiver functions are performed in interrupt service routines, whereby the processor falls into an idle mode if no interrupts need to be serviced.

10.3.1 Device Drivers

A software module that controls how a processor communicates with a device is called a Device Driver. In SDLR, the interface from the DSP firmware to the hardware is abstracted into a set of device drivers. The device drivers separate the high level firmware and protocol specific modules from the low-level Input/Output (IO) routines of hardware. Device drivers are provided for each of RF's transmit and receive modules as well as for actuators and sensors.

SDLR uses a special abstraction to access device registers independent of the underlying implementation. It hides the mechanisms to access a specific part of the address spaces. The use of this abstraction is in almost all cases as efficient as an assembly language access. These device drivers are designed to provide access to the hardware in a protocol independent manner. That allows the change of communication protocol without the need of changing the rewriting low level subroutines. The device driver Application Program Interface (API) is a a set of C callable functions for writing to or reading from the device or registers. This API is based on the POSIX file IO interface, using `read`, `write` and `ioctl` functions. A device is made active by calling `open` and released by calling `close`.

open()

This routine opens a device as a file for reading, writing, or updating, and returns a file descriptor for that file. The arguments to `open` are the device name and the type of access. In general, `open` can only open pre-existing devices and files. Files cannot be created with `open`.

The return value of this call is a file descriptor number, or ERROR if a file name is not specified, the device does not exist, no file descriptors are available, or the driver returns ERROR.

close()

This routine closes the specified file and frees the file descriptor. It calls the device driver specific function to do the work.

The return value is the status of the driver close routine, or ERROR if the file descriptor is invalid.

ioctl()

The `ioctl` call provides an interface to device specific configuration function and performs an IO control function on the device. The control functions used by SDLR device drivers are defined in the header file `io.h`. Most requests are passed on to the driver for handling. Since the availability of `ioctl` functions is driver-specific, these functions are implemented separately for each specific device.

The return value is the return value of the driver, or ERROR if the file descriptor does not exist.

read()

This routine reads a number of bytes (less than or equal to maxbytes) from a specified file descriptor and places them in a buffer. It calls the device driver to do the work.

The return value is the number of bytes read (between 1 and maxbytes, 0 if end of file), or ERROR if the file descriptor does not exist, the driver does not have a read routines, or the driver returns ERROR. If the driver does not have a read routine, errno is set to NOTSUP.

write()

This routine writes a number of bytes from buffer to a specified file descriptor. It calls the device driver to do the work.

The return value is the number of bytes written, or ERROR if the file descriptor does not exist, the driver does not have a write routine, or the driver returns ERROR. If the driver does not have a write routine, errno is set to NOTSUP.

The precise meaning of reading or writing from or to a device depends on the nature of the device. For example writing to an RF driver causes the data to be modulated over the output RF signal and reading from the RF driver, fills an input buffer with samples from an ADC chip. Reading and writing to or from some devices might be illegal. For example reading from the transmitter and writing to the receiver driver are illegal operations.

10.3.2 EPC Module

The EPC software module is entirely implemented on the DSP. It is based on EPC specifications and supports both EPC Class 0 and Class 1 protocols as well as ISO 18000-6 protocols. It is also designed to accommodate Generation 2 protocol by EPC Global (C1G2) by adding some variables in function calls.

This module consists of functions for generating EPC Class 1 Generation 1 commands such as *Ping, Global Scroll* and *Masked Scroll* and interpreting the tag reply. It can communicate with EPC 64-bit and 96-bit tag code structure and is capable of handing anti-collision protocols.

10.4 Conclusion

By minimizing the hardware requirements for different protocols and by implementing software modules that abstract away the differences between protocols, this reader achieves superior performance to most other solutions in terms of hardware cost and software flexibility.

This possibility has motivated the concept of the SDLR, whereby the digital-to-analogue and analogue-to-digital conversion are performed as close as possible to the radio frequency. The aim of this work was to extend the digital domain and to implement modulation, demodulation, channel coding and other required processing tasks in software.

Being software based allows it to be customized to end user needs. This design has a boot loader feature allowing a user to make changes to the code. It can be upgraded in the field thus lowering operating costs.

Chapter 11

Experiments On Tags and Protocols

Observation and measurement are central features of practical activity in science. Having completed the construction of an early prototyped of the SDLR and evaluated the most important performance aspects, a number of initial tests were performed. The first section of this chapter discusses the generic procedure pursued when performing an experiment, followed by a discussion of various other experiments and optimizations which are made possible using this instrument. The chapter also discuses the design and modeling of an anti-collision protocol based on the use of a beacon channel and several data channels.

11.1 Introduction

The design and construction of SDLR is covered in the previous chapters. This chapter is concerned with the applications of an early prototyped of the SDLR and how it can be used to improve the performance of RFID systems.

A data logging reader can be used for the purpose of collecting information and monitoring tag reading activities. It has the capability to be equipped with: temperature sensors, pressure sensors, strain, gauges, speed sensors, current loop transmitters, weather & hydrological sensors, laboratory analytical instruments and much more.

Having collected the information, one can look back on the past events and identify areas of interest viewing. These events could assist in improving: efficiency, performance, accuracy, reliability, quality assurance, etc.

The SDLR dedicated data logger has many inherent advantages over other alternatives for the bulk of data acquisition tasks. These include low power operation, standby power sources and security of data in the event of power or communications failure. Being specifically designed for the task, errors due to influences such as poor noise immunity and unstable operating systems are minimized. It also is able to process and forward data to a PC in real time.

11.2 Experimental Procedure

Prior to starting an actual data acquisition the instrument is calibrated and a self test is performed in order to check its stability and overall performance. The system must be temporally calibrated, which is usually done prior to any measurements. The data acquired from the instrument are usu-

ally pre-processed and transferred to a host computer for further processing and analysis.

11.2.1 Data Acquisition

Experiments are automatically executed under computer control according to a pre-defined data acquisition protocol. A decent PC processor can compute signal processing functions and rival many of the fastest DSPs on the market. Usually though, the PC processor is responsible for the user interface as well as other system management tasks and data acquisition is not the best use of PC resources. For an RFID data logging application where the task involves hard real-time constraints, the PC is unable to perform FFTs, adaptive filters, etc. As such, most of the low level signal processing tasks are performed within the on-board DSP and the results are transfered to a PC for further processing.

11.2.2 Communication Protocol Optimization

The emergence of RFID as a ubiquitous new technology allows automatic item management and requires the RFID readers to be instantly interconnected into ad hoc networks. These short range ad-hoc wireless networks, from hereon referred to as an EPC networks, operate in the unlicensed 915 MHz or 2.54 GHz ISM (Industrial-Scientific-Medical) band.

This operation creates interference on a reader from other devices operating in the same frequency band. Some devices include microwaves, mobile and wireless phones and devices enabling various wireless LAN standards. This section uses a signal capture model or data logging to study EPC protocol performance. Furthermore, simulations are used to validate the through-

put obtained from this model. These results reveal important performance implications of the effect of reader to reader interference on the throughput.

11.2.3 Timing Measurements

The SDLR has the capability to capture a complete time record of a tag reply. When a reader searches for tag it is referred to as *polling*. Should polling be delayed, it is possible to analyze the cause using SDLR. Also, associated with polling are number of timing measurements defined in RFID standards. One key measurement is turn-around-time, or the time it takes for a tag to reply after being queried by a reader. The SDLR is able to measure the time gap between the end of transmit from the reader to the start of the response from the tag. Figure 11.1 shows such timing measurements.

Baseband Recovery Time

Another important factor in RFID reader design is the baseband recovery time, which must be less than the tags' turn-around-time. The plot depicted in Figure 11.2 demonstrates the SDLR's transient recovery time. This measurement method has no tag present in the interrogation field. The base band signal has been generated by a signal generator transmitting a weak CW signal (-40 dBm), offset from the carrier (907.7 MHz) by amount equal to the desired baseband frequency (200 kHz). The plot in Figure 11.2 broadly resembles Figure 11.1, but shows the reader satisfies the requirements for correct measurement of the tag's turn-around-time.

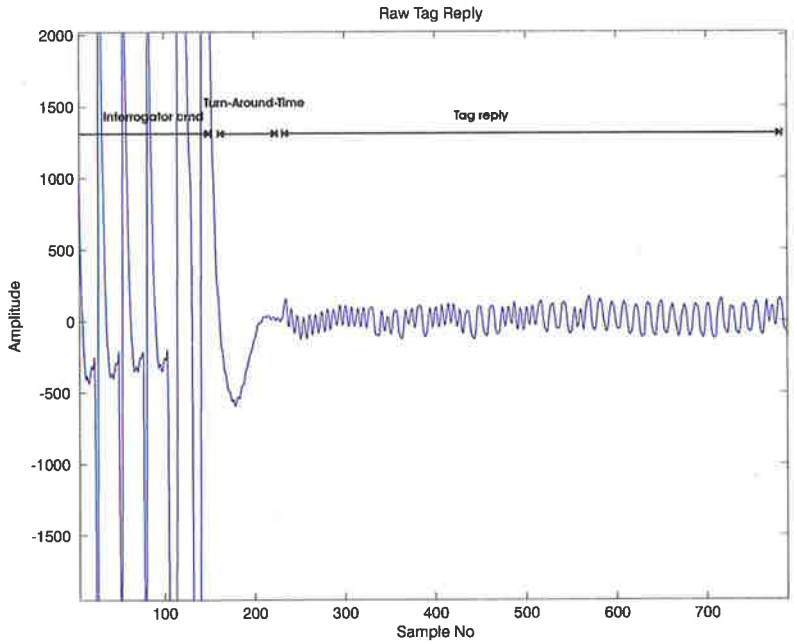


Figure 11.1: A plot showing reader command, tag reply and turn-around-time.

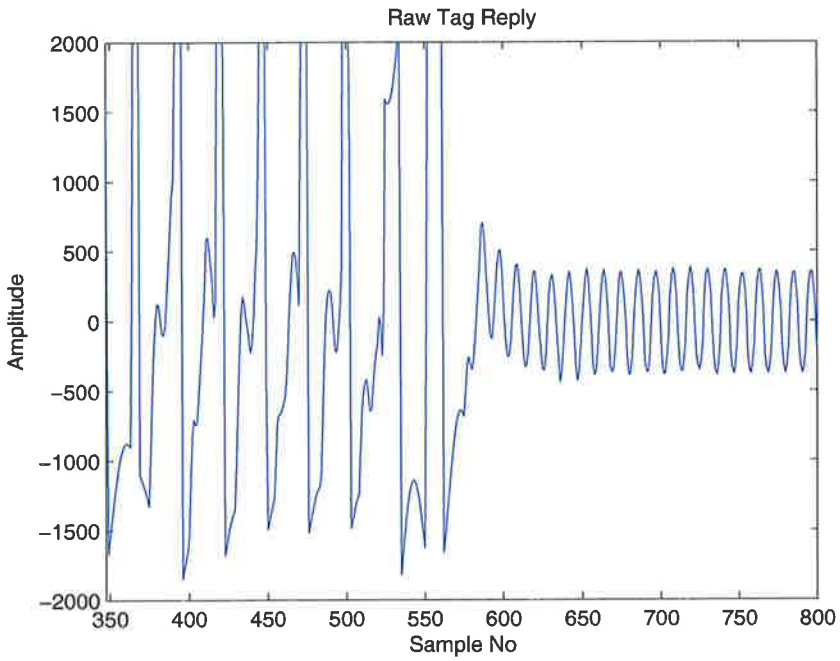


Figure 11.2: A plot showing the reader's baseband recovery time.

11.3 Read Range vs. Frequency

Placing tags in close proximity to conducting objects or other tags, bending their antenna structure or changing their antenna orientation can detune the tag antenna, preventing them from going into resonance, thus becoming inoperative or reducing their reading range. Consequently, frequency deviation and read range measurements are critical to ensuring compliance with various RFID standards.

Another experiment performed was to tune and optimize a novel antenna for beer kegs. This work has been done in collaboration with Ms. Mun Leng. The optimization was performed by changing the operation frequency of the reader and measuring the successful reading rang of the tags. Knowing the frequency that the tag replies with the strongest signal, we were able to determine its resonant frequency. From there we were able to modify the antenna design until the best performance was achieved at the middle of the UHF band.

If a tag is not operating at its resonance frequency or not matched to its antenna properly, it will not have enough power to complete its response to a reader command. Figure 11.3 shows a tag reply where the tag runs out of power as soon as it starts modulating the carrier signal, while Figure 11.4 shows a reply from the same tag after antenna optimization has been completed.

The performance of several tags has been tested when they are attached onto a beer keg. To observe the characteristic change of the tags' antenna, the results are then compared with the one measured when the tags are placed in free space. Both commercial and prototype tag circuits were used for this experiment. The parameter of interest is the maximum read range at output power of 1 W EIRP. The frequency at which maximum read range was

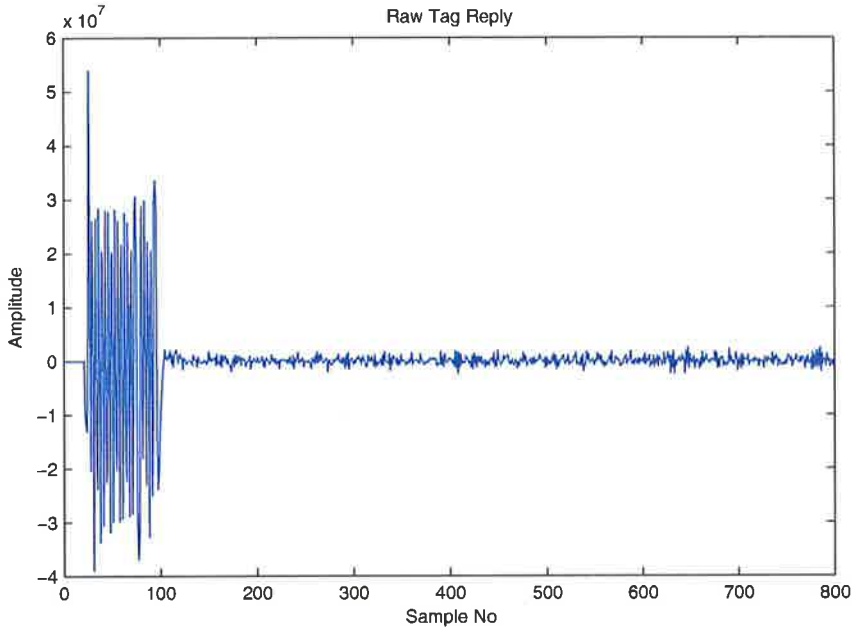


Figure 11.3: A short tag reply as a result of tag being detuned.

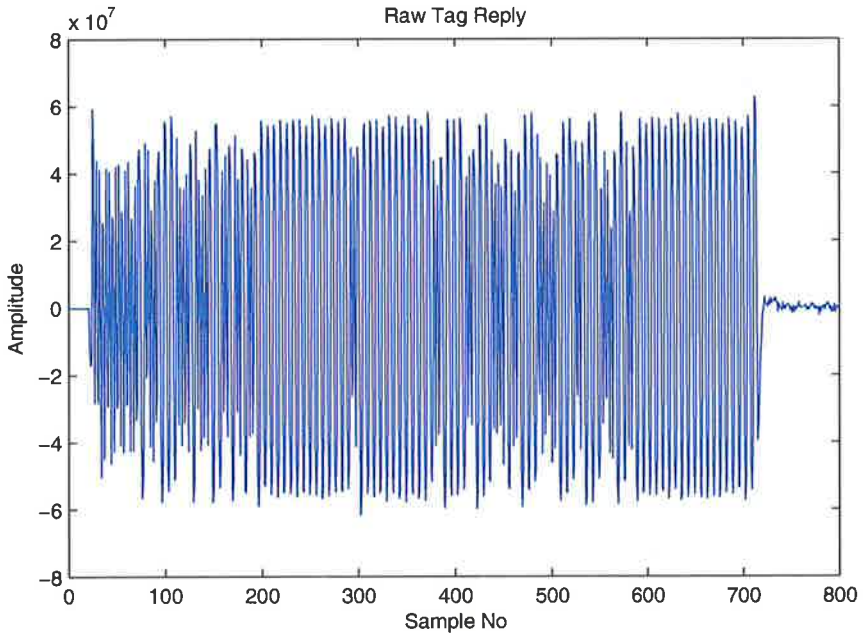


Figure 11.4: A complete tag reply recorded using SDLR.

achieved is also recorded. Table 11.1 shows the results of the measurements taken for 5 different tag antennas in free space.

Table 11.1: Read range (in cm) vs. frequency measurements in free space

Antenna Type	Frequency (MHz)					
	900.2	**907.9**	**915.6**	**923.3**	**931**	**938.7**
Square	26	21	26	30	25	10
Circular Loop	55	33	29	40	33	16
ALL-9250	100	108	104	125	125	72
ALL-9250 Folded	16	20	19	24	24	10
ALL-S	133	144	132	174	154	108

Although diligence in measurement has been exercised, the measurements are not absolute as reflection from objects surrounding the measurement area may have affected the results.

As can be seen from the above tables, the performance of the commercial antennas outperform the one designed in this lab. The principle reason is the size of the antenna. The ALL-9250 is 14 cm in length, while the Circular Loop antenna is only 2.5 cm in diameter. Another reason could be that the commercial tags have already gone through an intensive fine tuning process and are manufactured with high precision, while the prototype ones are suffering from systematic and random errors resulting from low precision measurements.

For all the tags used in this experiment, except for the ALL-9250, the

maximum read ranges obtained were actually better when the tags were placed onto the beer keg.

Table 11.2: Read range (in cm) vs. frequency measurements on a beer keg

Antenna Type	**Frequency (MHz)**					
	900.2	**907.9**	**915.6**	**923.3**	**931**	**938.7**
Square	16	19	33	45	32	14
Circular Loop	69	52	49	63	36	23
ALL-9250	78	95	92	106	104	68
ALL-9250 Folded	16	16	35	36	18	15
ALL-S	102	198	171	234	129	88

On average, the maximum read range of tags attached to the beer keg measured at approximately 923 MHz were as shown in Table 11.3.

Table 11.3: Maximum read range at optimum vs. frequency on a beer keg.

Antenna Type	**Read Range (cm)**
Square	45
Circular Loop	63
ALL-9250	110
ALL-9250 Folded	39
ALL-S	234

11.4 Reader Collisions and Phantom Tags

11.4.1 Introduction

Many applications require the readers to operate in close proximity to each other, that causes the signals from one reader to interfere with those of other readers. Reader to reader interference can occur in different situations.

One such a scenario arises when a strong signal from one reader, (say R2), interferes with the weak reply from a tag (T1) being interrogated by another reader (R1). The weak tag reply signal reaching reader R1 from tag T1, can easily get distorted by the signal from R2, as illustrated in Figure 11.5.

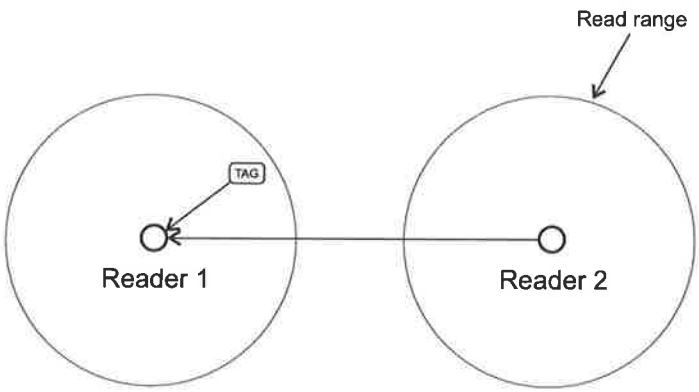


Figure 11.5: Reader interference with tag reply.

Another scenario might occur when multiple readers simultaneously try to read a tag which is located within their read range. This phenomena is known as tag confusion and comes in two varieties. It can occur as shown in Figure 11.6. For example when a hand-held reader tries to read a tag while a stationary reader is located close by. In such a situation the tag cannot decode the command from either reader and therefore might not be able to reply at all.

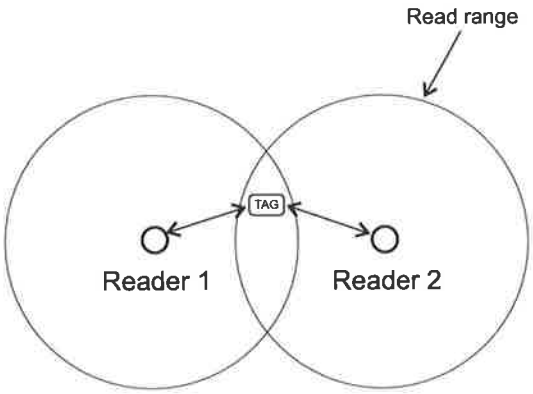


Figure 11.6: Tag Confusion case 1.

Such situations can occur even when both readers have implemented carrier sensing scheme and the sensitivity of that scheme is adjusted such that the RF transmitter fields of the readers still overlap but are not simultaneously active, refer to Figure 11.7.

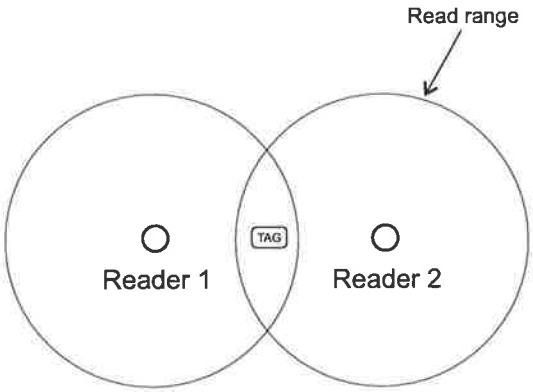


Figure 11.7: Tag confusion case 2.

Finally there is the phenomena known as reply collisions such as illustrated in simple form in Figure 11.8, where replies from two tags collide in a single receiver, or in more complicated form as illustrated in Figure 11.9, where replies from two tags collide in a single receiver but the tags are commanded from two different readers.

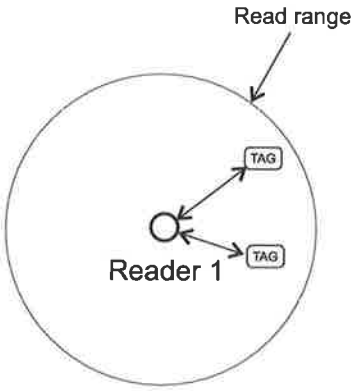


Figure 11.8: Reply collision.

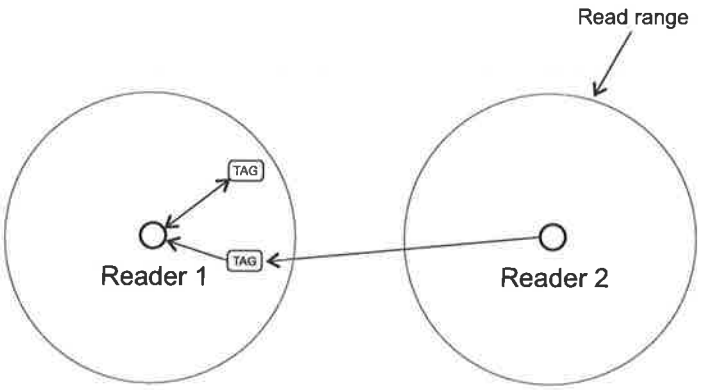


Figure 11.9: Reply collision with tag confusion.

This problem can be mitigated by separating the reader spectrum from the tag spectrum. But the extreme weakness of tag reply for passive tags means a high degree of transmitter signal filtering is required.

Reader and tag collisions, not only result in a reduction of over all read rate, but also aggravate other problems such as increasing bandwidth usage and causing security risks.

The SDLR has been used during this project to investigate reader collision phenomena and to develop a distributed protocol to mitigate this problem for RFID systems. Extensive simulation and measurement of the effectiveness

of the proposed protocol has been carried out using the SDLR reader and are reported later in this chapter.

The SDLR offers the ability to store signals in its internal memory for post-capture processing. This is very useful for measuring interaction with multiple tags in order to verify collision management. ISO 18000-3 section 6.2.7.9 indicates that a system must be capable of reading 500 tags within 390 ms. If only a PC and a dumb/ordinary reader are used to record the interaction and test for compliance, it is impossible to know if and at what point collisions have occured or if there is a particular tag that is being problematic. However, using SDLR, it is possible to monitor over the air interference of tag replies and troubleshoot when a collision occuring. Figure 11.10 shows the plot of a collision that has occured as a result of two tags replying simultaneously.

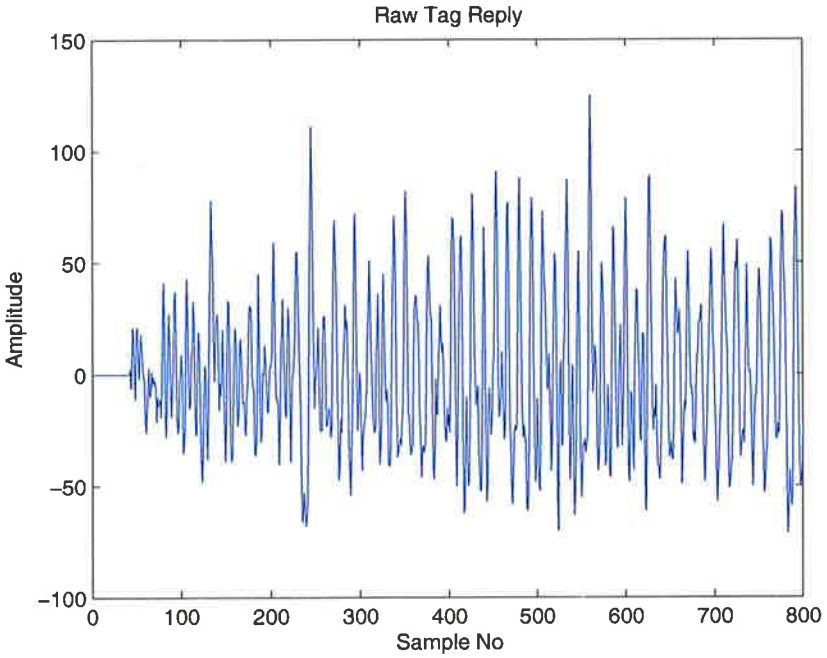


Figure 11.10: A plot of a collision between two tag replies.

11.4.2 Reader Collisions

As noted earlier it very difficult to use carrier detection techniques to solve reader collision problems. This is because a reader may not see another reader as their antennas might be placed at angle to one another (assuming directional antenna), while a tag located a distance from them can see both signals coming from each of the readers, as depicted in Figure 11.11.

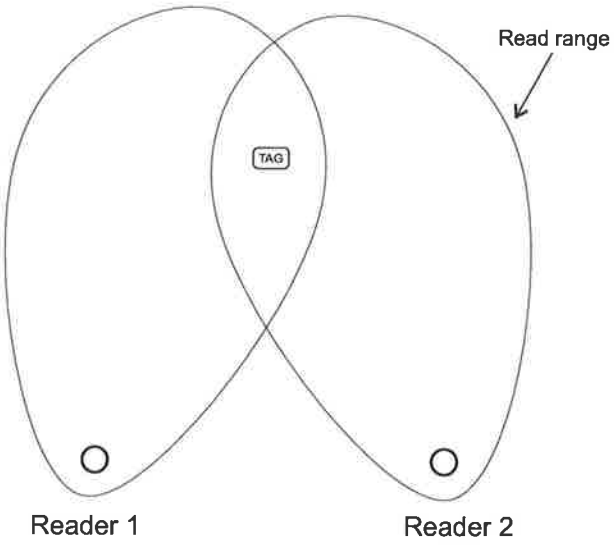


Figure 11.11: Reader configuration makes carrier sensing ineffective.

In such a scenario, the queries from multiple readers collide and signals interfere with one another at the tag level resulting in mis-interpretation of the commands by the tag. The assumption here is that the tags are passive and their circuitry is made as simple as possible. Therefore they cannot communicate with one another or with the readers in order to help with collision avoidance.

11.4.3 Existing Approach to Reader Collision

The latest RFID standards ratified by EPC Global [107] are known as Class 1 Generation 2 UHF (C1G2) [108]. These standards make use of a variety of Frequency Division Multiple Access (FDMA) protocols. This configuration separates the reader transmissions from the tag replies spectrally. As a result, tags may collide with tags and readers may collide with readers but no collisions between tags and readers occur. Such a protocol relies on the fact that readers and tags operate in separate frequency bands. The problem arises from the fact that tags do not have the ability to switch their operating frequency and as such if they are commanded from two different readers (at two different frequencies), the tags cannot tune to a particular frequency which results in tag confusion. Thus multiple readers to tag interference is still a real problem to consider. Also, such collisions can cause a reader to report the presence of a tag that doesn't exist. This phenomenon is called a phantom transaction or false read.

Another body developing standards for RFID in Europe is ETSI [12]. ETSI EN 302-308 [109] was developed based on Carrier Sense Multiple Access (CSMA) [113] protocol which is also known as "Listen Before Talk". In this standard a reader shall listen for an on going communication in the channel it wishes to transmit in for a specified minimum amount of time before it starts transmitting. If the channel is busy the reader must go to idle mode for a random amount of time before trying again. This method suffers from the same problem as C1G2 protocol as it relies on carrier sensing only.

11.4.4 Anti-Collision Protocol Format

In designing an anti-collision protocol for RFID readers we have to consider that the tags are passive and have a very simple circuitry and as such they will

not be able to participate in collision detection. Adding any more complexity to tags would results in increase in their price and would hamper their large scale deployment. Therefore in design of anti-collision protocols for readers, the only participant parties are readers not tags.

A simple yet effective method would be to have a notification mechanism whereby the readers can talk to one another and inform each other of their intention to perform a particular task, reading tags for example. This notification can be send through a broadcast message known as "beacon". The beacon needs to be transmitted on a separate control channel. The control channel can be a sub-channel of the spectrum used by RFID systems. A reader shall not use this particular channel for communicating with tags. The beacon signal should be designed such that it requires minimum amount of data transfer, thus consuming a small amount of bandwidth. The control channel is only used for reader-to-reader communication. The format of a basic beacon command is composed of three fields as shown in Figure 11.12.

Figure 11.12: Basic beacon command structure.

- **SPINUP:** Every basic command is prefixed by a series of logical zeros for timing synchronization. The reader/tag circuitry uses this part of the message to establish on board timing for reading and decoding messages and clocking subsequent replies.
- **CRC:** Is the CRC value of the command as defined in the EPC Global specification.

- **COMMAND:** Is an 8-bit field that specifies the command begin broadcast to all other readers. This 8-bit field yields up to 256 commands.

In this protocol as soon as a reader contends for a channel (wants to query a tag), it checks to be sure the data channel is clear (no other reader is transmitting at that time). This is achieved by listening for the beacon signal in the control channel for a period of time called the backoff factor, and is counted down by a backoff counter. If it receives no beacon, implying that the data channel is clear, each reader intending to interrogate tags, decrements its backoff timer. The reader whose timer expires first, starts interrogating the tags and the remaining readers stop their timers and defer their transmission. If the data channel is not clear, the reader resets its backoff timer to a randomly chosen value, and then checks again to see if the data channel is clear. If the data channel is clear when the backoff counter reaches zero, the reader communicates with the tags. If the data channel is not clear when the backoff counter reaches zero, the backoff factor is set again, and the process is repeated.

On the other hand a reader that is interrogating tags shall transmit a beacon signal on the control channel at a regular intervals. That would notify other readers of the status of the data channel thus avoiding possible collisions.

If after a predetermined amount of time, a reader does not receive any beacon signal then it concludes that there are no neighboring readers present at that location and hence it can operate as an stand-alone reader without being worried about interference from other readers. This is useful as an optimization factor in reader operation.

11.4.5 Simulation

The above Ethernet like protocol that we will call the ELRF protocol for UHF RFID network has been simulated in Matlab. The data channel frequency is set to 915 MHz and the control channel frequency is set to 930 MHz. Li [110] had implemented the similar CSMA protocol without a Collision Avoidance scheme. Li's original code was used as a basis of the simulation and few improvements have made to the code. The final simulation model has the following characteristics:

- No inter-channel interference between the data and the control channel.
- Free space propagation path loss.
- Packet collision only results in packet loss.
- All the RFID readers are equipped with omni-directional antennas.
- Data processing delay and the channel switching delay are negligible.
- The transmission power of the RFID readers is adjustable.
- Display of beacon packets.
- Number of DATA and ACK packet collisions.
- Number of mobile reader stations.
- Transmission range of each reader.
- Average transmission time as function of packet size.

In order to simplify the simulation task, some certain assumptions were made as follows:

- Distributed Control Function is in use.
- Propagation delay is assumed to be zero.

11.4.6 Theoretical Analysis and Modeling

This section presents a detailed analytic model based on a discrete time queuing technique which allows for evaluation of networks under consideration for general traffic arrival patterns and arbitrary number of readers.

This model considers the case where multiple readers use the protocol to share a wireless channel without a coordinating base station. It assumes that the stations are homogeneous in generating traffic, and channel noise is negligible. This analysis is similar to that used for IEEE 802.11 Random Access MAC analysis presented in [111, 114–117]. The analysis shows that the probability of collision, p, for small packets does not depend on the packet length and the physical layer. The maximum throughput S and p depends on the minimum window size W and the number of readers N, consequently halving W is like doubling N. The results suggest guidelines on when and how W can be adjusted to suit measured traffic, thus making the protocol adaptive. The analysis variables used in the following simulations are listed with their definition in Table 11.4.

Collision Probability (p): consider a scenario when there are sufficiently

Table 11.4: Glossary of terms used in modeling

Variable	Definition
W	Minimum contention window size
N	The number of readers in a location
$\overline{W}$	Average contention window size
p	Probability of a collision
W_{bf}	Backoff window size

many other readers in the environment, so that the transition from R1 to R2 is not synchronized, R1 could start transition anywhere along the timeline, so its probability of colliding with R2 is $1/W_{bf}$. The probability that R1 collides with any other reader can therefore be approximated as [111]:

$$p = 1 - \left(1 - \frac{1}{\overline{W}}\right)^{N-1} \tag{11.1}$$

Read Cycle (T_{read}): is defined as the time between two successful channel captures by a reader. A reader captures the data channel for a duration of T_{read}, during which the reader transmits multiple queries successively.

Backoff Time Decrement Interval (T_{bf}): is defined to be the time period after which the backoff value is decremented. Its value depends on three different scenarios, first; when there is no collision it has a value of 1 empty time slot ($T_e = 1$ [empty slot]). Second; when there is a collision, it needs to be one empty time slot plus one collision time slot, thus $T_c = 1$ [collision] + 1 [empty slot]. Third; when another reader is using the slot and it has a successful tag read, in such a case T_{bf} duration is $T_s = T_{rcad} + T_{min} +$ 1 [empty slot]

The probabilities of each of the these cases are derived next. A T_{bf} is said to be active if it contains a transition from at least one reader. The probability that a given T_{bf} is active is given by:

$$P_{active} = 1 - \left(1 - \frac{1}{\overline{W}}\right)^N \tag{11.2}$$

and the probability that T_{bf} contains a collision given that it is active is given by:

$$P_{collision|active} = \frac{1 - \left(1 - \frac{1}{\overline{W}}\right)^N - \frac{N}{\overline{W}} - \left(1 - \frac{1}{\overline{W}}\right)^{N-1}}{1 - \left(1 - \frac{1}{\overline{W}}\right)^N} \tag{11.3}$$

Thus, the probability that a T_{bf} contains a collision is

$$\begin{aligned} P_c &= P_{collision|active} \times P_{active} \\ &= 1 - \left(1 - \frac{1}{\overline{W}}\right)^N - \frac{N}{\overline{W}}\left(1 - \frac{1}{\overline{W}}\right)^{N-1} \end{aligned} \tag{11.4}$$

Similarly the probability that a given T_{bf} contains a successful transmission is:

$$\begin{aligned} P_s &= P_{success|active} \times P_{active} \\ &= \frac{N}{\overline{W}}\left(1 - \frac{1}{\overline{W}}\right)^{N-1} \end{aligned} \tag{11.5}$$

Therefore the average duration of T_{bf}, using the theorem of total probability is given by [112]:

$$T_{bf} = P_e T_e + P_s T_s + P_c T_c \tag{11.6}$$

Backoff Window Size (W_{bf}): As discussed earlier a reader might transmit and collide with probability p, after which it chooses a random backoff time value from 0 to W and transmits when the backoff counts down to 0. This goes on until it has a successful beacon transition. Thus the number of transition attempts can be modeled as a geometric distribution with success probability of $(1-p)$. Therefore the expected value of backoff window size is given by [111]:

$$\begin{aligned} W_{bf} &= (1-p)\frac{W}{2} + p(1-p)^2\frac{W}{2} + p^2(1-p)^2\frac{W}{2} + ... \\ &= \frac{W}{2(1-p)} \end{aligned} \tag{11.7}$$

The average read cycle duration can now be given by:

$$T_{cycle} = T_{bf} \times W_{bf} + T_{read} \tag{11.8}$$

Throughput (S): Let us assume that each reader is allowed to communicate with tags for a maximum of x beacon intervals. Therefore T_{read} has x time-slots and each time-slot consists of one beacon transmission on the control channel and several transmissions on the data channel. Thus each read cycle, T_{read} consists of:

$$T_{read} = ([t_q + l_q] \times Q_r) + x\,[t_b + l_b] \tag{11.9}$$

where Q_r is the number of queries sent by a reader in time T_r, l_b is the beacon length and t_b is beacon turn-around-time. l_q is the query length on data channel and t_q is the data channel turn-around-time.

The average number of all queries sent by all readers in one second which can be interpreted as system throughput is given by:

$$S = \frac{Q_r \times P_s \times W_{bf}}{T_{cycle}} \tag{11.10}$$

Utilization (U): is defined as the ratio of total time spent by all the readers in communicating with tags to the total time duration of a cycle.

$$U = \frac{T_{read} \times P_s \times W_{bf}}{T_{cycle}} \tag{11.11}$$

11.4.7 Simulation Results

For simulation we use MATLAB. For simplification it is assumed that there is inactive terminal and no noise in the system. It is also assumed that the readers are not in saturation and that they always have a query to send to tags. The duration of a collision is exactly one beacon interval. In reality a reader might detect a collision in a data channel and can retreat from operation, which in fact saves time and bandwidth. A list of parameter values used in this analytical simulation is shown in Table 11.5.

Figure 11.13: System analytical simulation results

N	$\overline{W}$	p	W_{bf}	P_c	P_e	P_s	T_{bf}	T_{cycle}	U	S
2	16	0.06	17	0.004	0.12	0.88	0.4755	12.1157	0.660302	1833.74
4	16	0.18	19	0.022	0.21	0.77	0.8321	20.1592	0.793683	2204.16
8	16	0.36	25	0.085	0.32	0.6	1.2832	36.2564	0.882603	2451.1
16	16	0.62	42	0.26	0.38	0.36	1.5312	68.5063	0.934221	2594.45
32	16	0.86	120	0.6	0.27	0.13	1.0940	133.428	0.959318	2664.15
64	16	0.98	930	0.92	0.07	0.02	0.2849	269.896	0.948513	2634.14
128	16	1	5800	1	0.002	0.0003	0.0188	1097.66	0.4664	1295.38

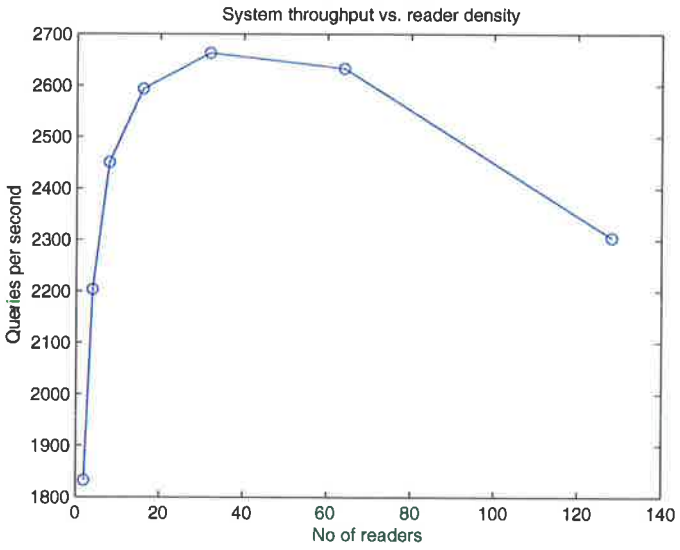


Figure 11.14: System throughput versus number of readers in the field.

Table 11.5: Parameter values used in the simulation

Variable	Value
W	32
T_{bi}	5000 μs
T_{min}	$3 \times T_{bi}$
T_{read}	4 s
l_b	265 μs
t_b	1 μs
l_q	345 μs
t_q	1 μs

The observations deduced from the simulation can be summarized as follows:

- For small number of readers, P_e is high, as there are many slots that are empty and there are a small number of collisions in the system.
- A N increases, there are more readers to transmit and hence P_e decreases resulting in increase in P_s. Therefore the system throughput increases as well, however some readers now experience collisions and their successful read rate decreases.
- The utilization can reach up to 95%.

11.4.8 Conclusion

In this section we presented and evaluated the performance of a novel ELRF anti-collision protocol. The performance evaluation is done by developing a queuing model for each reader in the network.

The ELRF protocol has been designed such that any two readers that

might interfere with one another on the data channel, are still able to communicate using the control channel. This can be achieved by making the readers transmit at a higher power on the control channel than the data channel. The control channel can be a sub-band in the RFID spectrum.

The Australian regulatory bodies have granted an Australia wide experimental license for up to 4W EIRP, in the band 920 to 926 MHz. The readers in Australia have to comply with 1 Watt EIRP if they operate in 918 to 920 MHz. Hence the control channel can be set to a sub-channel from the top of the spectrum. For ELRF protocol to operate efficiently, it is assumed that a reader is able to simultaneously receive on both the control and the data channel.

The system throughput obtained from the simulation shows very promising results. At this stage the author was able to perform experimental evaluation of the proposed protocol with only two readers. This shortcoming is due to the time restriction and shortage of parts and equipment.

Chapter 12

Conclusions and Future Work

12.1 Summary of contribution

Passive transponder read range, multiple label reading and read accuracy capability are the three most important characteristics of an RFID system. In this dissertation we investigated many features of those topics.

Passive labels derive their power source by rectifying the interrogator RF signal, therefore they require an efficient rectifier circuit. In this work, a novel Schottky Barrier Diode on a standard CMOS process has been designed, fabricated, tested and characterized. The first generation of the device suffered from excessive junction capacitance. This was corrected in the second generation by scaling down the geometry, optimizing junction area, paying attention to layout parasitics, using p^+ guard rings and implementing a multi-finger configuration. This resulted in substantial improvement in extending the RC cut-off frequency of the SBD, reduce parasitics, reduce loss and increase efficiency from 9% to almost 20%.

Those improvements allowed the RFID tags to function correctly under

small, unreliable and highly variable power supplies that can be extracted from the interrogation field of an RFID system. It should be noted that designing circuits for these constraints involves designing for a context which is utterly different from normal microelectronic design, and that there is very little published work on this subject.

The build of SBD has been refined from an early fabrication using an AMI 1.5 μm process to a later fabrication using the Charted Semiconductor 0.35 μm process. The latter work is documented in Chapter 3 to allow other investigators to check and continue this work.

Also, critical circuits of RFID transponder tags and an RFID interrogator have been built in order to realize some of the potential promised by the Schottky Barrier Diode. These circuits are shown in photo-micro-graph of Figures 4.18 and 4.19. Their testing is regarded as future work.

A new software based RFID reader architecture has been designed and constructed with a real time data logging capability for post-capture processing. This feature allows the evaluation and optimization of RFID communication protocols, optimization of tag antenna and matching circuits and makes it possible to manage and troubleshoot when a collision occurs either within a multi-transponder environment or with other interrogators. It allows a developer to analyze and understand the interrogator and transponder behaviour.

As RFID systems proliferate, reader density will increase and the likelihood of interference between readers will subsequently increase. Such interference can be very harmful to the integrity of communication systems. Thus the SDLR has been used to test, develop and optimize a novel ELRF anti-collision protocol for RFID systems. The system throughput obtained from the simulations shows very promising results.

In the area of electromagnetic radiation and propagation, there are situations that need more exploration. In logistic applications, for example, the environment typically includes a great deal of metal. This can cause problems in time varying EM fields, and can affect the over all performance of the system significantly. Antennas allow many degree of freedom in their configuration. The SDLR has also been used to optimize tag antenna geometry and study the effects of the environment on its performance.

12.2 Suggestions for further work

The function of this section is to provide a succinct summary of suggested future work. Research in the RFID area can be followed in several paths. At circuit design level, new circuits for performing signal conditioning and processing in more efficient ways are required. At the architectural level, methods for improving integration of different circuit parts are needed. In the following some of the major issues that require further study and research are highlighted.

Transponder circuits are a combination of analog and digital VLSI circuits. The analog part must be highly sensitive to detect small variations in signal level, in order to be able to demodulate the incoming signal. Although, design of such circuits by itself is straight forward, problems arise when the chip contains both analog and digital signals, as the noise generated by switching of the digital circuit can easily dominate the weak input analog signal. Separating analog and digital circuits can provide a solution, but for a transponder circuit, which is required to be monolithic, such a solution is impractical. Another solution would be to decrease the sensitivity of the analog circuit, which defeats the long range transponder idea.

Even though I have done much work on RFID reader architecture, I think there are still areas that should be addressed. At most of the frequencies there are differences in bandwidth and there are field strength limitations between different regions. Use of different coding techniques and modulation methods should be studied further. Filtering techniques can be used to shape the pulses before the modulation stage. Spectral shaping, i.e. using shaped pulses rather than pure square pulses should be studied more as it can help to reduce the bandwidth even further.

Another area which needs more attention is the mixing stage in the reader. Balanced and unbalanced mixers should be studied further as they play an important role in distinguishing between a strong transmitted field from the reader and a weak reply from the tags.

Appendix A

Semiconductor Diode Properties

This appendix section provides the theoretical aspects of semiconductor theory relevant to the thesis and introduces the concept of Schottky diodes and their electrical activity. Further, an introduction to semiconductor theory, which forms the foundation for the interpretation of the Schottky diode property measurements, is given.

A.1 Introduction

A Schottky diode is a special type of diode with a very low forward-voltage drop. When current flows through a diode, it has some internal resistance to that current flow. The two major reasons for this internal resistance are the Ohmic loss in the material and the diode's barrier potential difference. The internal resistance causes a small voltage drop across the diode terminals. A normal diode has a voltage drop between 0.7-1.7 V, while a Schottky diode has a voltage drop between approximately 0.15-0.45 V and this lower voltage

drop translates into higher system efficiency.

Another problem with a pn junction diode is the junction capacitance effect, which becomes more and more dominant at high frequencies. In a pn junction diode, current conduction is carried by minority carriers. On the other hand, the dominant transport mechanism in a Schottky diode is due to majority carriers. We will discuss this further towards the end of the chapter.

Therefore Schottky diodes have favorable characteristics in high frequency applications, and have been widely used in various of RF circuits. However, it is not easy to implement Schottky diodes in normal CMOS processes. It requires many extra steps during the lithography process, which increases the cost of the chip.

This chapter describes aspects of semiconductor theory and introduces the concept of doping and the resulting electrical properties [37], [38], [40]. We consider the capture and emission processes responsible for the electronic interactions of energy levels within the conduction band and the valence band. Finally, the influence of dopant within a semiconductor is described in some detail [41]. We will consider the theoretical background of semiconductor diodes and will cover all the areas such as forward voltage and junction capacitance in detail.

A few sections of this chapter have been expanded to provide supplementary background information for some of the later chapters.

A.2 Current flow in semiconductors

Silicon is an example of a semiconductor. Silicon has a diamond lattice structure in which each silicon atom is surrounded by four nearest neighbor atoms forming a regular tetrahedron as shown in Figure A.1. The silicon lattice constant is 5.43 Å.

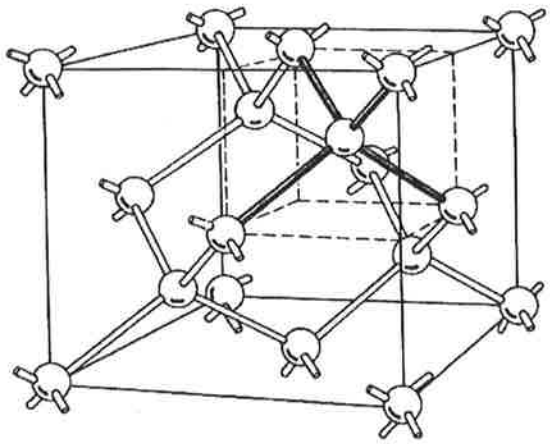


Figure A.1: Diamond crystal structure [38].

A crystal of pure silicon has a regular structure where atoms are held in their position by atomic bonds, called covalent bonds. This is formed by four valence electrons associated with each silicon atom. At room temperature, some of these bonds are broken by thermal ionization and some electrons are freed. A free electron can move through the silicon crystal structure. At the same time, the atom that lost one electron can attract an electron from one of its neighboring atoms. The absence of an electron in the valence band is called a hole. The process of stealing a neighbor's electron can be continued, so the hole can move all over the crystal. A hole behaves very much as if it were a carrier with a charge of opposite to that of an electron.

Semiconductors such as silicon have properties somewhere between those of a conductor and an insulator. The ability of a semiconductor to conduct electricity can change dramatically by doping. Doping is the process of adding impurity to the semiconductor. There are two basic types of semiconductor, n-type and p-type. A semiconductor crystal is made n-type by the addition of an impurity element with a large number of free electrons (negative charge carriers) available for conduction. Each impurity atom is called a donor atom since it donates an electron. The electron is free to move and can contribute to the conduction current.

A semiconductor crystal can be made p-type by doping it with a different element so that there are a large number of positive charge carriers available for conduction. The positive charges actually correspond to vacancies or deficiencies of electrons in the bonds holding the atoms in the crystal lattice. These positive charges are called holes. The holes can move through the lattice as well, but their movement in fact is due to the movement of a bound electron from one bond to another.

In a n-type semiconductor, most of the mobile carriers are electrons. For that reason electrons are called majority carriers in an n-type semiconductor and holes are called minority carriers. Similarly, holes are the predominant mobile charge carriers in a p-type semiconductor, so holes are called majority carriers and electrons minority carriers.

An electric current can flow in a semiconductor as a result of movement of holes and/or electrons. There are two important processes that cause current flow in a semiconductor; drift and diffusion. Drift occurs as a result of applying an electric field while diffusion currents result from a non-uniform charge distribution.

A.2.1 Drift Process

Applying an electric field across a semiconductor will cause electric charges to drift through the crystal lattice. The total electric current produced by an electric field in a semiconductor is the sum of the currents carried by the holes and electrons, thus;

$$J_{drift} = q(p\mu_p + n\mu_n)E \tag{A.1}$$

The coefficient of E in this result is simply defined as the electrical conductivity, σ, of the semiconductor:

$$\sigma = q(p\mu_p + n\mu_n) \tag{A.2}$$

where $q = 1.6 \times 10^{-19}$ C, is the magnitude of the charge of an electron, μ_n is the mobility of electron, μ_p is the mobility of holes, having the unit of $m^2/(Vs)$, n and p are the electron and hole concentration respectively. The total current is equal to the sum of hole current (to the left) and electron current (to the right) as shown in Figure A.2.

A.2.2 Diffusion Process

A drop of ink in a glass of water diffuses through the water until is evenly distributed. The same process, called diffusion, occurs in a semiconductor. If some free electrons are introduced into a semiconductor, these free electrons will distribute themselves so they have a uniform concentration. In this example, electrons will move from the region of high concentration to the lower concentration area. The higher the localized concentration, the greater the diffusion rate will be. The same is true if we were to introduce free

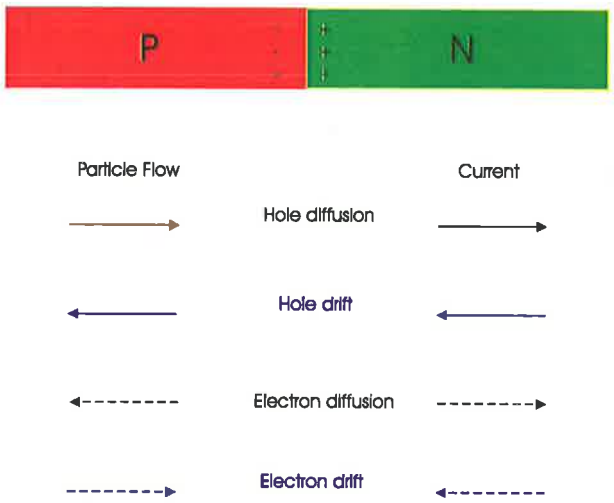


Figure A.2: Direction of the four components of particle flow within the transition region, and the resulting current.

holes into a semiconductor. The diffusion current crossing a unit area is give by [42]:

$$J_{diff} = -q(pD_p\frac{dp}{dx} + nD_n\frac{dn}{dx}) \tag{A.3}$$

Where $q = 1.6 \times 10^{-19}C$, is the charge of an electron, D_n and D_p are the electron and hole diffusion coefficient respectively with unit of cm^2/s.

A.2.3 Simultaneous presence of drift and diffusion currents

In a semiconductor material both drift and diffusion currents are simultaneously present. For a small deviation from equilibrium it is reasonable to regard the total hole or electron density as a linear combination of the drift and diffusion current densities. Thus the net hole current density can be

written as;

$$J_p = q(p\mu_p E - D_p \frac{dp}{dx}) \tag{A.4}$$

and the nett electron current density can written as:

$$J_n = q(n\mu_n E + D_n \frac{dn}{dx}) \tag{A.5}$$

This description of hole and electron motion in non-equilibrium situations in terms of drift and diffusion can be justified in detail in terms of statistical-mechanical concepts and techniques [52].

A.3 pn Junction Diode

Let us consider separate regions of p and n-type semiconductor material, brought together to form a junction. Before they are joined, the n material has a large concentration of free electrons and few holes, whereas the converse is true for the p material. Upon joining the two region, diffusion of carriers take place because of the large concentration gradients at the junction. As soon as a junction is formed, free electrons from the n-type block will diffuse across the junction to the p-type side where they will combine with some of the holes in the p-type material. Similarly holes from p-type will diffuse across the junction in the opposite direction and recombine with electrons on the n side. However, this process cannot continue indefinitely, because an opposing electric field is created at the junction.

It is interesting to note that within the depletion region there are very few mobile charge carriers of any type, so the drift current would be small,

despite the strong electric field, as the carrier concentration is very small. For the same reason, the gradient of charge concentration is small, and the diffusion current is almost zero. So, in fact, the balancing between drift and diffusion takes place at the edge of the depletion region where we are making the transition between regions of significant charge concentration and substantial electric field.

A.3.1 The Contact Potential

Recombination of electrons and holes in the vicinity of the junction leaves a narrow region on either side of the junction that contains no mobile charge. This narrow region which has been depleted of mobile charges is called depletion layer or *transition region* W. It extends into the both n-type and p-type regions. There is then a separation of fixed positive charges (which are un-compensated donors, left behind) on the n-type and fixed negative charges on the p-type. This separation of charges causes an electric field to extend across the depletion region. A potential difference must therefore exist across the junction. This potential difference (opposing electric field) does not allow the resulting diffusion current to build up indefinitely.

The resulting electric field is directed from the positive charge towards negative charge. Thus E is in the direction opposite to that of diffusion current for each type of carrier. Therefore the field creates a drift component of current from n to p, opposing the diffusion current.

Since we know that no nett current can flow across the junction at equilibrium, the current due to the drift of carriers in the E field must exactly cancel the diffusion current. Therefore the electric field E builds up to the point where the nett current is zero at equilibrium. The electric field appears in some region W about the junction, and there is an equilibrium potential

difference V_0 across W. The potential difference V_0 is called *contact potential.* For a typical silicon pn junction diode, V_0 is about 0.7 volts. It varies with doping concentration and temperature.

The importance of this built-in potential is that it hinders the flow of holes and electrons across the junction. For this reason the built-in potential is called a potential barrier or potential hill. In practice a pn junction is formed within a single crystal rather than joining two pieces together. The resulting device is called a pn junction diode.

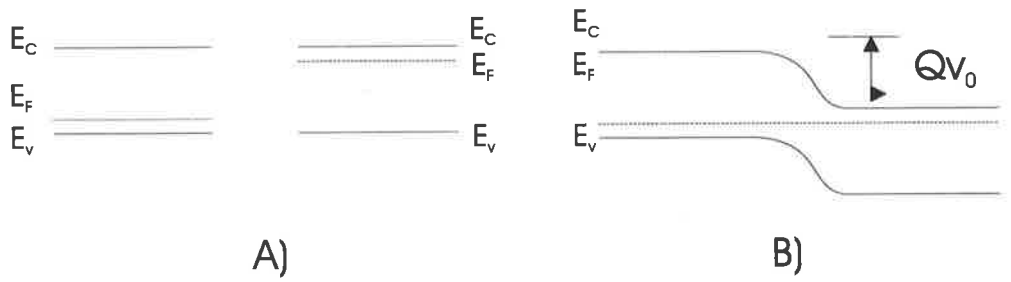


Figure A.3: Junction showing contact potential and the resulting separation of energy bands. a) before and b) after junction is made.

The contact potential separates the bands as in Figure A.3; the valence and conduction energy bands are higher on the p-side of the junction than on the n-side by the amount qV_0. The separation of the bands at equilibrium is just that required to make the Fermi level constant throughout the device.

To obtain a quantative relationship between V_0 and the doping concentration on each side of the junction, we use the requirements for quasi-equilibrium in the drift and diffusion current equations. The drift and diffusion components of the hole current cancel at equilibrium, so:

$$J_p(x) = q[\mu_p p(x)E(x) - D_p \frac{dp(x)}{dx}] = 0 \qquad \text{(A.6)}$$

where the x direction is arbitrarily taken from p to n. The electric field can be written in terms of the gradient in the potential, $E(x) = -dV(x)/dx$, so Equation A.6 can be written as

$$-\frac{q}{kt}\frac{dV(x)}{dx} = \frac{1}{p(x)}\frac{dp(x)}{dx} \tag{A.7}$$

In the above we made use of the *Einstein relation*, $\frac{KT}{q} = \frac{D}{\mu}$. The Equation A.7 can be solved by integrating both sides over the appropriate limits. In this case the limits would be the potential on either side of the junction which are V_p and V_n, and hole concentration just at the edge of the transition region on either side, p_p and p_n. Integration of the above equation gives the potential difference V_0 in terms of the equilibrium hole concentrations on either side of the junction:

$$V_0 = \frac{KT}{q}\ln\frac{p_p}{p_n} \tag{A.8}$$

If we consider the step junction to be made up of material with N_a acceptors/m^3 on the p side and concentration of N_d donors on the n side, we can write the above equation as:

$$V_0 = \frac{kT}{q}\ln\frac{N_a N_d}{n_i^2} \tag{A.9}$$

Here we are considering the majority carrier concentration to be the doping concentration on each side. Another useful form of the Equation A.8 is given below, this is very valuable in calculation of the I-V characteristic of the junction.

$$\frac{p_p}{p_n} = \frac{n_n}{n_p} = e^{qV_0/kT} \tag{A.10}$$

A.3.2 Space-charge at a junction

Within the transition region, electrons and holes are in transit from one side of the junction to the other. Some electrons diffuse from n to p side, some are swept by the electric field from p to n side (conversely for holes). There are however very few free carriers within the transition region at any given time as the electric field across the junction serves to sweep out carriers which have wandered into transition region, W.

Therefore we can consider the space charge within the transition region as due only to un-compensated donor and acceptor ions. The charge density on the n side is just q times the concentration of donor ions N_d, and the negative charge density on the p side is $-q$ times the concentration of the acceptors N_a.

Since the dipole about the junction has equal number of charges on either side of the junction, the transition region may extend into the p or n side *unequally*, depending on the relative doing of the two sides. For example, if the p side is more heavily doped than the n side, the space charge region must extend farther into the n material than into the p material, to uncover an equivalent amount of charge.

An expression for the width of the transition region in terms of the contact potential, the doping concentration, and constants q and ϵ is given by [42]:

$$W = [\frac{2\epsilon V_0}{q}(\frac{N_a + N_d}{N_a N_d})]^{\frac{1}{2}} \tag{A.11}$$

The transition region extends farther into the side with lighter doping concentration. For example, if $N_a << N_d$, position x_{p0}, of the boundary on the p-side is larger than the position x_{n0}, of the boundary on the n-side. Another important result of Equation A.11 is that the transition width varies

as the square root of the potential across the region. Therefore an applied external voltage can be used to increase or decrease the potential across the transition region by aiding or opposing the electric field.

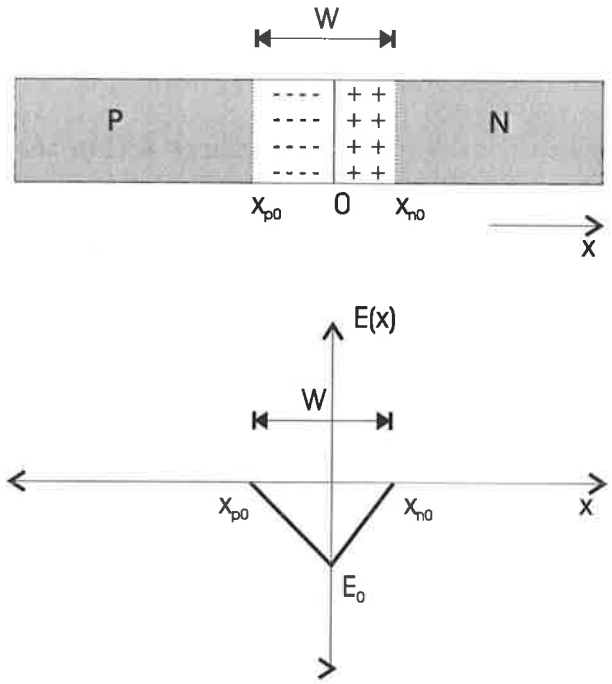


Figure A.4: Space charge and electric field distribution within the transition region of a pn junction diode.

A.3.3 Current Flow at a Junction

When the n-side of a diode is connected to negative terminal of a battery and p-side is connected to positive terminal, the diode is said to be forward biased. The application of forward bias voltage to a junction diode reduces the built-in potential for V_i to $V_i - V$. This reduction of built-in potential is due to the applied voltage forcing more electrons into the n-type region and

more holes into the p-type region, thus covering some of the fixed charges and narrowing the depletion layer. As the built-in potential opposes the flow of majority carriers across the junction, a reduction in built-in potential makes it easier for the carriers to cross the junction. That causes the current through the junction to become greater. When the applied forward voltage reaches the potential barrier of a diode, the potential hill is almost removed. There is then little opposition to the flow of carriers across the junction and a large current can flow through the diode.

As the electric field within the transition region is deduced from the potential barrier, we notice that the field decreases with forward bias, since the applied electric field opposes the built-in field. With reverse bias the field at the junction increases, which is in the same direction of the equilibrium field.

The change in electric field at the junction calls for a change in the transition region width, W. Thus we would expect the width W to decrease under forward bias and to increase under reverse bias.

The diffusion current is composed of majority carrier electrons on the n side surmounting the potential energy barrier to diffuse to the p side, and holes surmounting their barrier from p to n. At equilibrium there is a distribution of energy for electrons on the n side conduction band, and only small number of electrons have enough energy to diffuse across the barrier. With forward bias, however, many more electrons in the n-side have sufficient energy to diffuse from n to p over a small barrier. Therefore the diffusion current can be quite large with forward bias. Similarly more holes can diffuse from p to n under forward bias because of the lowered barrier potential. For reverse bias the barrier becomes so large that virtually no carriers have enough energy to surmount it. Therefore the diffusion current is usually negligible for reverse bias.

Therefore drift current is small, not because of the size of the barrier, but because there are very few minority electrons in the p side to participate. Every electron on the p side that diffuses to the transition region will be swept down the potential energy hill, whether the hill is large or small. Similar comments apply regarding the drift of minority holes from the n side to the p side. To a good approximation drift current at the junction is independent of the applied voltage. The supply of minority carriers on each side of the junction required to participate in the drift component of current is generated by thermal excitation.

The drift current is therefore relatively insensitive to height of the potential barrier, because the drift current is limited not by *how fast* the carriers are swept down the barrier, but rather *how often.*

In summary, the most important thing to remember about the pn junction diode is its ability to offer very little resistance to current flow in the forward bias condition but maximum resistance to current flow when it is reverse biased. A pn junction diode is called a minority carrier device as electric current in a pn junction diode is mainly due to the diffusion of minority carriers on either side of the junction.

A.4 The Schottky Barrier Diode

A.4.1 Introduction

For power rectification diodes there are two main device structure concepts:

- **pn diode**
  Bipolar diode that offers low leakage current but shows reverse recovery current charge during switching as a consequence of minority (holes)

and majority (electrons) carriers both being involved in the current conduction.

- **Schottky diode**
  Unipolar diode that offers extremely high switching speed, but suffers from high leakage current. A unipolar diode means that the current conduction is governed only by majority carriers (electrons).

Schematic cross sections of Schottky and PN diode structures are shown in Figure A.5.

A Schottky diode is formed when a metal layer is directly deposited onto a n or p type semiconductor region. When the two materials are brought into contact to one another, the difference in potential gives rise to a barrier potential height that the electrons have to overcome for the current to flow. The metal connector is called the anode and the semiconductor is the cathode. This type of diode is called Schottky Barrier Diode. In forward conduction mode, the current flows through the conductive channel under the Schottky contact with a voltage drop determined by the metal semiconductor Schottky barrier height.

In the next few sections we represent theoretical techniques used for characterization of Schottky barrier diodes.

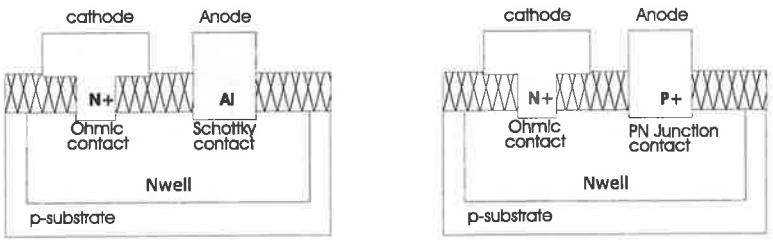


Figure A.5: Cross sectional view of a planar Schottky and p^+n junction Diode.

A.4.2 Energy Bands

A Schottky diode is formed when a metal of work function $q\phi_m$ and a n-type semiconductor of electron affinity $q\chi_n$ and work function $q\phi_s < q\phi_m$ are joined. The work function is defined as the energy required to excite an electron from the Fermi level to the vacuum level. The electron affinity is defined as the energy required to excite an electron from the conduction band to the vacuum level. The different position of Fermi levels in the two isolated materials causes the diffusion of electrons from the semiconductor to the metal, leaving behind un-compensated donor ions in a depleted space charge region. In thermodynamic equilibrium, the energy band diagram of a Schottky diode is constructed from the requirements of constant Fermi level and continuous vacuum level, as illustrated in Figure A.6. In the ideal case, the Schottky barrier from the metal to the semiconductor is given by $q\phi_B = q(\phi_m - \chi)$. This barrier height prevents metal electrons from injecting into the semiconductor conduction band. On the other hand, the built-in potential barrier from the semiconductor to the metal V_{bi}, which prevents further net electron diffusion from the semiconductor conduction band into the metal, is given by:

$$V_{bi} = \phi_m - \phi_s \tag{A.12}$$

which makes V_{bi} a slight function of the semiconductor doping, as was the case in a p^+n junction diode.

An externally applied bias will disturb the fine balance of electron transport across the junction and allow a net current to flow through the device. The junction is forward biased if a positive voltage V_f is applied to the metal with respect to the semiconductor. The junction is reverse biased if a positive voltage V_r is applied to the semiconductor with respect to the metal. The total potential across the junction is reduced to $V_f - V_{bi}$ in forward bias and

increased to $V_{bi}+V_r$ in reverse bias, while the Schottky barrier is only weakly dependent on the applied bias. Real Schottky diodes show some deviations from this simple model but the above description is adequate for our purpose.

The current-voltage characteristics of a Schottky diode is similar to that of a p^+n junction diode. While the properties of the Schottky barrier depletion region are similar to that of p^+n, it is clear that the analogy does not include forward bias hole injection, therefore the current mechanism here is due to the flow of the majority carrier electrons. The current flow is an exponential function of the forward bias voltage V_f.

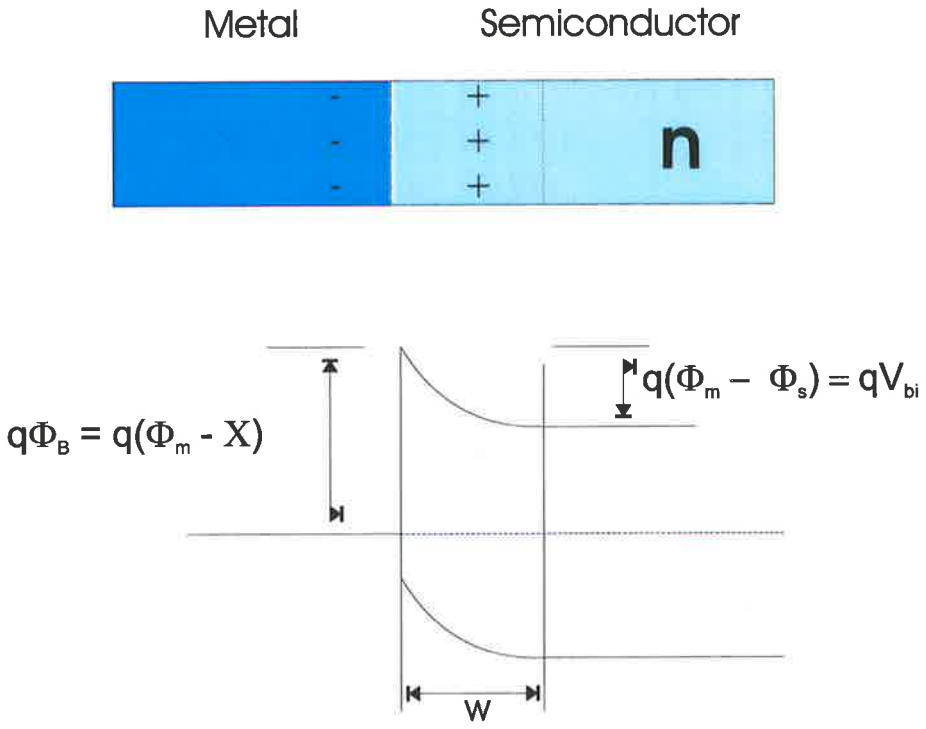


Figure A.6: Energy band diagram of a Schottky diode in thermodynamic equilibrium.

A.4.3 Space Charge Region

The space charge region is characterized by the presence of un-compensated space charge due to partial or complete depletion of free carriers. We start by calculating the electric field distribution within the transition region. Using *Poisson's Equation* which relates the gradient of electric field to the local space charge at any point x we have:

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}(p - n + N_d^+ - N_a^-) \tag{A.13}$$

This equation is greatly simplified within the transition region if we neglect the contribution of the carriers (p - n) to the space charge. With this approximation in mind and considering the case for Schottky contact, where one side of the junction is metal (only have N_d), the above equation will be simplified as:

$$\frac{dE(x)}{dx} = \frac{q}{\epsilon}(N_d^+) \tag{A.14}$$

The maximum value of the electric field E can be found by integrating both sides of Equation A.14 over appropriate limits,

$$\int_0^{E_0} dE(x) = \frac{q}{\epsilon} N_d^+ \int_0^W dx \tag{A.15}$$

Therefore the maximum value of the electric field is

$$E = -\frac{q}{\epsilon} N_d^+ \, W \tag{A.16}$$

This simply relates the electric field to the contact potential, since the

electric field at any point is the negative of the potential gradient at that point.

Thus, the relation between the total potential V_{total} across the junction and the width W is obtained by integration of the electric field, using the boundary condition that the band bending is zero in the electrically neutral region. The solution gives the general result:

$$-V_{total} = \int_0^W E(x)dx \tag{A.17}$$

where $V_{total} = V_{bi} - V_F$ in forward bias and $V_{total} = V_{bi} + V_R$ in reverse bias. Assuming a uniform space charge density in the space charge region, equation Equation A.17 reduces to:

$$W = \sqrt{\frac{2\epsilon_s V_{total}}{qN_d}} \tag{A.18}$$

In silicon, for a typical doping density of $N_d = 10^{21}m^{-3}$, the width of the space charge region is $\approx 1.1\mu m$ at equilibrium and expands to $2.8\mu m$ under reverse bias $V_R = 5V$.

We work under the assumption that no free carriers exist within the space charge region and that the boundary to the electrically neutral region is sharp. This assumption is known as the depletion approximation. In reality, there exists a small transition region, known as the Debye tail, which is only partly depleted of free carriers. The assumption of abruptness between the space charge region and the neutral region is satisfied when the width of the space charge region is much larger than the Debye length. Although Debye tail effects do play a role in characterization of the Schottky diode, we work under the depletion approximation.

A.4.4 Current-Voltage Characteristics

The dominant forward current transport mechanism in the Schottky diode is due to the injection of majority carriers from the semiconductor to the metal over the potential barriers between the metal and the semiconductor. This is opposed to minority carriers in a pn junction diode. A quantitative analysis [38] shows that the ideal current-voltage (I-V) characteristics has the form:

$$I = I_s(e^{(\frac{qV}{KT})} - 1) \tag{A.19}$$

where $V = V_F > 0$ in forward bias and $V = -V_R < 0$ in reverse bias. In here the assumption is made that the barrier height in much larger than KT. The saturation current Is given by:

$$I_s = AA^*T^2e^{(\frac{-q\phi_{Bn}}{KT})} \tag{A.20}$$

$$A^* \equiv \frac{4\pi em^*K^2}{h^3} \tag{A.21}$$

where A is the diode area and A^* is the effective Richardson's constant, m^* is the effective mass of electrons and K is the Boltzmann's constant. The I-V characteristics of the Schottky diodes used in this work are well described by Equation A.19.

A.5 Conclusion

A Schottky diode is formed by making a metal-semiconductor contact between a metal and an n or p doped semiconductor material. For the case of a diode formed by a metal n-doped semiconductor, at the junction of these two

dissimilar materials, free electrons flow across the junction from the semiconductor to the metal. This flow of charge-carriers creates a junction potential. The difference in energy between the metal and the semiconductor materials is referred to as a Schottky barrier.

Although the current-voltage relationship of the Schottky diode given by Equation A.19 is of the same form as the one given for pn junction diode, there are two very important differences between a Schottky barrier diode and a pn junction diode. The first is the magnitude of the reverse saturation current densities, and the second is in the switching characteristics.

The reverse saturation currents in the two devices are very different. The current in the pn junction diode is determined by the diffusion of minority carriers while the current in a Schottky barrier diode is determined by thermionic emission of majority carriers over a potential barrier.

The reverse saturation current in a pn junction diode is dominated by the generation current and is approximately two to three orders of magnitude less than that of reverse saturation current of a Schottky barrier diode.

The second major differences between a Schottky barrier diode and a pn junction diode is in the frequency response, or switching characteristics. Current in a Schottky diode is due to the injection of majority carriers over a potential barrier. That is why Schottky diodes are referred to as majority carrier devices. This fact means there is no diffusion capacitance associated with a forward biased Schottky diode. Elimination of this diffusion capacitance makes the Schottky diode a higher frequency device when compared to a pn junction diode.

A Schottky diode has many more favorable properties such as:

A low forward voltage at all current levels ensures that the maximum/minimum

voltage seen by the system or component.

Fast Switching of the diode between ON and OFF states guarantees the operation of diode at high frequency.

High current-handling capability, the ability of a diode to be used for power rectification. A key diode parameter in current-handling capability is the diode's series resistance. Low series-resistance diodes are preferred for power efficient rectification. In addition, lower diode series resistance gives rise to less device self-heating under high-current conditions.

As our goal during this project is to build power efficient rectifiers for RFID systems, there is no doubt that Schottky diodes are our number one choice.

Appendix B

Matlab Scripts and SPICE model

B.1 MATLAB Programs

========== SUBROUTINE 1 ==========

```
function output = regresion_RS(m)
% A program to find the best fit line for RS measurements
% Diode equation : Id = Is * ( exp(Vd/N *Vt) - 1)
% Convert that into Log format we get
% log(Id) = log(Is) + [ 1 / (N * Vt)] Vd
% This has a format like y = a + b * x
% where y = log(Id), a = log(Is), b=1/(N * Vt) and x = Vd

Vd=(m(:,1));
Id=m(:,2);
n = size(Vd,1);
Vt=0.0256;

for N=1:0.05:3 % Sweep N to find the best fit
```

```
    y=log(Id);
    x=Vd;
    % calculate regression line parameters
    Sxx= sum( x.^2) - (1/n) * (sum(x)).^2;
    Syy= sum( y.^2) - (1/n) * (sum(y)).^2;
    Sxy= sum(x .* y) - (1/n) * sum(x) * sum(y);
    b= Sxy/Sxx;
    yb = mean(y);
    xb = mean(x);
    a= yb - b*xb;
    m = -b;
    nn= 1/(m * Vt);

    % Now put the values that we found into ideal diode eqn.
    IIs = exp(a);
    IId = IIs * ( exp( Vd./(N * Vt)) -1 );
    str = sprintf('N= %d IIs=%d m=%d n=%d', N, IIs, m, nn);
    disp(str);
    % Print the result & comapre them with the measured values
    clf;
    semilogy(Vd, Id, 'k');
    hold on;
    semilogy(Vd,IId);
    pause;

end
```

========== SUBROUTINE 2 ==========

```
function output = regresion_CV(m)
% A program to find the best fit line for CV measurements
% Diode equation : Id = Is * ( exp(Vd/N *Vt) - 1)
% Convert that into Log format we get
% log(Id) = log(Is) + [ 1 / (N * Vt)] Vd
% This has a format like y = a + b * x
% where y = log(Id), a = log(Is), b=1/(N * Vt) and x = Vd
```

```
Vd=(m(:,1));
Cs=m(:,2);
n = size(Vd,1);

for Vj=0.1:0.1:1

    y=log(Cs);
    x=log(1 - (Vd ./ Vj));

    slop= (y(n) - y(1))/( x(n) - x(1));

    Sxx= sum( x.^2) - (1/n) * (sum(x)).^2;
    Syy= sum( y.^2) - (1/n) * (sum(y)).^2;
    Sxy= sum(x .* y) - (1/n) * sum(x) * sum(y);
    b= Sxy/Sxx;
    yb = mean(y);
    xb = mean(x);
    a= yb - b*xb;

    m = -b;
    CCj = exp(a);
    CCs = CCj * ( 1 ./ (1 - Vd./Vj).^m);
    str = sprintf('Vj= %d Cj=%d m=%d', Vj, CCj, m);
    disp(str);
    clf;
    plot(Vd, Cs, 'k');
    hold on;
    plot(Vd,CCs);
    pause;
end
```

========== SUBROUTINE 3 ==========

```
function output = Measuring_plotting_Cj(m)
% A program to measure and plot Cj from measurements
```

```
% In this case matrix $s_raw$ is filled with s-parameters
% as a function of V_r at a constant frequency.

s11= s_raw(:,2) +  s_raw(:,3) * j
zin = ( ( 1+ s11) ./ ( 1- s11) ) * 50;
Cr2 = ( imag(zin) .* (2 * pi * 60e6) ).^2
Cj = 1 ./ ( -imag(zin) .* (2 * pi * 60e6) )

plot(Cr2)
xlabel('Vr (volts)')
xlabel('Vr (volts)')
ylabe('1/c^2')
```

========== SUBROUTINE 4 ==========

```
function output = Simulate_ELRF(m)
% A program to simulate Ethernet Like RF

format long e

N = n;
CW = 32;
Wbar = CW/2;

x = 800; % number of beacon during tag enquiry
Tbi = 5000e-6; % Beacon interval 5000us
Tmin = 3 * Tbi; % Min waiting time
Tread = 4; % time it takes to query a tag

% Duration of BDI
Tc = (1+1)* Tbi; % if there is a collision
Ts = Tread + Tmin + Tbi; % if successful read by another reader
Te = 1 * Tbi; % if emptry slot

beacon_size = 20;
query_size = 40;
```

```
Lbeacon = 265e-6; % length of query
Tbeacon =0; % turn-around-time
Lquery = 341e-6;
Tquery = 0;



p = 1 - ( 1 - 1/Wbar)^(N-1);
Pactive = 1 - ( 1 - 1/Wbar)^N;
Pcollision_active = ( Pactive - (N/Wbar)*( 1 - 1/Wbar)^(N-1) )/ Pactive ;
Pc = Pactive .* Pcollision_active;
Ps = (N/Wbar)*( 1 - 1/Wbar)^(N-1);
Pe = ( 1 - 1/Wbar)^N;
ETbdi = Pe*Te + Ps*Ts + Pc*Tc;
Ebdi = CW /(2*(1-p));
ETcycle = Ebdi * ETbdi + Tread;
U = (Tread * Ps * Ebdi) / ETcycle;
QTread = (Tread - x *(Tbeacon + Lbeacon) )/(Tquery + Lquery);
S = (QTread * Ps * Ebdi) / ETcycle;
str = sprintf('%d & %d & %0.2g & %0.2g & %0.2g & %0.2g & %0.2g & %g & %g & %g & %g \
disp(str);

% These are the outputs gathered from before
n=[2 4 8 16 32 64 128];
m=[1833 2204 2451 2594 2664 2634 1295];
```

========== SUBROUTINE 5 ==========

```
% ##########################################################################
% # A Matlab function that reads a file in CITIFILE format generated
% # by Agilent 8510C vector network analyzer, converts it into a Touchstone
% # file in real-imaginary format, save the results in *.s1p or *.s2p file
% # and return S-parameter matrix back to to calling program.
% #
```

```
% ##########################################################################
% filename citi2touchs.m
function sparam = citi2touchs(fileprefix)
filename = strcat(fileprefix,'.txt'); % Input file extension is .txt
s=sprintf('\nReading CITIFILE S-parameters from file %s ...',filename);
disp(s);
citifile = fopen(filename,'r'); % open input citifile file.
% Ignore first five lines
ignore = fgetl(citifile);ignore = fgetl(citifile);ignore = fgetl(citifile);
ignore = fgetl(citifile);ignore = fgetl(citifile);
% Ignore next line
ignore = fgetl(citifile);
% Read next line
s = fgetl(citifile);
if (s=='DATA S[2,1] RI')
portnum=2;
filename = strcat(fileprefix,'.s2p');
% Skip next three lines
ignore = fgetl(citifile);ignore = fgetl(citifile);
ignore = fgetl(citifile);
else
portnum=1;
filename = strcat(fileprefix,'.s1p');
end; % s==
% Read next line
s = fgetl(citifile);
P = sscanf(s,'%s %f %f %f');
fstart = P(4)./1E+9; % f in GHz
fstop = P(5)./1E+9;
pointnum = P(6);
% Ignore next four lines
ignore = fgetl(citifile);ignore = fgetl(citifile);
ignore = fgetl(citifile);ignore = fgetl(citifile);
fstep = (fstop-fstart) ./ (pointnum-1);
f = fstart:fstep:fstop;
% Read S11;
for i=1:pointnum;
% Read real-imaginary data line by line.
```

```
s = fgetl(citifile);
P = sscanf(s,'%f,%f');
re11(i) = P(1);
im11(i) = P(2);
end;
% Open output file
outfile = fopen(filename,'w'); % Open output TouchStone file.
% Write output file header
fprintf(outfile,'# GHz S RI R 50\n');
% If 1-port, write data to Touchstone file.
if (portnum==1)
sparam = [f' re11' im11'];
s=sprintf('Writing Touchstone S-parameters to file %s...',filename);
disp(s);
fprintf(outfile,'%f %f %f\n',sparam');
end; % end portnum==1
% If 2-port, read S21 S12 S22
if (portnum==2)
% Ignore next two lines
ignore = fgetl(citifile);ignore = fgetl(citifile);
% Read S21;
for i=1:pointnum;
% Read real-imaginary data line by line.
s = fgetl(citifile);
P = sscanf(s,'%f,%f');
re21(i) = P(1);
im21(i) = P(2);
end; % for i
% Ignore next two lines
ignore = fgetl(citifile);ignore = fgetl(citifile);
% Read S12;
for i=1:pointnum;
% Read real-imaginary data line by line.
s = fgetl(citifile);
P = sscanf(s,'%f,%f');
re12(i) = P(1);
im12(i) = P(2);
end; % for i
```

```
% Ignore next two lines
ignore = fgetl(citifile);ignore = fgetl(citifile);
% Read S22;
for i=1:pointnum;
% Read real-imaginary data line by line.
s = fgetl(citifile);
P = sscanf(s,'%f,%f');
re22(i) = P(1);
im22(i) = P(2);
end; % for i
sparam = [f' re11' im11' re21' im21' re12' im12' re22' im22'];
% Print data to Touchstone file.
s=sprintf('Writing TouchStone S-parameters to file %s ...',filename);
disp(s);
fprintf(outfile,'%f %f %f %f %f %f %f %f %f\n',sparam');
end; % if portnum==2
% Close files
fclose(outfile);
fclose(citifile);
return;
```

========== SUBROUTINE 6 ==========

```
% ##########################################################################
% # A Matlab function that converts S-paramters of DUT and PAD to
% # Y-parameters. Subtract Y of PAD from Y of DUT and store de-embedded
% # Y-parameters in dmby. De-embedded Y-parameters are converted back to
% # S-parameters. De-embedded S-parameters are stored in dmbs and saved to
% # an S-parameter file outfile.s1p or *.s2p.
% ##########################################################################
% filename de_embed.m

function [dmbs,dmby] = de_embed(dut,pad,dmbfileprefix)
% Determine frequency matrix and number of data points.
f = dut(:,1); % All data in column 1 are f
```

```
% Number of data points is number of elements of matrix f
pointnum=size(f);
% Determin number of ports
if (size(dut,2)>3) % check number of ports
portnum = 2;
else
portnum = 1;
end;
% Define S11
duts11 = dut(:,2) + sqrt(-1).*dut(:,3);
pads11 = pad(:,2) + sqrt(-1).*pad(:,3);
if (portnum==1)
% Convert S to Y and find Yin1P
% Yin = [1/Z0]*[(1-S11)/(1+S11)]
yindut = ((1-duts11)./(1+duts11))./50; % Z0 = 50 Ohm.
yinpad = ((1-pads11)./(1+pads11))./50; % Z0 = 50 Ohm.
yin1p = yindut - yinpad;
% Convert Yin1P back to S11
% S11 = (1-Y*Z0)/(1+Y*Z0)
yin1p = yin1p.*50;
s111p = (1-yin1p)./(1+yin1p); % Z0 = 50 Ohm.
% Write de-embedded S-parameter to output file.
filename = strcat(dmbfileprefix,'.s1p');
outfile = fopen(filename,'w');
s = ...
sprintf('Writing de-embedded one-port S-parameter to %s ...',filename);
disp(s);
fprintf(outfile,'# GHz S RI R 50\n');
dmbsin = [f real(s111p) imag(s111p)];
fprintf(outfile,'%f %f %f\n',dmbsin');
fclose(outfile);
% Write de-embedded S-parameter to output file to be used by HSPICE.
filename = strcat(dmbfileprefix,'hspice.s1p');
o = fopen(filename,'w');
s = ...
sprintf('Writing de-embedded two-port S-parameter to %s ...',filename);
disp(s);
fprintf(o,'# Hz S MA R 50\n');
```

```
mgs11 = abs(s111p);
angs11 = 180.*angle(s111p)./pi;
dmbs = [f.*1E+9 mgs11 angs11];
fprintf(o,'%6.4e %6.4e %6.4e\n',dmbs');
fclose(o);
% Creat de-embedded S and Y parameter matrices
dmbs = [s111p];
dmby = [yin1p];
end; % if portnum==1
if (portnum==2)
% Define S21, S12, S22.
duts21 = dut(:,4) + sqrt(-1).*dut(:,5);
duts12 = dut(:,6) + sqrt(-1).*dut(:,7);
duts22 = dut(:,8) + sqrt(-1).*dut(:,9);
pads21 = pad(:,4) + sqrt(-1).*pad(:,5);
pads12 = pad(:,6) + sqrt(-1).*pad(:,7);
pads22 = pad(:,8) + sqrt(-1).*pad(:,9);
% Convert S of dut to Y
delta = ((1+duts11).*(1+duts22))-(duts12.*duts21);
duty11 = ((((1-duts11).*(1+duts22)) + (duts12.*duts21))./delta)./50; % Z0 = 50.
duty21 = ((-2.*duts21)./delta)./50; % Z0 = 50.
duty12 = ((-2.*duts12)./delta)./50; % Z0 = 50.
duty22 = ((((1+duts11).*(1-duts22)) + (duts12.*duts21))./delta)./50; % Z0 = 50.
% Convert S of pad to Y
delta = ((1+pads11).*(1+pads22))-(pads12.*pads21);
pady11 = ((((1-pads11).*(1+pads22)) + (pads12.*pads21))./delta)./50; % Z0 = 50.
pady21 = ((-2.*pads21)./delta)./50; % Z0 = 50.
pady12 = ((-2.*pads12)./delta)./50; % Z0 = 50.
pady22 = ((((1+pads11).*(1-pads22)) + (pads12.*pads21))./delta)./50; % Z0 = 50.
% De-embedding.
dmby11 = duty11 - pady11;
dmby21 = duty21 - pady21;
dmby12 = duty12 - pady12;
dmby22 = duty22 - pady22;
% Convert Y back to S.
y11 = dmby11 .* 50; % Normalize Y
y21 = dmby21 .* 50;
y12 = dmby12 .* 50;
```

```
y22 = dmby22 .* 50;
delta = ((1+y11).*(1+y22)) - (y12.*y21);
s11 = (((1-y11).*(1+y22)) + (y12.*y21))./delta;
s21 = (-2.*y21)./delta;
s12 = (-2.*y12)./delta;
s22 = (((1+y11).*(1-y22)) + (y12.*y21))./delta;
% Write de-embedded S-parameter to output file.
filename = strcat(dmbfileprefix,'.s2p');
outfile = fopen(filename,'w');
s = ...
sprintf('Writing de-embedded two-port S-parameter to %s ...',filename);
disp(s);
fprintf(outfile,'# GHz S RI R 50\n');
dmbs2p = [f real(s11) imag(s11) real(s21) imag(s21) ...
real(s12) imag(s12) real(s22) imag(s22)];
fprintf(outfile,'%f %f %f %f %f %f %f %f %f\n',dmbs2p');
fclose(outfile);
% Write de-embedded S-parameter to output file to be used by HSPICE.
filename = strcat(dmbfileprefix,'hspice.s2p');
o = fopen(filename,'w');
s = ...
sprintf('Writing de-embedded two-port S-parameter to %s ...',filename);
disp(s);
fprintf(o,'# Hz S MA R 50\n');
mgs11 = abs(s11);
mgs21 = abs(s21);
mgs12 = abs(s12);
mgs22 = abs(s22);
angs11 = 180.*angle(s11)./pi;
angs21 = 180.*angle(s21)./pi;
angs12 = 180.*angle(s12)./pi;
angs22 = 180.*angle(s22)./pi;
dmbs = [f.*1E+9 mgs11 angs11 mgs21 angs21 mgs12 angs12 mgs22 angs22];
fprintf(o,'%6.4e %6.4e %6.4e %6.4e %6.4e %6.4e %6.4e %6.4e %6.4e\n',dmbs');
fclose(o);
% Creat de-embedded S and Y parameter matrices
dmbs = [s11 s21 s12 s22];
dmby = [y11 y21 y12 y22];
```

```
end; % if portnum==2
return;
```

B.2 SBD SPICE Model

```
% ##########################################################################
% # SPICE model used for simulating SBD
% ##########################################################################

.MODEL mySBD d
+ LEVEL=1
+ BV=9
+ CJO=0.7e-12
+ EG=0.69
+ IBV=10e-4
+ IS=2.2e-8
+ N=1.08
+ RS=56
+ PB=0.56
+ XTI=2
+ MJ=0.5
*
```

Appendix C

Formula Statements and Physical Constants

C.1 Equations

C.1.1 Regression Analysis

$$S_{xx} = \sum_{i=1}^{n} x_i^2 - \frac{1}{n}(\sum_{i=1}^{n} x_i)^2 \tag{C.1}$$

$$S_{yy} = \sum_{i=1}^{n} y_i^2 - \frac{1}{n}(\sum_{i=1}^{n} y_i)^2 \tag{C.2}$$

$$S_{xy} = \sum_{i=1}^{n} (x_i \times y_i) - \frac{1}{n}(\sum_{i=1}^{n} x_i \times \sum_{i=1}^{n} y_i) \tag{C.3}$$

$$m = \frac{S_{xy}}{S_{xx}} \tag{C.4}$$

$$b = \overline{y} - m * \overline{x} \tag{C.5}$$

C.1.2 Impedance and Admittance

For Z-Parameters:

$$V_1 = z_{11}I_1 + z_{12}I_2 \tag{C.6}$$
$$V_2 = z_{21}I_1 + z_{22}I_2 \tag{C.7}$$

and for Y-parameters:

$$I_1 = y_{11}V_1 + y_{12}V_2 \tag{C.8}$$
$$I_2 = y_{21}V_1 + y_{22}V_2 \tag{C.9}$$

C.1.3 S-parameters

$$b_1 = s_{11}a_1 + s_{12}a_2 \tag{C.10}$$
$$b_2 = s_{21}a_1 + s_{22}a_2 \tag{C.11}$$
$$s_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \tag{C.12}$$
$$s_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{C.13}$$
$$s_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \tag{C.14}$$
$$s_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \tag{C.15}$$

C.2 Physical constants

constant	symbol	magnitude
Avogadro's number	NA	6.022×10^{23}
Boltzmann's constant	k	1.381×10^{-23} J/K
Planck's constant	h	6.626×10^{-34} J s
speed of light	c	2.998×10^{8} m/s
electron charge	e	1.602×10^{-19} C
electron mass	me	9.109×10^{-31} kg
proton mass	mp	1.672×10^{27} kg

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