Low-Cost Small-Scale Wind Power Generation

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Dedicated to my late grandmother, Χρισούλα Ηλιάδου (Chryssoula Iliadis)

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Abstract

This research investigates a low-cost generator and power electronics unit for small-scale (<10kW) wind turbines, for both standalone and grid-connected applications. The proposed system uses a high-inductance permanent magnet generator together with a switched-mode rectifier (SMR) to produce a variable magnitude output current. The high inductance characteristic allows the generator to operate as a current source, which has the following advantages over conventional low-inductance generator (voltage source) systems: it offers simple control, and avoids the need for bulky / costly energy storage elements, such as capacitors and inductors.

The SMR duty-cycle is controlled in an open-loop manner such that 1) maximum power is obtained for wind speeds below rated, and 2) the output power and turbine speed is limited to safe values above rated wind speed. This topology also has the ability to extract power at low wind speeds, which is well suited to small-scale wind turbines, as there is often limited flexibility in their location and these commonly see low average wind speeds.

The thesis is divided into two parts; the first part examines the use of the SMR as a DC-DC converter, for use in standalone applications. The duty-cycle is essentially kept constant, and is only varied for maximum power tracking and turbine speed / power limiting purposes. The SMR operates in to a fixed voltage source load, and has the ability to allow current and hence power to be drawn from the generator even at low wind and hence turbine speeds, making it ideal for battery charging applications. Initial dynamometer testing and limited wind-tunnel testing of a commercially available wind turbine show that turbine power can be maximised and its speed can be limited by adjusting the SMR duty-cycle in an open-loop manner.

The second part of the thesis examines the use of the SMR as a DC-AC converter for grid-connected applications. The duty-cycle is now modulated sinusoidally at the mains frequency such that the SMR produces an output current that resembles a full-wave rectified sinewave that is synchronised to the mains voltage. An additional H-

bridge inverter circuit and low-pass filter is used to unfold, filter and feed the sinusoidal output current in to the utility grid. Simulation and initial resistive load and preliminary grid-connected tests were used to prove the inverter concept, however, the permanent magnet generator current source is identified as non-ideal and causes unwanted harmonic distortion.

The generator harmonics are analysed, and the system performance is compared with the Australian Standard THD requirement. It is concluded that the harmonics are caused by 1) the low-cost single-phase output design, 2) the use of an uncontrolled rectifier, and 3) the finite back-EMF voltage. The extent of these harmonics can be predicted based on the inverter operating conditions. A feed-forward current compensation control algorithm is investigated, and shown to be effective at removing the harmonics caused by the non-ideal current source. In addition, the unipolar PWM switching scheme, and its harmonic components are analysed. The low-pass filter design is discussed, with an emphasis on power factor and THD grid requirements. A normalised filter design approach is used that shows how design aspects, such as cutoff frequency and quality factor, affect the filter performance. The filter design is shown to be a trade-off between the output current THD, power loss, and quality factor.

The final chapter summarises the thesis with the design and simulation of a 1kW single-phase grid-connected inverter. The inverter is designed based on the low-pass filter and feed-forward compensation analysis, and is shown to deliver an output current to the utility grid that adheres to the Australian Standards.

Statement of Originality

This work contains no material which has been accepted for the award of any other degree or diploma in any university or other tertiary institution to David M. Whaley and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

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Date

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List of Publications

[1] G. Ertasgin, **D.M. Whaley**, N. Ertugrul and W.L. Soong, "Implementation and Performance Evaluation of a Low-Cost Current-Source Grid-Connected Inverter for PV Application", *in Proceedings of the IEEE International Conference on Sustainable Energy Technologies*, Nov. 2008, Singapore.

[2] G. Ertasgin, **D.M. Whaley**, N. Ertugrul and W.L. Soong, "Analysis and Design of Energy Storage for Current-Source 1-ph Grid-Connected PV Inverters", *in Proceedings of the IEEE Applied Power Electronics Conference and Exposition*, Feb., 2008, pp. 1229 – 1234.

[3] G. Ertasgin, **D.M. Whaley**, N. Ertugrul, and W.L. Soong, "A Current-Source Grid-Connected Converter Topology for Photovoltaic Systems", *in Proceedings of Australasian Universities Power Engineering Conference*, 2006.

[4] **D.M. Whaley**, G. Ertasgin, W.L. Soong, N. Ertugrul, J. Darbyshire, H. Dehbonei, and C.V. Nayar, "Investigation of a Low-Cost Grid-Connected Inverter for Small-Scale Wind Turbines Based on a Constant-Current Source PM Generator", *in Proceedings of the IEEE Industry Electronics*, Nov., 2006, pp. 4297 – 4302.

[5] C.Z. Liaw, **D.M. Whaley**, W.L. Soong, and N. Ertugrul, "Implementation of Inverterless Control of Interior Permanent Magnet Alternators", *in IEEE Transactions on Industry Applications*, vol. 42, no. 2, Mar. - Apr., 2006, pp. 536 – 544.

[6] **D.M. Whaley**, W.L. Soong, and N. Ertugrul, "Investigation of Switched-Mode Rectifier for Control of Small-Scale Wind Turbines", *in Proceedings of the IEEE Industry Applications Conference*, vol. 4, Oct., 2005, pp. 2849 – 2856.

[7] C.Z. Liaw, **D.M. Whaley**, W.L. Soong, and N. Ertugrul, "Implementation of Inverterless Control of Interior Permanent Magnet Alternators", *in Proceedings of the IEEE Industry Applications Conference*, Oct., 2004.

[8] **D.M. Whaley**, W.L. Soong, and N. Ertugrul, "Extracting More Power from the Lundell Car Alternator", *in Proceedings of Australasian Universities Power Engineering Conference*, 2004.

Portions of the work presented in this thesis have been previously published. The material in Chapters 2 and 3 correspond to work in publications [6], whilst Chapter 4 corresponds to the work presented in publication [4]. Reprints of these publications are found in appendix B, for convenience.

Conventions

This thesis employs the IEEE reference style for citations, and is written using Australian English, as defined by the Macquarie English Dictionary 2005.

All voltages and currents shown in figures and equations are expressed as RMS (root-mean squared) quantities, unless otherwise stated.

The *hat* symbol is used in Chapters 5 and 6 to indicate peak value, i.e. $\widehat{\alpha}$ and $\widehat{\alpha}_0$ indicate the peak values of α and α_0, respectively. Similarly, the *check* symbol is used in Chapter 6 to represent the nadir (minimum) value, e.g. $\check{\beta}$ represents the minimum value of β.

Measured data is represented by hollow points, e.g. circles, squares, diamonds etc. and is often accompanied by solid lines that correspond to the equivalent analytical or computer based simulations. Multiple cases of measured (and simulated) data commonly appear on a single figure, and are differentiated by colour and shape. In contrast, coloured / shaded points represent calculated data. These are also shown with solid lines, however, these are for aesthetic purposes, i.e. they simply join the calculated data.

The above convention is used for the majority of this thesis, i.e. Chapters 2 to 5, however, the convention is modified for Chapter 6, as the data presented in this chapter is either simulated or analytically calculated. The simulated data, of Chapter 6 is hence shown as shaded points, whilst the analytical calculations are shown by the solid lines.

Nomenclature

α	normalised rectifier voltage	pu
α_0	ratio of grid to open-circuit rectifier voltage	
α_{cu}	temperature coefficient of copper	/°C
β	normalised rectifier current	pu
$\check{\beta}$	normalised minimum inverter input current	pu
β_{app}	normalised approximated rectifier current	pu
β_{exp}	normalised experimental rectifier current	pu
β_{id}	normalised ideal rectifier current	pu
Δ	difference	
δ	skin depth	m
η_{gen}	generator efficiency	%
η_{inv}	inverter efficiency	%
λ	tip-speed ratio	
μ	permability	H/m
ω	machine angular speed	rad/s
ω	turbine angular speed	rad/s
ω_{cn}	normalised cutoff frequency (relative to f_1)	pu
ω_e	electrical angular frequency	rad/s

ω_g	grid angular frequency	rad/s
ω_m	mechanical angular frequency	rad/s
ϕ	filter delay	deg
ϕ	power factor angle	deg
Ψ_m	RMS flux linkage	Wb or Vs
ρ	air density	kg/m^3
σ	conductivity	$(\Omega\ \mathrm{m})^{-1}$
$\widehat{\alpha}_0$	peak value of α_0	
ξ	saliency ratio	
C	capacitance	F
c_p	turbine coefficient of performance	
d	duty-cycle	%
d_a	adjusted duty-cycle	%
d_i	stored duty-cycle	%
dB	decibels	
E	induced back-EMF voltage	V
f	frequency	Hz
f_1	fundamental frequency	Hz
f_{cn}	normalised cutoff frequency (relative to f_{sw})	pu
f_c	cutoff frequency	Hz
f_m	machine frequency	Hz
f_{res}	resonant frequency	Hz
f_{sw}	switching frequency	Hz

$H(s)$	filter transfer function	
h_1	fundamental harmonic magnitude	%
h_f	harmonic frequency	Hz
h_m	harmonic magnitude at m multiples of f_1	%
h_{tot}	total harmonic components	%
I	current	A
I^*	compensation current command	A
$i_{c\ exp}(t)$	compensated current using the experimental I-V locus	pu
$i_{c\ id}(t)$	compensated current using the ideal I-V locus	pu
I_{ch}	characteristic current	A
$i_c(t)$	time-varying compensated current	A
I_{DC}	DC current	A
I_d	damping resistor current	A
I_f	damping resistor current (from inverter)	A
I_g	grid drawn current (from grid)	A
I_{inv}	inverter output current	A
I_{in}	input current	A
I_L	line current	A
$i_{out\ (id)}(t)$	normalised time-varying ideal output current	pu
I_{out}	output current	A
I_{ph}	phase current	A
$i_{R\ (id)}(t)$	normalised time-varying ideal rectifier voltage	pu
$I_{R\ min}$	minimum rectifier output current	A

I_R	rectifier output current	A
$i_R(t)$	normalised time-varying rectifier current	pu
$i_{ws\ (id)}(t)$	normalised time-varying ideal wave-shaper current	pu
I_{ws}	wave-shaper current	A
j	$\sqrt{-1}$	
k	back-EMF constant	V/rpm
k_{ph}	phase back-EMF constant	V/rpm
L	inductance	H
L_1	transformer primary inductance	H
L_2	transformer secondary inductance	H
L_{eq}	equivalent inductance	H
L_{ph}	phase inductance	H
L_s	stator inductance	H
m	number of machine phases	
m	positive integer	
m_a	modulation index	%
n	machine / generator speed	rpm
n	positive odd integer	
n	transformer turns ratio	
n_k	machine speed	k rpm
P	power	W
P	real power	W
p	number of machine pole-pairs	

P_{CU}	copper loss	W
P_d	damping resistor power loss	W
P_{IFW}	machine iron, friction and windage loss	W
$P_{inv\ in}$	total inverter input power	W
P_{inv}	inverter output power	W
P_{in}	input power	W
P_{loss}	SMR / generator power loss	W
P_L	machine power loss	W
P_{SMR}	SMR output power	W
P_{sw}	switching power loss	W
P_T	wind turbine power	W
P_W	wind power	W
$pk - pk$	peak to peak	
Q	quality factor	
Q	reactive power	VAr
Q_C	capacitive reactive power	VAr
Q_L	inductive reactive power	VAr
R	resistance	Ω
r	blade radius	m
R_1	transformer primary resistance	Ω
R_2	transformer secondary resistance	Ω
R_{cold}	cold resistance	Ω
R_d	damping resistance	Ω

R_{eq}	equivalent resistance	Ω
R_{hot}	hot resistance	Ω
R_L	load resistance	Ω
R_{ph}	phase resistance	Ω
R_s	stator resistance	Ω
$rect(t)$	normalised time-varying rectifier ripple	pu
S	apparent power	VA
S	number of stator slots	
s	$j\,\omega$	
T	torque	Nm
t	time	s
t_{off}	device *turn-off* time	s
t_{on}	device *turn-on* time	s
t_q	thyristor turn-off time	s
V	voltage	V
v	wind speed	m/s
V_C	capacitor voltage	V
V_{DC}	DC link voltage	V
V_{DC}	DC voltage	V
v_{eq}	turbine equivalent wind speed	m/s
$V_{g\ pk}$	peak grid voltage	V
V_g	grid voltage	V
$v_g(t)$	normalised time-varying grid voltage	pu

v_i	internal wind tunnel wind speed	m/s
V_L	line voltage	V
$V_{ph\ pk}$	generator phase peak voltage	V
$V_{R\ pk\ OC}$	peak rectifier voltage	V
v_r	rated wind speed	m/s
$v_R(t)$	normalised time-varying rectifier voltage	pu
$v_{ws}(t)$	normalised time-varying current wave-shaper voltage	pu
X	reactance	Ω
X_{ph}	phase reactance	Ω
X_s	stator reactance	Ω
Z_{0n}	normalised characteristic impedance	pu
Z_0	characteristic impedance	Ω
Z_s	stator impedance	Ω

Acronyms

AC	alternating current
AS	Australian Standard
CCS	constant current source
CM	control modes
CSI	current-source inverter
CWS	current wave-shaper
DC	direct current
DCC	duty-cycle command

DFT	discrete Fourier transform
ESR	equivalent series resistance
F&P	Fisher & Paykel®
FC	filter configuration
FFT	fast Fourier transform
GC	grid connected
GCI	grid-connected inverter
HF	high-frequency
IFW	iron, friction and windage
IPM	interior permanent magnet
IR	International Rectifier®
ISA	integrated starter alternator
LA	*Lundell* alternator
LF	line-frequency
MPPT	maximum power point tracker
NEG	net energy gain
NICS	non-ideal current source
OC	open circuit
PM	permanent magnet
pu	per-unit
PV	photovoltaic
PWM	pulse-width modulation
RMS	root-mean-squared

rpm	revolutions per minute	
RR	rectifier ripple	
SC	short circuit	
SC	squirrel cage	
SG	synchronous generator	
SMR	switched-mode rectifier	
SPM	surface permanent magnet	
THD	total harmonic distortion	%
TL	transformerless	
TSR	tip-speed ratio	
UCG	uncontrolled generation	
VSI	voltage-source inverter	
WF	wound field	
WR	wound rotor	

Abbreviations

CL	capacitive-inductive
I-V	current vs. voltage
LC	inductive-capacitive
LCL	inductive-capacitive-inductive
P-V	power vs. voltage
RLC	resistive-inductive-capacitive
SPP	slots per phase per pole

SW	switch
THY	thyristor

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Chapter 1

Introduction

This chapter introduces wind energy and justifies it as a competitive renewable and non-polluting energy alternative to fossil fuels. Its utilisation, recent growth and technological advances are briefly discussed. The principles of wind energy conversion, along with small-scale turbines and their generators are examined. Common standalone and grid-connected power converters are discussed, and a novel low-cost grid-connected inverter topology is proposed. The chapter concludes with the aims of the research project, discusses its original contributions and describes the structure of the thesis.

1.1 Wind Energy

Wind is defined as the movement of air from regions of high pressure to regions of low pressure, and is primarily caused by uneven heating of the Earth's surface, where an estimated 1% of the Sun's energy is converted to wind [1]. The second cause of large-scale air movement, also referred to as *atmospheric circulation*, is the rotation of the planet or the *Coriolis* effect [1–3].

The definition of wind (moving mass), implies it has an associated kinetic energy. This is converted to mechanical energy using a wind mill or wind turbine, which slows the passing wind; the energy conversion takes place by virtue of the law of *conservation of energy*. The instantaneous use of the wind's energy is referred to as *wind power*.

Wind Power Utilisation

Wind power has been used for over three thousand years [4, 5], firstly by the Persians and more recently the Europeans and Americans in the mid 13^{th} and 19^{th} centuries,

respectively. It has been used for transportation, e.g. ship propulsion, and more recently mechanical applications such as milling grains, sawing wood and pumping water etc. [2, 3, 6]. It was not until the advent of the electrical machine, in 1888, that wind power was used to generate electricity [6]. Note that the term *windmill* refers to a device that extracts wind energy for mechanical applications, whilst a *wind turbine* is used to generate electricity.

Recent Growth

Global wind power has been growing at an average rate of 28% per annum over the last decade [7] in response to the growing demands for electricity. Worldwide electricity production has been steadily increasing at a rate of 3.4% per year on average between 1973 and 2002 [8], as a result of population growth and the industrialisation of developing countries.

1.1.1 Electricity Usage and Conventional Generation

As it is well known, electricity is a form of energy that is widely used in domestic, commercial and industrial applications. It can be easily converted to other forms of energy including mechanical, thermal, light and chemical and is readily and effectively transported over long distances by transmission lines.

Figure 1.1 gives a breakdown of the sources of energy from which electricity was generated in 2005 [8]. It is seen that approximately two thirds of the world's electricity is generated by fossil fuels, such as coal, oil and gas. This causes two serious issues:

1. Environmental impacts - fossil fuel combustion releases gases that contribute to pollution and impact the environment, wildlife and human health. These gases include sulphur dioxide, carbon dioxide and nitrous oxides, which are responsible for acid rain, global warming and photochemical smog, respectively.

2. Depleting reserves - fossil fuels, such as coal, oil and gas, are formed in the ground over long periods of time by chemical and physical changes to plant matter under conditions of high temperature and pressure. Currently these fuels are being consumed at a much greater rate than they are being formed.

The combination of increasing electricity demands, depleting fossil fuel reserves and environmental issues, has created an urgent need to investigate non-polluting and renewable energy sources to generate electricity to ensure a sustainable future.

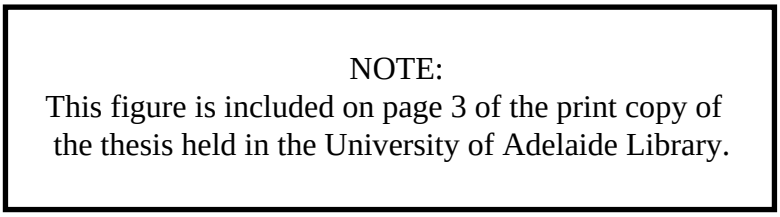


Figure 1.1: Breakdown of worldwide electricity production for 2005 [8].

1.1.2 Alternative Energy Sources

Figure 1.1 showed that after fossil fuels, the next two largest sources of energy used for electricity generation are hydro schemes and nuclear fission, which each make up almost the remaining third of the total. Hydro schemes are non-polluting and renewable, however, requires large-scale water storage in dams and has limited potential for further utilisation. Nuclear power has been used for many decades but there is still significant public concern about its safety and possible long term pollution issues after incidents such as *Three-Mile Island* (1979) and *Chernobyl* (1985).

Of the remaining alternative energy sources, i.e. wind, photovoltaic, biomass etc., large-scale (> 250kW) wind power is one of the most economical. The majority of research effort has been placed on developing large-scale wind turbines, which has resulted in the cost of wind-generated electricity decreasing rapidly over the last 20 years. At present, it is comparable in price to that of coal-fired power [9]. This is mainly attributed to government incentives, improvements to aerodynamic efficiency, the evolution of power semiconductors and control methods, and improved grid integration [9, 10].

Net Energy Gain

In addition to low cost, wind power offers the lowest *net energy gain* (NEG) period, compared to other renewable sources of energy. This period is defined as the operating time required to regain all the energy used to construct the electric power generation

source. The NEG of large wind turbines is in the order of months [11], compared to photovoltaic (PV) cells, which is in the order of years. This, is shown in Table 1.1 along with the NEG of various PV materials and other fossil-fuel based power generation. Note that the NEG period for both wind and PV cells depend on operating conditions, i.e. average wind speed and solar irradiance, respectively. Hence, as listed in the table, careful site location or selection of technology will reduce the NEG period of wind and photovoltaic systems, respectively.

Table 1.1: Comparison of net energy gain (NEG) periods of conventional and renewable energy sources [11].

Despite the low cost and short NEG period of large-scale wind turbines, small-scale wind energy systems are more expensive and have longer NEG periods, making them less competitive with conventionally derived electricity [4]. This is due to the majority of research focussing on large-scale wind turbine optimisation, as small blade efficiency improvements would significantly increase the turbine output power, whilst an increased blade efficiency will only slightly increase the output power of a small-scale wind turbine.

1.1.3 Large and Small-Scale Turbine Classification

The term *Wind Power* often manifests an image of large wind turbines arranged together to form a wind farm. These large-scale turbines are typically rated in the order of MW, and account for the majority of recent worldwide wind power growth.

Small-scale wind turbines are mainly used to generate electricity in remote areas. They differ from their large-scale counterparts in physical size, power rating, and by the types of generators, speed limiters and power converters used. The key differences between small and large-scale wind turbines are summarised in Table 1.2.

Table 1.2: Comparison of small and large scale wind turbine properties.

	Small Scale	Large Scale
Blade Length	< 5m	20–50 m
Rated Power	< 100kW	1–3 MW
Turbine Speed	several hundred rpm	15–30 rpm
Transmission Type	Directly Driven	Gearbox
Generator Types	DC, PM synchronous	Induction (SC and WR), Synchronous (WF and PM)
Speed Control	Furling, Blade stall, Power electronics control	Blade pitch, Rotor resistance (WR IM), Power electronics control
Applications	Standalone, Grid-connected	Grid-connected
Stator Grid Connected	via full-scale grid- connected inverter	Directly, via full-scale converter
Rotor Grid Connected	-	via partial-scale converter

Note: SC, WR, PM and WF denote, squirrel cage, wound rotor, permanent magnet and wound field, respectively.

1.1.4 Small-Scale Turbine Development

In 1925, Marcelleus and Jacobs began working on the first high-speed, small-sized, affordable battery-charging wind turbines [12]. By the 1930's many Midwest manufacturers built wind-chargers, small battery-charging wind turbines that often provided the only source of electricity for many homesteads [13]; these were used to power lights and electric motors [14]. Their demise, however, was brought about in the late 1930's when the Rural Electric Association began spreading AC transmission lines across rural America [14]. Small DC wind turbines had no economical way of either interconnecting to the AC grid or supplying power for the many new appliances that began to fill farm households [12].

Interest in wind power was renewed in the early 1970's, as a direct result of the oil crisis [4, 13, 14]. Since then, a new generation of small-scale wind turbines appeared, i.e. DC generators were replaced with permanent magnet (PM) generators. Induction generators were also examined in the 1980's, and are now generally used for turbines rated higher than 10kW.

1.1.5 Technology Improvement

Wind turbine technologies have significantly improved since the 1980's, allowing turbine size, efficiency, and ease of installation to increase. Currently the largest generator is about 100 times the output power of those used in 1980, and the rotor diameters have increased 8-fold [15]. In addition, turbine efficiency has increased due to improved blade design, and modern turbines are modular and hence quick and easy to install.

1.1.6 Market Growth

The sales of both large and small-scale turbines has experienced substantial growth in recent years. The worldwide wind power market (which is predominantly large-scale) grew by 40% in 2005, bringing the cumulative installed capacity to about 59GW [7, 16] which meets the electricity needs of more than 25 million households worldwide. Global wind power has been growing at an average rate of 28% per annum, over the last 10 years, and grew by 46% in 2007, with US $9 billion invested in wind plants alone [17]. The installed capacity is expected to reach 160GW by 2012 [7]. The USA is claimed to be the fastest-growing wind power market for the last three years. Wind power accounted for 35% of all new US electricity generation capacity in 2007 [17].

The growth in small-scale wind turbines is more difficult to quantify, however, it is hence estimated that the small-scale turbine market is growing at roughly 40% per year [18]. It is also estimated that the US alone will sell a total of US $25M–$55M worth of such turbines by 2010 [19], depending on the market and other factors such as government rebates, tax incentives etc. Within this market there is an increasing demand for low-cost grid-connected wind turbines, and it is expected that by 2020 small-scale turbines will provide 3% of the US electrical energy consumption [18].

1.2 Principles of Wind Power

1.2.1 Wind and Turbine Power

The power available in the wind, P_W, is directly proportional to the air density, ρ, the cube of the wind speed, v, and the blade sweep area πr^2, where r is the blade radius, as summarised by Equation (1.1). The turbine co-efficient of performance, c_p, represents the efficiency of the turbine in converting the power in the wind to mechanical power (turbine power), P_T, as shown in Equation (1.2). The c_p is a function of the tip-speed ratio, λ, where λ is the ratio of blade linear tip velocity and wind speed, summarised by Equations (1.3) and (1.4), where ω is the turbine angular velocity.

$$P_W = \frac{1}{2}\,\rho\,\pi\,r^2\,v^3 \tag{1.1}$$

$$P_T = c_P\,P_W \tag{1.2}$$

$$c_p = f\,(\lambda) \tag{1.3}$$

$$\lambda = \frac{\omega\,r}{v} \tag{1.4}$$

The c_p typically has a maximum value of 40–45%, as shown in Figure 1.2, which shows a typical three-bladed turbine c_p characteristic. The dashed line represents the theoretical peak c_p of 59%, known as *Betz' limit*, after its discovery by Albert Betz in 1919 [20].

Figure 1.2: Typical coefficient of performance, c_p, vs. tip-speed ratio, λ, curve of three-bladed wind turbines [21]. The dashed line represents the theoretical peak c_p of 59%.

1.2.2 Coefficient of Performance

The turbine coefficient of performance vs. tip-speed ratio (TSR) characteristic allows a turbine's power characteristic to be predicted, for any wind speed. A comparison of various wind turbines and their respective c_p characteristics is shown in Figure 1.3 [22]. The figure shows that turbines with *high solidity* (total blade area) reach their peak c_p at low values of λ, as seen for the American, Dutch and Savonius turbines. These turbines hence have high starting torques [4]. In contrast, low solidity turbines, such as the two and three-bladed turbines, have a higher peak c_p, which occurs for higher TSR values, and hence produce low starting torque.

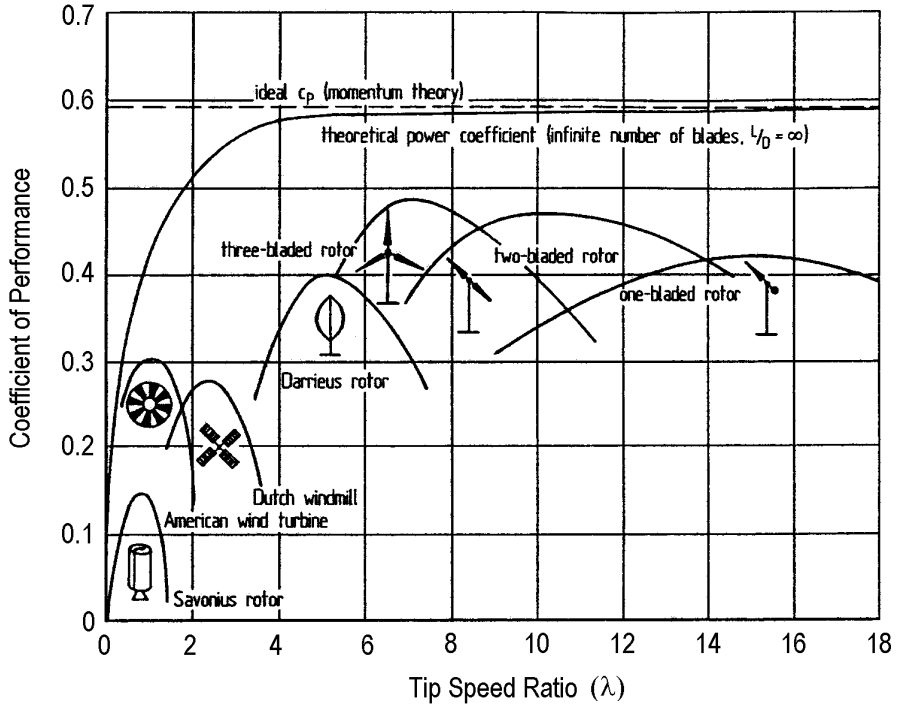


Figure 1.3: Comparison of various turbine coefficient of performance vs. tip-speed ratio characteristics [22].

High optimal TSR turbines are more difficult to start in low wind speeds, due to their low starting torque, and have the potential to produce unwanted acoustic noise. The starting problem can be solved by initially driving the turbine up to operational speed. The Darrieus rotor, for example, does not produce torque at standstill, and needs to be driven up to a rotational speed where aerodynamic forces take over [23].

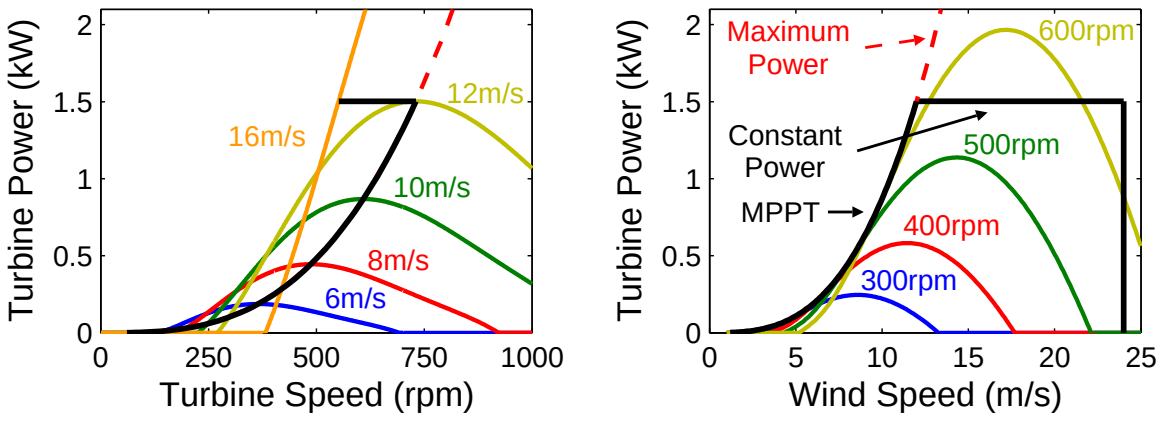
1.2.3 Principles of Turbine Operation

Turbine Operating Regions

Modern small-scale and large-scale wind turbines use variable-speed operation, due to the benefits compared to constant-speed operation, such as higher energy yield (about 10%), reduced noise and reduced mechanical stress [10, 12, 24]. More energy is extracted from a variable-speed turbine as the turbine c_p, and hence power, is maximised by adjusting its speed in accordance with wind speed (see Equation (1.4)). Turbines operate using maximum power point tracking (MPPT) below rated wind speed, generally 12m/s. As the wind speed increases beyond rated, the turbine usually maintains constant output power until the shut-down wind speed. The shut-down speed is typically 25m/s (about twice that of rated speed) and the turbine is stopped for safety reasons at this wind speed.

Turbine Power

Figure 1.4 shows the simulated power vs. turbine and wind speed characteristic of a turbine with a blade radius of 1m and with the c_p curve shown in Figure 1.2. The dashed lines show that turbine power is maximised for a given wind speed by adjusting the turbine speed. The solid black lines represent the turbine operating range and show that power is maximised below rated wind speed (12m/s), whilst power is maintained at rated power (1.5kW) for high wind speeds, and that the turbine is stopped at 24m/s.

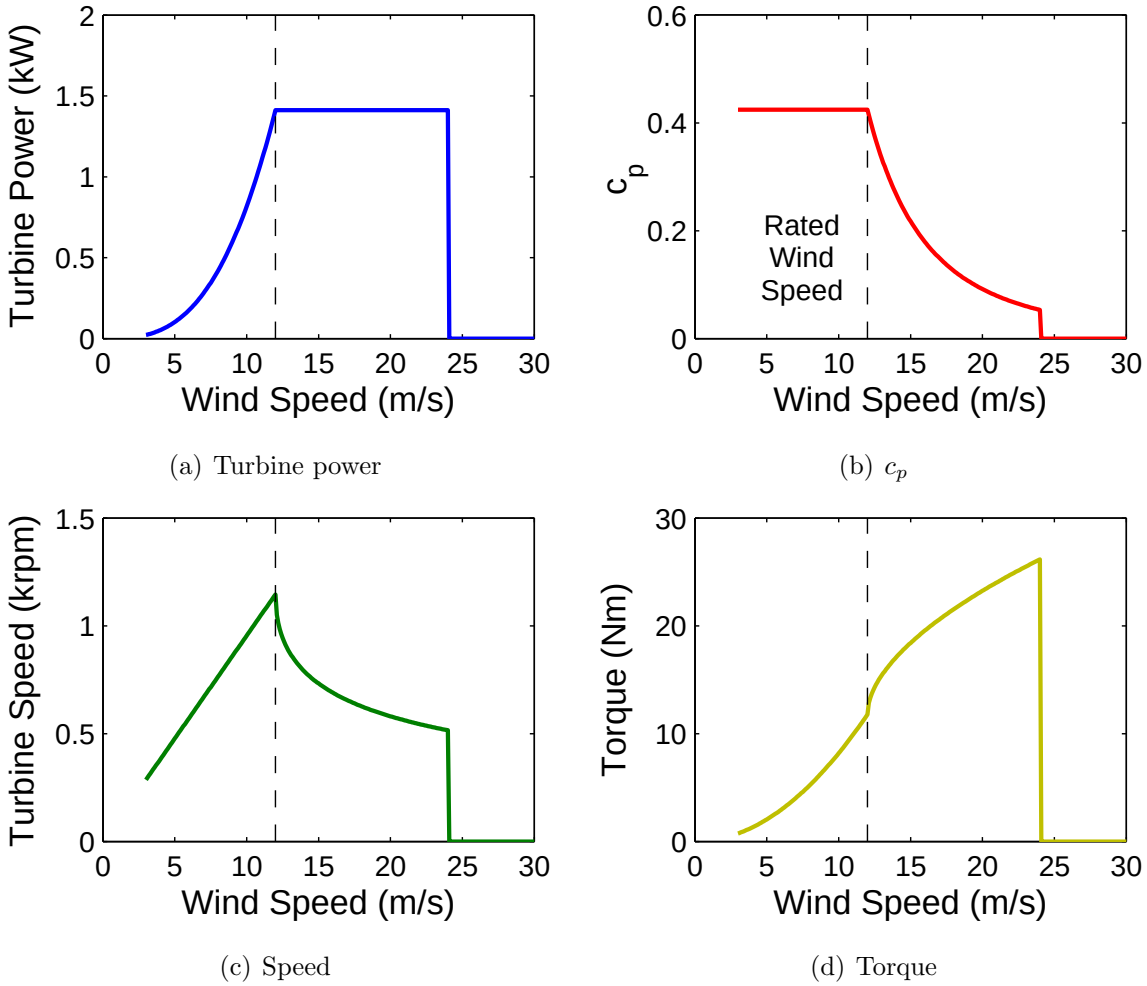


(a) Turbine speed

(b) Wind speed

Figure 1.4: Simulated typical turbine power vs. (a) turbine, and (b) wind speed characteristic. The solid black lines show the power maximisation (MPPT) and constant power modes of operation, i.e. below and above rated wind speed (12m/s), respectively.

The above figures indicate that power is maximised below rated wind speed and maintained constant above rated wind speed by increasing and decreasing turbine speed, respectively. The latter reduces the turbine c_p and increases torque. This operating state is summarised by Figure 1.5, which shows the turbine's response to both MPPT and constant power operation. In practise, the turbine torque can be increased by controlling the generator output current via a power converter. This principle is experimentally verified later in Section 3.3.3, using a DC-DC converter, and shown by simulation in Section 6.4.1 using a grid-connected inverter.



(a) Turbine power

(b) c_p

(c) Speed

(d) Torque

Figure 1.5: Simulated turbine (a) power, (b) c_p, (c) speed, and (d) torque response to power maximisation and constant power modes below and above rated wind speed, respectively. The vertical dashed lines represent rated wind speed.

1.3 Small-Scale Wind Turbines

1.3.1 Applications

Small-scale wind turbines are used to generate electricity in one of three systems, these include standalone, grid-connected and micro-grid systems. Each system is discussed below:

Standalone System

Early small-scale wind turbines were predominantly used to generate electricity in remote regions or properties such as farms or ranches, and are currently used in remote areas to provide power for communication systems etc. [4]. These are known as *standalone* systems, as the electrical power is generated without the presence of a utility grid. The advantage is that remote properties can operate from locally-generated electricity without incurring the high cost of extending the power grid to the property. The drawback is that the wind energy must be stored, for periods of low or null wind speeds. Although several energy storage options, such as thermal storage, inertia storage, storage by compressed air, hydrogen storage or electrical accumulators (batteries) exist [3], batteries are most commonly used.

Grid-Connected System

Small-scale wind turbines are also used in regions where utility power lines provide electricity. The electricity generated by the turbine is directly fed to the utility via a *grid-connected* inverter (GCI). The main advantages of this arrangement are that energy storage, e.g. bulky deep-cycle battery, is avoided, and that utility operators purchase excess power fed to the grid. Despite the advantages, the cost of a GCI is about the same as a deep-cycle battery and its required charger; based on data obtained from a renewable energy technology supplier catalogue [25].

Micro-Grid System

A micro grid is a small-scale power supply network that is designed to provide energy for a small community, such as a housing estate, isolated rural community or municipal region etc. [26]. These operate in a similar manner to large-scale power systems, i.e. micro grids aim to match the power with the real-time demand without energy storage. The main

challenges of micro grids are power system and frequency control issues. Micro grids are beyond the scope of this work.

1.3.2 Turbine Properties

Small-scale wind turbines use short fixed-pitch blades (up to a few metres), which operate at relatively high turbine speeds, due to their small radius (see Equation (1.4)). This high rotational speed avoids the need for a gearbox, which reduces maintenance and costs, and also improves reliability and efficiency at low wind speeds [27]. Small-scale wind turbines operate at variable speed to maximise the c_p and hence output power. The turbine speed needs to be limited under high wind speeds to avoid high stress on components [28], which may damage the turbine and generators. The turbine speed is limited by using *over-speed protection* mechanisms or *speed-limiting* devices.

Turbine Speed Limiters

Early small wind turbines that were used for simple battery charging applications used DC generators, and have some form of natural speed control. Although the induced voltage is proportional to the generator speed, the generator output voltage is set by the battery voltage, and hence the machine output current increases with wind speed. The torque is proportional to the machine output current and hence the generator speed is set by a balance of the wind turbine and electrical torque [6].

Alternative forms of turbine speed control include *furling* and *stall control*. Furling uses a governor-flyball or spring arrangement [3], which yaws or tilts the turbine out of the direction of the incoming wind [29]. Furling is a self governing action that occurs once the wind exceeds rated speed; the concept is illustrated in Figure 1.6. The turbine is shown to be perpendicular to the incoming wind, for wind speed v_1, which corresponds to a wind speed less than rated. The turbine begins to furl as the wind speed increases to v_2 and then v_3, increasing the axial force on the turbine and hence the tension and length of the spring. The turbine is substantially furled for wind speed v_3. Note that the figure illustrates the concept for horizontal furling, however, vertical furling also exists, where the turbine appears similar to a helicopter [4, 13].

Stall control is another method that limits turbine speed and power under high wind speed conditions. This method, unlike furling, does not require mechanical components, as the blades are specifically designed to be less efficient at high wind speeds [2, 5]. The

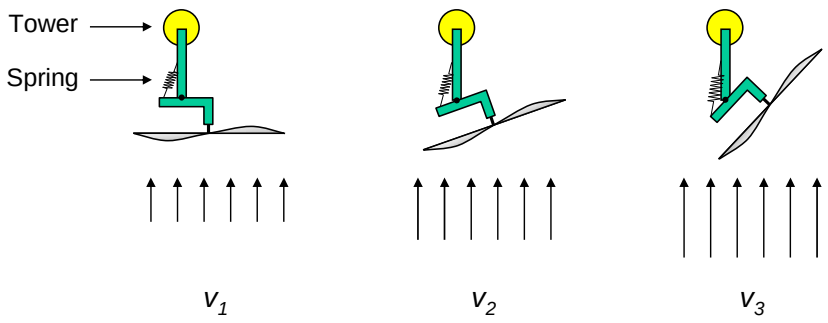


Figure 1.6: Furling action taken by small-scale wind turbines under increasing wind speeds, v_{1-3}. The turbine begins to furl for v_2, and is largely furled for v_3. Note that the vector lengths indicate relative wind speeds.

resulting turbine rotates slower than fixed-pitch blades under increasing wind speeds, which reduces the tip-speed ratio and hence c_p.

The drawback of both furling and stall control is the unwelcome acoustic noise [30], caused by the high tip-speed ratio and the angle of the passing air with respect to the blades. Hence, lower noise speed limiting mechanisms are required. One solution is to control the machine current and hence torque using a power converter; an alternative, which is applicable only to DC generators, is to adjusting the field excitation.

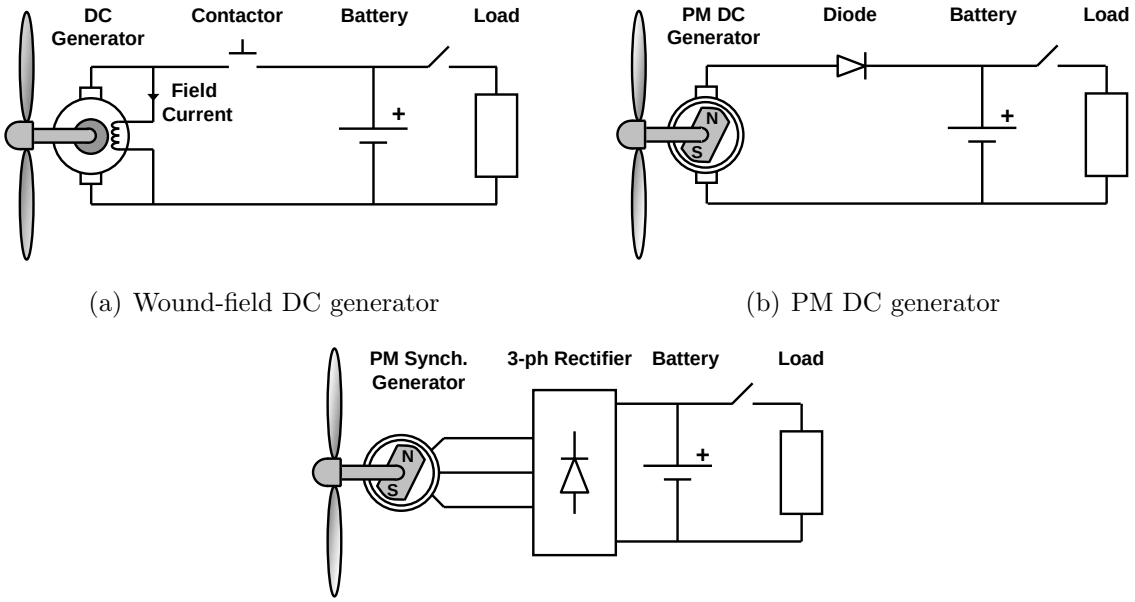
1.3.3 Generator Varieties

Standalone Wind Turbines

Small-scale turbines of the 1930's used shunt-excited DC generators and were used to charge batteries. The generator was directly driven and its output was connected to a battery via an automatic contactor that closed, allowing current to flow from the generator to the battery, once the wind speed and induced voltage exceeded that of the battery. This arrangement is shown in Figure 1.7(a), which also shows that loads, such as electric motors or lights, were connected to the battery via switches.

The main drawback with this arrangement is that the full power is fed to the battery via a carbon brush and commutator arrangement, which requires regular brush replacement [23]. A diode replaced the contactor with the advent of semiconductors, and PM DC generators replaced the wound-field DC generators. The advantage of such a generator is a constant excitation, without the need for field current and hence field winding copper losses. The drawback however, is the lack of excitation control and that full power is still

transmitted through carbon brushes. Permanent magnet synchronous generators offer the best solution, as carbon brushes are not required. These however, require a full-bridge diode rectifier, due to their three-phase AC output voltage / current. The circuits of the DC, PM DC, and PM synchronous generators used for battery charging, are shown in Figure 1.7.



(a) Wound-field DC generator

(b) PM DC generator

(c) PM synchronous generator

Figure 1.7: Comparison of early and modern small-scale turbine topologies used for battery charging, including (a) wound-field DC, (b) PM DC, and (c) PM synchronous generators.

Grid-Connected Wind Turbines

During the late 1970s, small-scale wind turbines were first used for grid-connected power generation. Research was carried out in the U.S. where generators such as induction, synchronous, and Lundell automotive alternators were used [23]. Although synchronous machines also use a carbon brush arrangement, they were favoured over DC machines, as the carbon brushes are not replaced as often. This is due to the small amount of current, that required to excite the field, that is transmitted through the slip ring / carbon brushes arrangement.

Induction machines were widely used both in Denmark and in the US, as they are cheaper than synchronous machines. Induction machine production peaked in 1981 in

the US, however, these moved away from small-scale to medium-scale wind turbines, as those used for small-scale applications were deemed a failure [13]. The drawback of directly-connected synchronous machines was the requirement to operate at synchronous speed, such that power was fed to the grid at the grid frequency.

The advantages of variable-speed operation were known, and two methods to integrate variable-speed wind turbines were examined in the literature. The first used a *rotary inverter*, which consisted of a variable-speed AC generator that controls a DC machine that is coupled to a second AC generator. The concept was to operate the grid-side generator at synchronous speed, by controlling the speed of the DC machine. The main drawback of this arrangement is the poor peak efficiency, of about 60% [23], which is due to the use of three electrical machines.

The second method investigated to grid-connect variable-speed generators, was the use of power converters. This will be further discussed in Section 1.5.

1.3.4 Current Trends

A survey of currently available small scale wind turbines is presented in [31]. This catalogue suggests that for wind turbines rated below about 10kW, PM synchronous generators are used, whilst induction machines are used for rated powers above 10kW. The catalogue also suggests that small wind turbines rated at 1kW or less are generally not grid connected, whereas turbines upward of 1kW generally are, through the use of power converters. The survey shows that small scale turbine power is controlled by microprocessors or battery regulators, and that speed is controlled by furling or stall control.

PM excitation is generally favoured in modern small-scale turbine designs since it allows for higher efficiency, and does not require external excitation current [32]. In addition, these are capable of variable speed operation, which is required to maximise aerodynamic efficiency. The drawback of these generators, however, is the lack of back-EMF voltage control, i.e. the back-EMF voltage is controlled by the turbine speed. The use of a three-phase PM generator and three-phase rectifier are nowadays common. The turbine operating speed is controlled by the generator torque [33]. This is achieved using a power converter.

Power Converters

Power converters are required for directly-driven permanent magnet (PM) synchronous generators, as the variable-frequency and magnitude AC output current / voltage (pro-

duced by variable-speed operation), is unsuitable for transmission, storage or use. Batteries and the majority of power converters require a constant DC voltage, which is easiest achieved using an uncontrolled or controlled rectifier. Rectifiers can either be used alone or in conjunction with an additional standalone or grid-connected power converter. Standalone and grid-connected power converters will be discussed in detail in Sections 1.4 and 1.5, respectively.

Permanent Magnet Material

Small-scale PM generators tend to use rare-earth magnets, such as *Neodymium Iron Boron* magnets. These are preferred as they have a magnetic energy product up to 10 times greater than those of *ferrite* and other permanent magnets, such as the *Aluminium Nickel Cobalt*, varieties [34]. Rare-earth magnets offer high remanent flux densities and can be used to produce machines which achieve high efficiencies and have high (generator) power densities. These properties make rare-earth magnets the magnet of choice for for many applications, including direct drive wind turbines [34].

1.3.5 Inductance Classification of PM Generators

PM generators used in wind turbine applications may have low or high inductance. The majority of PM generators have short-circuit currents that are greater than the rated current which are referred to as *low-inductance* machines. These machines are well-suited to drive the voltage-source inverters which are commonly used in grid-connected inverters. Low-inductance machines require an oversized power converter in order to achieve a wide field-weakening range, and can produce high currents under fault conditions. High currents can also be produced during over-speed conditions. If a power converter, such as the boost converter, is used, the induced back-EMF voltage can exceed that of the DC link, which can produce high currents.

In contrast, some generators have such high values of inductance that their short-circuit current at high speed equals their rated current [35]. These machines are referred to as *high-inductance* generators and can readily achieve a wide constant power speed range. Note that care needs to be taken not to open-circuit these machines at high speeds, due to their large back-EMF voltage.

A comparison of the current vs. voltage (I-V) locus of a conventional low-inductance and a high-inductance generator is shown in Figure 1.8. The figure shows the I-V characteristics of an ideal PM machine for speeds of n and $2n$, and load resistance lines for

high and low resistances. Note that the generator produces an open-circuit voltage that is proportional to its speed, whilst the short-circuit current is fixed for all speeds, as the stator reactance also increases with generator speed. The figure shows that a traditional low-inductance machine operates as a variable-magnitude voltage source, whilst a high-inductance machine operates as a fixed-magnitude current source when its output voltage is much less than its open-circuit voltage. This concept, along with an explanation of the ideal machine model used to determine the loci, will be further discussed in Section 2.1.2.

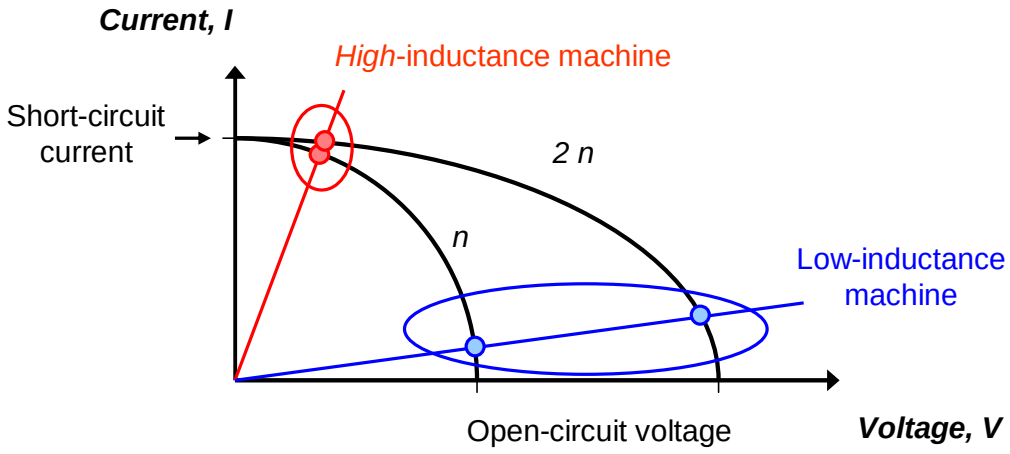


Figure 1.8: Current vs. voltage locus of low and high-inductance PM generators, for generator speeds of 1 and 2pu.

1.4 Standalone Power Converters

The most common standalone power converters are discussed below, these are used for battery charging, turbine power maximisation, or to operate household appliances.

1.4.1 Common Power Converters

Power converters, such as inverters [36] and rectifiers have been used to obtain constant DC voltages from AC generators. Rectifiers have either been controlled [37,38], or uncontrolled and used as a switched-mode rectifier [39], or with a DC-DC converter. Common DC-DC converters include the *boost* [40–44], *buck* [45], and *buck-boost* converter [46], of which the boost converter is the most common.

Note that the use of rectifiers and power converters for small-scale wind generation, is similar to that for automotive power generation using an alternator. Hence, a summary of automotive and small-scale wind power generation research, including the types of power converters and generators investigated, is shown in Table 1.3, where IPM, ISA, LA and SG, are acronyms for interior PM, integrated starter-alternator, *Lundell* alternator and synchronous generator, respectively.

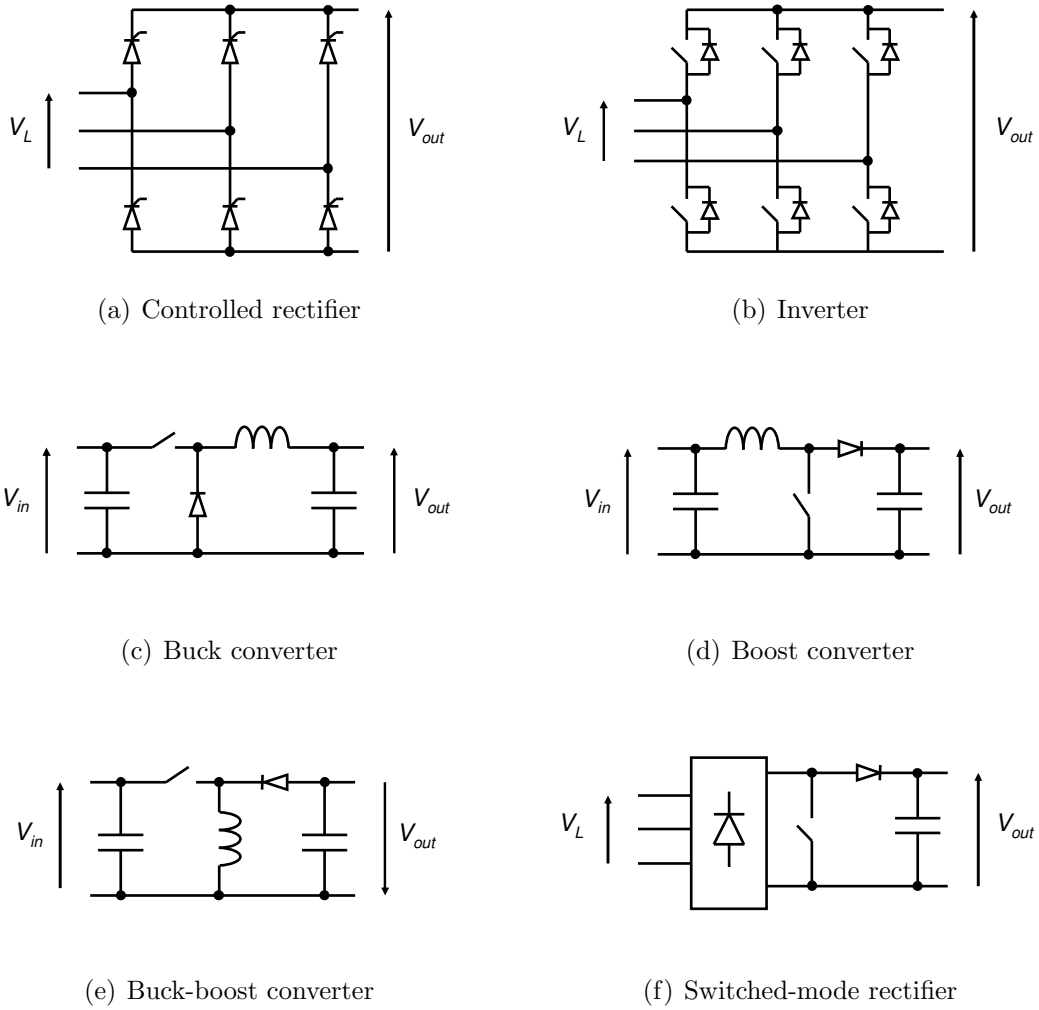
Table 1.3: Summary of the research and the type of generators and power converters, used for small-scale wind and automotive power generation.

Converter \ Application	Wind	Automotive
Inverter	IPM - Morimoto [36]	ISA - Lovelace [47]
Controlled Rectifier	Jones [37] PM - Raju* [38]	LA - Liang [48] PM - Naidu [49]
SMR	PM - Venkataramanan [39]	LA - Hassan [50], Rivas [51] and Perreault [52] IPM - Soong et al. [53]
Boost	PM - Chen* [40], Hao [41] SG - Prats* [42], Song* [44] Smith* [43]	PM - Tolbert [54]
Buck	PM - Chau* [45]	PM - Gutt [55]
Buck-Boost	SG* [46]	PM - Tolbert [54]

Note: * indicates that the power converters are used as part of a grid-connected system.

Converter Circuits

The circuits of the controlled rectifier, inverter, buck, boost, buck-boost and switched-mode rectifier (SMR) are shown in Figure 1.9, whilst the key properties and differences are summarised in Table 1.4. Note that the figure does not include the uncontrolled rectifier. However, it is included in the table as it can be used for battery charging and other DC applications without an additional power (DC-DC) converter. In addition, the switches of each power converter, with the exception of the controlled rectifier, are controlled using pulse-width modulation (PWM) techniques.



(a) Controlled rectifier

(b) Inverter

(c) Buck converter

(d) Boost converter

(e) Buck-boost converter

(f) Switched-mode rectifier

Figure 1.9: Comparison of DC power converter equivalent circuits, showing the (a) controlled rectifier, (b) inverter, (c) buck, (d) boost and (e) buck-boost converters, and (f) the switched-mode rectifier. The converter DC output voltage, V_{out}, is shown for each converter, along with its DC or AC (line) input voltage, i.e. V_{in} or V_L, respectively.

Table 1.4: Comparison of small-scale wind turbine generator DC power converters

Converter Topology	Switch Count	Control	Relative Cost
Uncontrolled Rectifier	0	-	low
Controlled Rectifier	6	medium	medium
Inverter	6	complex	high
Buck	1	simple	medium
Boost	1	simple	medium
Buck-boost	1	simple	medium
SMR	1	simple	low-medium

Although the buck, boost and buck-boost converters of Figure 1.9 are shown without an uncontrolled rectifier, this is required for use with a wind turbine as these converters require a DC input voltage. As such, the rectifier and boost converter combination appear similar in appearance to the SMR. However, the SMR avoids the rectifier output capacitor and inductor, making it cheaper and physically smaller than an equivalent boost converter. Note that the boost inductor, which is required to allow the voltage boosting action to occur, is conveniently provided by the machine inductance in the SMR. In addition, due to its widespread use, the boost converter is discussed further in this study together with the uncontrolled rectifier, inverter, controlled rectifier and SMR.

The high number of controllable switches accounts for the high and medium costs of the inverter and the controlled rectifier, respectively. In addition, both the controlled rectifier and the inverter require information about the generator rotor position, which complicates the control of each converter. In contrast, the SMR and boost converter do not require rotor position information and each have only a single controllable switch, which is controlled by a fixed duty-cycle PWM signal. These aspects reduce the control complexity and cost of each converter. Note that the boost converter with rectifier attracts a higher cost than the SMR, due to the required DC link capacitance and inductance.

Although inverters are conventionally used to convert DC voltage to AC voltage, they are also used to convert AC voltage to DC voltage. Despite its similar appearance to the controlled rectifier, the inverter uses forced-commutated switches, such as the MOSFET or IGBT, compared to thyristors that have controllable firing angles (if used as a rectifier). The inverter switches are more expensive than thyristors and are operated using a PWM switching scheme, which accounts for the high cost and complex control of inverter.

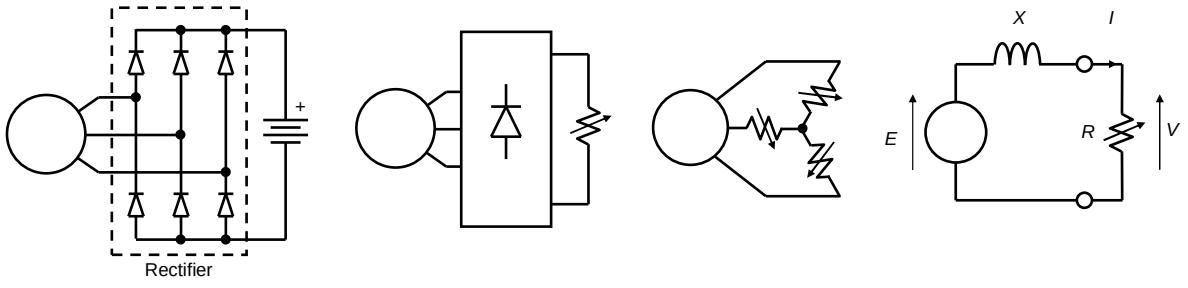
Converter Output Power Comparison

Although the SMR offers a low-medium cost and simple control, it is also important to consider the power characteristic of each converter. These are analysed and compared to that of a standard uncontrolled rectifier for reference. Note that the term "high" in high-inductance generator implies a rated current of 1pu.

1.4.2 Uncontrolled Rectifier Operation

The uncontrolled rectifier is the cheapest and the simplest power converter used in practical systems. It consists of 6 diodes and is used to convert AC voltage to DC, and as such can be used to charge a battery (see Figure 1.10(a)). Charging occurs providing the turbine speed is sufficiently high, i.e. the generator back-EMF voltage is greater than the battery voltage. Note that although the induced voltage is directly proportional to speed, the rectifier output (battery voltage) will remain fixed as the generator speed and hence back-EMF voltage increase.

The power characteristic of an uncontrolled rectifier can be determined by simplifying the generator, rectifier and battery models. The battery can be replaced by a variable resistive load. Since the rectifier forces the generator voltage and current to be in-phase [56], it can be modelled as a variable three-phase resistive load. The rectifier equivalent circuit and its simplified models, including the DC and three-phase resistive load models, are summarised in Figure 1.10. Note that the single-phase model also includes the generator induced voltage, E, generator phase reactance, X, equivalent load resistance, R, and resulting current, I, and voltage, V.



(a) (b) (c) (d)

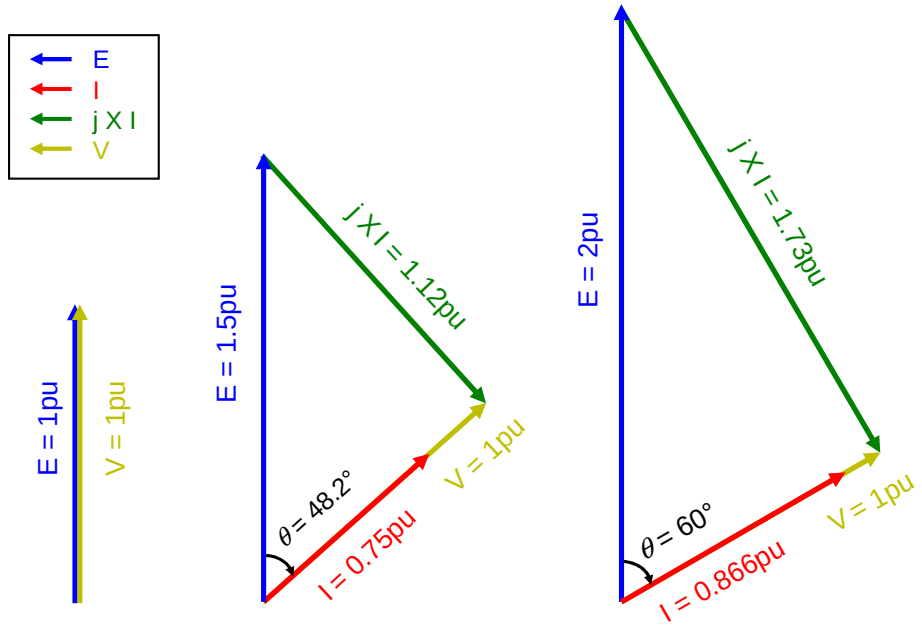
Figure 1.10: Uncontrolled rectifier modelling, showing (a) circuit diagram, (b) equivalent DC resistive loading, (c) simplified AC resistive loading, and (d) single-phase equivalent circuit. Note that the rectifier is represent by the dashed and solid boxes in (a) and (b), respectively.

Phasor Analysis

In this study, the machine equivalent output voltage, current and power is simulated for a DC link voltage of 1pu. It is assumed that a generator speed of 1pu yields a reactance and a generator back-EMF voltage of 1pu. The output voltage is the vector summation of the induced voltage and the voltage drop across the stator reactance, as shown in Equation (1.5). The machine power, P, is given by Equation (1.6), where ϕ is the angle between the output voltage and current phasors (see Figure 1.11). The figure shows that ϕ is equal to 0° as the rectifier forces the output current and voltage to be in-phase with each other. The phasor diagrams also show the angle between the induced voltage and current phasors, θ; the torque per ampere is maximised when this is equal to 0°.

$$V = E + j\,X\,I \tag{1.5}$$

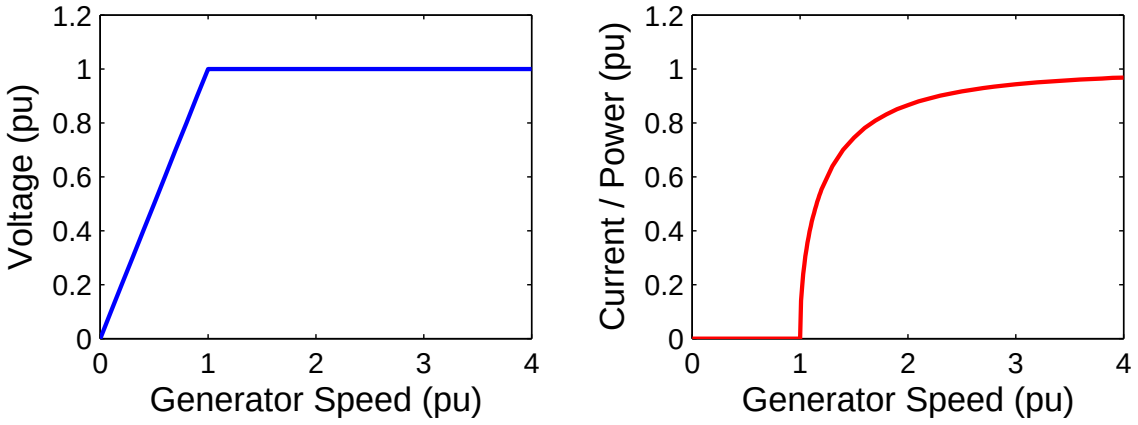
$$P = V\,I\,\cos(\phi) \tag{1.6}$$



(a) n = 1pu (b) n = 1.5pu (c) n = 2pu

Figure 1.11: Rectifier phasor diagram showing induced voltage, E, output voltage, V, output current, I, and voltage drop across the inductor, jXI, for generator speeds of (a) 1, (b) 1.5 and (c) 2pu. Note that current does not flow for speeds $\leq$ 1pu, and that the induced and output voltage phasors are equal for case (a); they are shown to be separated by a small distance for simplicity.

As shown in the above phasor diagram, the machine current does not flow to the load for generator speeds less than 1pu. This occurs as the induced voltage, which is directly proportional to machine speed, must exceed that of the DC link voltage for current to flow. The current (and hence power) sharply increases with generator speed above speeds of 1pu, and levels off approaching its peak value of 1pu as the generator speed increases. This is known as *uncontrolled generation* (UCG) [56], as the power increases with speed and is not controllable [33]. This is illustrated in Figure 1.12.



(a) Voltage

(b) Current and power

Figure 1.12: Generator output (a) voltage, and (b) current and hence power, vs. generator speed characteristic.

Small-scale turbines are often located in areas that experience low average wind speeds. The resulting low turbine and hence generator speeds indicates that the use of an uncontrolled rectifier will prevent power flow at low wind speeds. In addition the power generated at high wind speeds is uncontrollable (see the above figure). The solution is to use a power converter that allows the generator current and hence torque to be controlled. This allows power to be extracted at low wind speeds, and controls the turbine speed such that the peak aerodynamic efficiency (c_p) is obtained for all wind speeds. Therefore, a power converter can effectively operate as a maximum power point tracker, and is hence often used as an intermediate stage with another power converter, e.g. a grid-connected inverter (as seen in Table 1.3, references [38, 40, 42–46]).

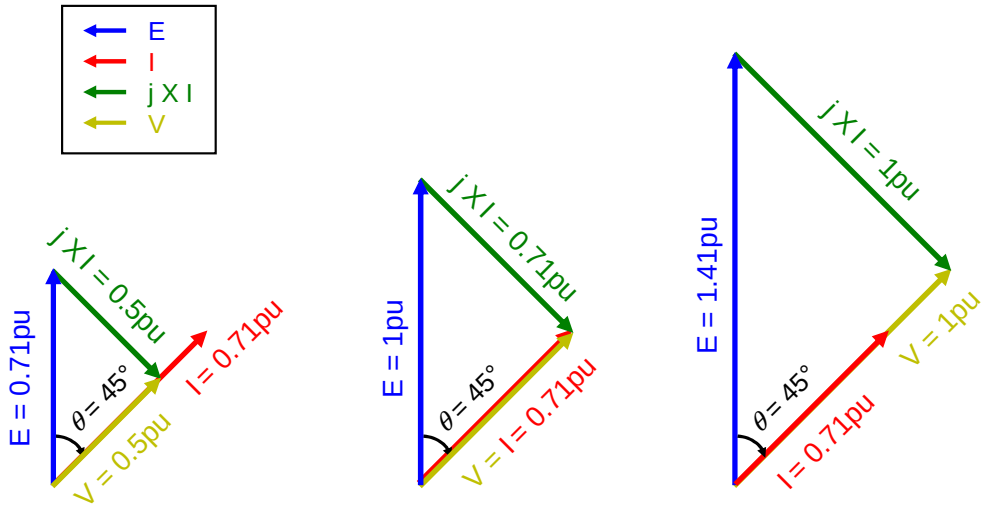
1.4.3 Switched-Mode Rectifier

The switched-mode rectifier operates in a similar manner to that of the boost converter, i.e. it increases (boosts) its input voltage to a fixed output voltage. The boosting action is

used to effectively reduce the rectifier output voltage to some value less than the induced machine voltage. This is achieved by varying the converter duty-cycle, and allows power to be produced by the machine even at low generator speeds. As such, the SMR is modelled in the same manner as the uncontrolled rectifier, except the effective rectifier output power can be controlled by the duty-cycle.

Phasor Analysis

The rectifier phasor diagrams of a SMR, corresponding to maximum output power below generator speeds of 1.41pu, are shown in Figure 1.13. Those corresponding to speeds greater than 1.41 pu are identical to those of the uncontrolled rectifier (Figures 1.11(b) and 1.11(c)), and are hence not repeated here. The output current and voltage phasors, of the previous section, was shown to be in-phase due to the resistive load model. In addition, the output current is equal to 0.71pu over the speed range, which corresponds to maximum power that was obtained when the phase resistance and reactance of Figure 1.10(d) are equal in magnitude. This is known as *load-matching*. Note that the phasor diagrams of Figure 1.13 are identical in shape, but scale in magnitude with generator speed.

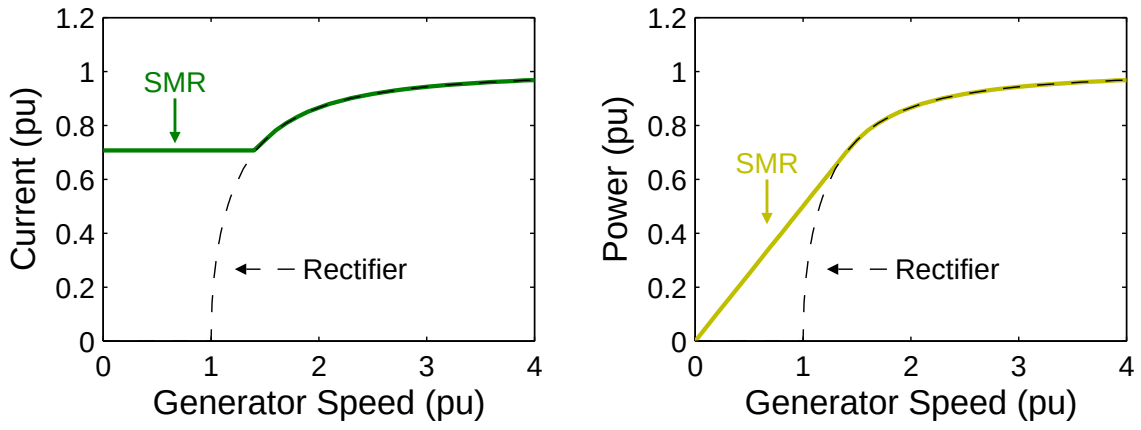


(a) n = 0.71pu (b) n = 1pu (c) n = 1.41pu

Figure 1.13: SMR phasor diagrams showing induced voltage, E, output voltage, V, output current, I, and voltage drop across the inductor, jXI, for generator speeds of (a) 0.71, (b) 1 and (c) 1.41pu.

The generator current and power (corresponding to the peak power obtainable using the SMR) is shown in Figure 1.14 as a function of generator speed. The peak generator

(and SMR) output power increases linearly with generator speed until a speed of 1.41pu, after which, the peak power increases in an identical manner as the uncontrolled rectifier. As such, the SMR is said to operate as boost rectifier at low generator speeds, whilst for speeds above 1.41pu, it acts as an uncontrolled rectifier under maximum output power operation. Note that any power below the solid line in Figure 1.14(b) can be obtained using the SMR. This is further discussed in Chapter 3, along with boost rectification.



(a) Current

(b) Power

Figure 1.14: Generator output (a) current, and (b) power vs. speed, corresponding to maximum power operation, using the switched-mode rectifier (SMR). The dashed line represents the current and power obtained using an uncontrolled rectifier.

1.4.4 Inverter Operation

The inverter is also capable of extracting power from the generator at low speeds, however, it requires an accurate rotor position sensor, which attracts a higher cost and complicates the control. The inverter is able to obtain rated current for all generator speeds and maintain it in-phase with the induced voltage at low generator speeds to maximise the output power. The inverter is hence able to extract more power than that obtainable using the SMR at low generator speeds. The corresponding machine model, under inverter operation, is shown in 1.15.

Phasor Analysis

The machine phasor diagrams corresponding to inverter operation are shown in Figure 1.16, for various speeds. Consider Figure 1.16(a), which corresponds to the phasor

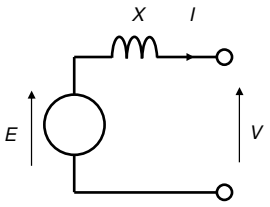
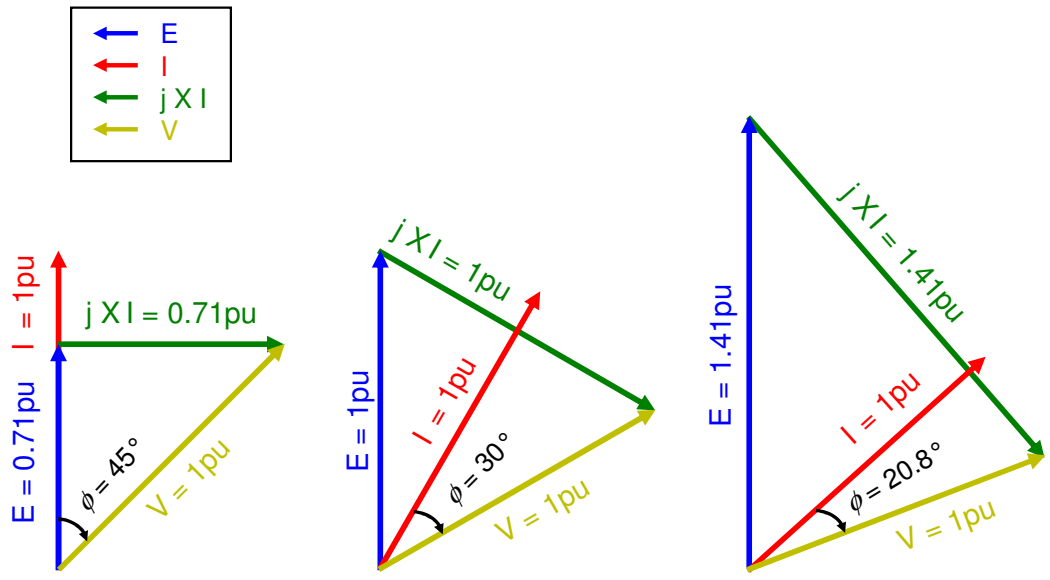


Figure 1.15: Simplified machine phase model operating with an inverter, showing the induced voltage, E, reactance, X, and output voltage, V, and current, I.

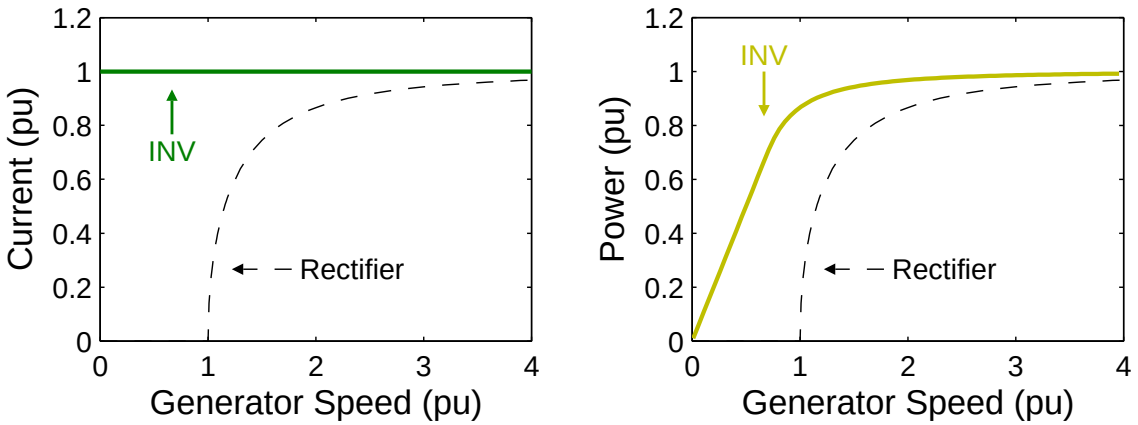
diagram at a generator speed of 0.71pu. Under this condition, the torque and hence machine power are maximised as θ is equal to 0°, i.e. the current and induced voltage phasors are in-phase with each other. The output voltage is now twice that obtained using the SMR (1 vs. 0.5pu), whilst the current is now also 41% larger (1 vs. 0.71pu). In addition, the current and output voltage phasors now have a 45° phase shift, i.e. power factor of 0.71 lead. Despite the phase shift, the increased current and voltage allows the inverter to extract twice the output power of the SMR (see Equation (1.6)).



(a) n = 0.71pu (b) n = 1pu (c) n = 1.41pu

Figure 1.16: Inverter phasor diagram showing induced voltage, E, output voltage, V, output current, I, and voltage drop across the inductor, jXI, for generator speeds of (a) 0.71, (b) 1 and (c) 1.41pu. Note that this figure shows ϕ, rather than θ as shown in the previous phasor diagrams.

The above phasor diagram shows that the voltage and current phasors remain fixed at 1pu for all speeds greater than 0.71pu. The phase angle of the current relative to the induced voltage, θ, is shown to increase with speed. This reduces the power factor angle, ϕ, which allows the inverter to approach unity power factor and hence a peak power of 1pu, as the generator speed increases. The machine current and hence power vs. speed characteristic, using an inverter, is summarised in Figure 1.17.



(a) Current

(b) Power

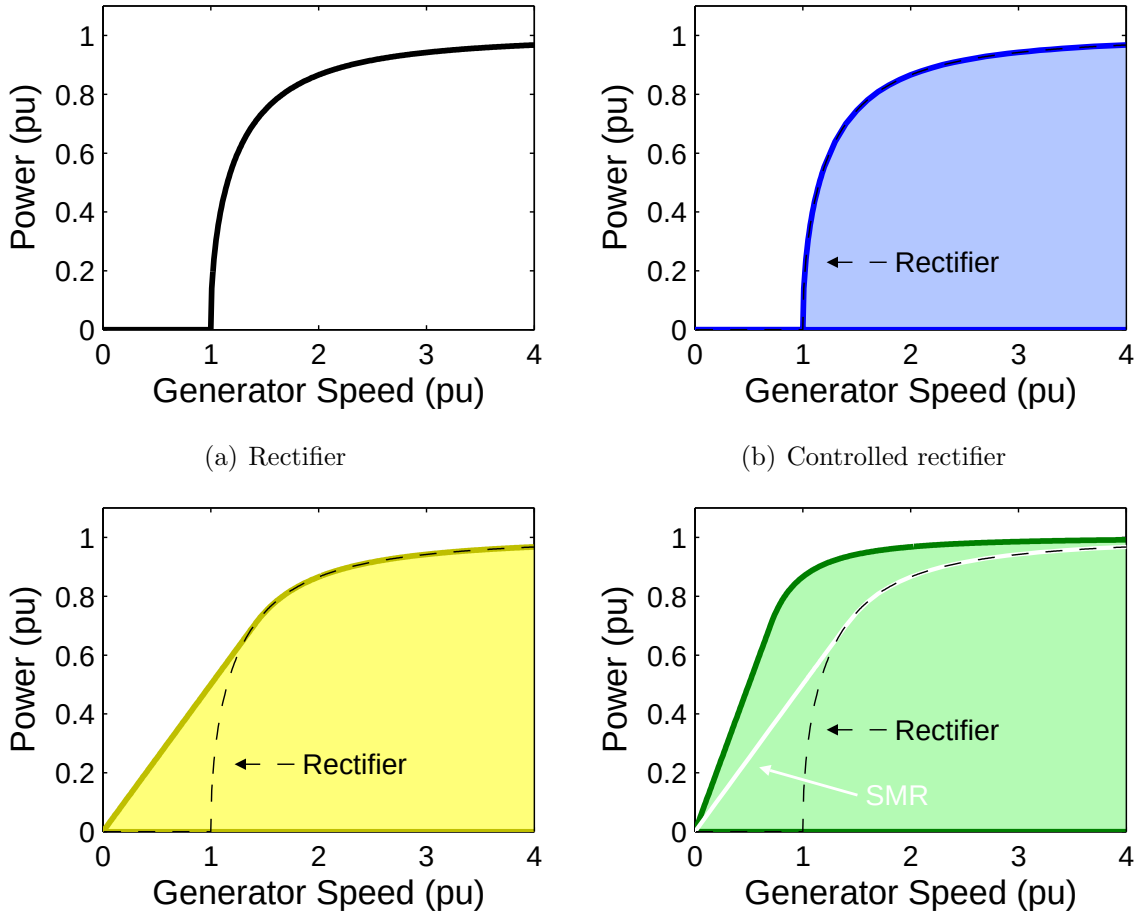
Figure 1.17: Generator output (a) current, and (b) power vs. speed, corresponding to maximum power operation, using the inverter (INV). The dashed line represents the current and power obtained using an uncontrolled rectifier.

1.4.5 Power Comparison of Standalone Converters

Figures 1.14(b) and 1.17(b) clearly show that both the SMR and inverter obtain power from the generator at low speeds, unlike the uncontrolled rectifier. Further comparison shows that the inverter is able to extract twice the peak power compared to the SMR at low generator speeds, whilst at high speeds, they both asymptote towards the same power, i.e. 1pu. Recall that both the SMR and inverter are able to reduce the power to any level below their maximum value. This is summarised in Figure 1.18, which also compares the power range of the uncontrolled and controlled rectifier.

The figure clearly shows the benefit of a controlled power converter, i.e. power can reduced to any desired value, unlike the rectifier whose output power is governed by the generator speed. The controlled rectifier is unable to extract power from the generator at low speeds. The SMR can extract power at low generator speeds and offers simple control. This is achieved by effectively load-matching the generator to the voltage source

load by choosing an appropriate duty-cycle. The inverter is able to offer twice as much power at low speeds than the SMR. This is achieved as the inverter offers greater control of the generator output current. Note that there is little difference between the high-speed output power of the inverter and SMR.



(a) Rectifier

(b) Controlled rectifier

(c) Switched-Mode Rectifier

(d) Inverter

Figure 1.18: Comparison of power converter output powers, showing that obtainable using an (a) uncontrolled rectifier, (b) controlled rectifier, (c) switched-mode rectifier (SMR), and (d) inverter. The dashed lines of (b)-(d) represent the power obtained by the (uncontrolled) rectifier, and are shown for reference. Subfigure (d) also compares the power obtained by the SMR, for reference.

Hence, the choice of power converter is selected based on a low-speed output power vs. cost trade-off. Despite producing only half of the inverter's low speed output power, the SMR is selected due to the absence of sensors, which reduce the total cost, and its simple control.

1.5 Grid-Connected Inverters

Grid-connected (GC) inverters used for small-scale wind turbines use a rectifier to obtain a DC voltage from the generator. The majority of the inverter is hence similar to those used for photovoltaic (PV) installations, and therefore the literature about PV inverter topologies is also reviewed and discussed.

1.5.1 Introduction

Small-scale wind turbines feed power to the utility grid using a grid-connected inverter (GCI). Unlike standalone inverters that control the output voltage, GCIs control the output current [57], as they are effectively connected to an infinite bus (fixed voltage source). However, these inverters must meet strict grid requirements, such as total harmonic distortion, power factor and DC current injection specifications, which will be discussed later in Section 4.1.1. Note that these requirements complicate the inverter design and control, which increase the total cost. This is illustrated in Figure 1.19 which compares the cost of commercially available standalone and GC inverters. The costs given in the figure are obtained from a catalogue [25], and are shown as a function of inverter power rating.

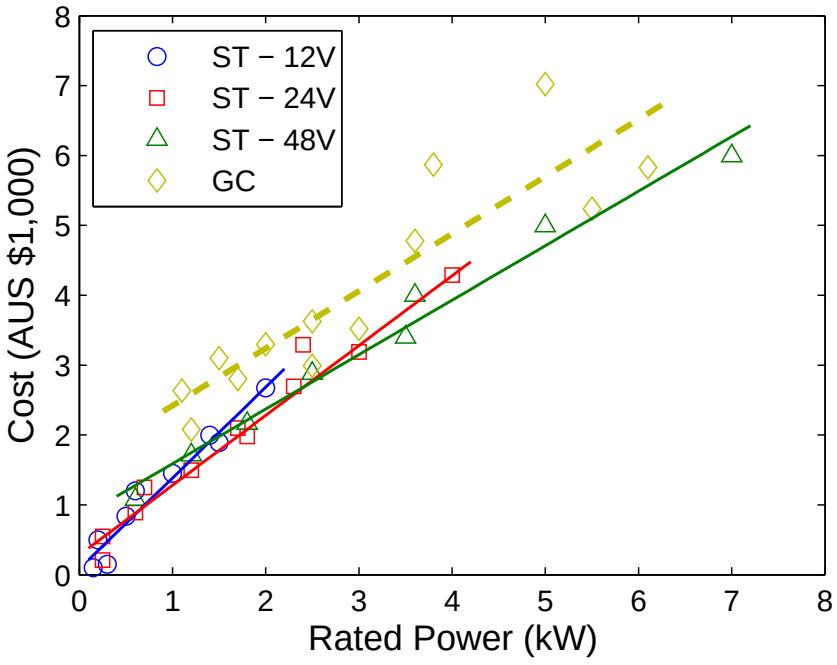


Figure 1.19: Cost comparison of standalone (ST) and grid-connected (GC) inverters. The solid and dashed lines represent cost trendlines for ST and GC inverters, respectively.

The above figure clearly shows the increased cost associated with a GCI, i.e. about AUS$1000 more than a similar-sized standalone inverter. The survey also shows that the input voltage increases with power, for standalone inverters. This is required to prevent high input currents (and hence losses), and to improve the overall efficiency. The figure also shows that the inverter cost can be optimised by using a 12V inverter for power levels below 650W, whilst a 24V inverter should be used below 2.4kW.

Inverters can be classified by many attributes, including input type, the switch / commutation type, controllable output variable, and transformer type, which are discussed in the following section.

1.5.2 Line-Commutated Inverters

Early GCIs used for PV applications in the late 1980's were line-commutated current-source inverters and in the order of several kilowatts [58]. This type of inverter was also used with wind turbines as the technology had been used for high-voltage DC transmission since the 1970's [59] and it was a mature, efficient, robust, low-cost and reliable technology [33, 58, 60]. However, the main drawbacks of this inverter are the reactive power drawn from the grid, which results in a power factor of between 0.6 and 0.7 [58] lag, and the high harmonic content of the output current. The output current of a line-commutated inverter is typically a square-wave of 120° conduction angle, which contains large low-order harmonic components in the range of 250–350Hz [61]. An example of the output current and the line-commutated current-source topology is shown in Figure 1.20. Note that the inverter shown in the figure corresponds to a three-phase CSI, and that neither the rectifier or the generator are included.

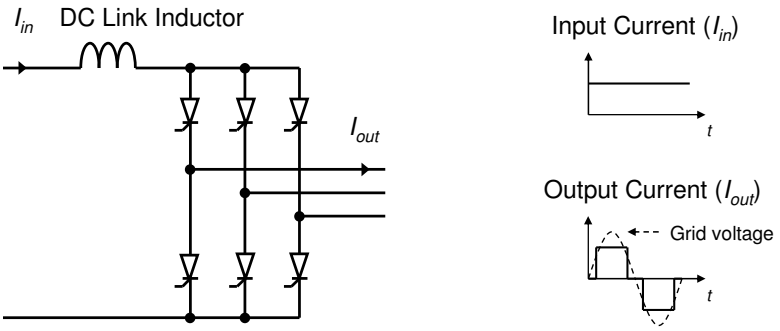


Figure 1.20: Circuit diagram and square-wave output current of the line-commutated current-source grid-connected inverter topology.

Harmonic Reduction

Compensators (based on auxiliary PWM VSI with line-current feedback [33]) and passive tuned filters have been examined in [60] to reduce the output current distortion and improve the power factor. The use of *Notch* filters will be examined in detail in Section 5.2.6, despite being large and costly for low-order harmonic frequencies [61]. Notch filters, tuned to the 5^{th} and 7^{th} order harmonics, together with a second-order damped filter, tuned to the 11^{th} order harmonic, were shown to significantly improve the power factor. However, they were ineffective at removing the low-frequency harmonics.

In contrast, the use of active power compensators (active parallel filters) was shown to significantly improve the output current distortion. This is achieved by controlling the compensators to generate AC currents which form an ideal output waveform, when combined with the distorted current [60]. Despite their success, the addition of active compensators increases system complexity and cost. An outline of a line-commutated inverter with passive filters and active compensation is shown in Figure 1.21.

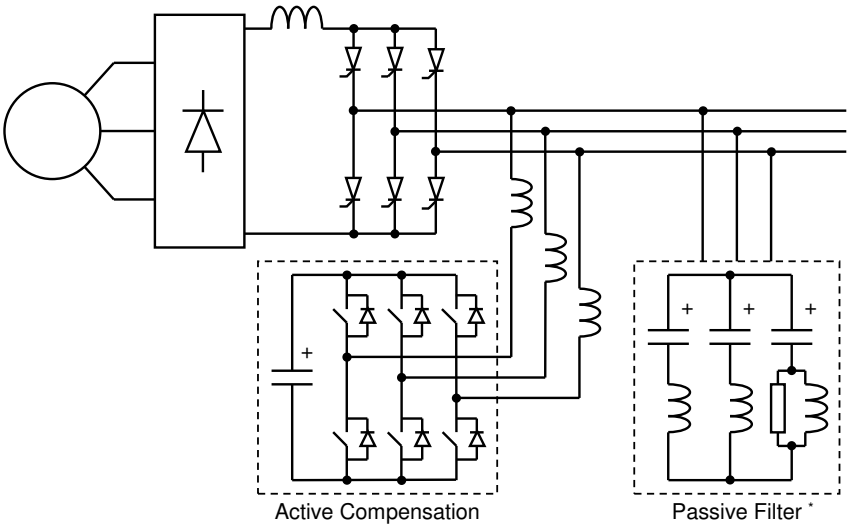


Figure 1.21: Current-source inverter with active compensation and passive filters, examined by Chen [60]. Note that the rectifier and PM generator are also shown, along with a three-phase passive filter*.

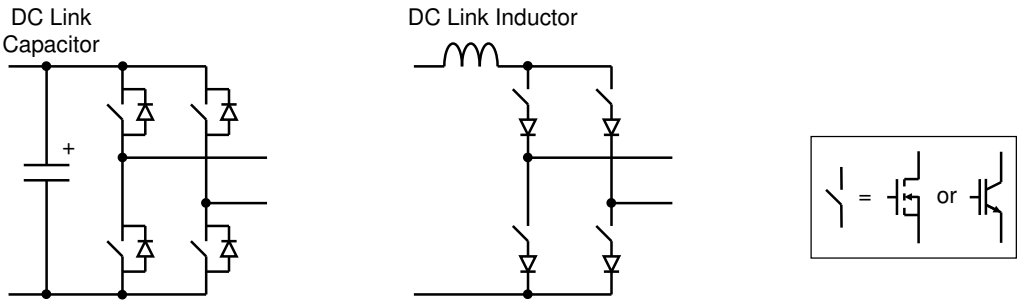
Note that active compensators are modern power electronic devices [60], which use self-commutating semiconductor switches, such as the IGBT or MOSFET. As it is well known, these switches have replaced thyristors in many power electronic converters, due to the recent rapid development of the semiconductor device industry [58,62]. As such, the majority of commercially available GCIs now use self-commutating switches, and high-

frequency (above 3 kHz [63]) pulse-width modulation (PWM) control strategies. The resulting high-frequency switching harmonics are attenuated using a smaller and lower loss filter than that required for a line-commutated inverter [61], and allow much greater control of the power factor. A survey of in [62] shows that modern inverters obtain power factors of 0.9 or greater, over a wide range of operating conditions.

1.5.3 Self-Commutated Inverters

Two types of self-commutated inverter exist, these are the voltage-source inverter (VSI) and the current-source inverter (CSI). The VSI requires constant DC input voltage, which is provided by a DC link capacitor, whilst a CSI requires a constant DC current, which is provided by a DC link inductor. These passive elements decouple the grid from the input power source and provide energy storage. This is required as it allows the inverter input and output powers to differ and prevents input current or voltage ripple, which affects output current distortion; this is further examined in Section 5.1.1. However, a trade-off exists as increased storage capacity increases the overall inverter cost and power losses.

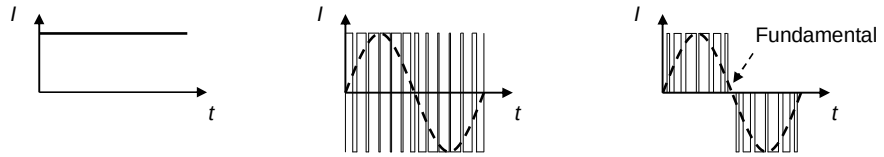
In addition, the arrangement of semiconductor switches, feedback controllers and low-pass filter arrangements of the VSI and CSI topologies differ; low-pass filters are discussed later in Section 5.3. The CSI requires a series-connected diode with each IGBT or MOSFET to provide unidirectional current flow and bidirectional voltage blocking [64, 65]. These diodes, however, increase the overall cost and conduction (power) losses [65]. Similarly, the switches of the VSI require anti-parallel (freewheeling) diodes to provide bidirectional current flow and unidirectional voltage blocking capability [64]. The key differences between the self-commutating VSI and CSI topologies are highlighted in Figure 1.22.



(a) VSI (b) CSI

Figure 1.22: Comparison of self-commutating (a) voltage-source inverter (VSI), and (b) current-source inverter (CSI) topologies. The key difference are the energy storage element and switch / diode configuration. Note that the switches are either MOSFETs or IGBTs.

Open-loop PWM switching schemes, such as the common bipolar and unipolar sinusoidal schemes, could yield an alternating current from an ideal current source, as shown in Figure 1.23. In practise, however, feedback is required as input currents / voltages vary. Both types of inverters use feedback control systems, that sample and adjust control signals, to deliver a sinusoidal current to the grid. This differs from standalone inverters that traditionally sample and regulate the output voltage [57]. The fixed grid voltage regulates the inverter output, allowing the output current of a CSI to be controlled in proportion to the modulation factor, which makes the CSI appropriate for a power conversion system [66].



(a) Input (b) Bipolar output (c) Unipolar output

Figure 1.23: Ideal (a) input, and (b) bipolar PWM and (c) unipolar PWM output currents.

Note that the bipolar output current is obtained by switching the state of both phase legs, whilst the unipolar scheme requires only one phase leg state to change [67]. The unipolar sinusoidal PWM switching scheme, including a harmonic analysis, is further discussed in Section 5.2.4.

PWM Control Strategies

Grid-connected inverters use a variety of feedback based PWM control strategies to control the output current, which include current hysteresis and space-vector modulation schemes [68]. A comparison of the operation of a 100kVA IGBT VSI using each control strategy, is reported in [68]. The space-vector control scheme results in the least current THD, i.e. 5%, however, it is the most complex scheme, has a slow current response, and attracts the highest cost. The current hysteresis scheme yields a current with 7.7% THD, and is well suited to fast-varying input powers, as it provides over-current protection and offers high power factor.

More information regarding both the open-loop and feedback based PWM control signals, including the derivation of control signals, is given in appendix A.1.

Voltage vs. Current-Source Inverters

Voltage-source inverters are generally regarded to be more efficient than an equivalent CSI, as the DC link capacitor has lower power losses compared to the resistive and core losses of a DC link inductor [69]. Despite this, the output voltage of a VSI must exceed that of the peak grid voltage, implying that either a high-voltage input source or the use of a step-up transformer or boost converter is required. The use of either increases the total cost and reduces the overall efficiency [64].

In contrast, the average output voltage of a CSI is equal to that of the grid. The CSI is also advantageous over the VSI as its output fault current is limited. However, care must be taken using the CSI to prevent open circuiting the DC link inductor, which may destroy inverter components. Similarly, VSIs must avoid simultaneous gating of two switches in the same leg to prevent high currents destroying components. Hence *dead time* must be introduced to the VSI controller. The drawback, however, is that dead time causes output current distortion [64]. The amount of distortion is proportional to the length of the dead time [70].

Switching Loss

The main drawback of self-commutating inverters is the higher switching power loss. This is caused by commutating the switches whilst the current flowing through (or the voltage drop across) the device is non zero, and is also referred to as *hard-switching*. The switching loss, P_{sw}, is proportional to the device turn-on and turn-off times, t_{on} and t_{off}, the output current, I_{out}, DC link voltage, V_{DC}, and the switching frequency, f_{sw}, as summarised in Equation (1.7) [67], assuming an inductive load.

$$P_{sw} = \frac{1}{2}\,(t_{on} + t_{off})\,V_{DC}\,I_o\,f_{sw} \tag{1.7}$$

Some inverter topologies use zero-voltage or zero-current switching techniques to reduce switching losses. These techniques involve commutating a switch when the current through or the voltage across the device is zero. These are known as *soft-switching* techniques. Examples of GCI topologies that employ soft-switching techniques are discussed in Section 1.5.6.

1.5.4 Transformer Type

Three transformer topologies exist for grid-connected inverters, these include the *line-frequency* (LF), *high-frequency* (HF) and *transformerless* (TL) topologies. Each topology is discussed below.

Line-Frequency Transformer

Line-frequency transformers are designed to operate at the grid frequency (50 or 60Hz) and are located between the grid and inverter output. The role of the transformer is to decouple (isolate) the inverter from the grid, provide voltage boosting (step-up transformer) and eliminate DC currents. The transformer also provides line reactance and a small amount of resistance that may assist with filtering or filter damping.

The majority of PV grid-connected inverters used in Korea employ LF transformers [71]. However, despite the above mentioned benefits, there is a trend to move away from this topology as these transformers are heavy, bulky and expensive [71].

High-Frequency Transformers

The physical size and cost of a transformer can be reduced by increasing its operating frequency [71]. Hence, transformers of frequencies 400Hz and above are used in some grid-connected inverters. Despite the size and cost benefits of a HF transformer, the GCI requires two inverter stages and additional components, which reduce the overall inverter efficiency and reliability [72], and increases control complexity [58]. In addition, DC currents may be injected in to the grid, which cause saturation and overheating of utility distribution transformers.

High-frequency transformers are preferred and used in inverters that have low rated powers, whilst LF transformers are generally used in high-power inverters [73, 74].

Transformerless Topologies

The transformerless inverter topology has been examined in [75], as it is physically smaller, lighter, cheaper and more efficient than topologies that contain transformers. This is verified in Table 1.5, which compares the peak efficiency, weight and cost of the transformer and TL GCI topologies [76].

Despite the benefits of the TL topology, it is unable to isolate the energy source from the grid, and can not remove DC components at the output. In addition, low voltage

Table 1.5: Comparison of single-phase grid-connected inverter properties [76].

NOTE:
This table is included on page 36 of the print copy of
the thesis held in the University of Adelaide Library.

sources such as parallel-connected PV cells require voltage boosting to transmit power to the grid. This is achieved using an additional DC-DC converter, which increases cost and reduces efficiency. The common-mode voltage and lack of isolation between the grid, PV cells and associated wiring are probable reasons that the TL topology is prohibited in Italy and the United Kingdom [58].

Cost / Performance Trade-Off

As stated above, each transformer topology has certain advantages and disadvantages associated with it. A summary of key transformer and transformerless GCI topology properties are given in Table 1.6.

Table 1.6: Comparison of line-frequency, high-frequency and transformerless grid-connected inverter topology properties.

Property \ Topology	Line-Frequency	High-Frequency	Transformerless
Operating Frequency	50 or 60Hz	>400Hz	-
Size (relative)	Large	Medium	Small
Weight (relative)	High	Medium	Low
Cost (relative)	High	Medium	Low
Provide Isolation ?	Yes	Yes	No
Remove DC Components ?	Yes	No	No
Provide Line Reactance ?	Yes	No	No
Boost Voltage ?	Yes	Yes	No

It should be noted that voltage boosting and isolation are important issues for PV applications, due to their low voltage and roof-top installations, respectively. These issues, however, are less likely to be of concern for a grid-connected wind turbine as an oversized generator can be used to produce higher voltages, and turbines are often located upon high towers away from inadvertent human interaction.

1.5.5 Voltage Source Topologies

Uncontrolled Rectifier

The use of an uncontrolled rectifier together with a current-controlled voltage-source inverter is the simplest type of GCI. This topology is reported in [68] and is shown in Figure 1.24. The inverter uses a fast analogue-to-digital converter (ADC) and microcontroller to adjust the inverter control signals based on the sampled output current, to produce the desired sinusoidal output currents.

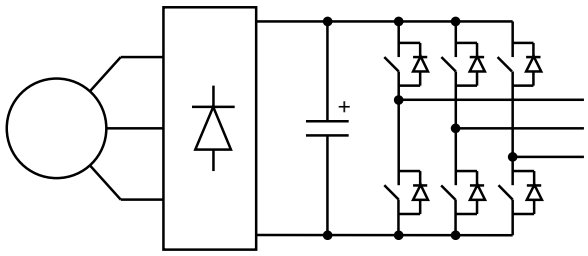


Figure 1.24: Common 3-phase voltage-source grid-connected inverter.

The main disadvantages of the above inverter topology are the limited life span, due to the DC link (electrolytic) capacitor, and the poor performance at low wind speeds. Low wind speeds cause the generator to rotate at low speeds, where the resulting induced voltage is less than the required DC link voltage. Under this condition the DC link capacitor is being charged through the inverter anti-parallel diodes, which causes excessive reactive power flow [77]. In addition, the controller loses its ability to control the output current and hence injects a highly distorted current, that may contain a significant DC component, to the grid.

To prevent high output current distortion and / or DC current injection, a normal IGBT inverter should disconnect itself from the grid at low wind speeds (3–5m/s [77]). This implies that the wind turbine will fail to extract energy at these low wind speeds, and may account for as much as 20% of the turbine's annual energy yield. A solution investigated in [77], was the inclusion of a reverse-blocking diode between the DC link capacitor and the inverter output stage, as shown in Figure 1.25. The diode is introduced to ensure unidirectional power flow at low wind speeds, i.e. prevent the grid charging the DC link capacitor. This solution has only limited success as the inverter is still unable to inject a high quality sinusoidal current to the grid at low wind speeds, due to the presence of low-order harmonics. This causes the overall power factor to be lagging and increases generator losses [77].

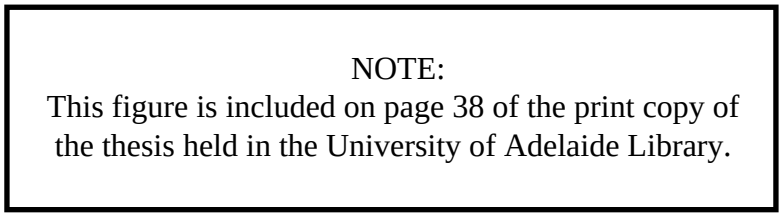


Figure 1.25: Single-phase voltage-source inverter with reverse-blocking diode, as investigated in [77], to prevent reactive power flow and high current distortion at low wind speeds.

Low Wind Speed Power Improvement

DC-DC power converters, such as the boost [40, 42, 44], buck [45], and buck-boost [46] converters have been used as an intermediate stage of a grid-connected inverter (see Table 1.3). These converters are used to maximise the turbine power by controlling the turbine speed such that the peak c_p is obtained. As such, these converters operate as maximum power point trackers (MPPT); a term which is more commonly used for PV GCI topologies.

The use of a boost converter is most common [78], and has the advantage of effectively adjusting the rectifier output and hence generator output voltage. This allows power at low generator (wind) speeds to be extracted, as previously seen in Section 1.4.3. The equivalent circuit of the combined boost converter and VSI is shown in Figure 1.26. The main drawback of this arrangement is the use of two electrolytic capacitors, which reduce the overall reliability, and the necessity of a boost inductor.

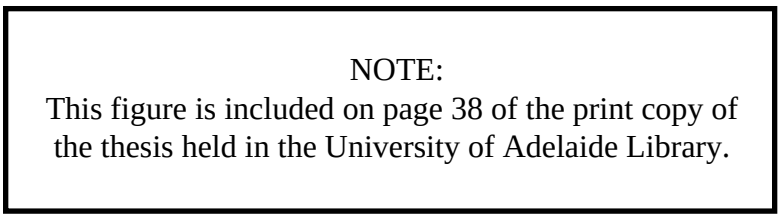


Figure 1.26: Voltage-source grid-connected inverter with boost converter.

The use of back-to-back PWM inverters was investigated in [79] to optimally control a PM generator in a wind turbine, and is now widely used [9]. The circuit is shown in Figure 1.27, which has a high switch count. This, together with the additional requirement

of a rotor position sensor and a complex controller, significantly increases the overall cost. Despite this drawback, the use of the inverter input stage allows better utilisation of the generator, compared to that of a boost converter and will allow the use of a smaller generator (see Figure 1.18).

Figure 1.27: Back-to-back PWM voltage-source grid-connected inverter configuration investigated in [79].

High-Frequency Transformer

A high-frequency transformer PV GCI was constructed and tested in [71]. The input stage consists of a DC-DC converter containing a transformer operating at 20kHz and is used to boost the PV array output voltage and provide an output current which resembles a full-wave rectified sine-wave, as shown in Figure 1.28. The transformer output current is filtered by a small inductance before being fed to an *unfolding* circuit to produce the desired AC output current.

Figure 1.28: High-frequency (HF) transformer inverter topology presented in [71]. The inverter consists of HF PWM DC-DC converter and a line-frequency H-bridge unfolding circuit. Note that various current and voltage waveforms illustrate the inverter operation.

Despite the advantage of the reduced size and cost of the transformer, the HF transformer inverter requires several additional components, which increase its complexity and can reduce its reliability and efficiency [72], compared to that of a LF transformer inverter.

1.5.6 Current Source Topologies

PWM Controlled Inverter

Various control strategies were examined with a sensorless self-commutated PWM current-controlled GCI in [21]. The wind energy system, which is shown in Figure 1.29, consists of an uncontrolled rectifier, DC link inductor and PWM current-source inverter. The turbine output power is maximised by adjusting the DC link voltage according to wind speed. This is achieved by varying the inverter modulation index, which ultimately adjusts the pule width (duty-cycle) of the PWM control signal. Five alternative power maximisation control strategies, including one based on an open-loop controller, were shown to improve the power maximisation capability of the turbine without significantly increasing the complexity of the control.

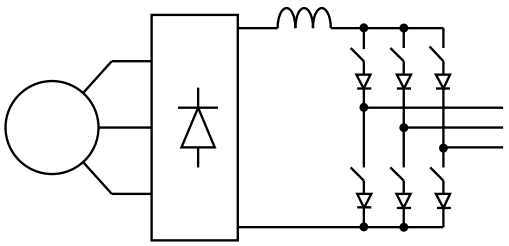


Figure 1.29: Three-phase current-source PWM grid-connected inverter circuit.

The main drawback of the above inverter is the high switching losses, due to the high-frequency PWM control signals, and the resistive and core losses associated with the DC link inductor.

H-Bridge Inverter

The line-frequency commutated H-bridge inverter is used as part of a PV GCI, as shown in Figure 1.30. The inverter input current is modulated by another converter stage and resembles that of a rectified sinusoid. The H-bridge inverter hence acts as an *unfolding circuit*, and operates at twice the grid frequency producing a sinusoidal output current.

The advantage of this circuit is the zero-current and zero-voltage switching scheme that effectively eliminates switching losses, i.e. only semiconductor conduction losses remain

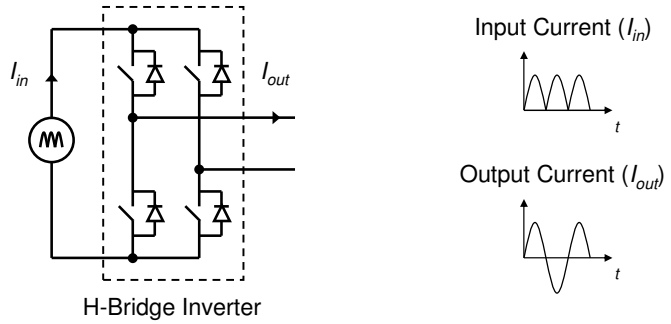


Figure 1.30: Line-commutated H-bridge inverter used as part of a photovoltaic grid-connected inverter, reported in [80]. The inverter input current, which resembles a rectified sinusoid, and the resulting sinusoidal output current is also shown.

[80]. The circuit cost could be reduced by using thyristor switches, which would naturally commutate based on the input current zero-crossings.

Alternative Soft-Switched Inverters

Two soft-switching current-source inverters have been investigated in the literature. The first study, investigated in [81] is shown in Figure 1.31, where a DC voltage source and DC link inductor provide the current-source input current. The inverter itself is based on a line-commutated topology, i.e. it uses thyristors. The key difference is that an additional parallel-connected IGBT is used to short the current-source output to ground using a high-frequency PWM control scheme. This allows the thyristors to commutate naturally, which is referred to as *active commutation*. However, the IGBT in this topology is hard-switched, which will cause significant switching loss.

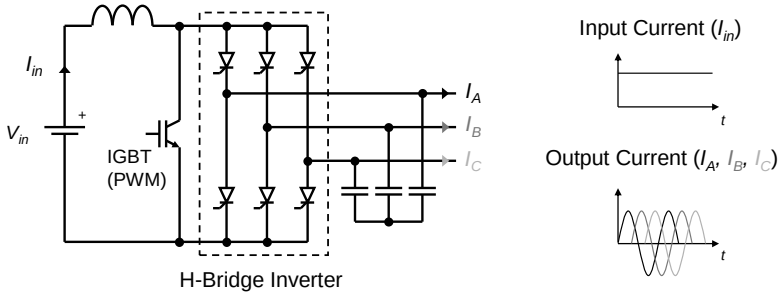


Figure 1.31: Actively-commutated thyristor based current-source inverter investigated in [81], showing the circuit and ideal input and output current waveforms.

The advantage of the above circuit is that rugged, high-power, low-cost thyristors are used for the H-bridge components [81]. These commutate naturally as a result of the high-frequency IGBT switching. The high-frequency PWM switching implies the size of the DC link inductor and filter capacitors can be reduced in size, and that the output current harmonic contents can be well controlled [81]. In addition, the use of thyristors, which have a blocking capability, avoids the need for series-connected reverse-blocking diodes, unlike a self-commutating CSI.

An alternative soft-switching CSI topology was also investigated for a PV GCI in [69]. The inverter topology is summarised in Figure 1.32, which consists of a DC link commutation circuit, and an IGBT H-bridge inverter with series-connected diodes. The commutation circuit is comprised of two semiconductor switches, two diodes and an LC resonant circuit, which provides a current path such that zero-current switching of the H-bridge can be achieved. The drawback, however, is the added cost and the increased control complexity of the LC resonant circuit, compared to that of a single IGBT used in [81].

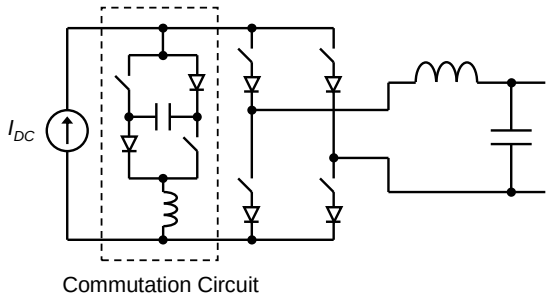


Figure 1.32: Soft-switching single-phase current-source grid-connected inverter topology examined by Han et al. [69], showing the current source, commutation circuit, current-source H-bridge inverter, and line output filter.

Note that the PV cell is treated as the current source, as PV cells have characteristics of both voltage and current sources [69].

1.5.7 Current Trends

A survey of PV GCIs [62], revealed that all modern inverters are of the voltage-source type. The majority (81%) of these control the inverter output current, whilst the remaining 19% control the inverter output voltage. A second survey done in [58], indicates that 55% of GCI incorporate a line-frequency transformer. High-frequency transformer topologies make up 0.3% of the market share, despite the size and cost benefits of such a transformer.

About 45% of the market share is made up of transformerless topologies, with about 96% of these employing a boost converter, whilst 4% incorporate a buck converter.

1.5.8 Proposed Grid-Connected Inverter

Despite the current trend of using voltage-source inverters, the proposed GCI is based on a CSI topology. This is shown in Figure 1.33, and will be further discussed in Chapter 4. The topology is similar to that investigated in [81], however, the proposed topology uses a high-inductance PM generator and uncontrolled rectifier as the inverter current source, rather than a DC voltage source and series-connected DC link inductor. A MOSFET is used to allow zero-current switching of the thyristor H-bridge inverter, which actively commutates the thyristors. Note that this will be referred to as the *current wave-shaper* in Part II (Chapters 4–6) of this study. A capacitive-inductive, CL, low-pass filter is used in the output of the inverter to remove high-frequency PWM harmonic components. In addition, the proposed inverter concept will be simulated and experimentally verified with operation into a voltage source (rather than a three-phase resistive load as tested in [81]).

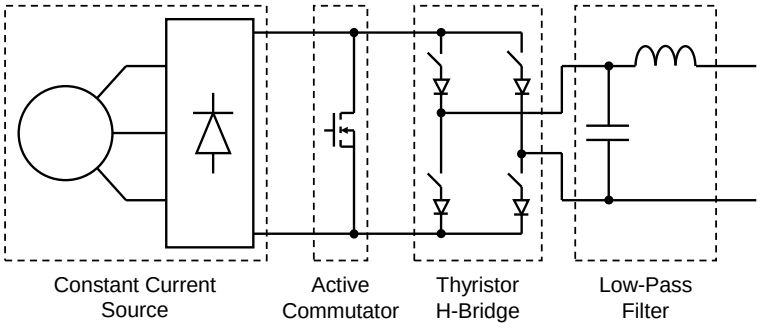


Figure 1.33: Proposed grid-connected inverter topology, including the PM generator current source, active commutator, thyristor H-bridge and low-pass filter.

It should be noted that the above topology has also been investigated for PV-based GCIs, as part of another PhD research project. Some of the publications were listed on page xvii of this thesis.

1.6 Thesis Overview

1.6.1 Aim of Research

The aim of this research is to design, test and validate a novel low-cost power converter topology to control a commercially-available small-scale wind turbine. The DC-DC and proposed grid-connected inverter, both of which are based on the switched-mode rectifier topology, must be able to i) maximise turbine power below rated wind speed, ii) maintain rated power above rated wind speed, and iii) reduce the turbine speed at high wind speeds, to prevent turbine damage.

The operation of each power converter is determined from open-loop dynamometer testing. In addition, the turbine and DC-DC power converter is tested using a small wind tunnel, whilst a high-powered (1kW) grid-connected inverter is simulated over wide range of wind speeds.

1.6.2 Justification for Research

There is growing interest in renewable energy sources due to sustainability and fossil fuels concerns. It has been estimated that the small-scale wind turbine market is growing at roughly 40% per year [18], and that the US alone will sell US a total of $25M–$55M by 2010 [19], depending on the market and other factors such as government rebates, tax incentives etc. Within this market there is an increasing demand for low-cost grid-connected wind turbines, and it is expected that by 2020 small-scale turbines will provide 3% of the US electrical energy consumption [18].

Reducing the cost of the power electronic converter, which make up a significant portion of the cost of a renewable energy conversion system, including solar [82] and wind, will encourage more people to utilise renewable sources of energy. Increased wind or solar power utilisation will reduce the demand for conventionally derived electricity, whilst meeting the increased energy demand. In addition to the environmental benefits, e.g. reduced greenhouse gas emissions, customers who utilise grid-connected inverters are able to reduce their electricity bills, as grid operators purchase their customer's excess electricity.

1.6.3 Original Contributions

The first original aspect of this research is to investigate the suitability of a SMR to control a high-inductance PM generator as part of small-scale wind turbine. This is different to the work presented in [39] where a conventional low-inductance generator is studied. The turbine was simulated and shown to operate at the peak c_p over a range of wind speeds, using a sliding mode current control strategy that compared the switch current to a value corresponding to peak power from a wind-speed look-up table. The work presented in this thesis, however, shows that the SMR can maximise and also limit turbine power, and limit turbine speed. This is simulated and experimentally verified using both a dynamometer and small wind tunnel.

The second original contribution is the investigation of a novel grid-connected inverter topology. The novel current-source inverter is based on the SMR topology and uses a high-inductance PM generator and rectifier as a constant-current source. In this research, the inverter operation is simulated and experimentally verified using a dynamometer test rig. The inverter topology, including a detailed generator model, low-pass output filter, and feed-forward controller, is analysed. An optimised high-powered (1kW) grid-connected inverter is designed and simulated, and shown to effectively control a wind turbine over a wide range of wind speeds.

1.6.4 Thesis Structure

This thesis contains five main chapters that are separated into two parts, as shown in Figure 1.34. Part I (Chapters 2 and 3), investigates the use of the SMR as a standalone (DC-DC) power converter. The selected high-inductance PM generator is described, modelled, characterised, simulated and experimentally tested in Chapter 2. The analytical and computer-based (PSIM®) models are compared with experimentally measured results

Chapter 3 discusses the equivalent circuit model and operating regions of the SMR. The SMR is simulated using PSIM® and is shown to match the experimentally measured data. The SMR is tested using both a dynamometer and wind tunnel test facility, as these arrangements allow the generator and wind speeds to be controlled, respectively. The SMR duty-cycle is varied in an open-loop manner, and its role as a power maximiser, and power and turbine speed limiter are successfully demonstrated.

Part II (Chapters 4, 5 and 6), investigates a novel grid-connected inverter topology based on the high-inductance PM generator and SMR topology. Chapter 4 discusses the

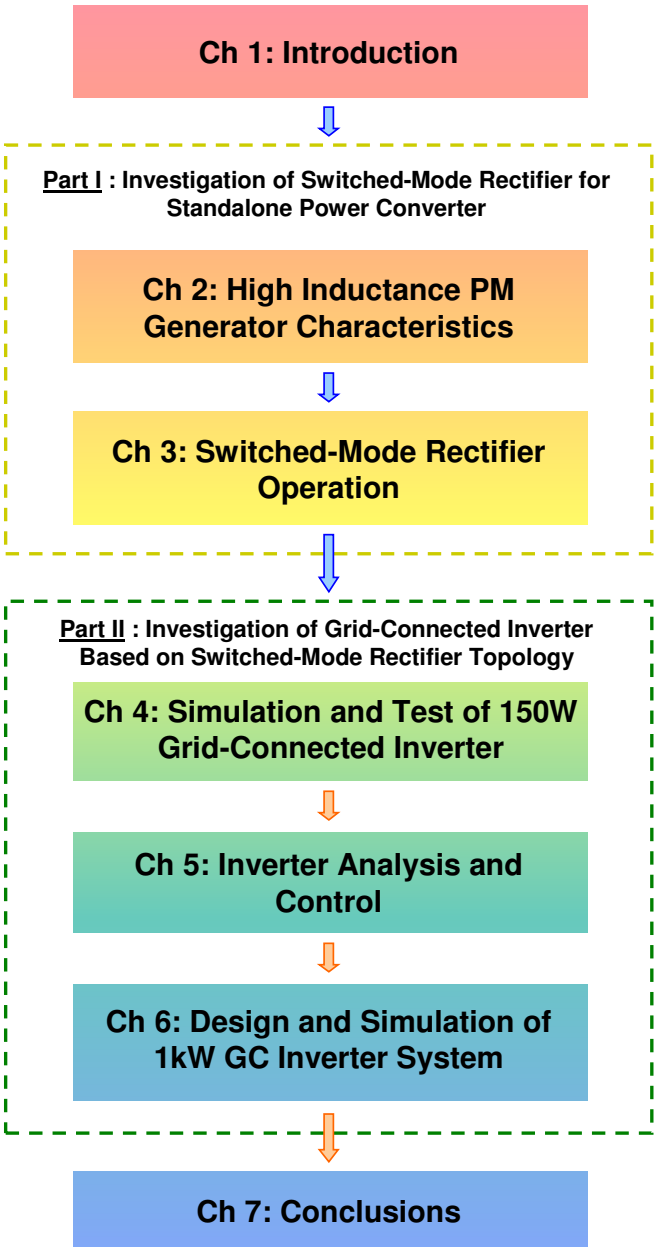


Figure 1.34: Thesis structure, showing part and chapter breakdown.

grid requirements, and the preliminary design, implementation and experimental testing of the proposed grid-connected inverter. The inverter concept is proved for a 150W case, by PSIM® simulations and by open-loop experimental testing.

Chapter 5 analyses in detail the proposed grid-connected inverter, low-pass filter design and a feed-forward based controller. The chapter begins by identifying the PM generator

and uncontrolled rectifier (current source), and the PWM-switching scheme as harmonic sources. The harmonics caused by the unipolar PWM switching are also examined, and techniques to reduce all sources of harmonic distortion are discussed.

The low-pass filter and open-loop control algorithm are identified as the main cause of output current harmonic distortion. As such, the design of the low-pass filter for this type of current-source inverter, is thoroughly analysed. Several damped filter configurations are compared, and the parallel damped inductor is identified as the optimal configuration, offering the best power loss vs. harmonic attenuation trade-off. In addition, Chapter 5 analyses the power factor, harmonic attenuation and damping resistance power loss, and summarises a normalised low-pass filter design approach. The chapter also analyses two feed-forward control algorithms that adjust the inverter modulation index and hence duty-cycle in real-time, to eliminate the input current harmonic components.

Chapter 6 combines the principles of wind energy conversion, described in Section 1.2, with the inverter analysis to design a higher-power (1kW) grid-connected inverter. The inverter is simulated using PSIM®, to investigate the control of the turbine power, torque and speed over a wide range of wind speeds, whilst delivering a high quality current waveform and hence power to the grid.

Finally, Chapter 7 summarises the aims and original contributions of the thesis. The chapter also identifies areas of work that are opportunities for further investigation.

Part I

Investigation of Switched-Mode Rectifier for Standalone Power Converter

Chapter 2

High Inductance PM Generator Characteristics

This chapter examines the machine characteristics of the selected permanent magnet generator. The machine construction and its high-inductance property are discussed. Experimental tests are performed to determine its parameters , which are then used to model the machine. The machine is simulated using analytical models and simulation packages, and experimentally tested over a wide range of operating speeds and loads to verify the models. Particular attention is paid to the DC load modelling and testing, as the PM generator will be used with a three-phase bridge rectifier for the majority of this research project.

2.1 Introduction

The generator selected for this project is a three-phase synchronous surface permanent magnet (PM) machine, that was originally designed and manufactured by Fisher & Paykel® (F&P) for motor applications. The machine was first reported in 1992 [83], and is directly coupled to the agitator and spin-bowl of F&P's range of Smart Drive™ washing machines. The direct-drive system operates effectively as the motor is able to provide high torque at low speeds while still capable of operating at high speeds; these features are required for the washing (agitation) and spin-drying stages, respectively.

Direct-drive systems replace the more conventional belt driven mechanical agitation and braking systems, which significantly improves the efficiency of the appliance [83]. Despite this, the motor requires additional components, such as a variable speed controller

and Hall-effect sensors, to be operated effectively. These components, however, are not required for generator applications, and together with the machine's ready availability, make the machine a convenient low-cost generator. The high torque and wide operating speed characteristic of the F&P surface PM machine make it ideal for a low-cost small-scale wind generator.

An example of an F&P PM machine is shown in Figure 2.1, which shows a 42 tooth concentrated-winding star-connected stator arrangement. These windings are non-overlapped coils (coils wound around a single tooth), which produce very short end-winding length and hence reduce the copper weight and copper loss of the machine [35,84]. In addition, concentrated windings reduce the machine manufacturing cost, due to the winding simplicity, and increase the inductance compared to conventional distributed windings, for the same magnet flux linkage [35]. This high-inductance property is useful when designing power converters, and is further discussed in Section 2.1.2.

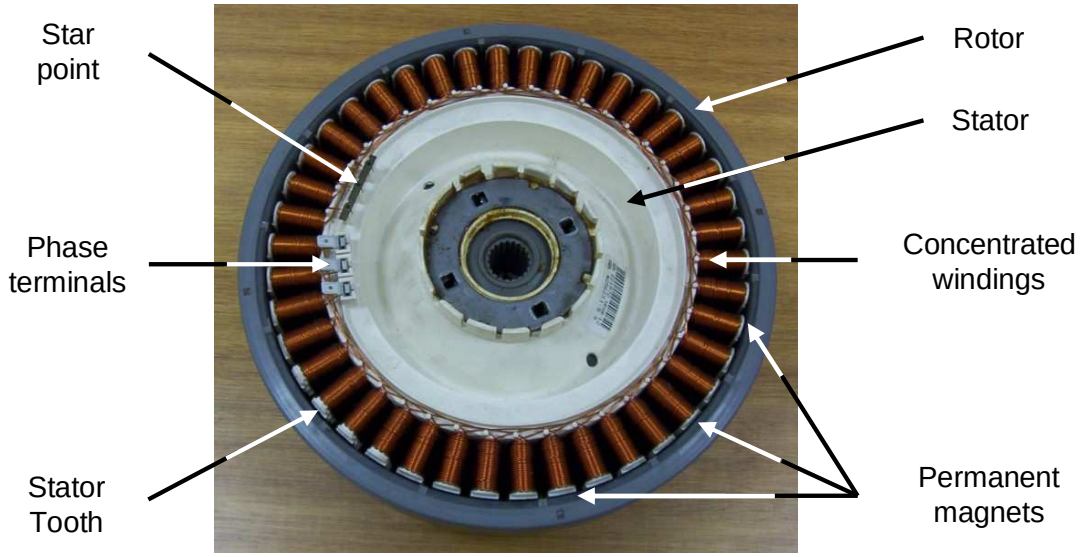
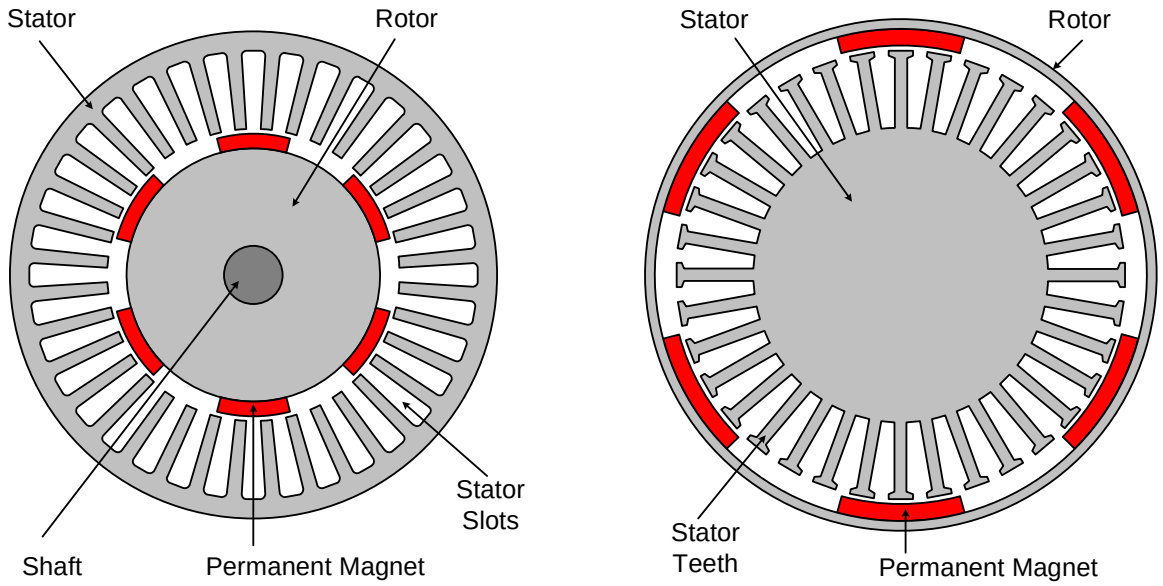


Figure 2.1: Fisher & Paykel® surface PM machine, showing the three-phase terminals, star point, concentrated stator windings, and permanent magnets.

The above surface PM machine uses an outer rotor configuration, as shown in Figure 2.2. The outer rotor configuration has several advantages over the more conventional interior rotor configuration, these include [85]:

- higher output torque due to larger rotor volume,
- magnets are more easily retained against centrifugal forces [86],



(a) Inner rotor

(b) Outer rotor

Figure 2.2: Cross-sectional views of (a) inner, and (b) outer rotor PM machines. Note that the stator windings are not included, for simplicity.

Commercially, the F&P surface PM machines are available in two varieties, these are the 56 magnetic pole / 42 stator teeth, and the 48 pole / 36 teeth configurations. The latter was introduced to reduce cogging torque [83]. These machines are classified as fractional slot winding types, as they have less than 1 slot per pole per phase (SPP). The machine SPP value is calculated according to Equation (2.1) [87], where S is the number of slots, p represents the number of magnetic poles pairs, and m is the number of phases; hence both F&P machines have a SPP value of 0.25. Fractional-slot PM machines with a SPP value of 0.25 or less allow the machine structure to have a lower output torque ripple, though the average output torque may be lower compared with PM machines with higher values of SPP [87].

$$SPP = \frac{S}{2p \,.\, m} \tag{2.1}$$

Fractional-slot concentrated winding PM machines with a wide range of SPP values exist [87]. Each SPP value offers different machine characteristics [35] and a SPP design procedure, based on specific criteria, is summarised in [35, 87]. PM machines with a SPP value of 2/5 or 2/7 are identified as the best candidates. Despite this, the F&P

surface PM machine is used for the small-scale test wind turbine in this study, as these are readily available. In addition, since this research project also investigates power electronic converter design, implementation, analysis, simulation and testing, an optimised machine design is not considered here.

2.1.1 Ideal Machine Model and Current vs. Voltage Locus

A simplified model of a surface PM machine with a three-phase resistive load, consists of a back-EMF voltage source, E, series stator reactance, X, and load resistance, R, as shown in Figure 2.3. The back-EMF voltage source has a voltage and frequency which are both proportional to the machine speed. Note that both the generator open-circuit voltage and stator reactance increase linearly with generator speed. Therefore, the subsequent short-circuit current remains fixed. The resulting normalised current vs. voltage (I-V) locus is shown in Figure 2.4(a). The locus is shown for generator speeds, ω, equal to 1 and 2pu, and load resistances of 0.3 and 10 pu.

The surface PM machine I-V locus is compared to those of the DC and interior PM (IPM) machines, in Figure 2.4(b). The loci comparison is obtained from [88] and is shown for reference only. Note that the interior PM machine shows a voltage over-shoot, i.e. its peak voltage under load is larger than its open-circuit voltage. This phenomenon occurs as the result of its saliency. The IPM locus shown in the figure represents a saliency ratio, ξ, of 4, which corresponds to a voltage over-shoot of about 16%. The saliency ratio represents the ratio of q-axis to d-axis inductance, and significantly increases the complexity of the machine model, compared with a non-salient machine. More information regarding IPM machine modelling can be found in [88].

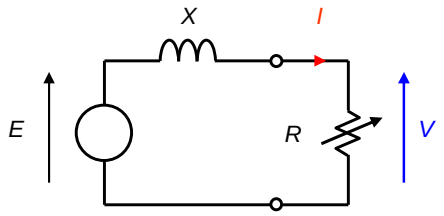
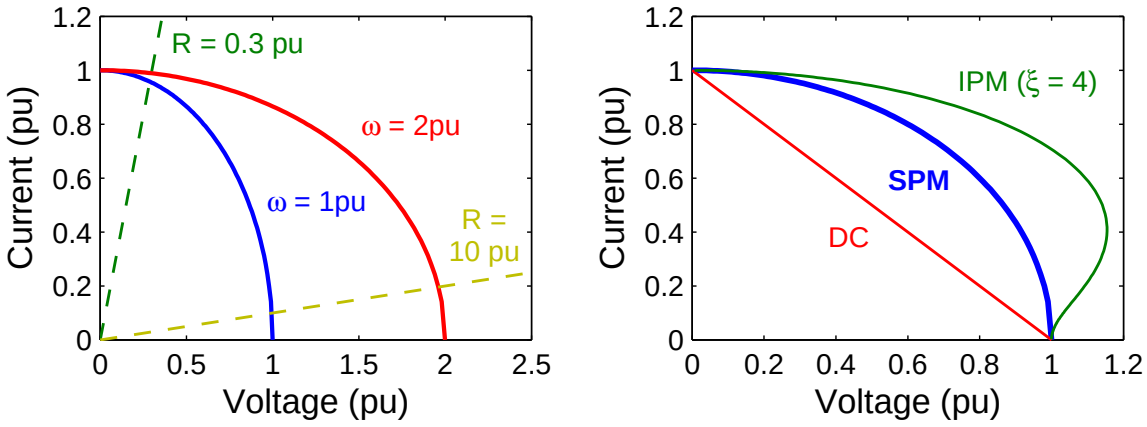


Figure 2.3: Simplified PM machine model, showing the back-EMF voltage source, E, stator reactance, X, variable load resistance, R, and the resulting output current, I, and voltage, V.



(a) I-V locus for surface PM machine

(b) Comparison of various machine I-V loci

Figure 2.4: Ideal I-V loci of (a) surface PM machine (SPM) and (b) surface PM, DC and interior PM, IPM, machines. Note that the SPM machine loci is shown for speeds, ω, of (a) 1 and 2pu, and (b) 1 pu; the IPM locus is shown for a saliency ratio, ξ, of 4, and has a 16% voltage over-shoot (peak voltage of 1.16pu).

2.1.2 Inductance Classification

Conventional surface PM synchronous machines generally have *low*-inductance stator windings as the permanent magnets mounted on the rotor surface behave as large air gaps in the machine's magnetic circuit [35]. The resulting characteristic current, I_{ch}, tends to be significantly higher than the machine's rated current, causing limitations on the machine's operation, due to the possibility of high currents. The characteristic current is expressed by Equation (2.2), where Ψ_m and L_s represent the RMS magnet flux linkage and stator inductance, respectively.

$$I_{ch} = \frac{\Psi_m}{L_s} \tag{2.2}$$

High stator currents increase copper losses and increase the temperature of the stator windings. Exposure of the rotor magnets to high temperatures for long periods may produce metallurgical changes that may impair the ability of the material to be magnetised, and may even render the magnet non-magnetic [89, 90]. The magnet's magnetisation will be reduced to zero if it reaches the *Curie* temperature. Despite this, the magnet may be re-magnetised providing no metallurgical changes have been made.

There is limited opportunity to reduce the magnet flux linkage in a conventional SPM machine, without degrading the machine's torque production capability [35]. Therefore, the I_{ch} can only be reduced by increasing the stator inductance, which is (conveniently) achieved by using fractional slot concentrated stator windings. The F&P test machine considered here is a *high*-inductance machine, which implies the I_{ch} is comparable to the machine rated current. One distinct advantage of any high-inductance machine is that the short-circuit or fault current magnitude is limited to roughly the machine's rated current.

A comparison of the operating regions of both high and the more conventional low inductance PM machines is shown in Figure 2.5. Conventional low-inductance PM generators operate at output currents which are small compared to the short-circuit current, I_{sc}, and output voltages that are close to the open-circuit voltage, V_{oc}. The output voltage is proportional to the machine speed and hence the generator acts like a variable voltage source. This output voltage variation complicates the design of a power converters, e.g. a voltage-source grid-connected inverter, as these require a constant input voltage. In contrast, a high-inductance PM generator has output voltages which are small compared to its V_{oc}, whilst the output current is close to the short-circuit current. The machine acts as a constant current source, whose magnitude is unaffected by operating, providing its output voltage is significantly less than its open-circuit voltage.

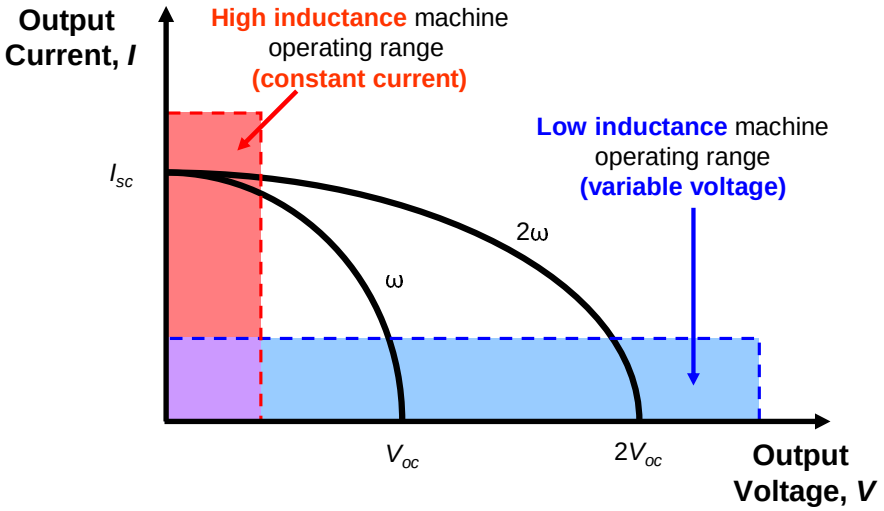


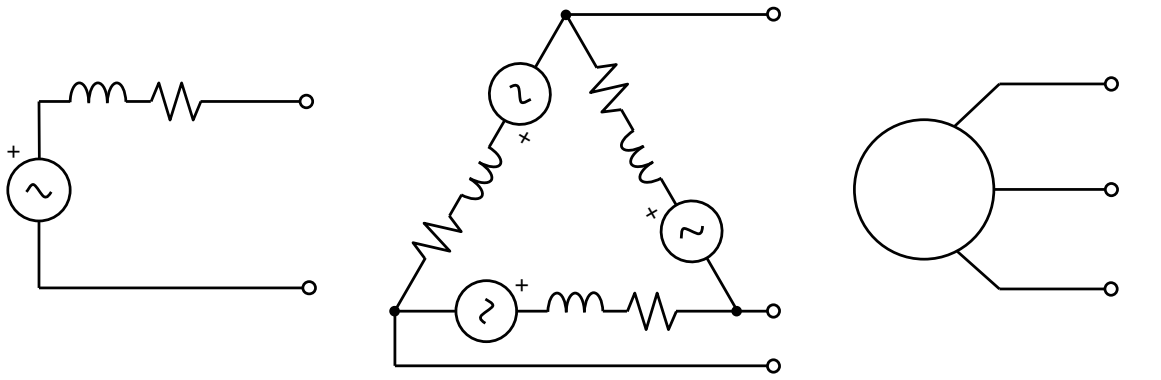
Figure 2.5: Operating regions of high and low-inductance PM machine,s operating at speeds ω and 2ω. The resulting open-circuit voltages occur at V_{oc} and $2V_{oc}$, whilst the short-circuit current for each case is equal to I_{sc}. The high-inductance machine operates near I_{sc} in the constant current region. Low-inductance machines operate close to V_{oc}, i.e. the variable voltage source region.

2.2 Machine Characterisation

The surface PM machine is modelled and simulated, using mathematical analysis and simulation software, prior to laboratory testing. However, the ideal PM machine model is replaced with one that is more realistic, which is later used to predict the machine performance. The detailed machine model, characterisation tests and parameters are discussed below.

2.2.1 Realistic Machine Model and Effect on Loci

The ideal surface PM machine model was discussed in Section 2.1.1. Stator resistance is now added to the ideal phase model, which allows copper losses to be modelled. The realistic phase model of the surface PM machine is shown in Figure 2.6(a). The delta connected machine equivalent circuit is shown in Figure 2.6(b), and a simplified model is shown in Figure 2.6(c).

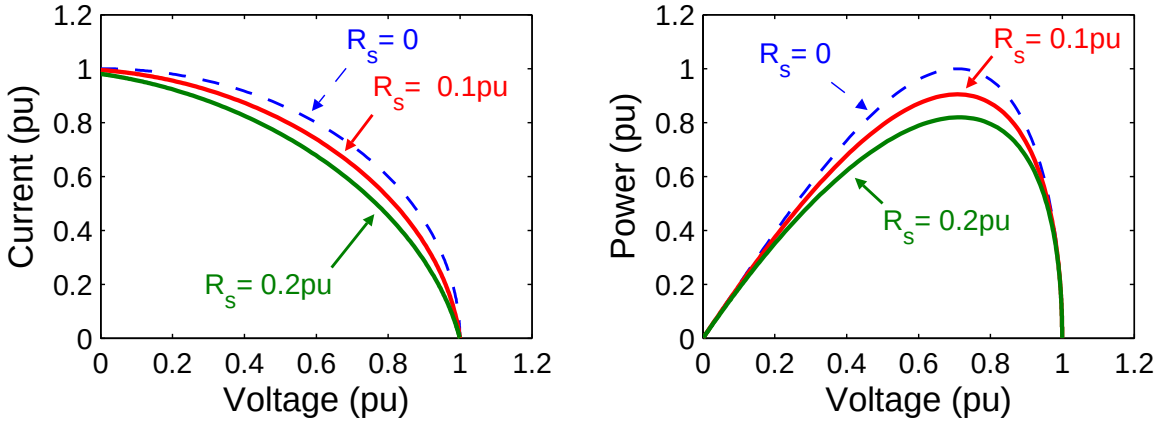


(a) Phase model (b) Delta connected circuit (c) Generator representation

Figure 2.6: Realistic surface PM machine model, showing (a) phase model, (b) delta connected equivalent circuit, and (c) symbolic representation . Note that the machine star point does not exist for a delta connected machine.

The effect of the stator resistance on the I-V locus and the resulting power vs. voltage (P-V) locus is illustrated in Figure 2.7, for stator resistances of 0.1 and 0.2pu. Note that the ideal curves (R_s = 0pu) are shown in the figure for reference, and that these are indicated by the dashed lines. The figure indicates that the introduction of R_s does not affect the open-circuit voltage, however, it does affect the machine output current. The short-circuit current is slightly reduced, whilst the machine current and hence power, between the short-circuit and open-circuit operating points, is significantly reduced. This

is highlighted in Figure 2.7(b), which shows that a stator resistance of 0.2pu reduces the peak machine output power by 18%, compared to the ideal model ($R_s = 0$). Note that this difference is largely due to the copper loss, P_{CU}, which is proportional to the square of the RMS current, I, and stator resistance, as summarised in Equation (2.3).



(a) I-V locus

(b) P-V locus

Figure 2.7: Effect of introducing the stator resistance to the ideal model, showing the (a) current vs. voltage (I-V) and (b) the resulting power vs. voltage (P-V) loci, for stator resistances, R_s, of 0.1 and 0.2 pu. The dashed line represents the loci of the ideal model ($R_s = 0$), and is shown for reference.

$$P_{CU} = I^2 R_s \tag{2.3}$$

The required machine parameters, such as k, L_s and R_s, are determined by a series of characterisation tests. The stator resistance is determined by applying a DC current (whilst the machine is stationary) to the stator windings and measuring the resulting voltage drop. In contrast, the back-EMF constant and stator inductance are found by rotating the machine at various speeds; k is found from the *open-circuit test*, whilst L_s is determined from the *short-circuit test*.

2.2.2 Test Arrangement

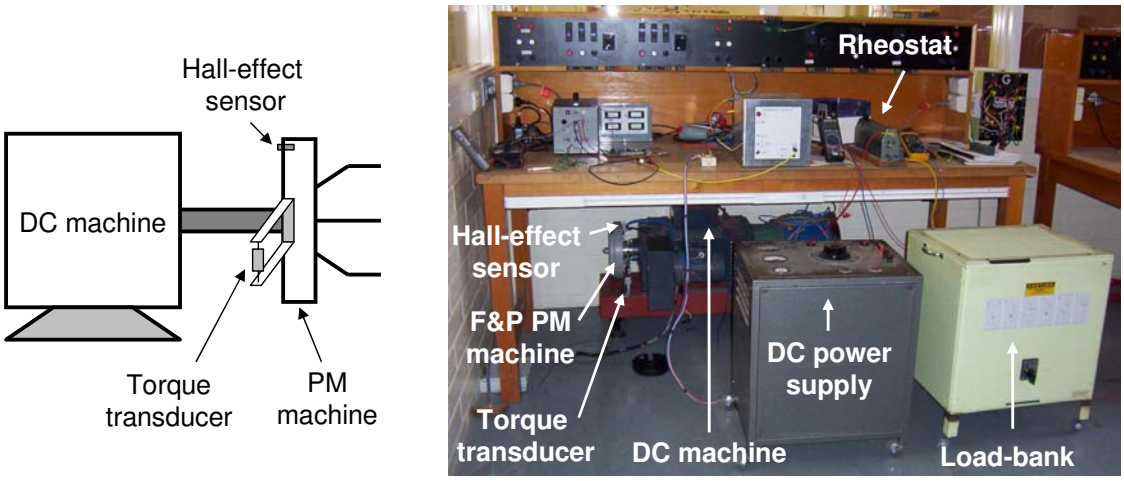
The surface PM machine is characterised over a wide range of speeds in the laboratory using a directly-coupled, separately-excited 5kW DC machine. The DC machine speed is controlled by adjusting the armature voltage, which is supplied by the rectified output of a

3-phase Variac; it is fine-tuned using a rheostat (variable resistor) that is series connected to the separately-excited field winding. The machine speed is measured using a simple Hall-effect sensor that fits in the PM machine air gap. The sensor delivers a 50% duty-cycle square wave voltage to a frequency meter. The machine speed, n, is calculated as shown in Equation (2.4), where P is the number of machine pole-pairs, and f represents the electrical frequency (Hz). Note that the machine speed is calibrated using an optical tachometer.

$$n = \frac{60\,f}{p} \tag{2.4}$$

In addition to the Hall-effect device, the stator of the PM machine is fitted with a reaction torque transducer. This force measurement sensor allows the shaft torque and hence PM machine mechanical input power, P_{in}, to be accurately measured. The input power is the product of the shaft torque, T, and the machine speed, ω, in rad/s, as shown in Equation (2.5). The machine test arrangement and the general block diagram is shown in Figure 2.8.

$$P_{in} = T\omega \tag{2.5}$$



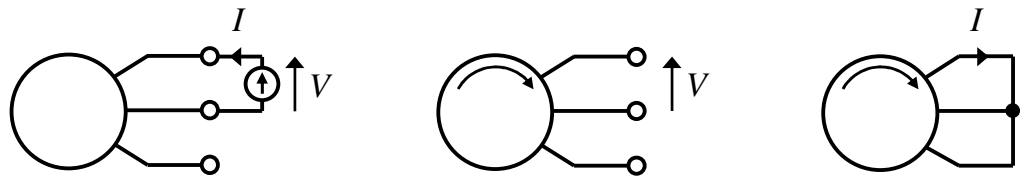
(a) Block diagram

(b) Photograph

Figure 2.8: Laboratory machine test arrangement, showing (a) block diagram, and (b) photograph. The directly coupled DC and PM machines, torque transducer and frequency (speed) sensor are shown in each figure, whilst the photograph also shows the DC power supply (rectified 3-phase variac), rheostat and a load-bank.

Load Arrangement

The machine is characterised by three tests, these are the DC resistance, open-circuit (OC) and short-circuit (SC) tests. The machine is loaded in various ways during these tests, as summarised by Figure 2.9. Note that the machine is stationary during the resistance test to prevent induced voltages affecting the readings, whilst it is rotated at various speeds during the OC and SC tests. In addition, each line voltage was measured for the resistance and OC tests, whilst each line current was measured for the SC test.



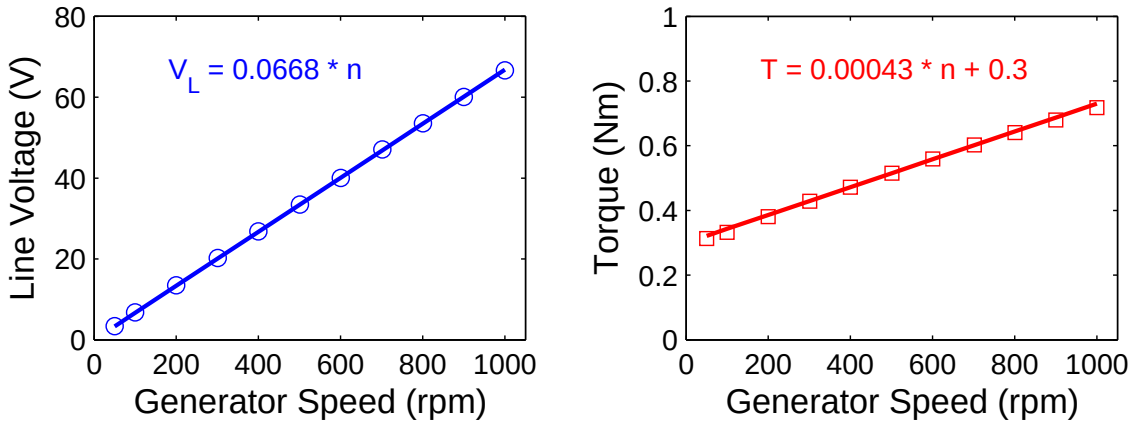
(a) Resistance measurement (b) OC (c) SC

Figure 2.9: PM machine characterisation arrangements, showing the (a) resistance measurement, (b) open-circuit (OC), and (c) short-circuit (SC) arrangements. The measured voltage and currents are represented by V and I, respectively. Note that the machine rotates for the OC and SC tests, and that all line voltages are measured during the resistance and OC tests, whilst all line currents are measured during the SC test.

2.2.3 Open-Circuit Test

The generator back-EMF constant is determined from the open-circuit test. The PM generator is driven over a wide range of speeds (50–1000 rpm), whilst the line voltages and input loss torque are measured. This test arrangement is seen in Figure 2.9(b), whilst the measured results are displayed in Figure 2.10. As can be seen from the figure, both the induced voltage (also see Equation (2.6)) and the input torque vary linearly with speed. The difference, however, is that the induced voltage intercepts the origin, unlike the torque plot. The input torque is vertically offset by 0.3Nm at zero speed, which represents the generator starting torque which includes the hysteresis and peak cogging torques, and the torque required to overcome the bearing and seal friction [86]. The measured OC test torque is further discussed in Section 2.2.5.

$$E = k\,\omega \tag{2.6}$$



(a) Open-circuit voltage

(b) No-load torque

Figure 2.10: Open-circuit characteristic, showing measured (a) line voltage, and (b) generator torque vs. generator speed. Note that the lines represent curve-fitted lines; the back-EMF constant, k, and torque curve equation is included.

An example of the measured generator open-circuit line voltages is shown in Figure 2.11, for a generator speed of 1000 rpm. The high-quality sinusoidal voltage waveforms shown each contain a small amount of total harmonic distortion (less than 0.5%). The distortion is attributable to the machine design and is hence independent of the generator speed. The term *total harmonic distortion* is defined and further discussed in Section 5.2.

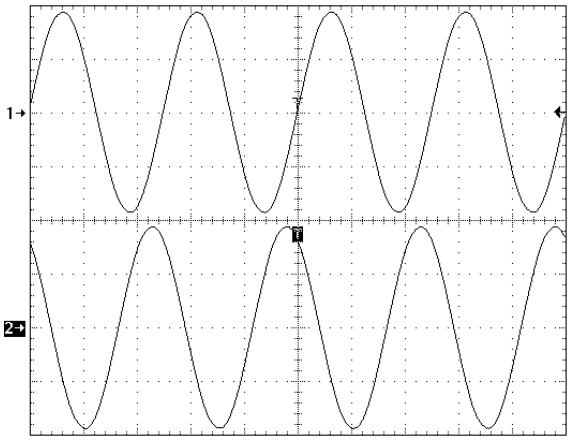
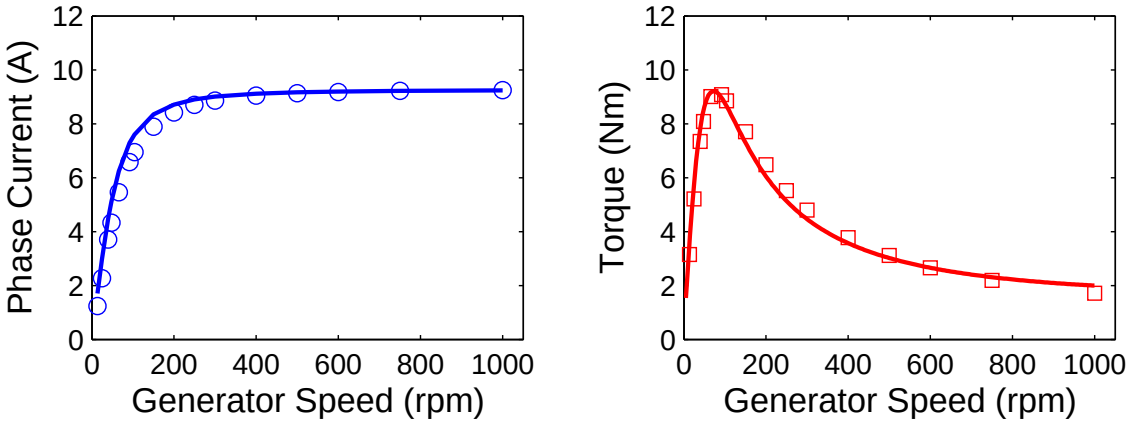


Figure 2.11: Measured generator open-circuit line voltage at 1000 rpm, showing (top) V_{AB}, and (bottom) V_{BC}. The zero position for each waveform is shown by the arrow on the left; the vertical and horizontal scales are 50V and 1ms per division, respectively.

2.2.4 Short-Circuit Test

The short-circuit (SC) test is performed to calculate the stator inductance. The stator terminals are shorted together and the current is measured whilst the machine is operated up to 1000 rpm (see Figure 2.9(c)). The phase current and generator torque is plotted in Figure 2.12, as a function of generator speed. The current is shown to rapidly increase at low generator speeds, and approach a limit of about 9.26A; this corresponds to the machine's characteristic current (see Equation (2.2)). In contrast, the measured SC machine torque is shown to rapidly increase at low speeds, reaching its peak of approximately 9.1 Nm at 92 rpm. The torque then decreases with increasing machine speed.



(a) Phase current

(b) Machine torque

Figure 2.12: Short-circuit characteristic, showing predicted and measured (a) phase current, and (b) generator torque vs. generator speed. The measured and predicted data are represented by points and solid lines, respectively.

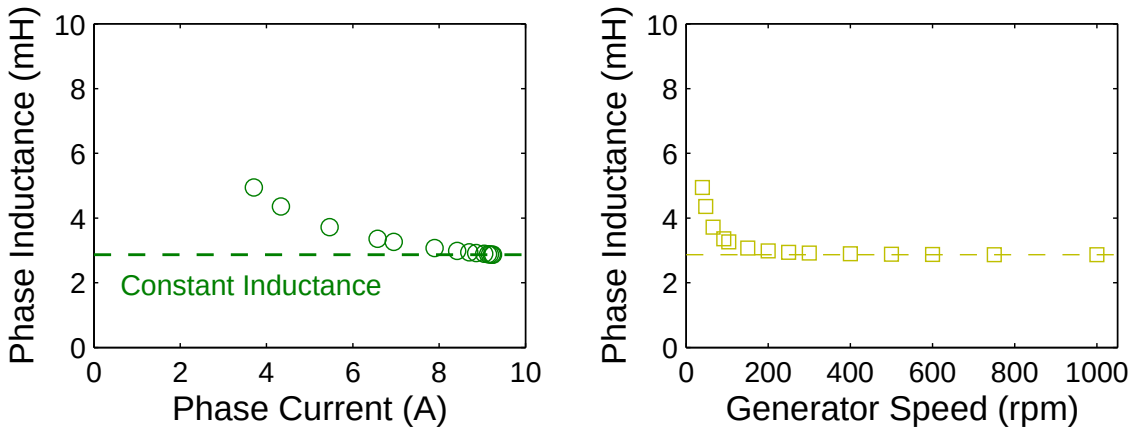
Note that the fundamental difference between the characteristic and short-circuit current is the inclusion of stator resistance in the calculation of the latter. The ratio of the SC to characteristic current is 0.997:1, at 1000 rpm.

The machine phase reactance, X_{ph}, and inductance, L_{ph}, are calculated from the measured SC current, the calculated induced phase voltage, E_{ph}, and the measured stator (phase) resistance, R_{ph}. These parameters are given by Equations (2.7) and (2.8), respectively, where ω_e is the electrical frequency and is equal to $2\pi f$.

$$X_{ph} = \sqrt{\left(\frac{E_{ph}}{I_{ph}}\right)^2 - {R_{ph}}^2} \tag{2.7}$$

$$L_{ph} = \frac{X_{ph}}{\omega_e} \tag{2.8}$$

The calculated phase inductance is shown in Figure 2.13 as a function of phase current and generator speed. Figure 2.13(a) shows that the phase inductance decreases at low currents and approaches a value of 2.87mH at high currents, whilst Figure 2.13(b) shows a relatively constant phase inductance over the range of 200–1000 rpm. Given that this is a surface PM machine the inductance is expected to be relatively constant. In addition, the bulk of experimental work presented in this thesis concentrates on a generator speed range of 200–1000 rpm, thus a constant inductance corresponding to the value at high currents was used in the model. This was also used to calculate the simulated curves of short-circuit current and input torque shown in Figure 2.12, and is shown as the dashed line in Figure 2.13.



(a) Phase current (b) Generator speed

Figure 2.13: Measured phase inductance vs. (a) phase current, and (b) generator speed characteristic, from the short-circuit test. The dashed line represents the constant inductance used in the modelling.

Note that it is likely that errors in the measurements and models used cause the large inductance variation at low currents. Although this work focusses on the 200–1000 rpm speed range, it is recommended that a phase inductance test is performed at stand still, in the future, to further verify the relatively constant phase inductance.

Stator Temperature

The high currents under SC or loaded operation produce high copper losses in the stator, which are dissipated as heat throughout the copper windings, causing the stator temperature to increase. In addition to possibly damaging or demagnetising the permanent magnets, high temperatures can damage the copper insulation causing short circuits in the stator windings. Safe operation of the test machine at high currents is tested by measuring the stator temperature during the SC test, using thermocouple that is directly connected to a stator winding. The measured temperature rise of the stator is shown in Figure 2.14 for a generator speed of 1000 rpm, along with a fitted curve, whose time constant is 10 minutes.

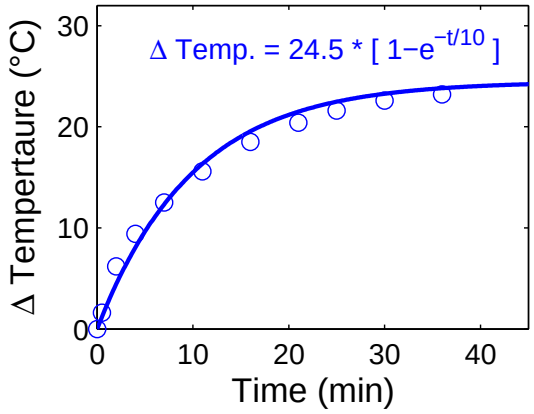


Figure 2.14: Stator temperature increase, Δ, vs. time under short-circuit conditions for a generator speed of 1000 rpm. The points represents experimentally measured data, whilst the solid line and equation corresponds to a fitted curve.

The maximum temperature rise is shown to be about 25°C, which implies that the machine is able to withstand high currents without compromising the stator insulation or permanent magnet integrity. It also indicates that the stator resistance will increase by about 10.7%, as summarised by Equation (2.9), where R_{cold}, R_{hot}, ΔT and α_{cu}, represent the initial (*cold*) resistance, the *hot* resistance, the difference between hot and cold stator temperatures, and the temperature coefficient of copper, respectively. Note that α_{cu} is equal to $4.27 * 10^{-3}$/°C at 0°C [91].

$$R_{hot} = R_{cold}\,(1 + \alpha_{cu}\,\Delta T) \tag{2.9}$$

2.2.5 Machine Losses

The torque measurements from the open and short-circuit tests allow the machine losses to be calculated. The input power from the OC test gives the machine iron, friction and windage (IFW) losses. The OC input torque curve of Figure 2.10(b) is linearly proportional to the generator speed, and hence the expected IFW (power) losses will be proportional to the square of the machine speed (recall Equation (2.5)). The calculated OC IFW loss is shown in Figure 2.15, as the dashed line.

The figure also shows the total, copper and IFW losses, under SC conditions. The total loss is equal to the machine input power which is calculated from the measured input torque (see Equation (2.5)). The total loss is shown to increase rapidly at low generator speeds and continues to increase monotonically at high speeds, due to the shape of the SC torque characteristic. The copper loss is calculated knowing the stator resistance and the measured current. This loss is expected to increase sharply at low generator speeds, due to the sharp current increase (see Figure 2.12(a)). The copper loss is also expected to approach a fixed value at high generator speeds, as the SC current approaches the characteristic current. Note that the stator resistance is assumed constant, although in

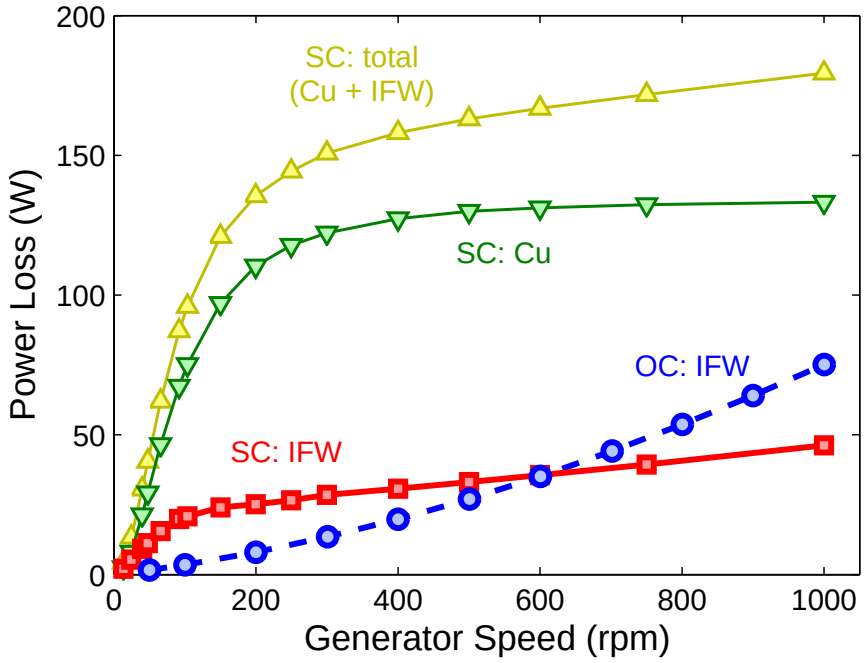


Figure 2.15: Calculated generator open and short-circuit losses vs. generator speed. The losses shown include: open-circuit (OC) iron, friction and windage (IFW), the short-circuit (SC) IFW, copper, Cu, and total (Cu+IFW) losses.

practise it will increase due to the stator temperature rise and perhaps skin effect at higher frequencies (see Section 2.4.1).

The SC IFW loss is calculated as the difference between the total loss and the copper loss (total - Cu). This loss is also plotted in Figure 2.15, and is shown to increase sharply at low generator speeds, up to about 150rpm. The SC IFW loss then continues to slowly increase linearly with speed. This is unlike the OC IFW power loss curve which increases with the square of generator speed. Hence, the SC IFW loss will be greater than the corresponding OC loss, at low generator speeds, whilst it will be less than the OC IFW loss at high generator speeds. This is seen in the figure, which shows that the SC and OC IFW losses are equal at about 600 rpm.

2.2.6 Machine Properties

A summary of the test PM machine properties is shown in Table 2.1. These include the physical properties, the calculated parameters and a summary of the extreme (maximum) measured conditions.

Table 2.1: Physical, measured and calculated PM generator properties.

	Parameter	Value
Physical	Stator Connection	Delta
	Phases	3
	Magnetic Poles	48
	Stator Teeth	36
	Slots per phase per pole	0.25
Measured (maxima)	Test Speed	1000 rpm
	SC Phase Current	9.24 A
	Ratio of I_{SC} : I_{ch}	0.997 : 1
	Torque	9.08 Nm
	Δ Stator Temperature	23°C
Measured Parameters	Back-EMF Constant, k_{ph}	0.0668 V/rpm
	Phase Inductance, L_{ph}	2.87 mH
	Phase Resistance, R_{ph}	0.519 Ω

Note: the ratio of short-circuit to characteristic current is shown for a generator speed of 1000 rpm.

2.3 Machine Modelling

The test PM generator is simulated over a wide range of speeds and AC and DC load conditions prior to experimental testing to gain an understanding of its power generation capabilities. Two models are used to predict the machine's generating performance, these are the analytical and PSIM® based models. The accuracy of the models are examined in Section 2.4, which compares the models to the experimentally measured data.

2.3.1 Analytical Model

The test machine is modelled as a synchronous generator with a load resistance, R_L. The single-phase machine model is shown in Figure 2.16. The machine phase parameters, k_{ph}, X_{ph} and R_{ph}, are obtained from Table 2.1.

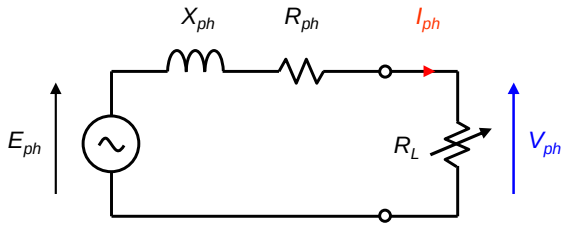


Figure 2.16: PM generator phase model.

The resulting phase current, I_{ph}, and voltage, V_{ph}, is calculated using Equations (2.10) and (2.11), respectively. These are converted to line quantities which are used to plot the machine I-V locus. Note that for the delta connected machine the phase and line voltages are equal in magnitude ($|V_L| = |V_{ph}|$), whilst the line current, I_L, is given by Equation (2.12). The machine power, P, is calculated from Equation (2.13), where $\cos(\phi)$ represents the power factor. Note that unity power factor is assumed here, as the load is assumed purely resistive. In practise, however, a small amount of inductance exists, which slightly reduces the power factor.

$$I_{ph} = \frac{E_{ph}}{|\,(R_{ph} + R_L) + j\,X_{ph}|} \tag{2.10}$$

$$V_{ph} = I_{ph}\,R_L \tag{2.11}$$

$$I_L = \sqrt{3}\,I_{ph} \tag{2.12}$$

$$P = \sqrt{3}\, V_L\, I_L\, \cos(\phi) \tag{2.13}$$

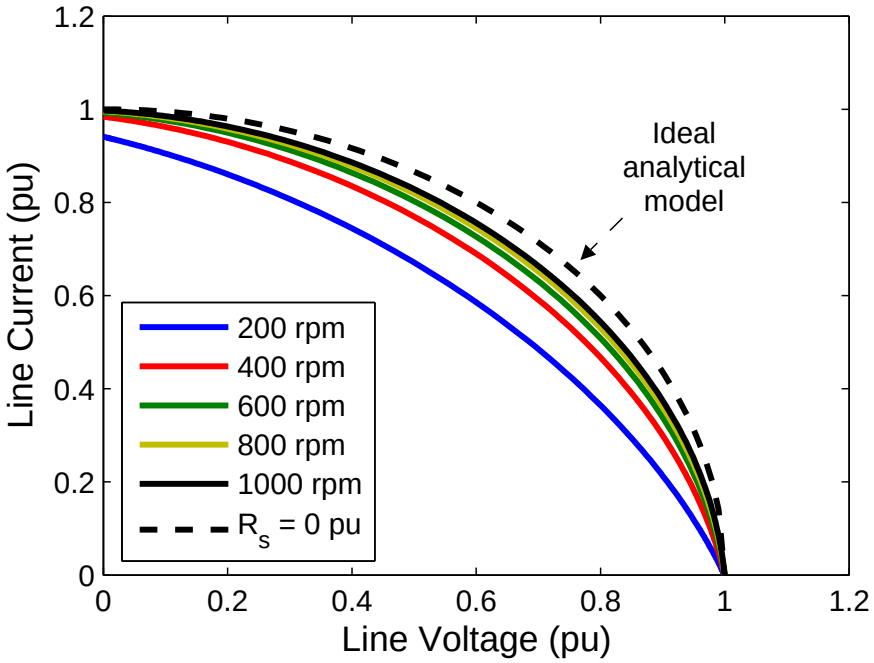
Normalised AC Voltage Loci

The normalised output I-V and P-V loci are shown in Figure 2.17, for generator speeds of 200–1000 rpm. At each speed the voltage, current and power is normalised to the open-circuit voltage, the characteristic current and the maximum power possible at that speed (with zero stator resistance), respectively. The solid lines represent the predicted machine performance, based on the measured parameters including stator resistance, whilst the dashed line represents the predicted ideal case, i.e. zero stator resistance. It is shown that despite the stator resistance, the machine current and hence power approaches the ideal case as the generator speed increases. This occurs as the stator reactance increases with frequency (machine speed), and becomes the dominating impedance, i.e. the ratio of stator resistance to reactance approaches zero. The resulting current approaches its characteristic value (1pu), as previously shown in Figure 2.7. Note that the following assumptions are made regarding the phase model and the subsequent normalised voltage loci:

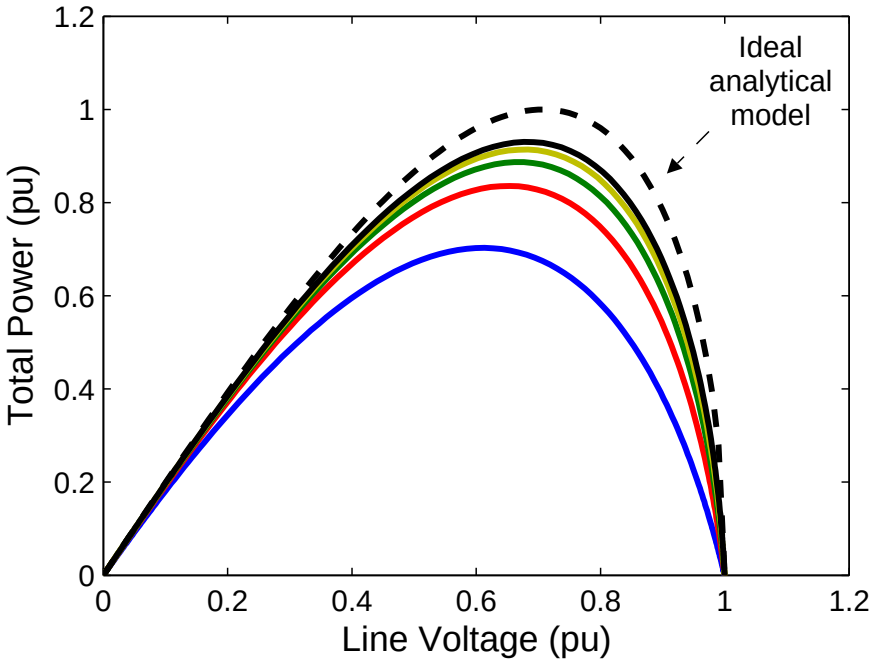
- the induced voltages are sinusoidal,
- the stator resistance is fixed, and equal to its DC measured value, and
- the load is purely resistive for all cases.

DC Quantities

The above equations allow the AC I-V and P-V loci to be plotted. However, the equivalent DC voltage loci are also required, as the proposed power converters will use an uncontrolled full-wave three-phase rectifier. These DC loci can be obtained by converting the AC line voltages and currents to equivalent DC quantities. The equivalent DC bus voltage, V_{DC}, corresponding to an AC line voltage, V_L, is expressed in Equation (2.14), which assumes the peak phase voltage is equal to $2/\pi\, V_{DC}$ [56]. The equivalent DC bus current, I_{DC}, corresponding to an AC line current, I_L, is shown in Equation (2.15). The equation is deduced from the three-phase power and DC voltage equations, and assumes a loss-less rectifier (i.e. the AC and DC powers are equal).



(a) I-V locus



(b) P-V locus

Figure 2.17: Normalised PM machine line voltage AC loci, showing (a) current, and (b) power loci, for generator speeds of 200–1000 rpm. The solid lines represent the various machine speed loci, whilst the dashed line corresponds to the ideal I-V locus (zero stator resistance).

$$V_{DC} = \frac{\pi}{\sqrt{6}} V_L = 1.283\, V_L \tag{2.14}$$

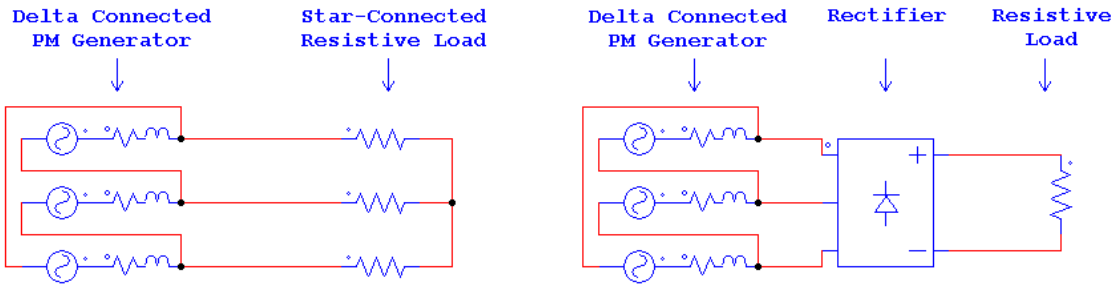
$$I_{DC} = \frac{3\sqrt{2}}{\pi} I_L = 1.35\, I_L \tag{2.15}$$

The resulting DC voltage loci differ from the AC voltage loci, due to the above equations linking the AC and DC quantities. Despite this, the normalised AC and DC voltage loci are identical. Note that the conversion of AC to DC quantities makes the following assumptions, and as such may not be accurate.

- the ratio of DC to AC quantities remain fixed for all conditions, and
- the rectifier voltage drop and resulting power loss is ignored.

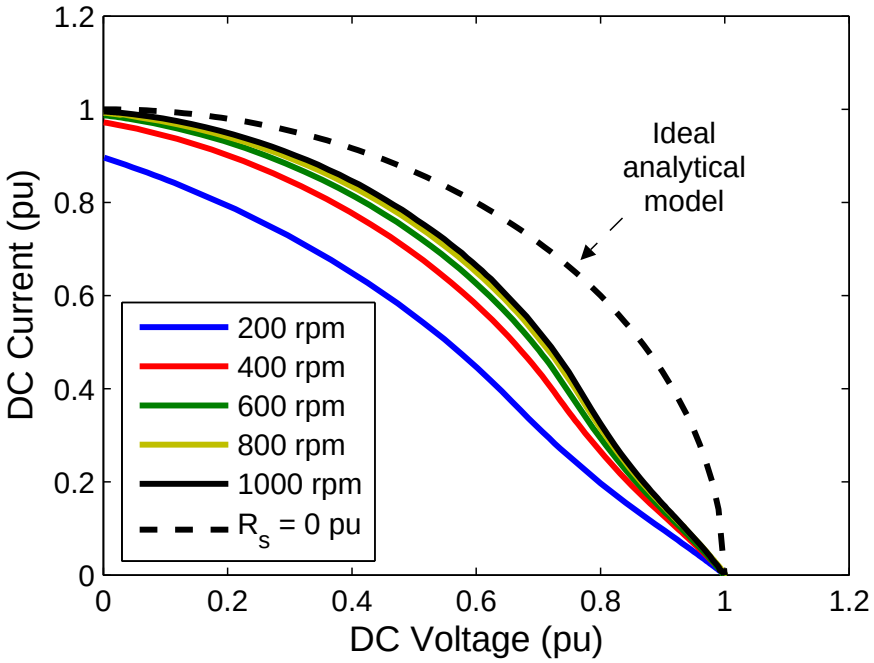
2.3.2 PSIM® Model

A computer based model is used to provide insight in to the rectifier modelling and to verify the analytical AC predictions. PSIM® is used as it is designed to simulate power electronics and motor control circuits. Compared to other simulations tools such as SPICE, PSIM® simulates faster and avoids convergence problems, as the nodes are analysed using the trapezoidal rule integration algorithm [92]. Figure 2.18 shows the delta connected PM generator with both the three-phase AC and DC (rectifier) resistive loads. The rectifier diodes were modelled with a voltage drop of 1V. The resulting calculated normalised DC I-V and P-V loci are shown in Figure 2.19.

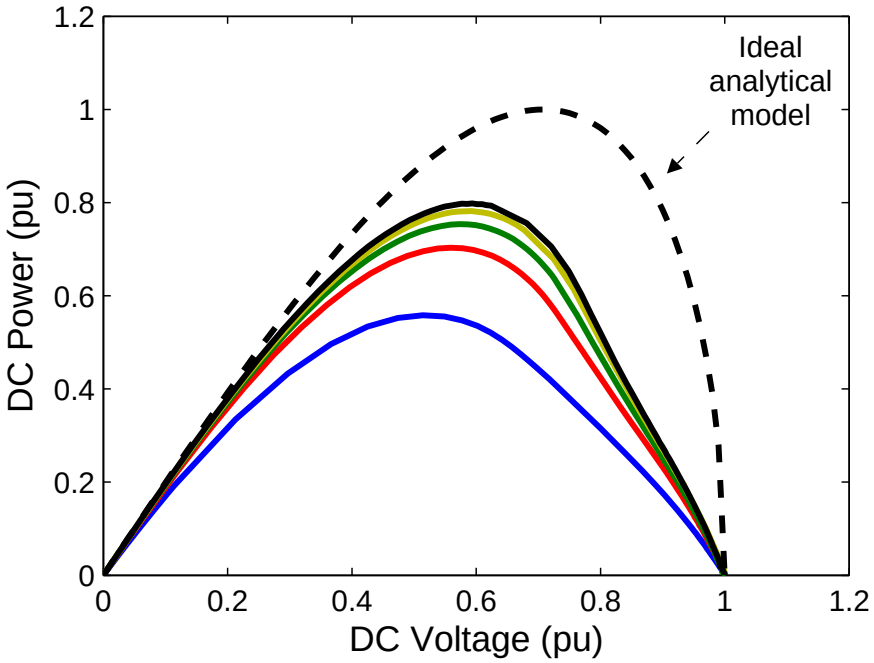


(a) AC resistive load (b) DC resistive load

Figure 2.18: PSIM® delta-connected PM machine model showing (a) AC, and (b) DC resistive loads. Note that the three-phase load is star connected.



(a) I-V locus



(b) P-V locus

Figure 2.19: Normalised PM machine DC output voltage loci, showing (a) current, and (b) power loci, for generator speeds of 200–1000 rpm. The dashed line represents the ideal analytical (zero stator resistance) model, whilst the solid lines correspond to the various machine speed loci.

The normalised DC loci are shown for generator speeds of 200–1000 rpm, as solid lines, whilst the dashed line corresponds to the ideal analytical case. At each speed the DC output voltage is normalised to the equivalent DC voltage obtained (using Equation (2.14)) with the open-circuit AC voltage. The DC output current is normalised (using Equation (2.15)) with the characteristic current, whilst the power is normalised to the maximum AC power possible at that speed with zero stator resistance.

The current and resulting power are again shown to increase with generator speed, as the ratio of stator resistance to reactance decreases. Despite this, the loci do not appear to approach the ideal analytical curves as much as the AC case, which indicates that the analytical DC model has limited accuracy. This is most likely due to the incorrect assumptions made regarding the rectifier voltage drop, power losses, and AC to DC conversion ratios. The latter is briefly investigated in Section 2.4.2.

In contrast, the AC voltage loci with a three-phase resistive load predicted by PSIM® are identical to those predicted using the analytical phase model (see Figure 2.17).

2.3.3 Power Maximisation

The maximum normalised power is shown in Figure 2.20, as a function of generator speed. This data is obtained from the AC and DC normalised P-V loci. The figure compares the AC power predicted by both models, to the DC power predicted by PSIM®. Note that the power is normalised relative to that obtained from an ideal (zero stator resistance) PM generator with a three-phase resistive load. This is represented by the dashed line in

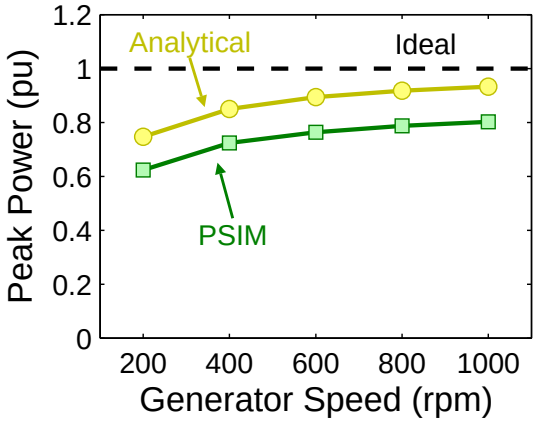
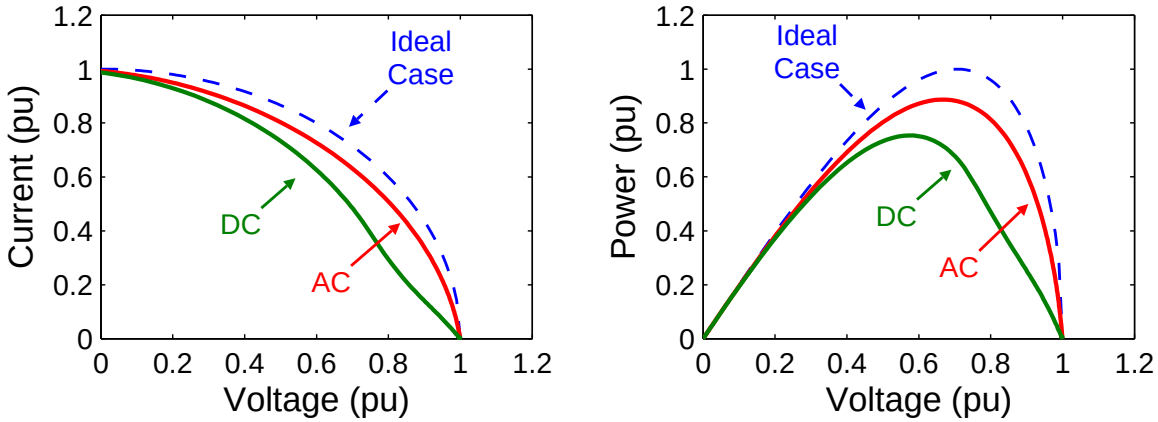


Figure 2.20: Model comparison showing the peak normalised DC output power vs. generator speed prediction, based on the analytical and PSIM® models. The dashed line represents the peak power obtained using the ideal analytical model.

the figure. Although both models predict the same AC loci, PSIM® consistently predicts about 0.1pu less power than the analytical model for the DC loci. This verifies that power is lost in the rectifier. This conduction loss is caused by the diode voltage drop, and is proportional to the rectifier output current.

2.3.4 Model Comparison

The normalised AC and DC voltage loci predicted by PSIM®, for a generator speed of 600rpm, are compared in Figure 2.21. The ideal analytical case, corresponding to zero stator resistance and a loss-less rectifier (for the DC case), is also shown for reference. The effect of stator resistance is clearly seen, as is the reduced current and hence power for the DC case. This is not caused by stator resistance, and is likely to be caused by the assumptions used to predict the DC quantities (i.e. fixed AC to DC voltage and current ratios and the use of a loss-less rectifier), which have only limited validity. Both the analytical and PSIM® predictions should be compared with experimentally measured data, to validate their respective models.



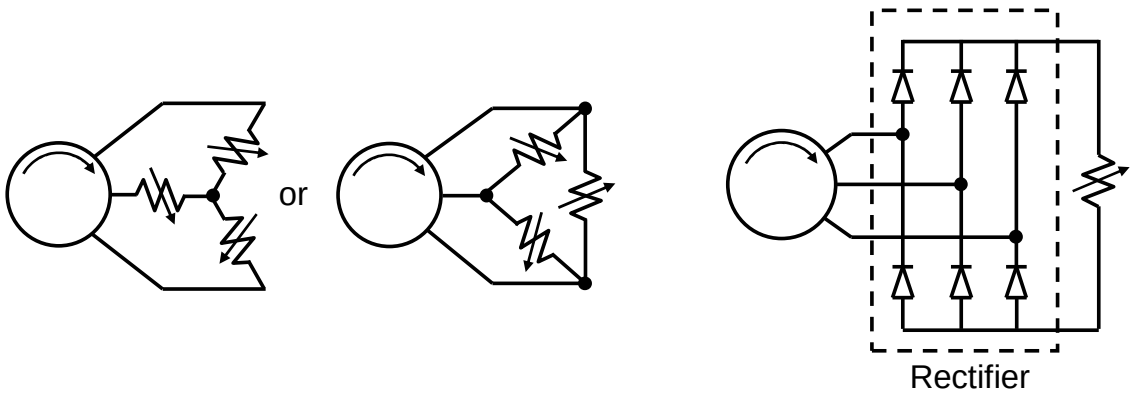
(a) I-V loci

(b) P-V loci

Figure 2.21: Comparison of ideal analytical and PSIM® models, showing (a) I-V, and (b) P-V loci, for both AC and DC cases for a generator speed of 600rpm. The ideal analytical predictions assume zero stator resistance and loss-less rectifier (for the DC case), and are represented by the dashed line.

2.4 Resistive Load Testing

The PM generator is loaded using a variable resistance, to verify the analytical and PSIM® models. It is first loaded by a three-phase (AC) variable resistive load, and secondly by a rectifier (DC) variable resistive load. The DC loading is achieved using an uncontrolled full-bridge three-phase rectifier, and along with the AC loading is shown in Figure 2.22. Note that the AC resistive load was connected in both the star and delta configurations to achieve a wider range of load resistances, as the delta connection effectively reduces the resistance to one third that of the equivalent star case.

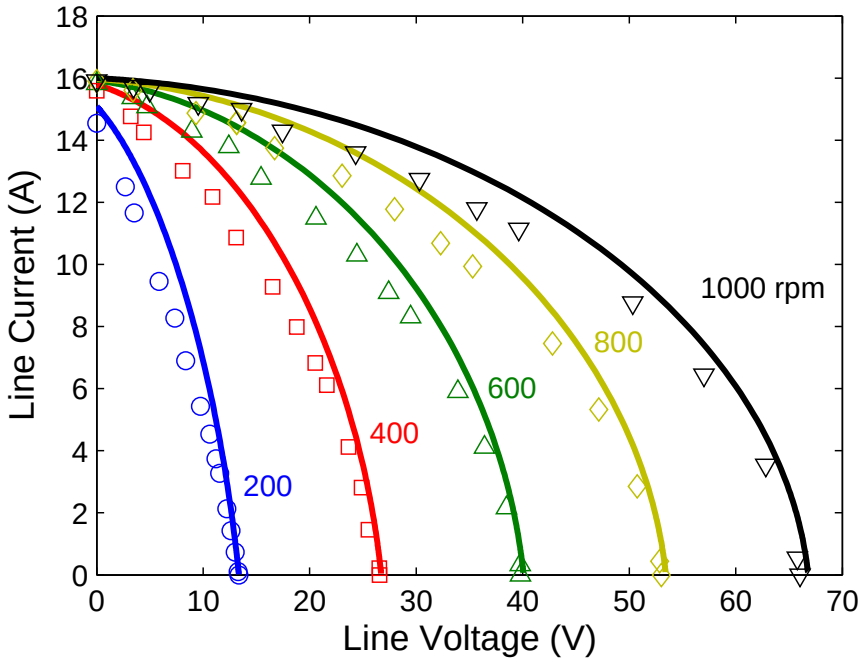


(a) AC resistive load (b) DC resistive load

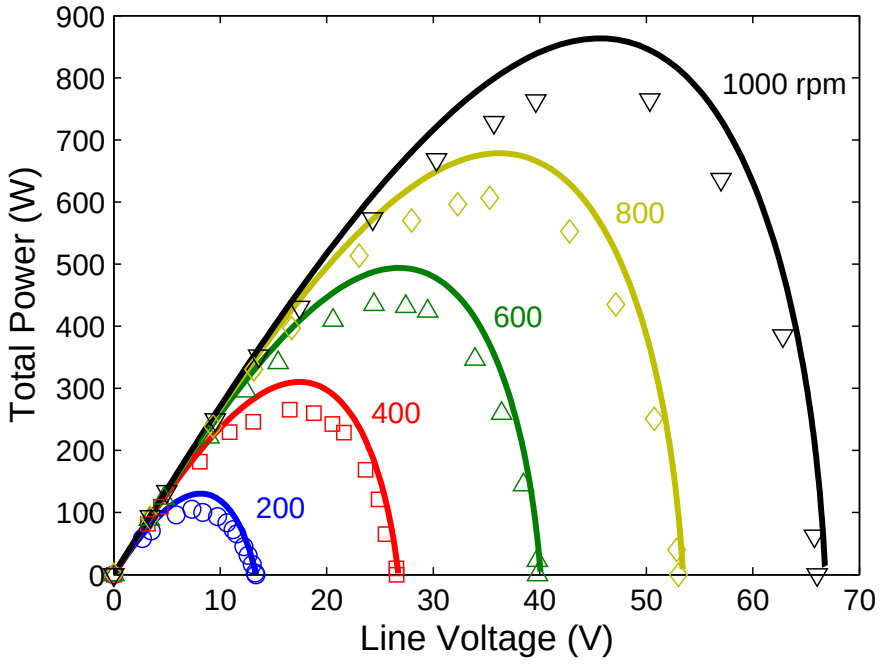
Figure 2.22: PM machine load arrangements, showing the (a) three-phase AC, and (b) DC resistive load arrangements. Note that the AC resistive load is shown for both star and delta connections, and that the dashed box represents the uncontrolled rectifier, as used for the DC resistive load case.

2.4.1 3ph Resistive Loading

The test machine is rotated at speeds of 200, 400, 600, 800 and 1000 rpm, whilst the load resistance is varied from very low to high resistances, i.e. 0.075 to 350Ω, respectively. The DC machine speed is kept constant via the field rheostat, as the varying load changes the PM generator output power and hence torque. The resulting measured current vs. voltage (I-V) and power vs. voltage (P-V) loci are shown in Figure 2.23 for the generator speeds mentioned above. The figure includes both the analytical and PSIM® model simulations, and the measured experimental data. Note that the currents and voltages are expressed as line quantities, whilst the power shown corresponds to total (three-phase) power.



(a) I-V locus



(b) P-V locus

Figure 2.23: PM machine line voltage AC loci, showing (a) current, and (b) power loci, for generator speeds of 200–1000 rpm. The points represent measured data, whilst the lines represent the analytical model and (matching) PSIM® simulations.

Increasing Stator Resistance

The generator I-V locus indicates that the simulations and experimentally measured data closely match, however, small discrepancies exist. These and are more clearly seen on the P-V locus, and are shown to increase with generator speed (frequency). This may be associated with an increase in stator resistance caused by the increase of stator temperature, and the *skin* and *proximity* effects. The rise in stator temperature accounts for a maximum stator resistance increase of 10% (see Section 2.2.4).

The skin effect causes current to flow on the outside of the conductors, which effectively reduces the conducting cross-sectional area (skin depth) and hence increases the resistance. The skin depth, δ, is defined as the depth below the surface of the conductor at which the current density decays to $1/e$ (about 0.368) of the current density at the surface [67, 93]; it is inversely proportional to square-root of the electrical frequency, f, the permeability, μ, and conductivity, σ, of the conductor, as summarised by Equation (2.16).

$$\delta = \frac{1}{\sqrt{\pi\, f\, \mu\, \sigma}} \tag{2.16}$$

The proximity effect is related to the current distribution in the conductor to changing due to magnetic fields, and can be reduced by positioning the coil away from the slot opening [94]. The use of *Litz* wire, thin insulated strands bundled together, reduces both the skin and proximity effects. Despite this, Litz wire may not be a desirable solution due to its high cost, relatively poor thermal conductivity and low packing factor [94].

Generator Efficiency

The generator efficiency, η, is calculated as output power divided by input power, as summarised and simplified in Equation (2.17). The mechanical input power is obtained using the torque transducer and generator speed, whilst the electrical output power is measured using a power analyser. Note that the three-phase resistive loads contain only a negligible amount of inductance. This is verified by the power analyser which repeatedly measured a load power factor of 0.999 lag.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\sqrt{3}\, V_L\, I_L\, \cos(\phi)}{T\, \omega} \tag{2.17}$$

The measured generator efficiency is plotted as a function of total (3-phase) output power, in Figure 2.24, for generator speeds of 200–1,000rpm. The peak generator efficiency increases from about 83%, at 200rpm, to approximately 87% at 1,000rpm. The P-V locus (Figure 2.23) shows that the same output powers can be obtained, for a fixed generator speed, with two values of load resistance. The same output power can be obtained with a low resistance producing a high current and low voltage, as with a high resistance producing a high voltage and low current. This implies that for each speed, the generator will have two efficiency vs. power curves which meet at the peak power. This is shown in the figure below, and is more clearly seen for the high speed cases. The lower efficiency curve corresponds to operation with higher currents and hence copper losses, which is associated with operation in the constant current region of the generator I-V locus.

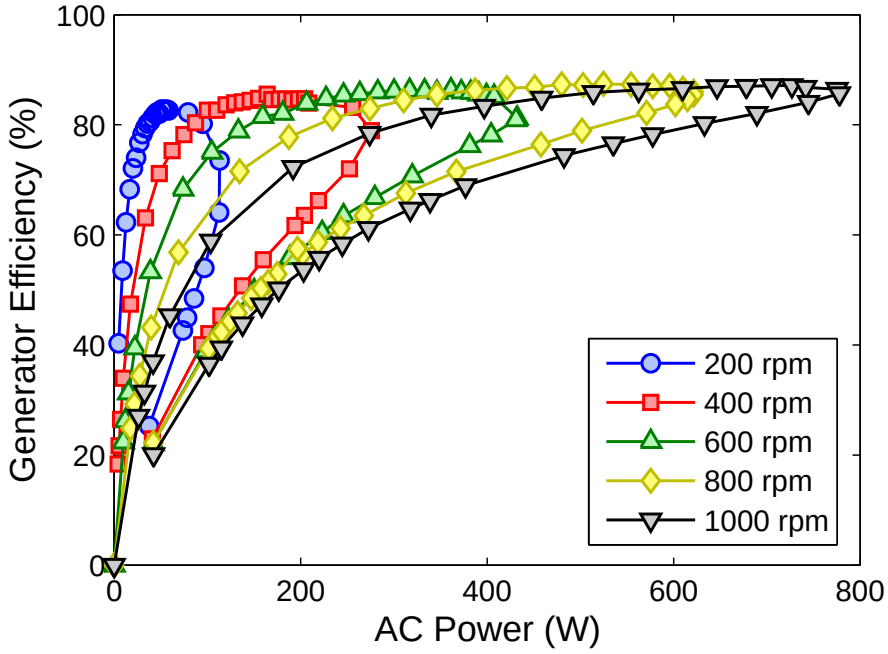
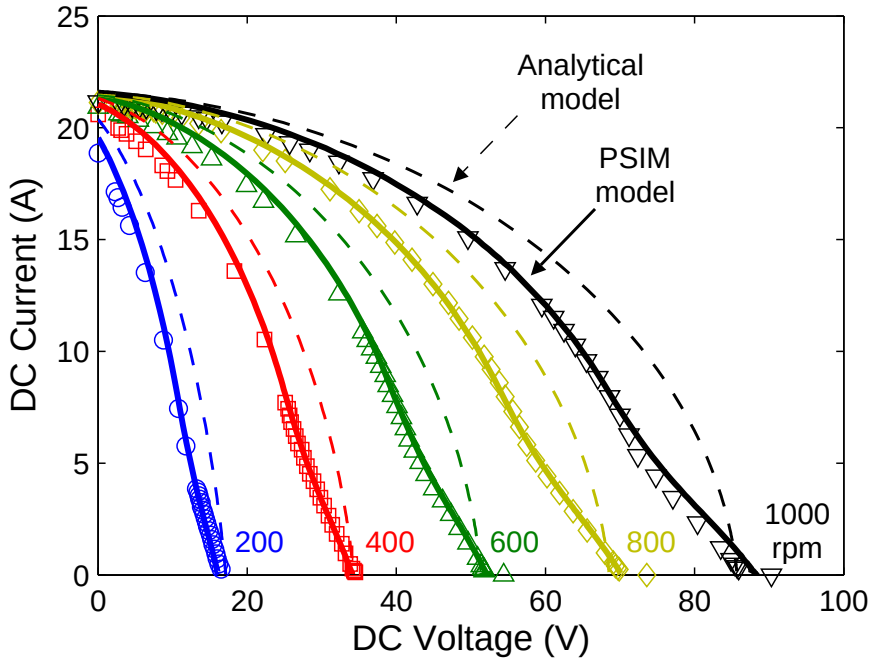


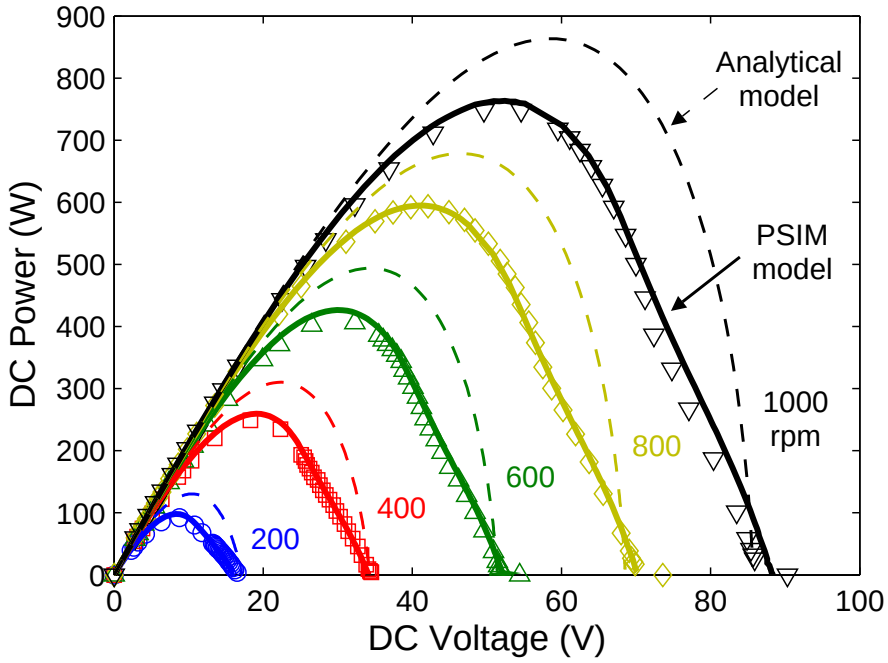
Figure 2.24: Measured generator efficiency vs. output power, for speeds of 200–1,000rpm.

2.4.2 DC Resistive Loading

The test generator is again loaded by a variable resistance, however, an uncontrolled rectifier is used to obtain a DC output voltage, current, and power. The resulting DC I-V and P-V loci are shown in Figure 2.25, which includes the analytical and PSIM® model based simulations, and the measured experimental data. There is a close match between the measured results and the PSIM® simulations, giving confidence in the model.



(a) I-V locus



(b) P-V locus

Figure 2.25: PM machine DC output voltage loci, showing (a) current, and (b) power loci, for generator speeds of 200–1000 rpm. The points represent measured data, whilst the dashed and solid lines represent the ideal analytical model and PSIM® simulations, respectively.

In particular, the PSIM® model accurately predicts the non-linearity in the rectified I-V locus near the open-circuit point. This non-liberality is likely to be associated with discontinuous input currents under this condition.

Power Maximisation

The normalised generator I-V and P-V loci of Figure 2.7 indicate that the maximum generator output power ideally occurs for an output current and voltage of 0.71pu ($1/\sqrt{2}$). The roughly constant short-circuit current and the open-circuit voltage, which is proportional to speed, implies that the peak output power will increase linearly with generator speed. The peak DC output power can also be assumed to be linearly proportional to the generator speed, as the rectifier has a fixed voltage drop and hence power loss. This can be seen from the P-V locus above, but is more clearly seen in Figure 2.26, which shows the both the analytical and PSIM® DC predictions, as well as the peak measured power. Note that the peak measured power is slightly less than that predicted by PSIM®. This may be due to the limited range of resistances, which do not necessarily correspond to the peak DC output power. This is evident for the 600rpm P-V locus.

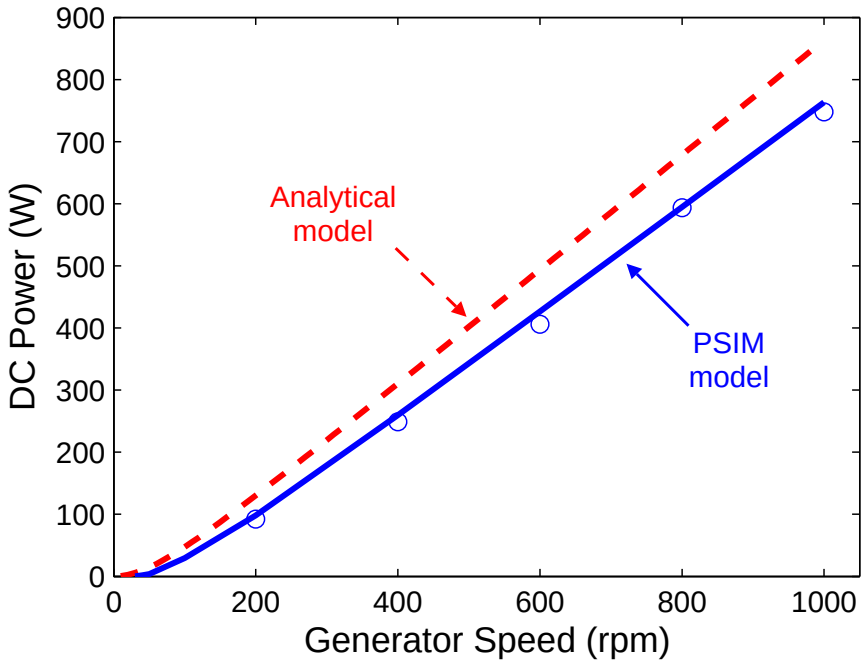


Figure 2.26: Maximum DC output power vs. generator speed. The points represent the experimentally measured data, whilst the solid and dashed lines correspond to the PSIM® and analytical model based simulations, respectively.

Modelling Discrepancies

The discrepancies between the analytical and PSIM® DC output predictions are clearly seen in Figures 2.25 and 2.26. This, along with the close match between the experimentally measured data and the PSIM® simulations indicate the simplifying assumptions, used with the analytical model, have only limited validity. This is briefly investigated here using a power analyser to compare the rectifier AC input and DC output current and voltage magnitudes. The rectifier output (DC) current is found to closely match that predicted by the analytical model seen in Equation (2.15), however, the DC voltage does not match the analytical prediction seen in Equation (2.14). This is likely due to the assumption that the generator currents and voltages are sinusoidal using the rectifier. In addition, it was shown in [63] that diode commutation, which can take up to 1ms at rated current, accounts for a lower mean voltage (on the DC link) than that expected.

The measured ratio of DC to RMS AC line voltage is shown in Figure 2.27, for generator speeds of 200–1,000rpm. The solid line in the figure represents the fixed AC to DC voltage ratio of the analytical model, whilst the dashed line corresponds to the calculated DC to RMS line voltage ratio. The calculated ratio assumes a sinusoidal voltage source

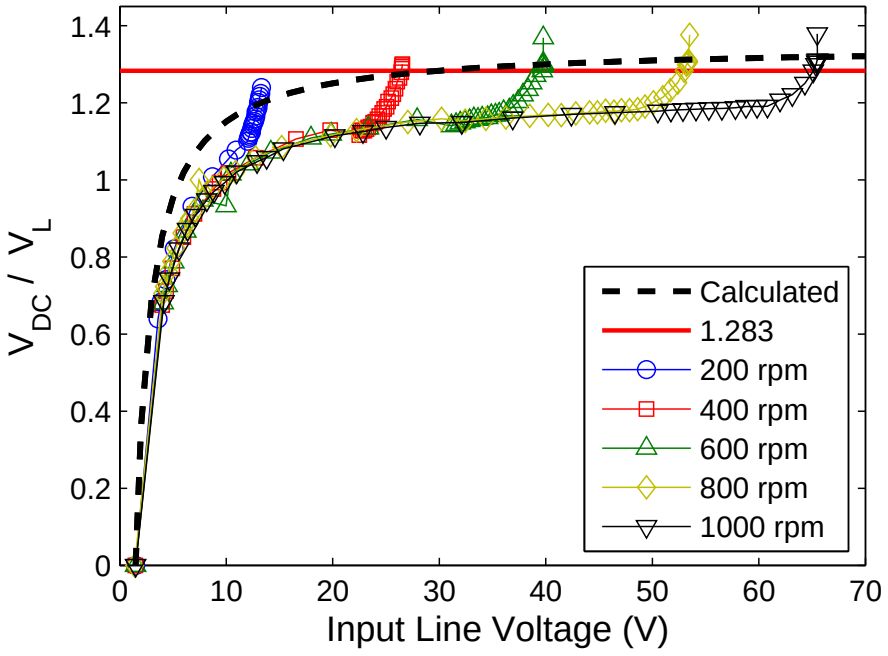


Figure 2.27: Measured DC to RMS line voltage ratio, for generator speeds of 200–1,000rpm. The solid line represents the fixed ratio, as used by the analytical model, whilst the dashed line represents the calculated ratio.

input, a fixed rectifier voltage drop (1V / diode) and a purely resistive load. This calculated ratio is shown to increase rapidly at small line voltages values, and becomes steady at high voltages, where it approaches 1.347. This occurs as the rectifier voltage drops are significant at low voltages, whilst these are negligible at high line voltages.

Although the measured ratio is shown to increase with line voltage in a similar manner to that of the calculated ratio, it approaches a value of about 1.2, which is somewhat less than the calculated limit of 1.347. In addition, the measured ratio is shown to rapidly increase once the line voltage exceeds about 0.91pu of its open-circuit voltage (see Figure 2.25(a)). The ratio then reaches a peak of 1.38 at open-circuit voltage, for each generator speed. This phenomenon is likely to be caused by the non-sinusoidal machine currents near the open-circuit point. Further investigation is required, however, it is beyond the scope of this work.

Generator + Rectifier Efficiency

The generator and rectifier efficiency is measured using the power analyser, and is shown in Figure 2.28, as a function of generator speed and DC output power. The combined efficiency appears similar to the generator (AC) efficiency (see Figure 2.24). However,

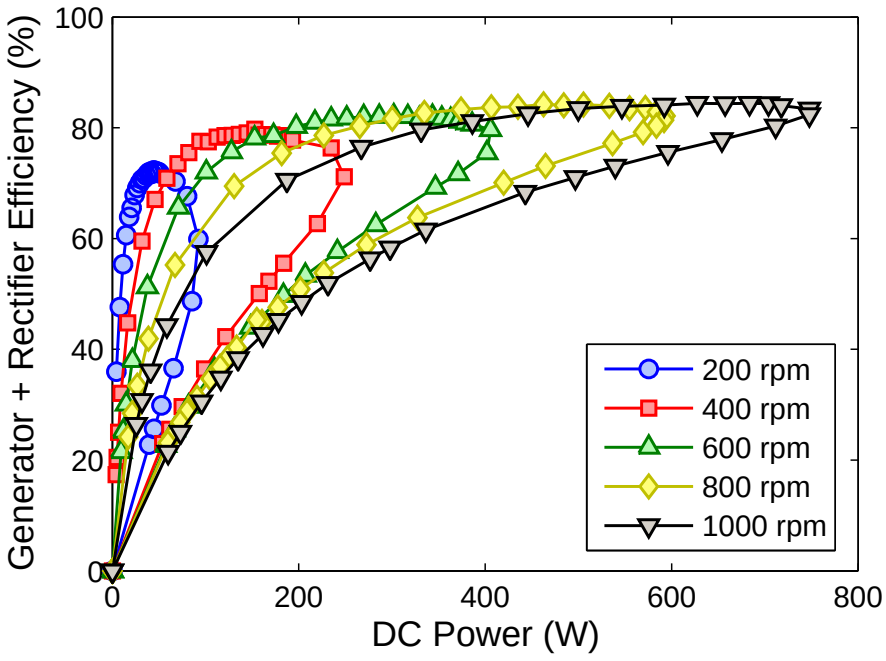


Figure 2.28: Measured generator and rectifier efficiency vs. DC output power, for generator speeds of 200–1,000rpm.

the efficiency is reduced at low powers (and hence generator speeds), due to the fixed maximum rectifier loss, which is more significant at low rectifier output powers. The rectifier loss is proportional to the fixed diode voltage drops and rectifier output current.

Note that the rectifier efficiency is combined with the generator efficiency here as both the DC-DC and the DC-AC power converters proposed in this study contain an uncontrolled full-bridge three-phase rectifier. The combined peak efficiency increases from 72%, at 200rpm, to 84% at 1,000rpm; compared to the previously measured peak generator efficiencies of 83 to 87%, over the same speed range (see Figure 2.24).

2.5 Chapter Summary

The use of a fractional-slot concentrated winding gives PM machines a high-inductance characteristic, which allows the machine to operate at currents close to the short-circuit current for prolonged periods of time. This was experimentally verified, which found that the temperature of the tested PM generator stator winding increased by about 25°C, after operating under three-phase short-circuit conditions at high speed for 40 minutes. This temperature rise corresponds to a stator resistance increase of 10.7%.

The high-inductance PM generator current vs. voltage (I-V) loci and hence power vs. voltage (P-V) loci are simulated based on simplified analytical modelling using the single-phase synchronous generator equivalent circuit. A second model based on a numerical circuit simulation software package, PSIM®, is also used. Both models predict similar generator AC output current and power vs. voltage loci, which closely match the experimentally measured data, especially at low generator speeds. Despite this, discrepancies exist, which increase with generator speed. These may be are caused by increasing stator temperature (and hence resistance), and by skin and proximity effects.

In contrast, when predicting the uncontrolled rectifier DC output characteristic, the analytical model, which is based on a converting AC to DC quantities by using a fixed ratio and assuming a loss-less rectifier, does not match the PSIM® based simulations. The PSIM® predictions match the experimentally measured data. This indicates the simplifying assumptions used in the DC analytical model have only limited accuracy. It is interesting to note that comparisons of the measured rectifier AC input and DC output quantities show that the AC to DC current ratio is fixed, whilst the AC to DC voltage ratio varies with the AC voltage.

The P-V loci indicate that output powers below that of the peak, can be obtained using two different voltage / current combinations. Therefore, two efficiency vs. power curves exist for each speed, which meet at the peak power. Regrettably, the least efficient curve corresponds to the constant-current region of the I-V locus, which is the proposed operating region, as the higher currents cause higher copper losses.

Chapter 3

Switched-Mode Rectifier Operation

This chapter discusses the equivalent circuit, modelling and operating regions of the switched-mode rectifier (SMR). The SMR is experimentally tested with the high-inductance PM generator from Chapter 2, using a dynamometer and small wind tunnel. The SMR duty-cycle is varied in an open-loop manner using the dynamometer and wind tunnel, which allows the generator and wind speeds to be controlled, respectively. The SMR is shown to effectively control the PM generator such that maximum power is obtained at low wind speeds, and that the turbine speed is limited under high wind speed conditions.

3.1 Introduction

The switched-mode rectifier is a simple single-switch power converter that converts the variable frequency and magnitude generator output voltage to a fixed DC voltage. It consists of a three-phase uncontrolled full-wave rectifier, a high-speed switch that shorts the rectifier output at a duty-cycle, d, a reverse-blocking diode and a storage capacitor, as summarised in Figure 3.1. The SMR is similar in appearance and performance to a boost converter with an uncontrolled rectifier, however, it requires fewer passive components, as it uses the phase inductance of the high-inductance PM generator, rather than an external inductance (recall Figure 1.9).

The SMR can deliver a controlled output current to a voltage-source load, and is hence suitable for use as a battery charger. The fixed output voltage, V_{SMR}, (often referred to as the DC link voltage) together with the parallel SMR switch, and the machine phase inductance allows the boosting action to occur. This effectively allows the rectifier output voltage (and hence generator output voltage) to be reduced below the DC link voltage.

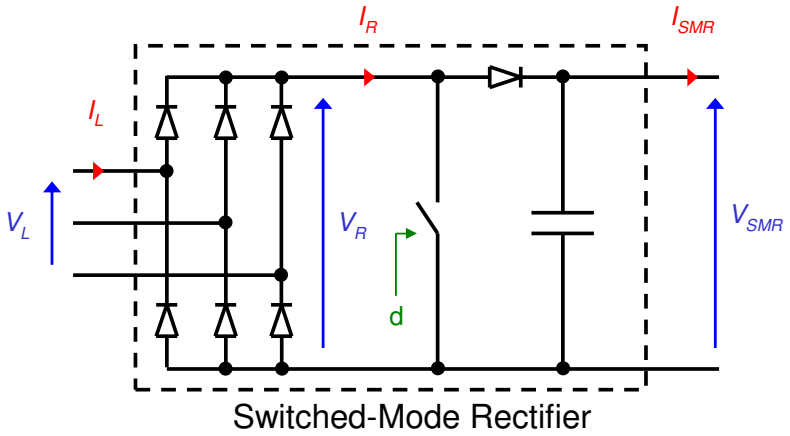


Figure 3.1: SMR equivalent circuit showing three-phase uncontrolled rectifier, switch, blocking diode and storage capacitor. The rectifier input and output, and SMR output currents and voltages are shown using subscripts $_L$, $_R$, and $_{SMR}$, respectively. The SMR switch duty-cycle, d, is also shown.

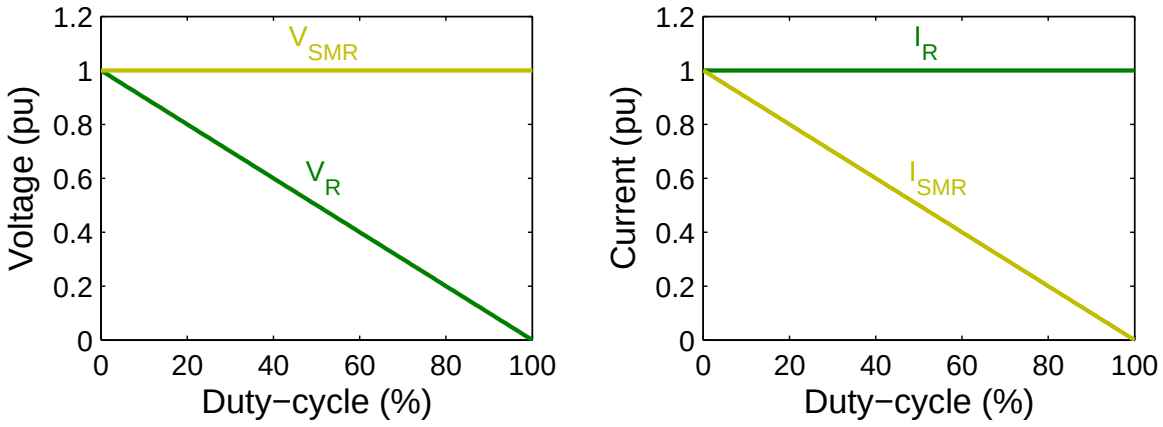
The rectifier voltage, V_R, is linearly proportional to the duty-cycle, and the constant DC link voltage, as summarised in Equation (3.1). Similarly, the SMR output current, I_{SMR}, is proportional to the rectifier output current, I_R, and the duty-cycle, as shown in Equation (3.2). This is derived assuming the SMR is loss-less, i.e. $V_{SMR}.I_{SMR} = V_R.I_R$. These ideal rectifier and SMR output voltage and current relationships are summarised in Figure 3.2. Note that the rectifier current and DC link voltage are both assumed to be constant and equal to 1pu, and that the rectifier current and voltages are proportional to the generator line currents and voltages, as discussed in Chapter 2.

$$V_R = (1 - d)\ V_{SMR} \tag{3.1}$$

$$I_{SMR} = (1 - d)\ I_R \tag{3.2}$$

3.1.1 Switched-Mode Rectifier Model

A switched-mode rectifier can be modelled as an uncontrolled rectifier with a voltage-source load, as the output voltage of the SMR is essentially constant. This model can be approximated by an uncontrolled rectifier with a resistive load, and thus further modelled as a three-phase resistive load. This approach is based on the assumptions that the rectifier forces the generator output current and voltage to be in-phase and that the current remains sinusoidal despite the non-sinusoidal voltages [56]. Using these assumptions,



(a) Voltage

(b) Current

Figure 3.2: Ideal SMR and rectifier output (a) voltages, and (b) currents vs. duty-cycle. The SMR output voltage, V_{SMR}, is fixed due to the voltage-source load, whilst the rectifier output current, I_R, is assumed constant.

the DC output voltage / current characteristic of the SMR can be modelled using the DC analytical model described in Section 2.3.1. Note that the DC load resistance is effectively varied by adjusting the duty-cycle.

Despite this, the DC analytical model was previously shown in Chapter 2 to significantly differ from the PSIM® simulations. In addition, the PSIM® predictions were shown to closely match the experimentally measured DC resistive load test data, giving confidence in this model. Therefore the remainder of simulations presented in this thesis are predicted using PSIM®. The PSIM® model of the SMR is shown in Figure 3.3, which includes the delta-connected PM (test) generator, and a voltage-source load. Note that the voltage source load fixes the voltage drop across the load resistance, and consists of a fixed load resistance, voltage source and reverse-blocking diode.

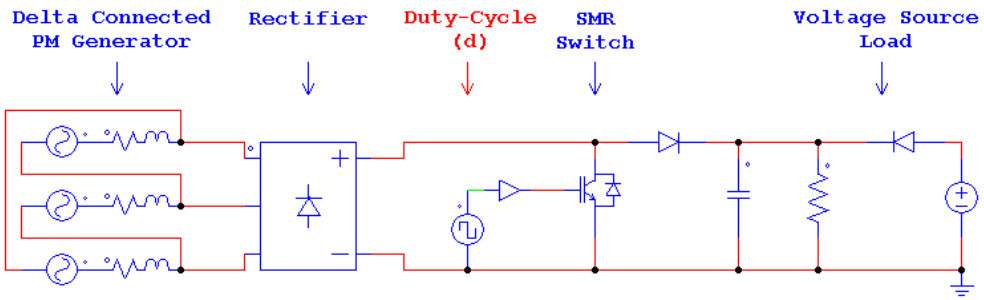


Figure 3.3: PSIM® model of the delta-connected PM generator and switched-mode rectifier connected to a voltage-source load. An IGBT is used as the SMR switch.

3.1.2 SMR Operation

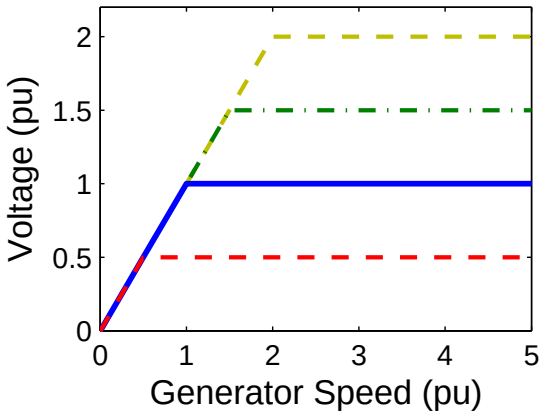
The SMR operates in a similar manner to a PM generator and rectifier operating in to a voltage-source load, where the load voltage can be changed by varying the duty-cycle. Note that the high-frequency switching of the SMR, together with the machine inductance, causes the PM machine to see only the time averaged effect of the PWM switching. Hence, the SMR operation is described and compared to that of a PM machine generating into a DC voltage-source load (e.g. battery), using an uncontrolled three-phase rectifier. This is commonly referred to as uncontrolled generation (UCG) [56].

Uncontrolled Generation

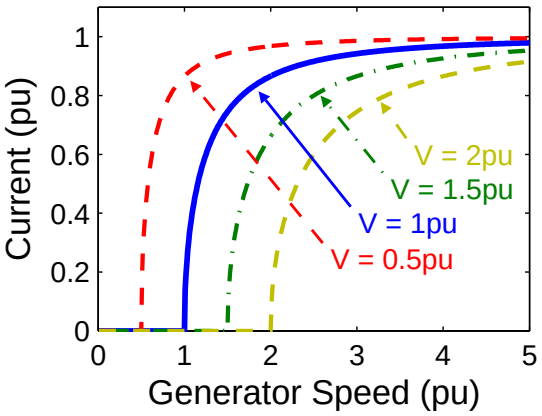
Consider a PM machine that is connected to a rectifier and operates into a voltage-source load. As the speed increases from standstill, the DC output current remains at zero until the speed at which the induced back-EMF is equal to the DC link voltage. Beyond this speed the generator output current increases rapidly and asymptotes towards its characteristic current (Equation (2.2)) at high speeds. This occurs as the output voltage remains fixed, whilst both the induced voltage and stator inductance increase with speed, i.e. the machine approaches the short-circuit operating condition.

An example of a PM generator operating under the UCG condition is shown in Figure 3.4, which shows the rectifier output voltage, current and power vs. generator speed, for DC link voltages of 0.5, 1, 1.5 and 2pu. Consider the 0.5pu DC link voltage case. It is seen that the induced and DC link voltages are equal at a speed of 0.5pu, after which current begins to flow. This highlights that the machine is able to deliver reduced power at lower speeds and hence induced voltages, providing the DC link voltage is reduced. Similarly, more output power is obtained if the DC link voltage is increased at high generator speeds.

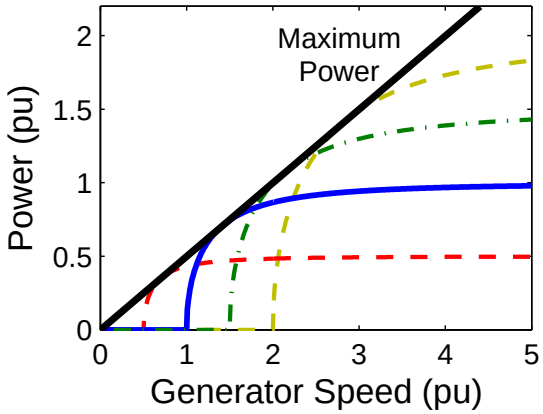
The figure also highlights that the maximum output power increases linearly with speed. This occurs as the induced back-EMF voltage and stator reactance are proportional to machine speed. In addition, the DC link voltage must also be increased with speed to maximise the rectifier output power. This is equivalent to matching the effective three-phase load resistance to the magnitude of the stator reactance. This concept is referred to as *load matching*, and allows maximum power to transfer from the source to the load. Maximum power corresponds to a current of 0.71pu, which occurs at a speed of $1.41\,V$ pu.



(a) Voltage



(b) Current



(c) Power

Figure 3.4: Ideal (a) voltage, (b) current, and (c) power, of a generator operating in to a rectifier and a voltage-source load with DC link voltages of 0.5, 1, 1.5 and 2pu. The solid line in (c) represents the maximum power, which increases linearly with speed.

SMR Operating Regions

The above figure shows that output power can be obtained even at low generator speeds, by using a low DC link voltage. This, however, limits the power at high generator speeds. The SMR overcomes this by adjusting the rectifier voltage (via the duty-cycle) as a function of generator speed, which effectively allows the SMR to *load-match* the PM generator and load. This allows the generator to transfer maximum power to the voltage-source load (battery), whilst operating into a fixed output voltage. This is referred to as the *Boost Rectifier* operating mode, and occurs for generator speeds below 1.41pu, where a higher output power is obtained, compared to that using an uncontrolled rectifier.

In contrast, the induced back-EMF voltage significantly exceeds the DC link voltage at high speeds, and the PM generator can be considered as a constant current source under these conditions. The SMR output current and hence power can be reduced below that of an uncontrolled rectifier, by adjusting the duty-cycle. This is hence referred to as the *Current Chopper* mode. Both operating modes and the regions they occupy are summarised in Figure 3.5. In addition, the dashed line represents the power obtained using an uncontrolled rectifier operating into a voltage-source load of 1pu; it is shown for reference. Note that the SMR output power can be controlled such that any amount of power within the shaded regions is transferred from the generator to the load.

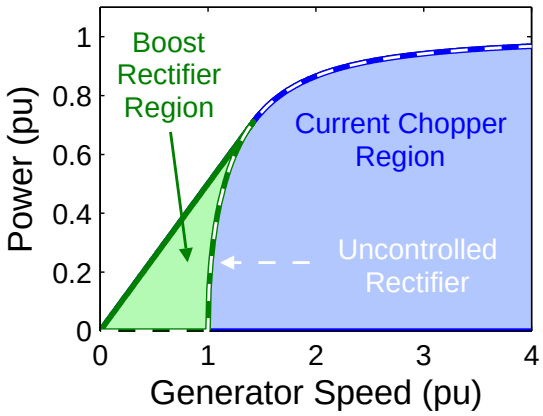


Figure 3.5: SMR operating areas, including the boost rectifier and current chopper regions. The dashed line represents the power obtained using an uncontrolled rectifier, and is shown for reference. The SMR output power can be controlled to any value within the shaded regions, by adjusting the duty-cycle.

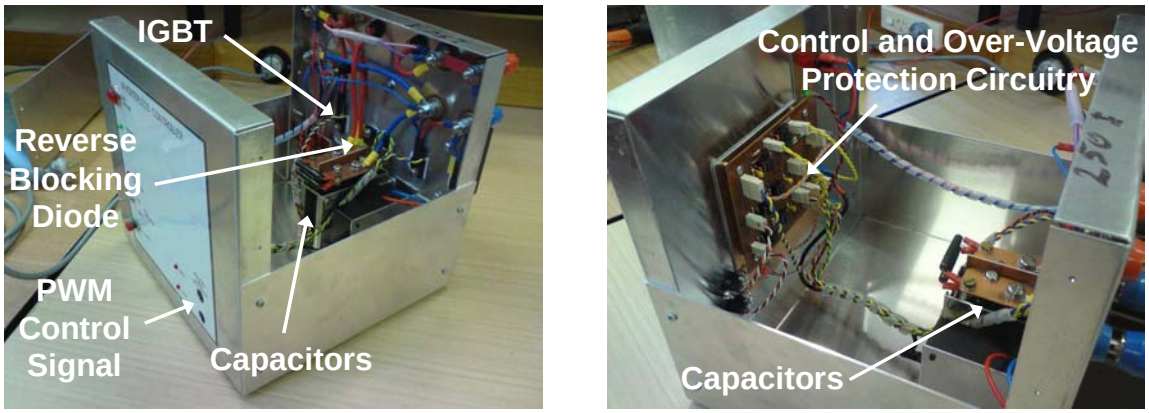
3.1.3 SMR Properties

The SMR used was designed and constructed for another application, and as such was designed with additional features such as over-voltage protection and dummy-load switching capabilities, which are beyond the scope of this work. The SMR components of interest include the IGBT, reverse-blocking diode, and the filter capacitors ($2\times$ 470μF). A summary of the components a photograph showing these and other aspects of the SMR, are shown in Table 3.1 and Figure 3.6, respectively.

Table 3.1: SMR component properties.

Component / Property	Rectifier	IGBT	Diode	Capacitor
Manufacturer	SEMIKRON	IR	IR	BHC Components
Part Number	SKD230/16	IRG4PC40F	40EPF10	ALS31A471DE400
Rating	230A, 1600V	27A, 600V	40A, 1000V	400V (470μF)
Voltage Drop	1V per diode	1.50V	1.25V	-
Maximum ESR	-	-	-	0.267Ω

Note: IR and ESR denote International Rectifier, and equivalent series resistance, respectively.



(a) Components

(b) Control circuitry

Figure 3.6: Photograph of SMR (a) semiconductor components, and (b) control and over-voltage protection circuitry.

3.2 Dynamometer Testing

The SMR is experimentally tested using the same PM generator characterised in Chapter 2, as its input. The generator is directly coupled and driven by a 5kW DC machine using a dynamometer test rig (see Section 2.2.2). The generator speed is controlled by adjusting the DC machine armature voltage and field current. The SMR is tested by varying its duty-cycle over a wide range of fixed generator speeds.

3.2.1 Test Arrangement

The PM generator and SMR test arrangement is shown in Figure 3.7. The SMR is connected to a voltage-source load that simulates a 42V battery. This DC link voltage was chosen primarily as this is a multiple of 14V, which is required to charge a standard 12V battery. In addition, this voltage exceeds the rectified open-circuit voltage of the PM machine for speeds below about 450rpm (see Section 2.4.2). This is useful as it demonstrates how the SMR will operate in the boost rectifier operating mode under low wind speed (generator speed) conditions.

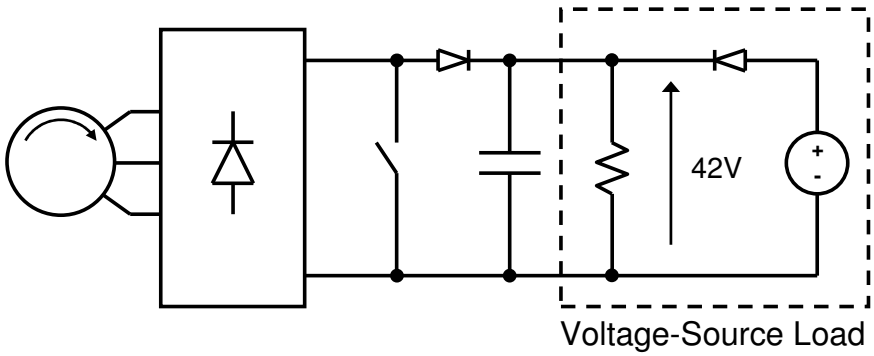


Figure 3.7: SMR dynamometer test arrangement, showing the PM generator, switched-mode rectifier, and the voltage-source load (VSL). The VSL consists of a DC voltage source, reverse-blocking diode and a load resistance; its output voltage is set to 42V.

3.2.2 SMR Test Results

The SMR is loaded by the voltage source whilst the PM machine is rotated at various speeds. The load voltage is fixed during the SMR tests, i.e. the SMR duty-cycle and machine speed are the only adjustable parameters. The SMR duty-cycle is swept from 0 to 100% for generator speeds of 200, 400, 600, 800 and 1,000rpm.

The simulated and measured rectifier voltages are shown in Figure 3.8 as a function of duty-cycle, d, and generator speed. The rectifier voltage is shown to be linearly proportional to (1-d), for speeds of 600rpm and above. This occurs as the rectified open-circuit voltage is greater than the DC link voltage for speeds above about 500rpm. In contrast, the rectified generator voltage is linearly proportional to (1-d) only for higher duty-cycles for the 200 and 400rpm cases. The voltage then sharply asymptotes towards its maximum value which corresponds to the rectified generator open-circuit back-EMF voltage. The rectifier can not transfer power to the SMR as its voltage is less than that set by the required voltage given by Equation (3.1). Even when the SMR duty-cycle is further reduced, the rectifier voltage remains unchanged for these generator speeds. This is highlighted in the figure for the 200 and 400rpm cases, which shows that the rectifier voltage must be less than 16.5 and 33V to transfer power from the generator to the SMR, respectively.

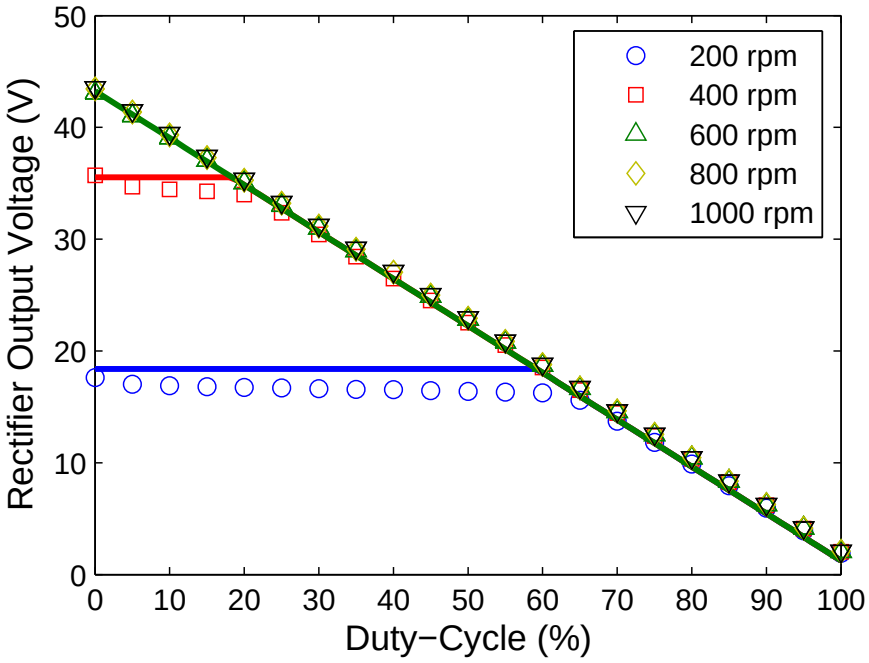


Figure 3.8: Rectifier output voltage vs. SMR duty-cycle, for generator speeds of 200–1,000rpm. The solid lines represent PSIM® simulations, whilst the points correspond to measured data. Note that the simulated and measured data for the 600–1000 rpm cases are identical and vary linearly with (1-d), whilst the rectifier voltage reaches its maximum value at duty-cycles of 60 and 20%, for the 200 and 400 rpm cases, respectively.

Note that the DC link voltage seen at the rectifier is offset by the SMR reverse-blocking diode forward voltage drop (1.25V). In addition, the rectifier voltage is limited at high duty-cycles by the IGBT voltage drop (1.5V).

The above figure indicates that output current and hence power will only be obtained for a duty-cycle greater than 60 and 20%, for speeds of 200 and 400rpm, respectively. This is verified in Figure 3.9, which shows the rectifier output current vs. duty-cycle characteristic, for the generator speeds mentioned above. The figure clearly shows that current ceases to flow for the 200 and 400rpm cases, if the duty-cycle is set below 60 and 20%, respectively. This, together with Figure 3.8 indicates that the SMR operates in the boost rectifier region for generator speeds less than 500rpm, as the rectified induced back-EMF voltage is less than DC link voltage for these speeds. Power is transferred to the SMR as the DC link voltage is effectively reduced by increasing the duty-cycle. In contrast, the SMR operates in the current chopper region for generator speeds above 500rpm, as the rectified induced back-EMF voltage exceeds that of the DC link.

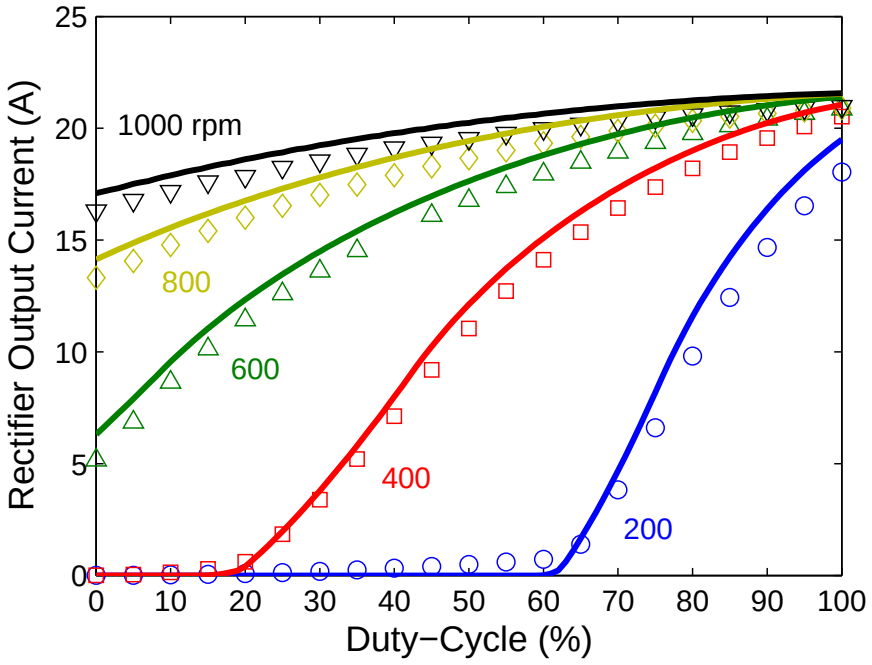


Figure 3.9: Rectifier output current vs. SMR duty-cycle, for generator speeds of 200–1000 rpm. The points represent measured data, whilst the solid lines correspond to PSIM® simulations.

The above figure also shows that the PM generator and rectifier start to operate as a constant current source at 1,000rpm. This occurs as the induced back-EMF voltage is significantly larger than the DC link voltage at this speed, and implies that the generator's ability to provide a relatively constant current decreases with speed, i.e. due to the decreasing induced voltage (see Section 2.1.2).

The SMR output current is shown in Figure 3.10 as a function of duty-cycle for the various generator speeds tested. It is expected that the current varies linearly with (1-d) for a constant rectifier current (see Equation (3.2)). This is seen for the 1,000rpm case, as the induced back-EMF is significantly greater than the SMR output voltage, except at low duty-cycles. The generator behaves less ideally as the speed and hence back-EMF voltages decrease, resulting in a substantial drop in the rectifier current at low duty-cycles. Note that the SMR is able to maximise its output current and hence power (see Figure 3.11) for generator speeds of 800rpm or less. Note also that the SMR output power and current plots are identical in shape, as the SMR output voltage is fixed by the voltage-source load. In addition, the SMR output power curves appear similar to the DC resistive load test loci of Figure 2.25(b), for DC voltages between 0 and 42V. The difference, however, is that the x-axis is reversed due to the (1-d) relationship stated in Equation (3.1).

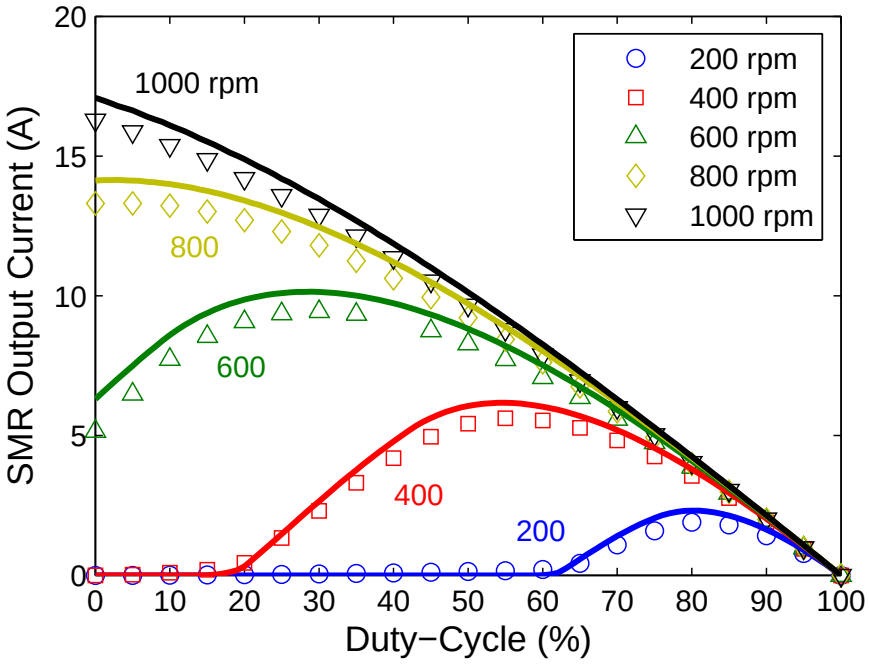


Figure 3.10: SMR output current vs. duty-cycle, for generator speeds of 200–1000 rpm. The points and solid lines represent measured data and PSIM® simulations, respectively.

The SMR output power is shown to vary with speed and duty-cycle, which implies that the rectifier and generator output power must also vary with these parameters. Therefore, the generator input power and hence generator torque must also vary with speed and duty-cycle. This is verified in Figure 3.12, which shows the measured machine torque as a function of duty-cycle and generator speed. The torque plot for the 200rpm

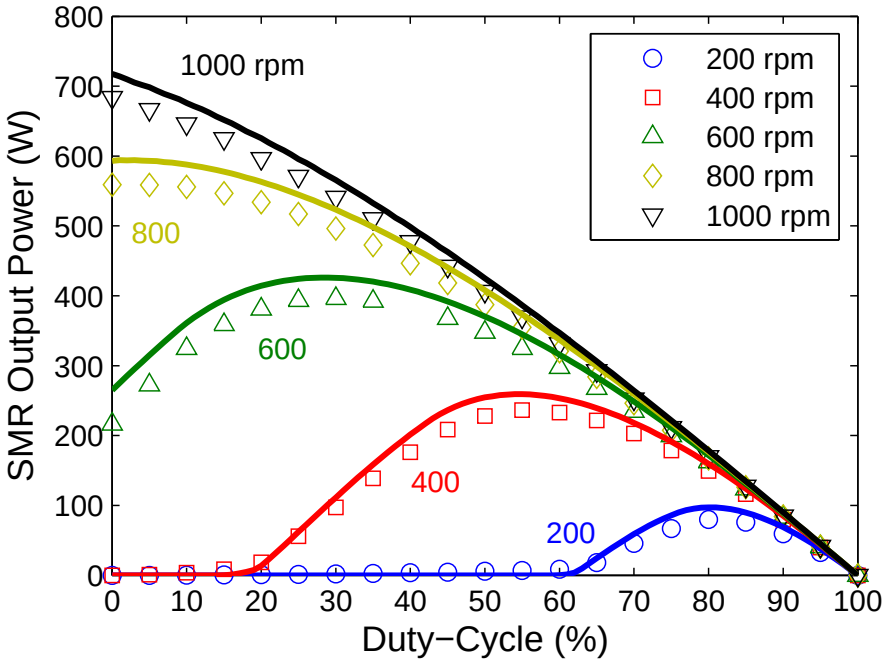


Figure 3.11: SMR output power vs. duty-cycle, for generator speeds of 200–1000 rpm. The solid lines and points represent PSIM® simulations and experimentally measured data, respectively.

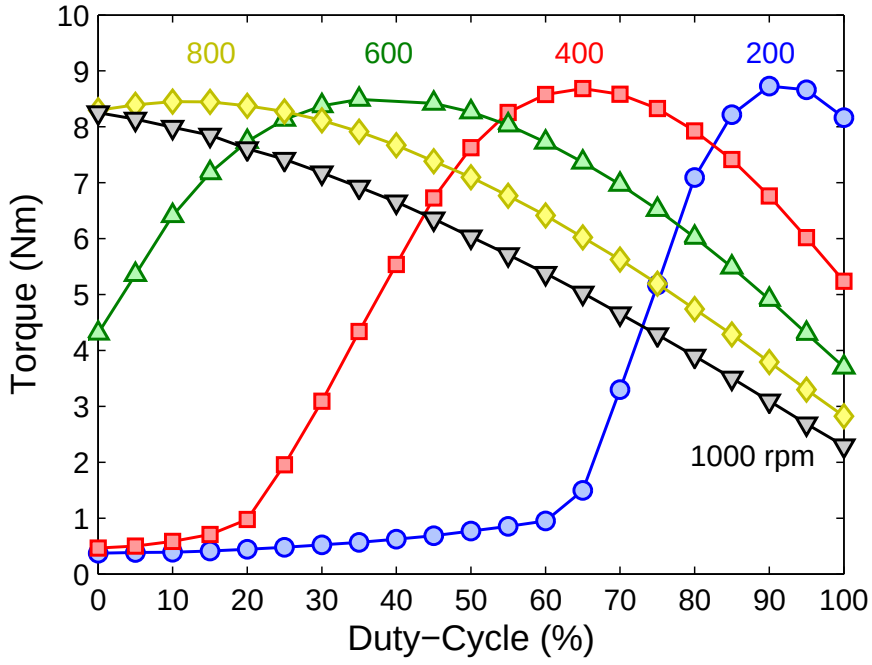
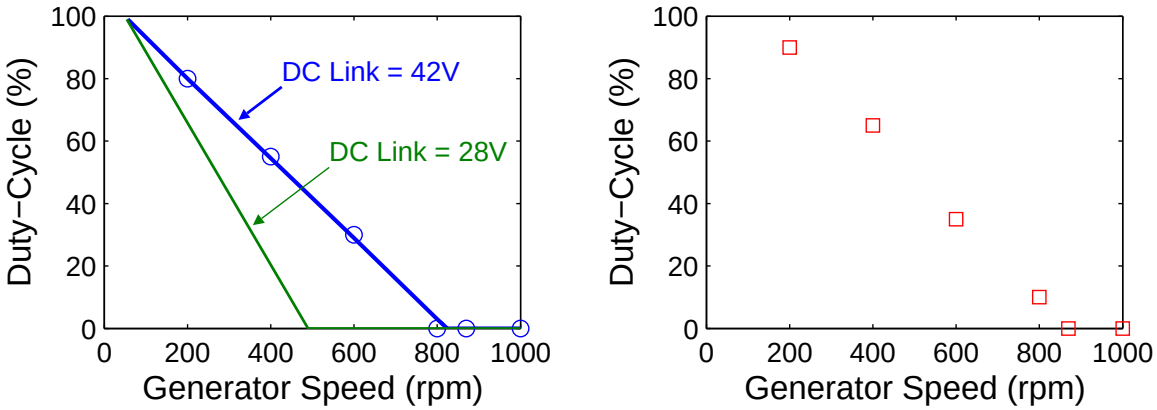


Figure 3.12: Measured torque vs. duty-cycle, for generator speeds of 200–1000 rpm.

case appears similar to that of the short-circuit test (Figure 2.12(b)), however, the x-axis is again reversed. The torque curve peak broadens and shifts to the left as the generator speed increases. This implies that in addition to the SMR output power, the machine torque can be controlled by adjusting the duty-cycle, for a fixed generator speed.

Power and Torque Maximisation

Figures 3.11 and 3.12 indicate that the SMR duty-cycle corresponding to maximum SMR output power and generator torque, varies with generator speed. This is more easily seen in Figure 3.13, which also shows that output power will only be produced for generator speeds above 56rpm. This is because 56rpm corresponds to the generator speed at which the induced voltage exceeds the rectifier and SMR reverse-blocking diode forward voltage drops. In addition, the SMR can only maximise the generator power by varying the duty-cycle for generator speeds less than 824rpm, as this corresponds to the speed at which the peak rectified generator back-EMF voltage equals that of the DC link. As such, the SMR will extract maximum generator power for duty-cycles of 0% for all generator speeds above 824rpm (see Figure 3.5). This implies that the SMR operates in the boost rectifier mode for generator speeds between 56 and 824rpm, whilst it operates in the current chopper modes for generator speeds above 824 rpm. Note that this range of speed is dependent on the DC link voltage, as shown in Figure 3.13(a) for a reduced V_{DC} of 28V.



(a) Power maximisation

(b) Torque maximisation

Figure 3.13: Duty-cycle corresponding to maximum (a) SMR output power, and (b) generator input torque, vs. generator speed. The solid lines and points represent PSIM® simulations and measured data, respectively. The simulations in (a) correspond to DC link voltages of 42 and 28V.

The duty-cycle corresponding to maximum generator torque is also linearly proportional to the generator speed. Similarly, Figure 3.13(b) shows that the generator torque can be maximised (by adjusting the duty-cycle) for generator speeds between 130 and 870rpm, i.e. the generator operates below its peak torque outside of this speed range. Note that this range of speed also varies with the DC link voltage.

SMR Efficiency

The measured SMR efficiency is shown in Figure 3.14, as a function of SMR output power. The efficiency is plotted for each generator speed, and its peak is shown to increase with generator speed from 82.9% at 200rpm to 94.0% at 600rpm. The 200, 400 and 600rpm cases show two efficiency vs. power plots that meet at the peak power. This was previously seen in Figure 2.28, which occurs as the same power can be obtained for two different rectifier voltages (or duty-cycles in this case). Note that only one efficiency vs. power plot exists for the 800 and 1,000rpm cases as the voltage corresponding to peak DC power occurs at voltages greater than the DC link. This is seen in Figure 2.25(b), which shows that maximum power occurs at speeds of 800 and 1,000rpm when the DC voltages are 42.2 and 56.2V, respectively.

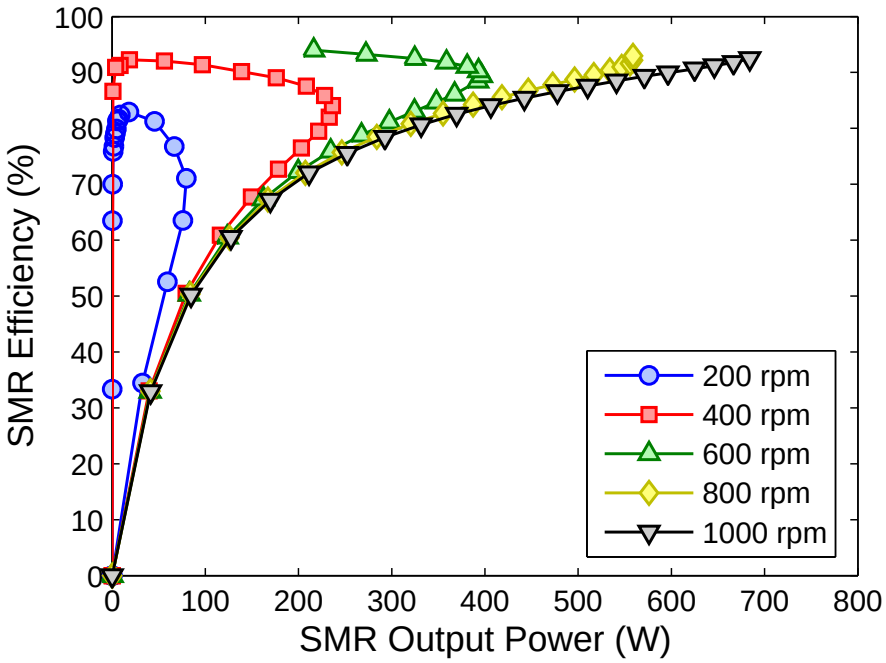


Figure 3.14: Measured SMR efficiency vs. power characteristic, for generator speeds of 200–1000 rpm.

System Efficiency

The measured torque allows the generator input power to be calculated, which is used to determine the total system efficiency. The system efficiency, i.e. that of the SMR and the PM generator, is shown in Figure 3.15. The figure shows that the peak efficiency increases from 65.9% at 200rpm to 80.9% at 600rpm, whilst it decreases slightly to 79.1% for the 1,000rpm case. This data indicates that the generator alone has a peak efficiency of approximately 79.5, 86.1 and 87.0%, for speeds of 200, 600 and 1,000rpm, respectively.

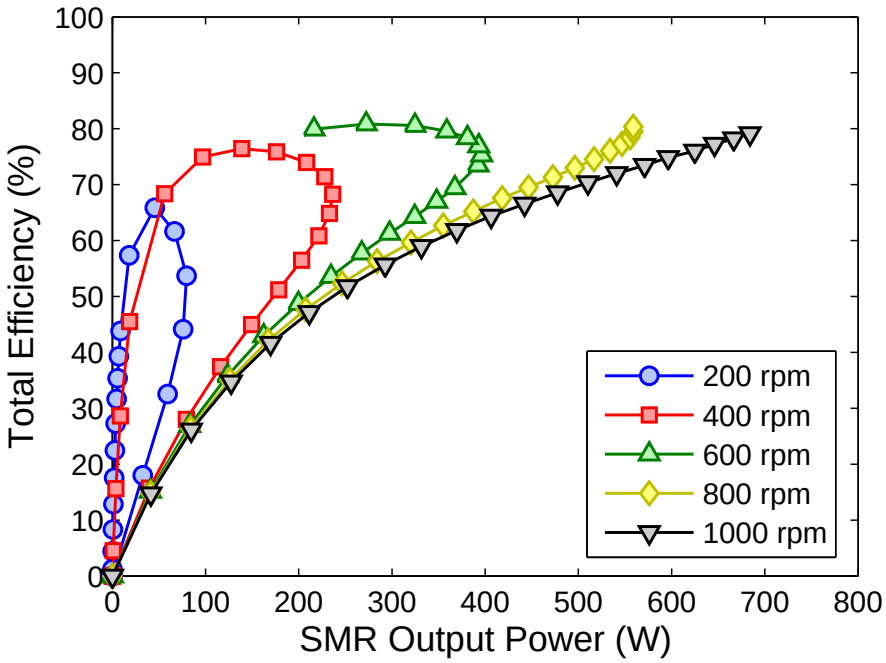


Figure 3.15: Measured total efficiency vs. SMR output power characteristic, for generator speeds of 200–1000 rpm. Note that the total efficiency includes the PM generator and SMR.

3.2.3 Summary of Testing

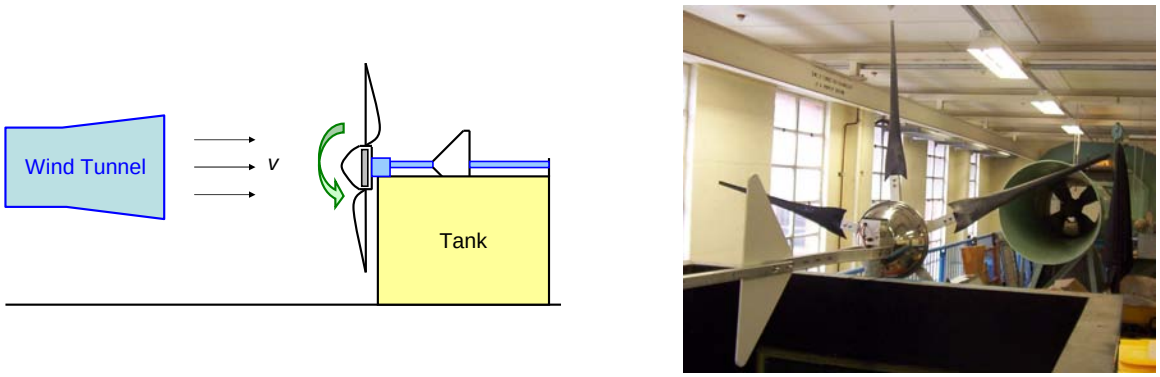
The SMR has demonstrated its ability to maximise the generator output power and control its input torque, over a wide range of speeds using the dynamometer test arrangement. This is important as the SMR is required to maximise the turbine power and limit its speed, at wind speeds below and above rated, respectively. Further testing, using a wind tunnel, is required to verify the SMR's ability to sufficiently control a small-scale wind turbine.

3.3 Wind Tunnel Testing

The SMR's ability to control a commercially available wind turbine, purchased from EcoInnovation® [95], was tested using a small wind tunnel. This allowed the wind speed to be controlled, whilst the SMR duty-cycle was varied. The generator used for this turbine is the F & P outer-rotor surface PM machine, which was tested in Chapter 2 and in Section 3.2. The generator (turbine) speed is again measured using the Hall-effect sensor, however, the torque transducer was unable to be fitted to the turbine. Therefore, the torque was calculated from other measured parameters and is used to estimate the turbine input power and hence blade coefficient of performance characteristics.

3.3.1 Test Arrangement

The wind tunnel test setup, made available by the School of Civil Engineering of the University of Adelaide, is predominantly used for fluid mechanics studies. The wind tunnel aperture diameter is 1m, which is less than the turbine blade diameter of 1.8m. Due to time and resource limitations, the turbine was mounted to a nearby tank, which is located approximately 4 metres from the wind tunnel, and shielded the lower half of the turbine. The turbine was fitted with a carbon brush / slip ring arrangement to allow yaw movement, however, the tail vane was fixed to the tank shortly after initial testing. This was required as the non-ideal test arrangement caused the turbine to oscillate significantly, which affected the turbine orientation (yaw) and wind turbine test results. A block diagram and photograph of the test setup is shown in Figure 3.16.



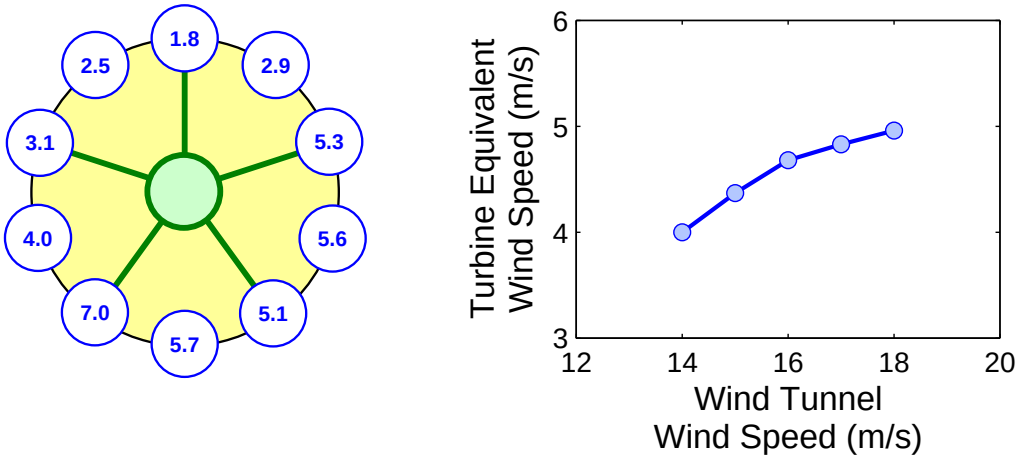
(a) Block diagram (*not to scale*) (b) Photograph

Figure 3.16: Wind tunnel test arrangement, showing (a) block diagram, and (b) photograph of the EcoInnovation® [95] wind turbine and the available wind tunnel. Note that the turbine and its tail vane are fastened to the water tank.

Wind Speed Estimation

Many factors, including nearby obstacles (not shown in Figure 3.16), reflections from the mounting tank, and the large distance between the wind tunnel and turbine, cause the wind speed to be non-uniform within the turbine blade-sweep area. An example of this is shown in Figure 3.17(a) for a wind tunnel (internal) wind speed of 17m/s. The wind speed is measured at 10 points around the blade circumference, using an anemometer. The turbine equivalent wind speed, v_{eq}, is approximated as the cube-root of the mean of the cube of the measured wind speeds, v_i, as the wind power is proportional to the cube of the wind speed. This is summarised in Equation (3.3), where $n = 10$. The wind tunnel was operated at (internal) wind speeds of 14, 15, 16, 17 and 18m/s, which correspond to equivalent wind speeds of 4.00, 4.37, 4.68, 4.83 and 4.96 m/s, respectively, as shown in Figure 3.17(b). The results show another limitation of the test arrangement in that only relatively low equivalent wind speeds (at the turbine) could be achieved. Note that this range of wind speeds was used in the tests, as 14m/s corresponds to the turbine cut-in speed, whilst 18m/s is the wind tunnel's rated wind speed.

$$v_{eq} = \sqrt[3]{\frac{1}{n}\sum_{i=1}^{n} {v_i}^3} \tag{3.3}$$



(a) Non-uniform wind speed distribution (m/s)

(b) Equivalent vs. wind tunnel wind speeds

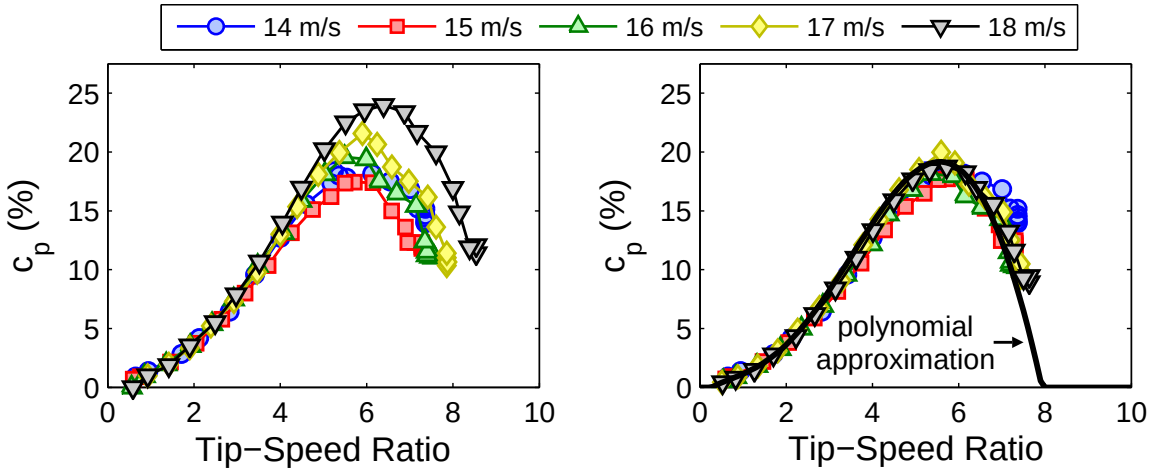
Figure 3.17: Equivalent wind speed calculation, showing (a) measured wind speed around the blade-sweep area for wind tunnel (internal) speed of 17m/s, and (b) the estimated equivalent wind speed vs. internal wind speed characteristic.

3.3.2 Turbine Coefficient of Performance

The turbine is operated at the five wind speeds mentioned above, whilst the SMR duty-cycle is varied from 0 to 100%, at increments of 5%. The PM generator is again connected to the SMR, which has a DC link voltage of 42V. The turbine speed, SMR output current and duty-cycle are recorded for each test, as these parameters allow the turbine (generator) input power to be estimated (based on the results of Section 3.2.2). This allows the turbine coefficient of performance, c_p, to be determined, based on the equivalent wind speed. The c_p is calculated from Equation (3.4), where ρ, r, P_{SMR} and P_{loss} represent the air density, blade radius, SMR output power, and estimated SMR / generator power losses, respectively.

$$c_p = \frac{2\,(P_{SMR} + P_{loss})}{\rho\,\pi\,r^2\,{v_{eq}}^3} \tag{3.4}$$

The resulting estimated c_p curve is shown in Figure 3.18(a), for each v_{eq}. The peak c_p is shown to be 24.0%, for an v_{eq} of 4.96m/s. The results show a consistent shape but do not show a good correspondence in the vertical scaling. It was hence assumed that the lowest wind (4.00 m/s) speed measurement was accurate and the values of higher wind speeds were adjusted to produce c_p curves at these speeds which more closely matched the peak of the 4.00m/s c_p curve. The resulting modified c_p curves are shown in Figure 3.18(b),



(a) Original (b) Modified

Figure 3.18: Estimated coefficient of performance, c_p, vs. tip-speed ratio curve, showing (a) original, and (b) modified data. Note that the legend shows wind tunnel (internal) wind speeds, and that the solid line represents a fifth-order polynomial approximation.

along with a fifth-order polynomial approximation (see Equation (3.5)), shown by the solid line. The value of tip-speed ratio corresponding to the peak c_p of the curve, i.e. 5.6, is consistent with the trend shown in [22] for 1, 2 and 3 bladed turbines. Note that c_p curve is set to zero, for $\lambda < 0.2$ and $\lambda > 8$, as the c_p must be greater than or equal to 0.

$$c_p(\lambda) = 8.1 * 10^{-5} * \lambda^5 - 0.0018 * \lambda^4 + 0.011 * \lambda^3 - 0.018 * \lambda^2 + 0.026 * \lambda - 0.0059 \quad (3.5)$$

The resulting peak c_p is 18.5%, which is significantly less than that expected for turbine of radius 0.9m, i.e. a c_p of about 31%. This value is linearly interpolated from data given in [1], which states that wind turbines of diameter around 1m generally have a maximum c_p of about 0.3 (30%), whilst a turbine of diameter about 10m has a peak c_p of about 0.42 (42%). The difference between the expected and estimated c_p values may be accounted for by the use of low-cost (and possibly poorly designed / inefficient) blades, and experimental error, particularly in the wind speed estimation. Despite the lower than expected peak c_p value, the polynomial approximated c_p curve is used to predict the turbine power and torque in the following sections. The resulting modified equivalent wind speeds are 4.0, 4.4, 4.8, 5.1 and 5.4m/s, and are shown in Figure 3.19, as a function of wind tunnel wind speed. The modified wind speeds are compared to the originally calculated data (from Equation (3.3)) for reference. The modified data is now linearly proportional to the wind tunnel (internal) wind speed, as would be expected for a linear system.

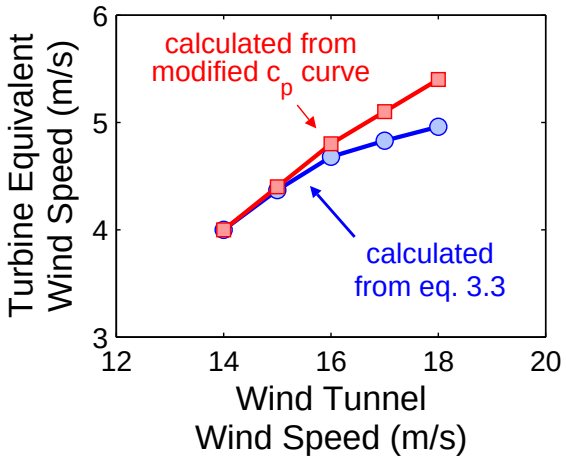


Figure 3.19: Estimated equivalent wind speed vs. internal wind tunnel wind speed. The solid line represents the wind speeds calculated from the cube-root expression, i.e. Equation (3.3), whilst the points correspond to the modified c_p curve of Figure 3.18(b).

3.3.3 Open-Loop Control Mode

The wind turbine is subjected to the small range of available wind speeds, i.e. 4.0 to 5.4m/s, whilst the generator is loaded by the SMR. The duty-cycle is varied for each wind speed, whilst the SMR output current and turbine speed is recorded. The estimated and analytical turbine (generator input) power vs. speed is shown in Figure 3.20. The estimated turbine power, derived from the measured SMR output power, duty-cycle and turbine speed. The results shows a good correspondence to the analytical values, which are based on the analytical turbine equations (Section 1.2.1), the polynomial approximated c_p curve, and the estimated equivalent wind speeds, as discussed above. The dashed line in the figure represents the PM generator's open-circuit iron, friction and windage loss (see Section 2.2.5), which increases roughly linearly with the square of generator speed. This loss is significant compared to the turbine output power, which is due to the low values of the available wind speeds, and prevents measurements being taken at light loads (below the dashed line).

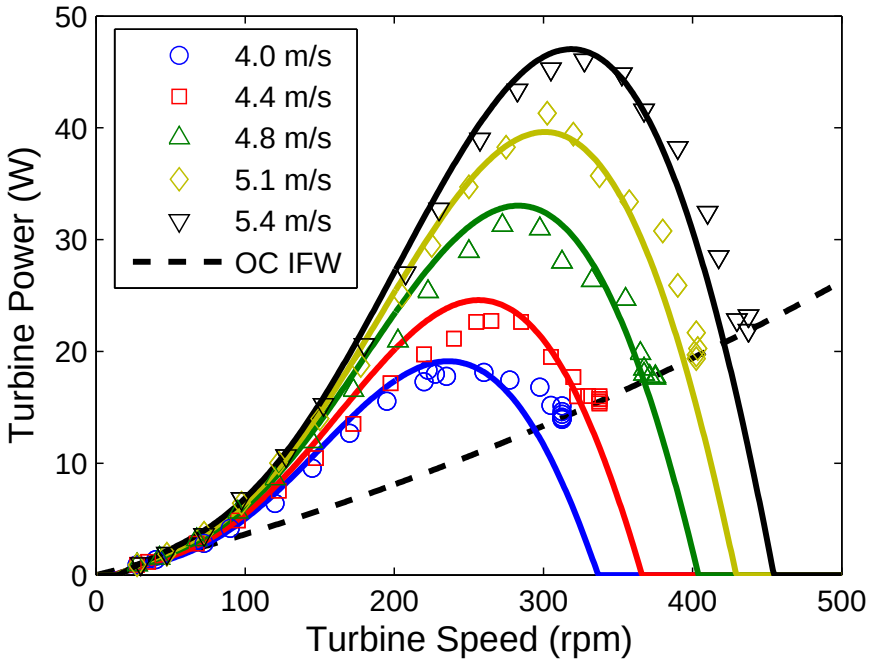


Figure 3.20: Estimated (from measurements) and analytical (lines) turbine power vs. measured turbine speed, for the small range of equivalent wind speeds. The dashed line represents the PM machine open-circuit iron, friction and windage (OC IFW) loss.

The resulting estimated machine input (turbine output) torque is shown in Figure 3.21 as a function of measured turbine speed. The dashed line represents the PM machine iron,

friction and windage loss, which only increases slowly with generator speed, as previously seen in Figure 2.10(b). Note that the vertical offset of 0.3Nm represents the torque required to overcome the machine's bearing, friction losses and cogging torque.

Note that the close match between the estimated and analytical turbine power and torque indicate that the modified c_p curve and the resulting equivalent wind speeds are accurate.

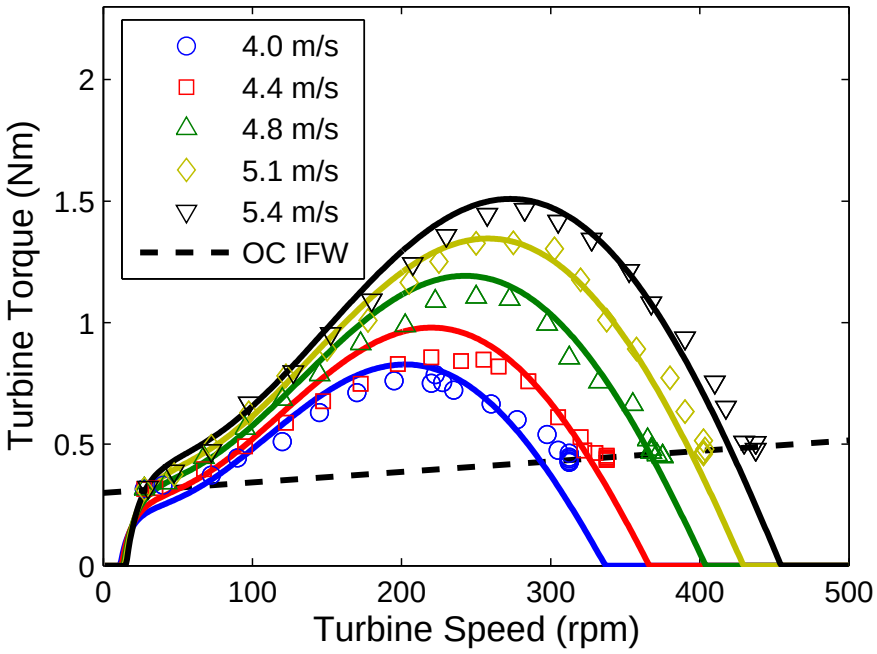


Figure 3.21: Estimated (symbols) and analytical (lines) torque vs. measured turbine speed, for a small range of wind speeds. The dashed line represents the PM machine's open circuit iron, friction and windage loss (OC IFW).

SMR Turbine Control

Although the above figures indicate that turbine power and torque vary with both turbine and wind speed, it is the manipulation of the SMR duty-cycle that has allowed the turbine speed and power to vary. The SMR output power is hence examined as a function of duty-cycle. This is shown in Figure 3.22 for the various estimated wind speeds mentioned above. The dashed line represents an artificial *rated* wind speed, which corresponds to the peak SMR output power at a wind speed of 4.8m/s. Note that this wind speed is required to demonstrate the SMR's ability to limit power beyond rated wind speed. The

figure clearly shows that the SMR can maximise and limit its output power at different wind speeds, by adjusting the SMR duty-cycle.

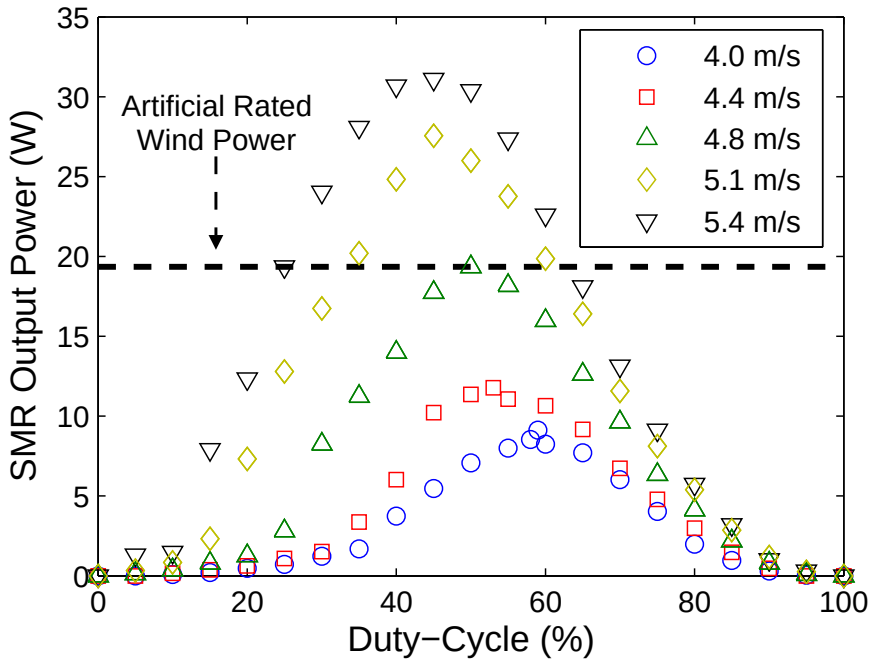


Figure 3.22: Measured SMR output power vs. duty cycle, for the various low wind speeds available. The dashed line represents an artificial *rated* wind speed, which corresponds to the peak SMR output power obtained at an equivalent wind speed of 4.80m/s.

In addition, the turbine speed is shown to be controlled by adjusting the duty-cycle for various wind speeds. This is seen in Figure 3.23, which shows the turbine speed is nearly linearly proportional to the duty-cycle, at high duty-cycles. However, this speed tends to level off as the duty-cycle approaches 0%. This occurs as the DC link voltage is higher than the rectified generator back-EMF voltage, i.e. current and hence electrical power will not flow from the turbine to the voltage-source load. This was previously seen in the dynamometer testing section (see Section 3.2.2) for the 200 and 400rpm cases, where it was found that the generator must operate at a minimum speed of about 500rpm to transfer power to the SMR for a duty-cycle of 0%. The maximum turbine speed is 438rpm, which indicates that the SMR output power will be zero for a duty-cycle of 0% for all test wind speeds. This is verified in Figure 3.22, under which condition, the turbine will operate at its no-load speed.

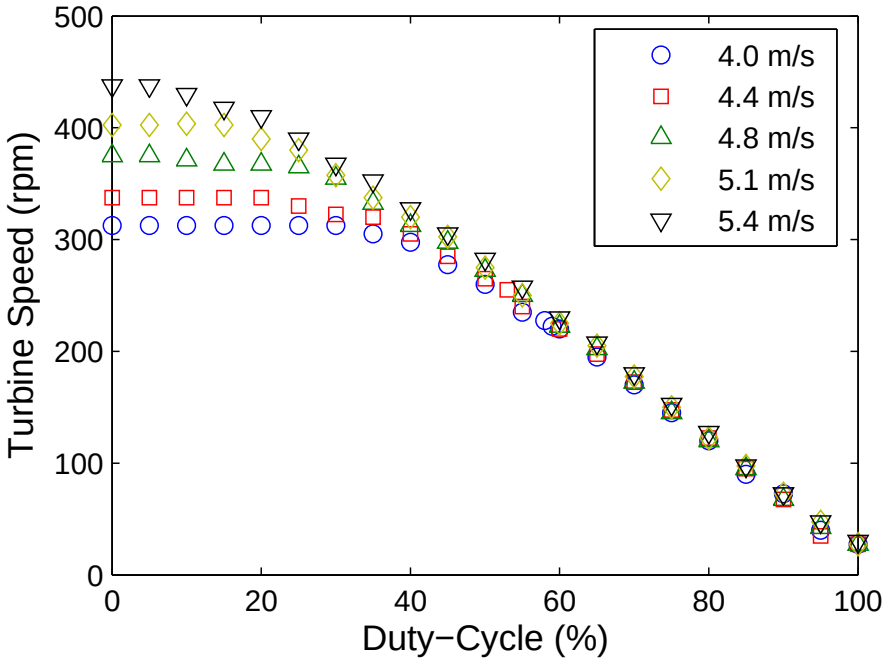


Figure 3.23: Measured turbine speed vs. duty-cycle, for the small range of low equivalent wind speeds.

3.3.4 Comparison of Control Modes

It has been demonstrated that the turbine power, torque and speed, and SMR output power can be controlled by adjusting the SMR duty-cycle. The results, however, are obtained from open-loop testing and do not demonstrate the SMR's ability to limit SMR and turbine power beyond rated wind speed. This is due to the available low equivalent wind speeds wind, and hence, an artificial rated wind speed of 4.80 m/s is selected to demonstrate the desired control principle. The corresponding rated SMR output power is 19.4W, which was shown by the dashed line in Figure 3.22.

Two control modes (CM) are examined here. The first (CM 1) maximises the SMR output power for all wind speeds, whilst the second (CM 2) limits the SMR output power to its rated value beyond rated wind speed. The corresponding SMR duty-cycle vs. wind speed plot is shown in Figure 3.24, for both control modes. The dashed line in the figure represents rated wind speed. The data is mainly measured, however, some points for CM 2, are interpolated from Figures 3.20–3.23. Consider CM 1, the duty-cycle corresponding to maximum SMR power is shown to decrease nearly linearly with wind speed. This is expected as the turbine speed that corresponds to maximum c_p and hence turbine power increases linearly with wind speed, whilst the rectifier voltage corresponding to maximum

DC power increases with turbine speed (recall Figure 2.25). Therefore, maximum power is extracted from the SMR by linearly increasing the rectifier voltage (duty-cycle) with wind (and hence turbine) speed.

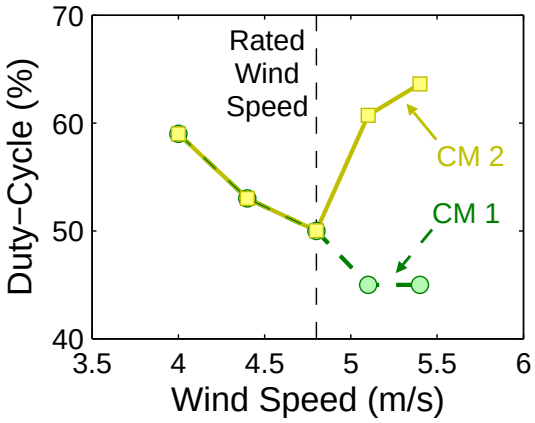


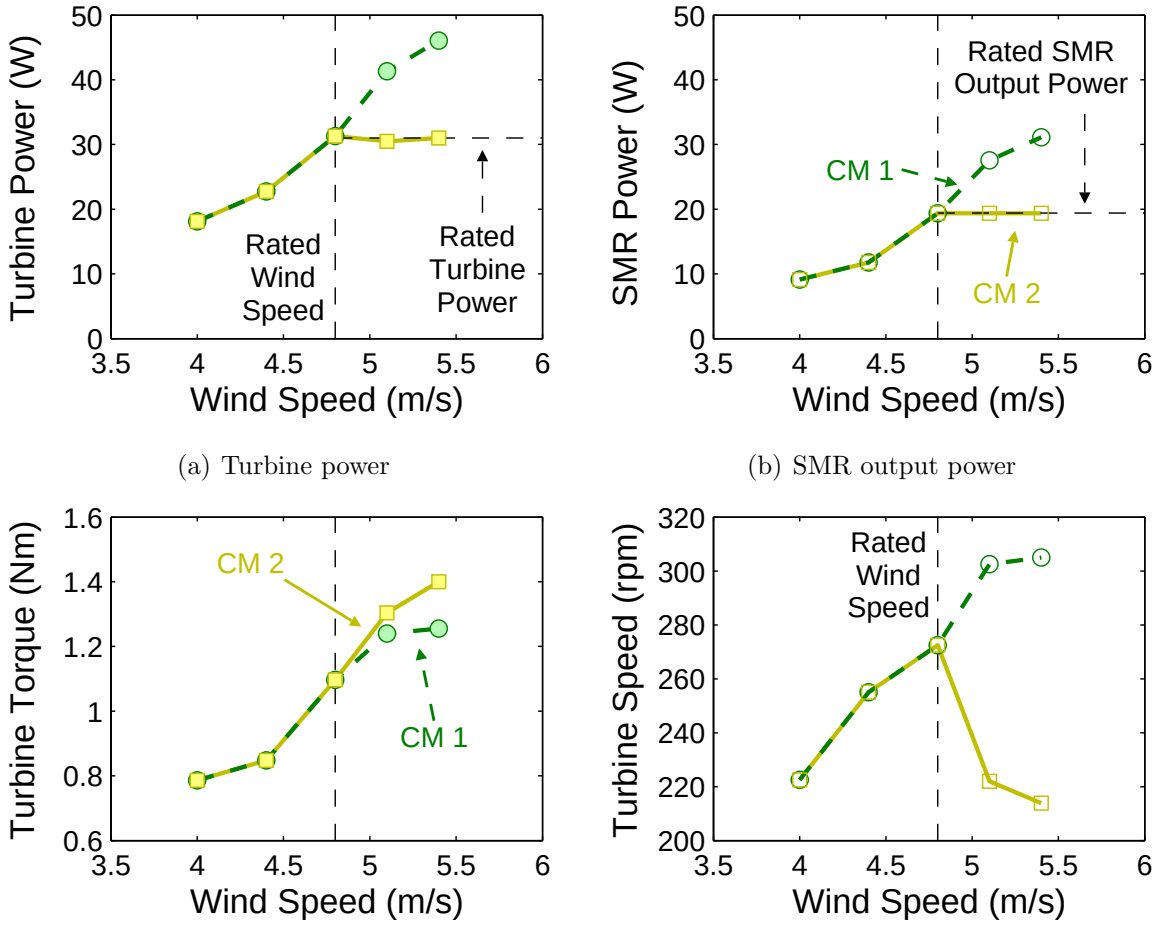
Figure 3.24: Measured duty-cycle vs. wind speed comparison of both control modes (CM). CM 1 aims to maximise power for all wind speeds, whilst CM 2 limits power beyond rated.

In contrast, the duty-cycle of CM 2 sharply increases beyond rated wind speed. This is expected as the turbine must reduce its speed to maintain rated power. This is achieved by increasing the duty-cycle beyond the maximum power point, which increases the generator torque. This concept was previously shown in Figure 3.23, and is also clearly seen in Figure 3.25, which shows the turbine and SMR performance characteristics, i.e the turbine power, SMR output power, turbine torque and speed as a function of wind speed, for both control modes. The vertical dashed lines represent rated wind speed (4.8m/s), whilst the horizontal dashed lines of Figures 3.25(a) and 3.25(b) represent rated turbine and SMR output powers, respectively. Note that the turbine torque and power graphs of Figure 3.25 are calculated, whilst the SMR output power and turbine speed graphs are measured. The solid and dashed lines simply connect the data.

Control Mode 1 - Power Maximisation

Consider CM 1 in Figure 3.25. Recall that the turbine speed corresponding to maximum power ideally increases linearly with wind speed, whilst the turbine torque and maximum power increases with the square and cube of wind speed, respectively. This is verified by the CM 1 plots in Figure 3.25, with the exception of the highest wind speed. The graphs indicate the calculated equivalent wind speed of 5.4m/s is larger than expected, which is likely caused by the non-ideal test facility and experimental errors. Despite this, the

SMR output power is shown to continually increase with wind speed. Its shape resembles that of the turbine power vs. wind speed plot, indicating a relatively constant generator and SMR power loss.



(a) Turbine power

(b) SMR output power

(c) Turbine torque

(d) Turbine speed

Figure 3.25: Measured turbine and SMR operating characteristics for both control modes (CM), showing (a) turbine power, (b) SMR output power, (c) turbine torque, and (d) turbine speed vs. wind speed. CM 1 maximises the SMR power for all wind speeds, whilst CM 2 limits it (to rated power) above rated wind speed (4.80 m/s). The vertical dashed line represents rated wind speed, whilst the horizontal dashed lines represents rated power. Note that the solid and dashed lines simply connect the data.

Control Mode 2 - Constant Power

Consider the second control mode (CM 2) in Figure 3.25. The turbine speed, torque and power is identical to that of CM 1 for wind speeds below rated, however, these differ for wind speeds above rated. The turbine torque torque is increased to reduce the speed and

hence limit the turbine and SMR output powers. The turbine and SMR powers are shown to be maintained at rated values for wind speeds above 4.80 m/s (rated). Although this control mode successfully demonstrates both the power maximisation and power limiting modes, as required, the SMR was controlled in an open-loop fashion. A closed-loop version of this control algorithm must be implemented, such that the SMR maximises power, below rated wind speed, and limits power (and turbine speed) above rated wind speed, autonomously.

SMR and Generator Efficiency

The estimated SMR and generator (total) efficiency is plotted as a function of SMR output power in Figure 3.26, for the available low equivalent wind speeds. The peak efficiency increases from about 50% at a wind speed of 4.0 m/s to 70% at a wind speed of 5.4 m/s. This occurs as the generator and SMR power losses are most significant at low powers (wind speeds). These losses appear fixed (deduced from Figures 3.25(a) and 3.25(b)), and should become less significant as the SMR output power (wind speeds) increase. Each wind speed has two efficiency vs. SMR power plots, which meet at the peak SMR power, this occurs as the same DC power can be obtained for two different

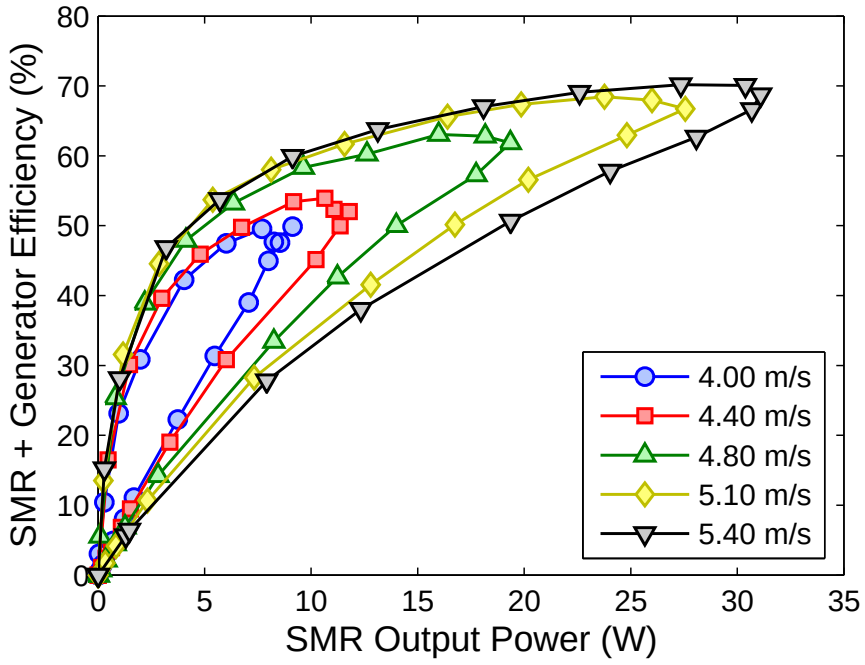


Figure 3.26: Estimated SMR and generator efficiency vs. SMR output power, for equivalent wind speeds of 4.0–5.4m/s.

rectifier currents / voltages. The higher of the two efficiency plots corresponds to the higher rectifier voltage (lower current) case, as previously seen with the DC generator and total (generator + SMR) efficiency vs. power curves, i.e. Figures 2.28 and 3.15, respectively.

3.4 Chapter Summary

The use of a SMR allows the rectifier output voltage to be controlled as it is proportional to the DC link output voltage and duty-cycle. This allows power to be transferred from the generator to the load at low speeds, which is not possible using an uncontrolled rectifier. Output power can be generated for a given speed, providing the rectifier voltage is set below the generator's rectified back-EMF voltage. This was experimentally verified using the dynamometer which saw that power was extracted for only a limited range of duty-cycles at low generator speeds. In contrast, power was obtained at any duty-cycle at high speed, as the rectified back-EMF voltage exceeds the DC link voltage.

The SMR output current is linearly proportional to the input current and SMR duty-cycle, allowing simple output current control when using a constant-current input source. The generator, however, only behaved as a near ideal constant-current source at the higher tested generator speeds where the back-EMF voltage significantly exceeded the DC link (SMR output) voltage. The machine's ability to provide a constant current output decreased with generator speed and back-EMF voltage. At a given generator speed, the duty-cycle can be controlled to maximise the SMR output current and hence output power. The duty-cycle corresponding to the peak output power is linearly proportional to the generator speed. This relationship also applies to the generator torque, however, the range of duty-cycles for which this (and the power can be maximised) applies, varies with the DC link voltage.

For a constant generator speed, the SMR DC output power vs. duty-cycle curve is shown to be the mirror image of the uncontrolled rectifier DC output P-V locus, as the rectifier output voltage is proportional to the complement of the duty-cycle $(1-d)$. Similarly, the torque vs. duty-cycle curve, for the lowest generator speed, appears as the mirror image of the short-circuit torque characteristic. The speed range for which the SMR output power can be maximised corresponds to the boost rectifier region, whilst the SMR operates as a current chopper for higher generator speeds. The range of speeds corresponding to each mode of operation varies with DC link voltage.

The SMR's ability to control the test wind turbine was demonstrated using a small wind tunnel. Despite the severe limitations of the available test facility used, it was demonstrated that the turbine power, torque and speed could be controlled by adjusting the duty-cycle. The turbine control requirements, such as power maximisation and speed reduction etc., were successfully demonstrated using an artificially reduced value of rated wind speed under open-loop conditions.

The wind turbine blade characteristics were estimated based on the wind tunnel testing. The c_p curves, calculated for each wind speed, did not agree in magnitude, however, matched in shape. The estimated wind speeds were then adjusted such that each c_p curve agreed in both shape and magnitude. This resulted in a low range of equivalent wind speeds, ranging from 4.0 to 5.4m/s, and hence a *rated* wind speed of 4.8m/s was used.

The turbine speed was found to vary in proportional to the duty-cycle, and to be independent of wind speed at high duty-cycles. In contrast, the turbine speed reached a limiting value at low duty-cycles, as the resulting rectifier voltage exceeded the generator's rectified back-EMF voltage, i.e. power did not flow from the generator to the load. The generator was hence open-circuited and rotated at a speed governed by the wind speed and the generator no-load torque (open-circuit power loss).

Part II

Investigation of Grid-Connected Inverter based on Switched-Mode Rectifier Topology

Chapter 4

Simulation and Test of 150W Grid-Connected Inverter

This chapter introduces the principles and features of a grid-connected inverter. This is followed by the design and discussion of a novel 150W current source grid-connected inverter topology that is based on a high-inductance PM generator and rectifier acting as a constant current source. The inverter concept is proved by computer-based simulations and experimental testing that considers both resistive and grid-connected loads. The constant current assumption and effect of grid parameter variations, e.g. grid voltage and inverter modulation index are investigated.

4.1 Introduction

The primary function of a grid-connected inverter (GCI) is to convert power from a renewable energy source, to an AC output that is directly fed to the utility grid. A general block diagram of a small scale grid-connected wind turbine is shown in Figure 4.1. The figure also shows the inverter output current, I_{inv}, and the grid voltage, V_g, where the grid voltage is in-phase with the inverter current. This operating condition is known as *unity power factor*, which maximises the active power fed to, and minimises the reactive power drawn from the grid. The grid is treated as an *infinite bus*, i.e. a fixed frequency constant voltage source, which is unaffected by any load or fault condition.

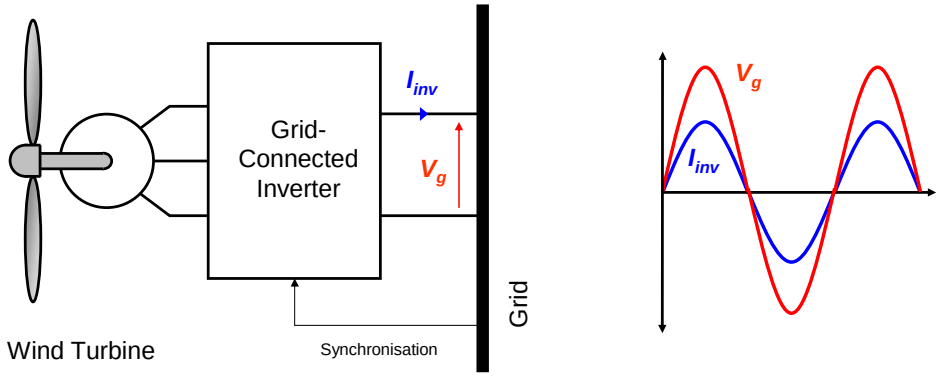


Figure 4.1: Simple block diagram of a small scale grid-connected wind turbine system (left), and the inverter output current, I_{inv}, and grid voltage, V_g, for unity power factor operation (right).

4.1.1 Inverter Requirements

Utility operators impose strict inverter power quality, power factor, direct current (DC) injection, and fault detection requirements. The grid-connected inverter is tested against the Australian Standards, using a power analyser [96]. The inverter must be shown to meet the standards before being made commercially available.

Power Quality

Nonlinear loads, such as adjustable-speed drives, arc furnaces, arc welders and fluorescent lights, draw non-linear currents which contain harmonics. These harmonic currents produce corresponding voltage harmonics and cause the supply voltage waveform to be distorted [97]. Excessive supply voltage distortion can affect the operation of sensitive loads, such as computers. Due to this, there are grid standards in place, e.g. the IEEE standard 519-1992 for utility operators and end users, and the Australian Standard (AS) 4777.1–3 for grid-connected inverters. Note that the THD requirements of AS 4777.2 are identical to those of IEEE standard 929-2000 [96].

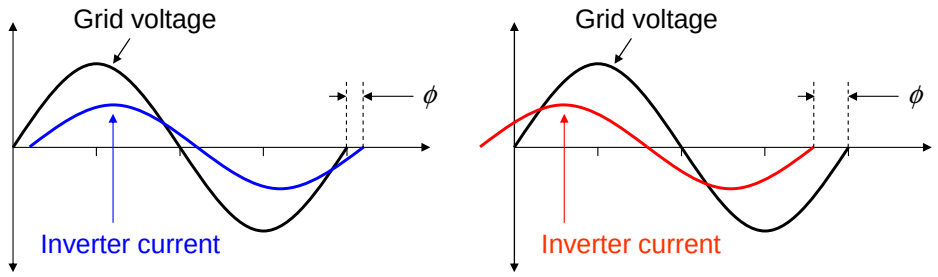
The Australian Standard 4777.1–3 covers grid-connection of energy systems via inverters. According to AS 4777.2 the grid-connected inverter must meet mandatory total harmonic distortion (THD) requirements. The current must contain less than 5% THD, up to and including the 50^{th} harmonic, as listed in Table 4.1. Although the grid voltage must also meet strict harmonic limits, the majority of grid-connected inverters control only the output current and hence are not required to monitor the output voltage harmonic distortion.

Table 4.1: Current harmonic limits of Australian Standard 4777.2 [96]

NOTE:
This table is included on page 119 of the print copy of the thesis held in the University of Adelaide Library.

Power Factor

The power factor angle, ϕ, refers to the phase angle of the current waveform, with respect to the voltage waveform. The power factor is defined as the cosine of the power factor angle, and is leading if $\phi > 0°$ (current waveform leads the voltage waveform), and lagging if $\phi < 0°$ (current waveform lags the voltage waveform). The AS 4777.2 specifies that the inverter must deliver a high quality current waveform at a power factor between 0.8 leading and 0.95 lagging, for inverter outputs between 20 to 100% of rated volt-amperes [96]. These power factors are illustrated in Figure 4.2, which shows a lagging power factor of 0.95 in Figure 4.2(a) and a leading power factor of 0.8 in Figure 4.2(b). Note that the power factor requirement considers the inverter as a load from the perspective of the grid [96].



(a) Lagging current (b) Leading current

Figure 4.2: Example of (a) 0.95 lagging and (b) 0.80 leading power factors, where $\phi = -18.2°$ and $\phi = +36.9°$, respectively.

Direct Current Injection

Injection of DC currents into the AC utility grid is not desirable as this can cause saturation and hence overheating of utility distribution transformers. The Australian Standard 4777.2 requires that a grid-connected inverter does not inject more than 0.5% of rated current or 5mA of DC current (whichever is greater) in to the grid [96]. The use of a line frequency a transformer between the grid and inverter avoids this problem, however, is undesirable due to its cost, size and weight issues, as previously seen in Section 1.5.4.

Fault Detection

Aside from inverter controlled parameters such as output power quality, power factor and DC injection, the grid-connected inverter must also be able to detect a range of grid faults. These faults include under / over voltage, under / over frequency and islanding. The inverter is required to disconnect itself from the utility grid within two seconds of such a fault [98]. Fault detection is beyond the scope of this research.

4.1.2 Desirable Features

Grid-connected inverters are designed to deliver a low distortion current to the grid at a high power factor, and in addition, be highly efficient and low cost [33, 99, 100]. The former were discussed in Section 4.1.1, whilst the latter are discussed below.

Cost

The cost of a GCI makes up a significant portion of the total cost of a small scale grid-connected wind turbine, and can discourage people from utilising wind power. Presently, a 1–7kW grid-connected inverter costs about AUS$1000 more than a similar sized stand-alone inverter, as previously shown in Figure 1.19. The excessive costs are associated with additional components and the overall complexity of the system. This research aims to design and develop a low-cost grid-connected inverter to encourage wind power utilisation.

It has been estimated that the small-scale wind energy market is growing at roughly 40% per year [18], and that annual sales, in the US alone, will be between US $27M and $57M by 2010 [19]; this value depends on factors such as government rebates and tax incentives etc. Within this market there is an increasing demand for low-cost grid-connected wind turbines, and it is expected that by 2020 small-scale wind turbines will provide 3% of the US electrical energy consumption.

Performance

The grid-connected inverter is the interface between the wind turbine and the grid, it hence has the responsibility of controlling the turbine torque and hence power. The grid-connected inverter should be designed such that power is extracted over a wide range of wind speeds, and that it is reliable and efficient.

1. General operation - The inverter should maximise turbine power below rated wind speed and maintain rated power above rated wind speed, in accordance with standard turbine practise. Improving the ability to extract power from the wind at low speeds is especially important as small-scale wind turbines suffer poor capacity factors, as they are typically located close to the local power demand. These turbines thus generally see lower average wind speeds compared to large (MW) wind turbines, whose siting is carefully chosen to optimise output power.

2. Reliability - The inverter should operate autonomously for long periods of time, e.g. years, without regular maintenance. Careful selection of inverter types and hence components may reduce the need for regular maintenance, e.g. a voltage source inverter requires the use of electrolytic (DC link) capacitors to regulate the input voltage. These are often large and bulky, as they have a limited life expectancy; this is mainly attributed to the electrolyte [101]. Current source inverters are generally more reliable than voltage source types as they do not use DC link capacitors.

3. Efficiency - Internal power losses are generally larger in current source inverters compared to voltage source types, as these inverters require a DC link inductor, which attracts copper losses. It is generally recognised that current source inverters are less efficient than their voltage source counterparts.

While both the current and voltage source inverters should be able to appropriately control a wind turbine, a reliability / efficiency trade-off exists. Despite this, the majority of purchased grid-connected inverters are the voltage source type; 81% of these are current controlled, whilst 19% control the output voltage [62]. Current control is more popular as high power factors can be obtained with simple control circuits, and transient current suppression is possible when disturbances, e.g. voltage changes, occur in the utility power system [62].

4.2 Proposed Concept

4.2.1 Inverter Overview

The proposed grid-connected inverter is based on a current source input. This is decided as i) a low-cost constant current source can be easily obtained using a high-inductance generator with a rectifier, and ii) the inverter output current can be linearly controlled using a single-switch converter, and without the need for a high-cost output current sensor or a fast feedback controller.

An equivalent block diagram of the proposed inverter is shown in Figure 4.3, along with the expected input and output currents of the four inverter stages, i.e. the *constant current source*, *current-wave shaper*, *unfolding circuit*, and *low-pass filter*. The inverter operates from an essentially constant input current, delivered by the PM generator and rectifier. The current wave-shaper and unfolding circuit stages are used to produce a unipolar PWM current, which is filtered and fed to the grid, via the low-pass filter. Each inverter stage is further discussed in the following sections.

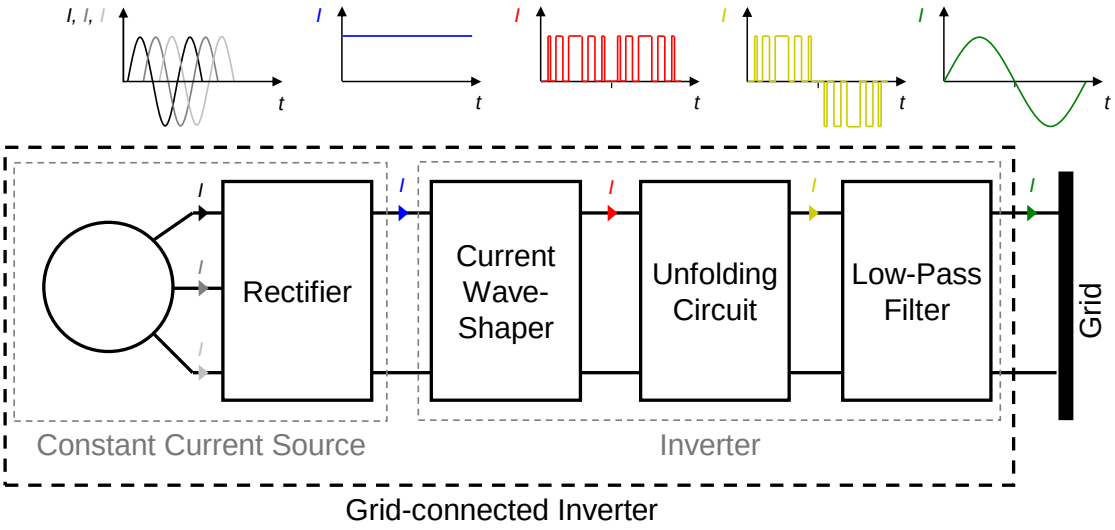


Figure 4.3: Overview of the proposed grid-connected inverter, showing the: rectifier, current wave-shaper, unfolding circuit and output filter. The output current of each stage is also shown. Note the input (machine) current is three-phase AC, of varying magnitude and frequency, which is speed dependent.

The inverter exploits the use of a high-inductance generator and rectifier to form the constant current source. The common DC link inductor (energy storage element) is therefore avoided, which will further reduce the cost and improve the overall efficiency.

4.2.2 Constant Current Source

The combination of the high-inductance generator and an uncontrolled rectifier, ideally provide the inverter with constant current. This arrangement and the idealised machine line and rectifier output currents are shown in Figure 4.4. This type of constant current source (CCS) is not reported amongst the literature, and forms the basis of the novel grid-connected inverter topology.

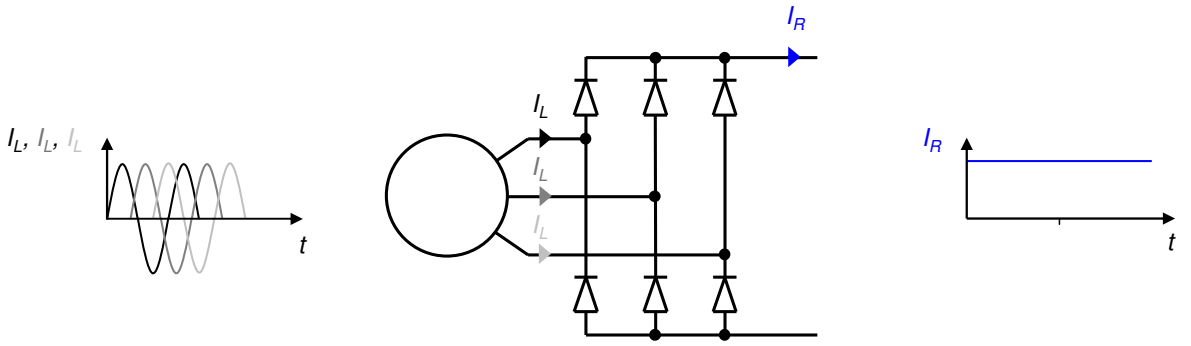


Figure 4.4: Constant current source, showing (left) the circuit, and (right) the ideal machine and rectifier output currents.

The rectifier output current, I_R, is expressed by Equation (4.1), where I_L is the RMS line current value. For example, a current source based on the same high-inductance PM generator that was used in part I, would deliver a maximum line current of about 16A$_{RMS}$, which corresponds to a DC (rectifier) output current of approximately 22A.

$$I_R = 1.35\, I_L \tag{4.1}$$

The lack of DC link inductor implies that the instantaneous inverter input and output powers must be equal. This is easily achieved using a 3ph inverter, as the summation of the instantaneous output powers is constant. However, this project focusses on a single-phase inverter whose instantaneous output power fluctuates at twice the grid frequency (the average power is constant). The inverter hence draws non-constant (pulsating) power from the generator, which causes the generator to vibrate [91] and the inverter input current and voltage to fluctuate at twice the grid frequency.

The fluctuating inverter input current contains harmonic distortion, which is ultimately seen in the output current. Despite this, the high-inductance generator and rec-

tifier act as a constant current source when the rectifier output voltage is much less than its open circuit voltage; a reasonable choice is 25%. This is seen experimentally in Section 4.4.2 and is analysed in Section 5.1. Feed-forward current compensation is examined in Section 5.4 to overcome this limitation. Note that the remaining inverter stages assume an ideal input current.

4.2.3 Current Wave-Shaper

The current wave-shaper (CWS) is essentially a high-speed switch and a reverse blocking diode, that shorts the input current to create a PWM chopped output current. The circuit, along with the ideal input and output currents, are shown in Figure 4.5. The output current, I_{out}, is the inverse of the PWM duty-cycle (control signal), d, as shown by Equation (4.2), where I_{in} is the input current.

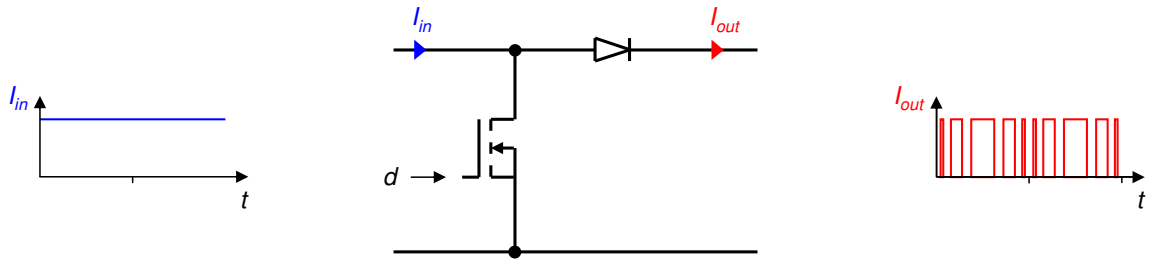
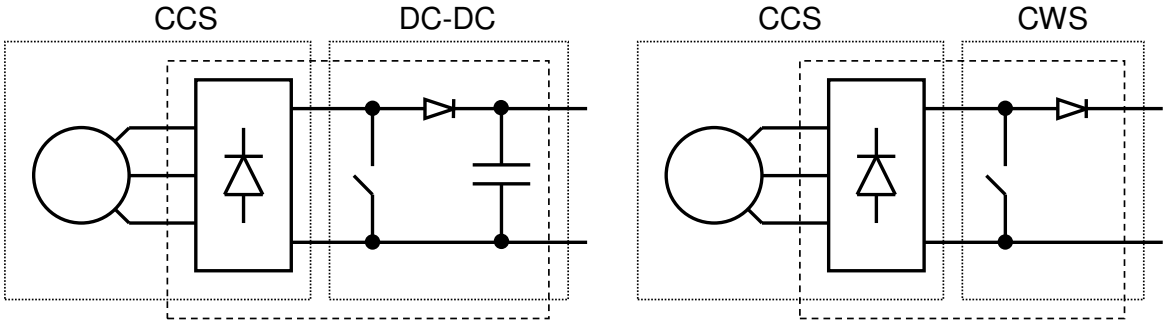


Figure 4.5: Current wave-shaper, and the input and output currents.

$$I_{out} = I_{in}(1 - d) \tag{4.2}$$

The combination of the constant current source and the current wave-shaper is the same as the SMR circuit and high inductance PM generator, previously examined as a DC-DC converter in part I. Both circuits make use of a reverse blocking diode, which prevents shorting the DC link capacitor, for the DC-DC converter case, and the grid for the inverter case. The key physical difference between the circuits is the removal of the DC link capacitor for the inverter application, which is summarised in Figure 4.6.

The modified SMR circuit is also controlled differently i.e. a time-varying duty-cycle is now applied to the high-frequency switch, as opposed to a constant duty-cycle for the DC-DC converter case. A comparison of the constant and time-varying duty-cycles is shown



(a) SMR for DC-DC converter (b) Modified SMR for inverter case

Figure 4.6: Comparison of (a) the switched-mode rectifier (SMR), and (b) modified SMR circuit, for use as a DC-DC converter and for the inverter, respectively. The SMR circuits are enclosed by the dashed boxes, whilst the dotted boxes of (b) show the constant current source (CCS) and the current wave-shaper (CWS) circuits. The key difference in (b) is the removal of the DC link capacitor.

in Figure 4.7. The combination of the new control signal and the removal of the DC link capacitor allows the proposed inverter to produce an AC output current that resembles that of a rectified unipolar PWM wave. This is converted into a unipolar PWM current by the unfolding circuit, and is then fed to the grid via the low-pass filter.

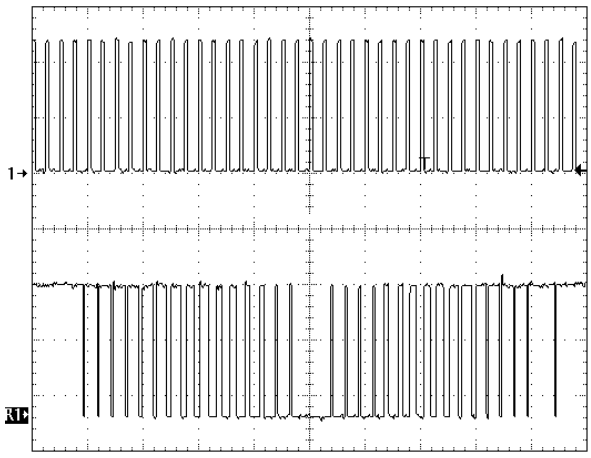


Figure 4.7: Comparison of the SMR control PWM duty-cycles, showing the (top) constant, and (bottom) time-varying signals, as used for the DC-DC converter and the inverter applications, respectively. The zero position for each waveform is shown by the arrow on the left; the vertical and horizontal scales are 2V and 2ms per division, respectively.

4.2.4 Unfolding Circuit

The unfolding circuit is essentially an H-bridge inverter. Its role is to *unfold* the input current at twice the grid frequency, ω_g, as summarised in Equation (4.3). The combination of this unfolding action and the CWS PWM switching, yield a unipolar PWM output current, whose fundamental frequency matches that of the grid. The unfolding circuit is built using low-cost thyristors and as shown in Figure 4.8, along with a demonstration of its unfolding action. The polarity is alternated by the correct triggering of opposing thyristors, e.g. THY 1 and THY 3 are triggered simultaneously to obtain a positive output current, whilst triggering THY 2 and THY 4 in unison, will cause the current to flow in the opposite direction.

$$I_{out} = I_{in} . \operatorname{sgn}\left[\sin(\omega_g\, t)\right] \tag{4.3}$$

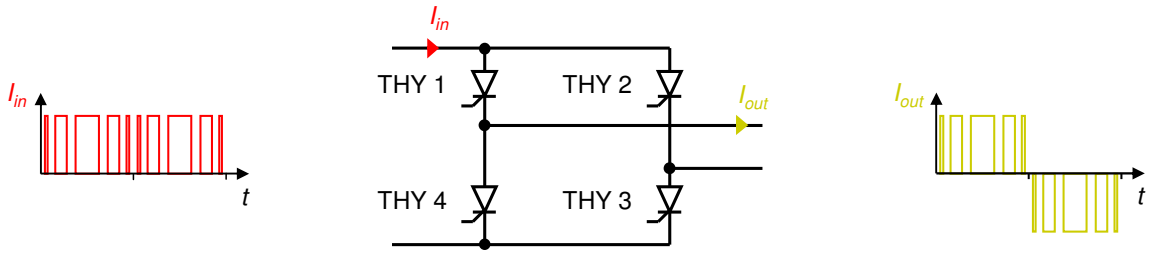


Figure 4.8: Unfolding circuit converter, and the input and output currents.

Thyristors are primarily selected, based on their low-cost. However, they also eliminate the need for series connected diodes, which are required for a current source H-bridge inverter, to block bi-directional voltages from the load and to allow uni-directional current flow [81, 102]. In addition, thyristors have a fixed voltage drop, and can hence reduce power losses in high voltage applications [103]. The drawback, however, is its inability to commutate (turn-off) when fed by a constant input current. A grid-connected current-fed thyristor H-bridge inverter will only commutate correctly if the load has a leading power factor [104]. To overcome these difficulties, the majority of grid-connected inverters and all PWM inverters force switch commutation. However, this attract additional circuitry, and increases the complexity and hence cost. The advantage of the proposed grid-connected inverter design is that the thyristors commutate naturally due to the nature of the wave-shaper output current, i.e. the current sufficiently falls below the thyristor holding current.

The drawback of this design is that the thyristors must now be triggered at the PWM switching frequency, which increases the inverter switching losses.

4.2.5 Low-Pass Filter

The low-pass filter is the final stage of the proposed gird-connected inverter. It is used to remove the high frequency PWM current components, whilst allowing the fundamental component to pass through to the grid. Figure 4.9 shows the low-pass filter required for a current source grid-connected inverter, and its expected input and output currents. Note that this capacitive-inductive (CL) filter differs from conventional second-order low-pass, i.e. inductive-capacitive (LC) filters, as the unfolding circuit output is essentially a current source, whilst the grid is effectively a voltage source. The *filter impedance mismatch criteria* states that the filter input impedance must hence be low and that its output impedance must be high, to correctly couple a high impedance current source and a low impedance voltage source (grid) [105].

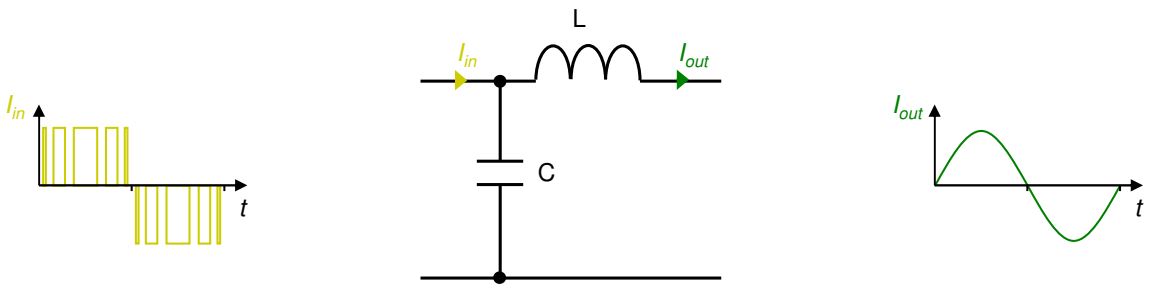


Figure 4.9: Inverter low-pass CL filter circuit, and the input and output currents.

4.3 Test Set-up, Implementation and Simulation

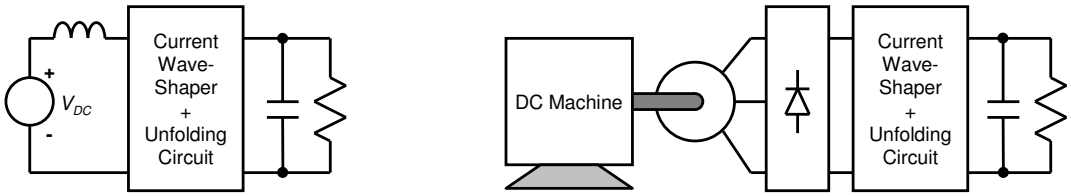
This section describes the inverter test arrangements, the PM generator current source, the power electronics and control hardware implementation, and the simulations used to validate the inverter concept and simulate inverter operation.

4.3.1 Dynamometer Test Arrangement

The dynamometer test-rig was used to drive the PM generator, which consists of a 5kW DC machine that is directly coupled to the PM generator. The PM generator acts as the inverter current source, and was rotated at constant speed to simulate inverter operation under steady-state wind conditions. Turbine speeds of 500 and 1,000rpm were selected as they represent turbine speeds at average and high wind speeds, respectively.

Proof of Concept

The inverter was initially designed, constructed and tested using a resistive / capacitive load. The circuit was tested first using an ideal current source, i.e. a DC voltage source in series with an inductor, and second using the high-inductance PM generator and rectifier acting as the current source. These test arrangements are summarised in Figure 4.10.



(a) Ideal current source set-up

(b) Dynamometer set-up

Figure 4.10: Preliminary resistive / capacitive load test arrangements, showing (a) the ideal, and (b) the PM generator current source test arrangements.

Grid-Connected Testing

Due to the use of a low-voltage generator, the inverter was grid-connected to an artificial (low-voltage) grid. This was achieved experimentally by using a 10A autotransformer, whose secondary voltage was varied between 5 and 20V_{RMS}. In addition, an isolation transformer was connected between the mains and the autotransformer for safety, as

shown in Figure 4.11. This figure shows the inverter arrangement as tested in the laboratory, which includes a resistive load, R_L and two switches, *SW1* and *SW2*, which are used to make the transition from resistive to grid-connected loading (the synchronisation procedure is explained at the end of this section). The transformers conveniently provide leakage reactance and resistance to assist with filtering. However, these parameters vary with turns ratio and are hence enclosed within the dashed box of Figure 4.11.

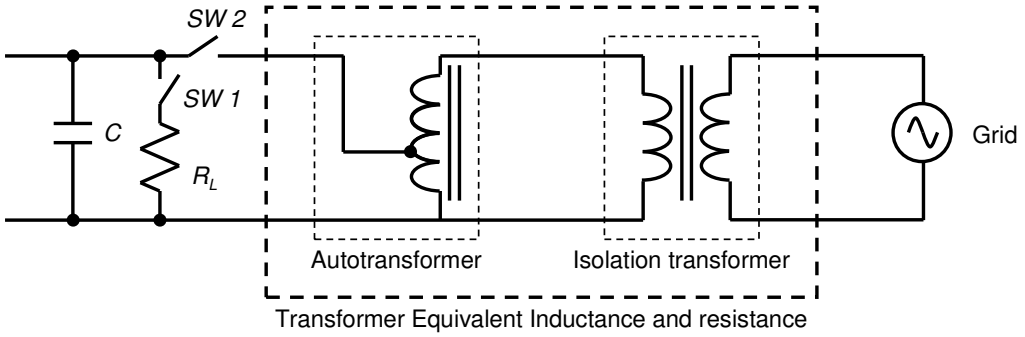


Figure 4.11: Grid-connected inverter test arrangement, showing the use of an isolation and autotransformer. The current source is not shown, however, it is achieved using the PM generator and rectifier, using the dynamometer test-rig.

The variable transformer parameters are approximated by an equivalent inductance, L_{eq}, and resistance, R_{eq}, which are expressed by Equations (4.4) and (4.5), respectively. Note that $R_1\,n^2$ and $L_1\,n^2$ represent the variable resistance and inductance of the autotransformer, where n represents the turns ratio. Similarly, R_2 and L_2 represent the fixed resistance and inductance of the isolation transformer. The equivalent (combined) transformer inductance and resistance is shown in Figure 4.12.

$$L_{eq} = L_1\,n^2 + L_2 \tag{4.4}$$

$$R_{eq} = R_1\,n^2 + R_2 \tag{4.5}$$

The equivalent transformer inductance and resistance was experimentally measured, for a number of autotransformer turns ratios. These were obtained using a second autotransformer to perform a short-circuit test on the first one. The results are expressed as a function of autotransformer output voltage, and are shown in Figure 4.13. The points represent the calculated data, whilst the lines correspond to fitted curves. Both fitted curves are quadratic, which is expected as both L_{eq} and R_{eq} have a variable term that is proportional to n^2.

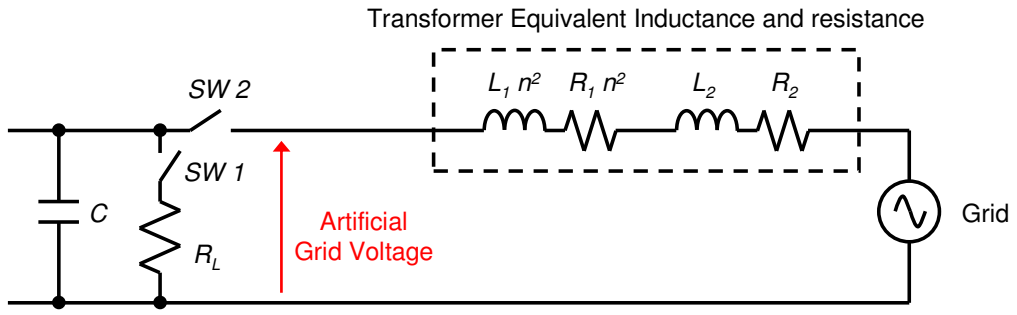
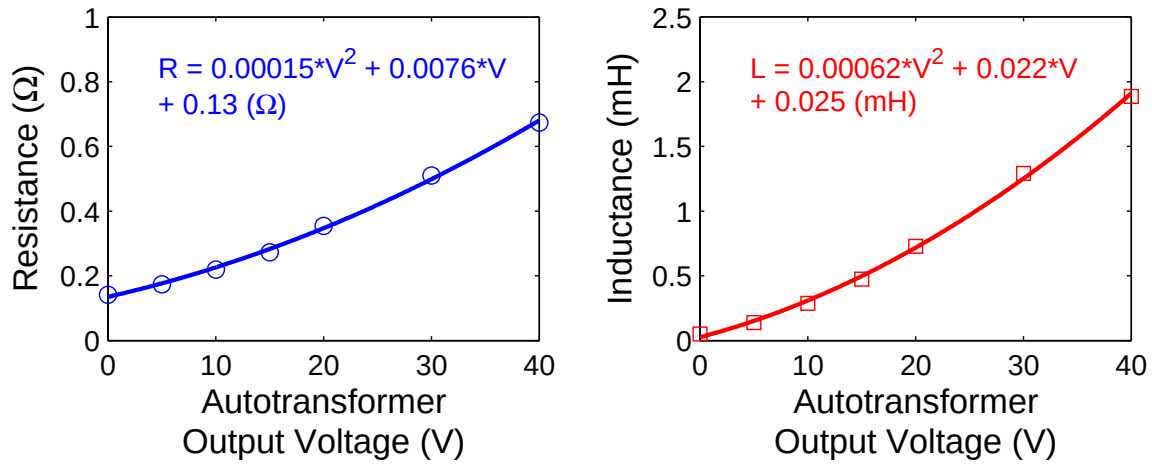


Figure 4.12: Equivalent circuit for test arrangement, showing the isolation and autotransformer leakage inductance and resistance inside the dashed box.



(a) Resistance

(b) Inductance

Figure 4.13: Measured transformer equivalent (a) resistance, and (b) inductance vs. autotransformer output voltage. Each subfigure includes a fitted curve, and its quadratic equation.

Synchronisation Procedure

The inverter was synchronised to the grid using the procedure listed below:

- Close switch 1, open switch 2 - before the inverter is powered on.
- Power the inverter - and rotate the PM machine at the desired speed.
- Synchronise the inverter to the grid - by adjusting the load resistance or the inverter modulation index until the voltage drop across R_L and the artificial grid is synchronised (both in phase and magnitude).

- Close switch 2 - the resistor is effectively connected to the grid and the inverter.
- Open switch 1 - such that the inverter is now grid-connected

Note that care must be taken when loading the current source inverter, as one switch must remain closed at all times to provide a current path. In the event that both switches are opened, the inverter output voltage will significantly increase which may damage the inverter components. This voltage increase is caused by both the high generator open-circuit voltage and the voltage boosting action of the un-loaded modified SMR.

4.3.2 Constant Current Source - PM Generator

The test PM machine selected is the same as that investigated in Chapter 2. This machine is again used because of its high inductance, which is due to the use of a concentrated stator winding, and its torque rating, which is consistent with a several hundred watt wind generator. The test machine is shown again in Figure 4.14, for convenience.

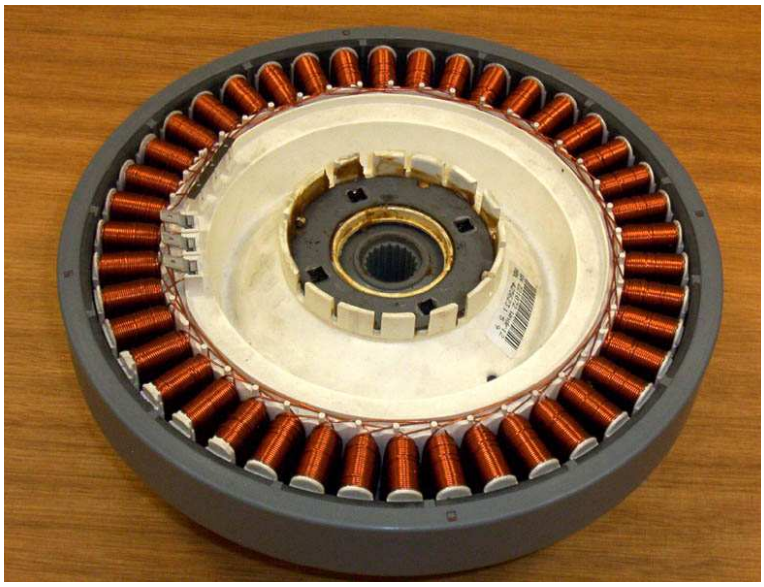


Figure 4.14: Photograph of an outer-rotor Fisher & Paykel PM generator.

The generator was tested over a range of speeds using the dynamometer test-rig. A summary of the PM machines's generating capability is shown in Figure 4.15, which shows the measured and simulated DC output current versus DC output voltage characteristics (DC I-V locus). This was measured at various speeds when operating into a resistive load

through a three-phase rectifier. The simulated results are obtained using PSIM® and are based on the machine parameters shown in Table 4.2. The calculated results show a good correspondence with the experimental results and give confidence in the simulation model. It is seen that the generator is a reasonable approximation to a constant-current source at high generator speeds and low DC output voltages.

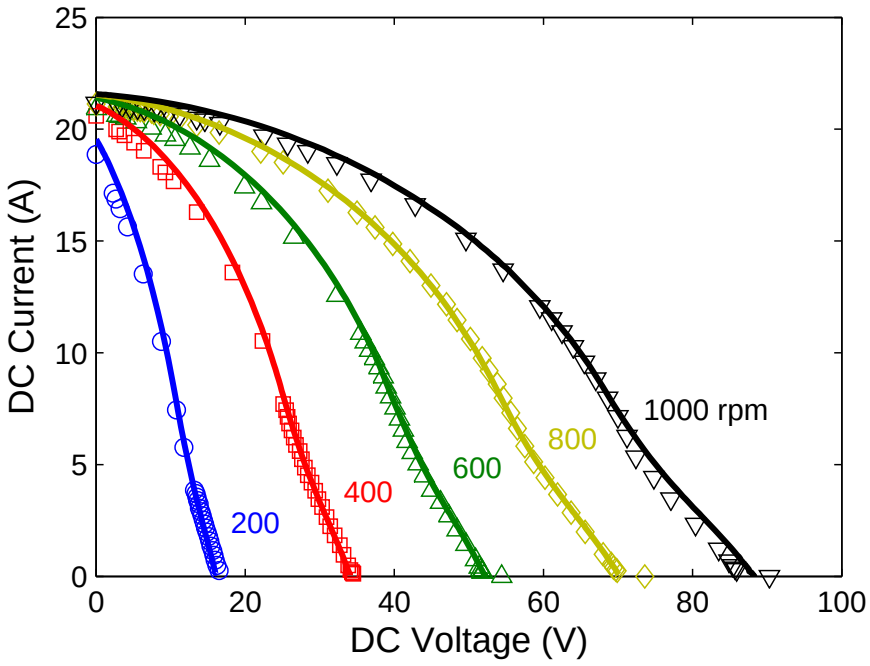


Figure 4.15: Current-Voltage locus of PM generator. The solid lines represent PSIM® simulations, whilst the points represent measured experimental data.

Table 4.2: Measured PM generator properties.

Parameter	Value
Stator Connection	Delta
Pole Pairs	24
Maximum Speed Tested	1000 rpm
SC Line Current (max. speed)	16 A_{RMS}
Back-EMF Constant, k	0.0668 V/rpm
Phase Inductance, L_{ph}	2.87 mH
Phase Resistance, R_{ph}	0.519 Ω

4.3.3 Power Electronics and Control Implementation

The proposed grid-connected inverter was constructed using a line frequency, three-phase uncontrolled rectifier, a high-current MOSFET and high-current thyristors. Note that the generator stator currents are continuous at high speeds, and hence the rectifier does not need a high-frequency switching capability. In addition, the thyristors and MOSFET are rated at 40A, despite an expected maximum rectifier output current of 22A, i.e. this provides some safety margin. Sections of the grid-connected inverter hardware, including the power electronic components and microcontroller are shown in Figure 4.16.

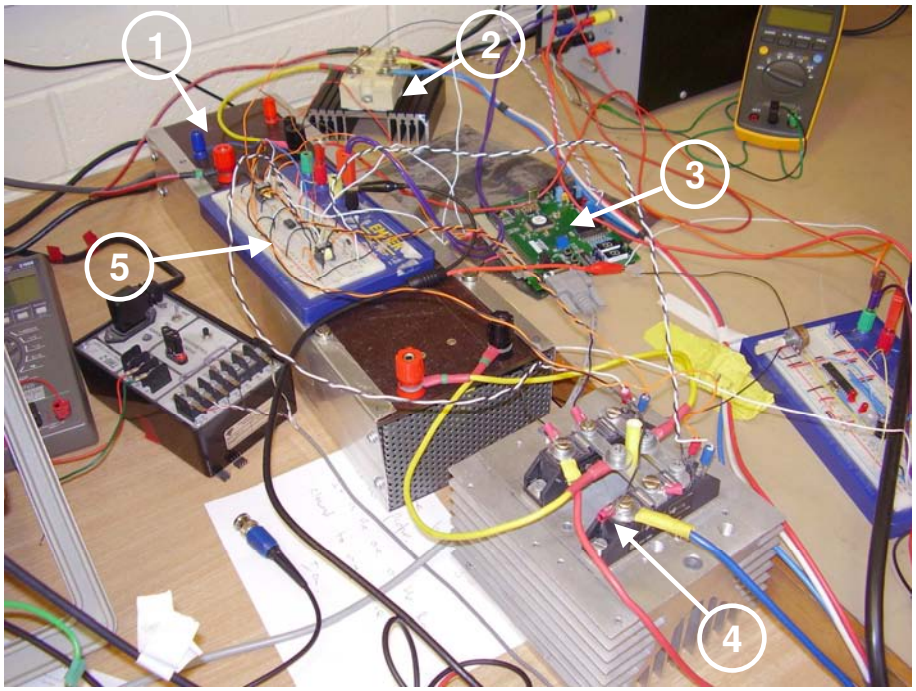


Figure 4.16: Photograph of power electronic components of the grid-connected inverter, showing (from top left and moving clockwise): ① the current wave-shaper, ② the full-bridge 3ph rectifier, ③ the microcontroller, ④ the unfolding circuit, and ⑤ the necessary MOSFET and thyristor gate drivers.

The inverter is controlled by a 16 bit Mitsubishi MSA0654A microcontroller in an open-loop manner. The zero-crossings of the grid voltage are used to generate the current wave-shaper PWM signal and thyristor trigger pulses. The PWM switching frequency is set to 4 kHz, as this is a reasonable trade-off between inverter switching losses and output quality, both of which are proportional to switching frequency. The PWM signal is based on a duty-cycle look-up-table whose pointer is reset at positive grid zero-crossings, which ensures that the unfolding circuit output current is in-phase with the grid voltage. The use

of a look-up-table is recommended in [106], as this improves power quality characteristics of the distribution network. The same reference explains that some inverters sample the grid voltage for their current reference. The resulting output current, of such inverters, hence contains the same distortion found in the grid voltage.

The look-up-table stores a normalised 180° conduction sinusoid, which corresponds to a modulation index, m_a, of 100%. The inverter output current magnitude and power is controlled by reducing the modulation index, which effectively increases the current wave-shaper PWM duty-cycle. The adjusted duty-cycle, d_a, is expressed by Equation (4.6), where d_i represents the stored duty-cycles.

$$d_a = 100 - m_a + \frac{(m_a \times d_i)}{100} \tag{4.6}$$

The microcontroller is programmed using the *C* language, and makes use of both software and hardware interrupts. A simplified overview of the microcontroller hardware and its software flow-chart is shown in Figure 4.17, and a copy of the code can be found in appendix C.2. Note that the thyristors trigger signals are synchronised to the falling edge of the CWS MOSFET control signal, and that the MOSFET is effectively shorted for two pulse widths before the zero-crossing to ensure thyristor commutation.

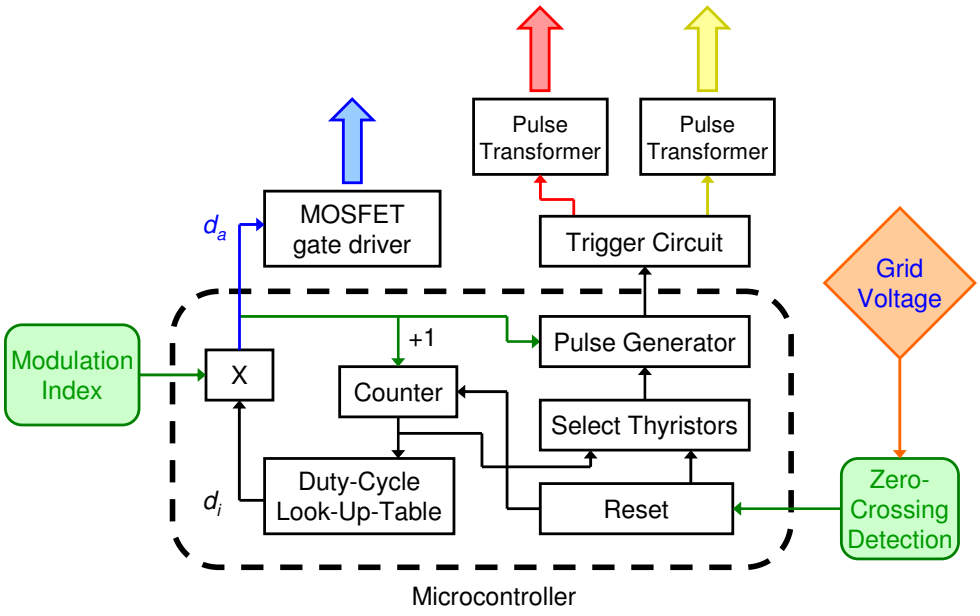


Figure 4.17: Overview of the Microcontroller hardware, and software flow chart. The large arrows represent control signals that are used to drive the semiconductor switches, whilst the shaded boxes represent microcontroller interrupts.

4.3.4 Inverter Simulation

The power electronic simulation tool PSIM®, was used to simulate the grid-connected and resistive load testing of the proposed inverter. The software is again used as it has previously modelled the PM generator loaded by a rectifier and resistive load, and operating with a switched-mode rectifier, with high accuracy. The PSIM® model of the grid-connected inverter is shown in Figure 4.18. Various components of the hardware are shown in the figure, including the PM generator, full-bridge rectifier, current wave-shaper, unfolding circuit, low-pass filter and the artificial (low-voltage) grid. Control components, such as the PWM duty-cycle look-up-table generator, modulation index controller and the zero-crossing detector, are also shown. Note that the reverse-blocking diode of the CWS is a carry-over from the SMR design and it is not strictly required due to the reverse-blocking capability of the thyristors. Despite this, the diode is incorporated into the simulation model and the inverter hardware, as it is used for testing purposes. In practise, the diode should be able to be removed without affecting the inverter's performance.

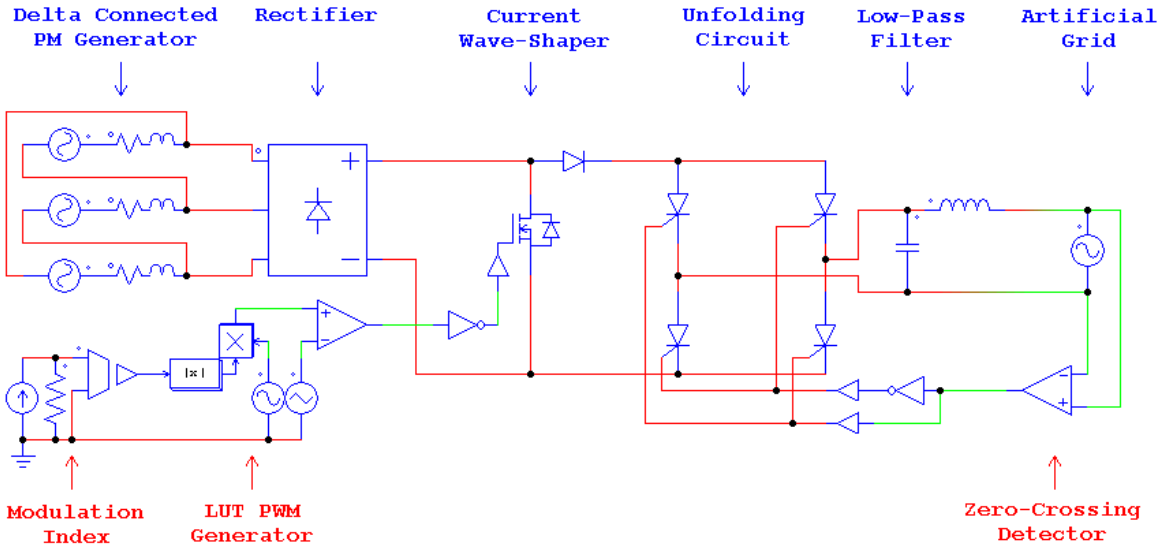


Figure 4.18: PSIM® grid-connected inverter model, showing the hardware and control components. Hardware components include the delta-connected PM generator, the full-bridge 3ph rectifier, current wave-shaper, unfolding circuit, low-pass filter and the artificial grid; control components include the PWM duty-cycle look-up-table generator, modulation index controller, and the zero-crossing detector.

The proposed grid-connected inverter is accurately modelled in PSIM®. The machine is modelled by three delta-connected voltage sources, with each phase containing series inductance and resistance equal to the values specified in Table 4.2. The back-EMF and

machine frequency is set for each turbine / generator speed. The semiconductor devices are also accurately modelled, i.e. the thyristor, reverse blocking diode and full-wave 3ph bridge rectifier voltage drops are included, as is the *on-resistance* of the MOSFET, and the latching and holding currents of the thyristors. This information is summarised in Table 4.3, and together with the machine modelling should result in simulations that closely match the experimentally measured data.

Table 4.3: Semiconductor properties.

Component / Property	Bridge Rectifier	MOSFET	Diode	Thyristors
Manufacturer	SEMIKRON	IR	IR	RS
Part Number	SKD230/16	IRFP150N	70HFLR	262-602
Rating	230A, 1600V	42A, 100V	70A, 1000V	40A, 1200V
Forward Voltage Drop	1V per diode	-	1.85V	1.95V
On Resistance	-	0.036Ω	-	-
Latching Current	-	-	-	0.6A
Holding Current	-	-	-	0.25A

Note that IR denotes International Rectifier.

Proof of Concept

The inverter concept is initially simulated using the PM generator as a current source, and a resistive / capacitive load. The generator is simulated at 500rpm, as this is the expected turbine speed under average wind speed conditions, for an arbitrarily selected load combination of 0.93Ω and 2,000μF. Various inverter current waveforms are shown in Figure 4.19, which prove the simulated inverter concept. The waveforms include the inverter input, and the current wave-shaper, unfolding circuit and filter output currents.

Modulation Index Variation

The effect of the inverter modulation index, m_a, variation is shown in Figure 4.20, for m_a equal to 100, 50 and 25%. It is seen that the output current magnitude is directly proportional to m_a, and hence the output power is proportional to m_a^2. This applies only to the resistive load case, as both the output current and voltage are dependent on m_a, whereas the power is only proportional to m_a, for the grid-connected case, as the inverter output (grid) voltage is fixed.

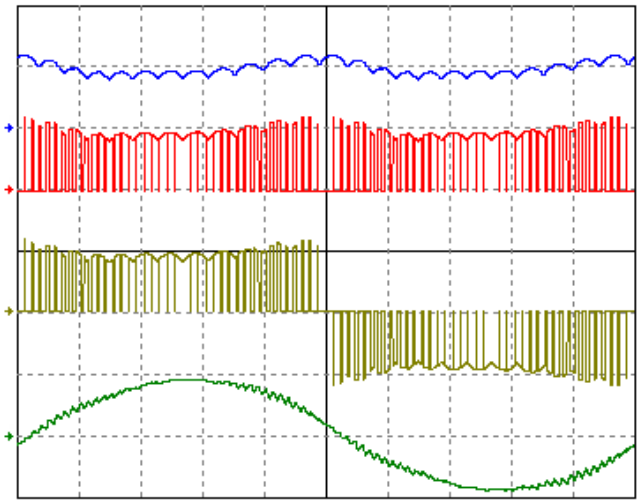


Figure 4.19: Preliminary PSIM® simulation proving the grid-connected inverter concept. The waveforms shown are the rectifier, current wave-shaper, unfolding circuit and filter output currents, from top to bottom, respectively. The zero position for each waveform is shown by the small arrow on the left. The vertical and horizontal scales are 20A and 2ms per division, respectively.

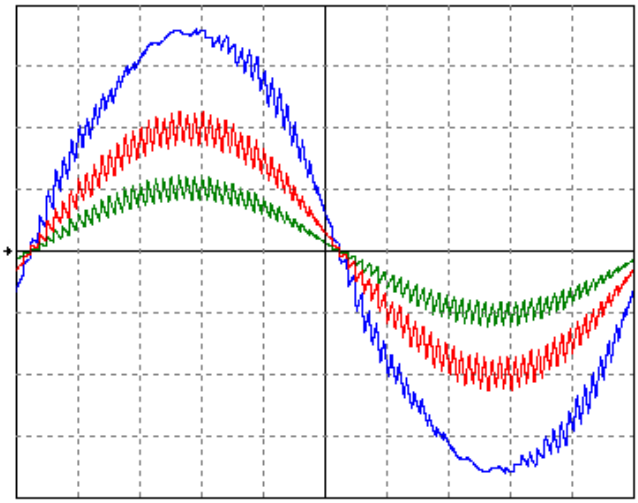


Figure 4.20: Simulated effect of modulation index, m_a, variation on inverter operation with resistive load. The resistive load currents for m_a equal to 100, 50 and 25% are shown. The vertical and horizontal scales are 5A and 2ms per division, respectively.

4.4 Experimental Testing

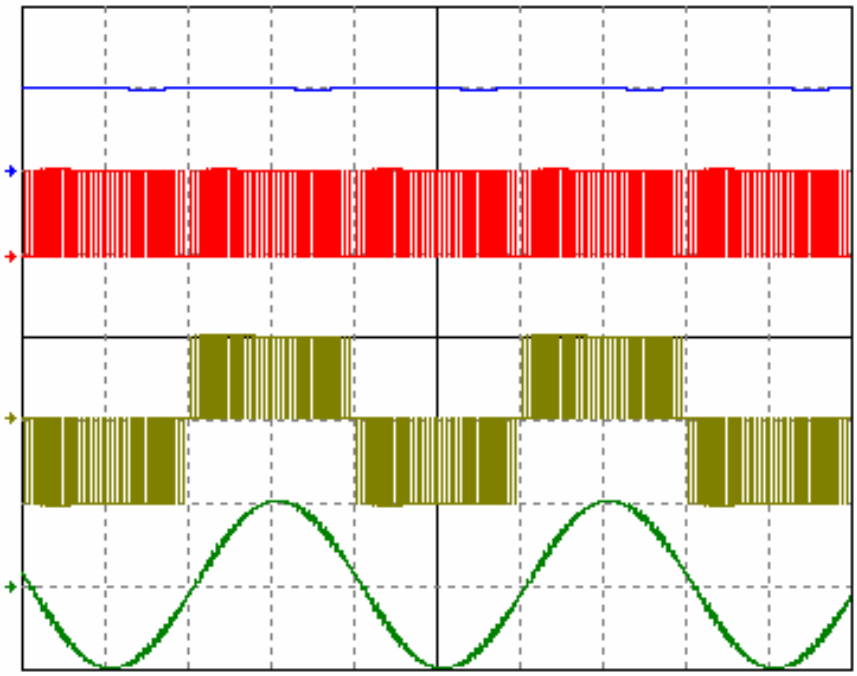
4.4.1 Proof of Concept - Resistive Loading

Preliminary tests on the inverter were carried out with two power sources. Firstly, a DC power supply and a series-connected inductor was used to simulate an ideal constant current source. Figure 4.21 compares the computer generated (PSIM®) simulation and measured results corresponding to an arbitrarily selected resistive / capacitive load. The load resistance is 0.5Ω, and a filter capacitance of 1000μF is selected to obtain a low-pass filter with cut-off frequency equal to 400Hz, i.e. 10% of the PWM switching frequency. The displayed waveforms include the rectifier, current wave-shaper, unfolding circuit and filter output currents, from top to bottom, respectively.

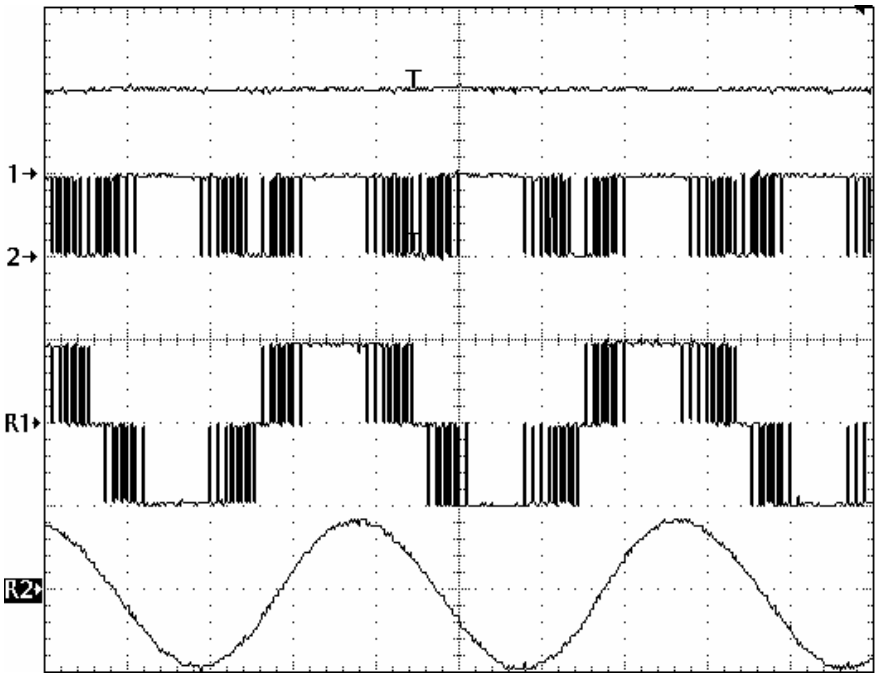
Secondly, the PM generator and rectifier was used as the inverter current source. Figure 4.22 compares the simulated and measured results, for the same resistive / capacitive inverter load. The figure also shows the rectifier, current wave-shaper, unfolding and filter output currents. The measured results show a good correspondence with the predicted waveforms and give confidence in the simulation model.

The current waveforms shown in Figures 4.21 and 4.22 illustrate the key principles of the inverter, i.e. the power source acts as a current source, and the wave-shaper acts as a PWM current chopper which produces a waveform whose fundamental component is a full-wave rectified sinewave. The action of the H-bridge inverter is illustrated, as is the low-pass filter's ability to sufficiently remove the high-frequency PWM components. The inverter output current is sinusoidal and fluctuates at the grid (mains) frequency.

Inspection of the PM generator's rectified output current shows that a high frequency ripple component, due to the bridge rectifier, is present. A low frequency 100Hz ripple component is also shown. This is caused by the inverter output voltage variation, which causes the inverter input current to vary (see the generator I-V locus in Figure 4.15). This 100 Hz input current variation ultimately affects the fundamental magnitude of the inverter output current, and hence should be limited to reduce output current distortion. The rectifier current ripple is less problematic, as it occurs at frequencies higher than the filter cut-off, and is hence not seen in the inverter output current. Despite the input current distortion from the rectifier ripple and power fluctuations, the simulated and measured results indicate that the inverter output current and its THD are not greatly affected by this, for this load condition. This is also summarised in Table 4.4, which shows a detailed comparison of the two current source cases.

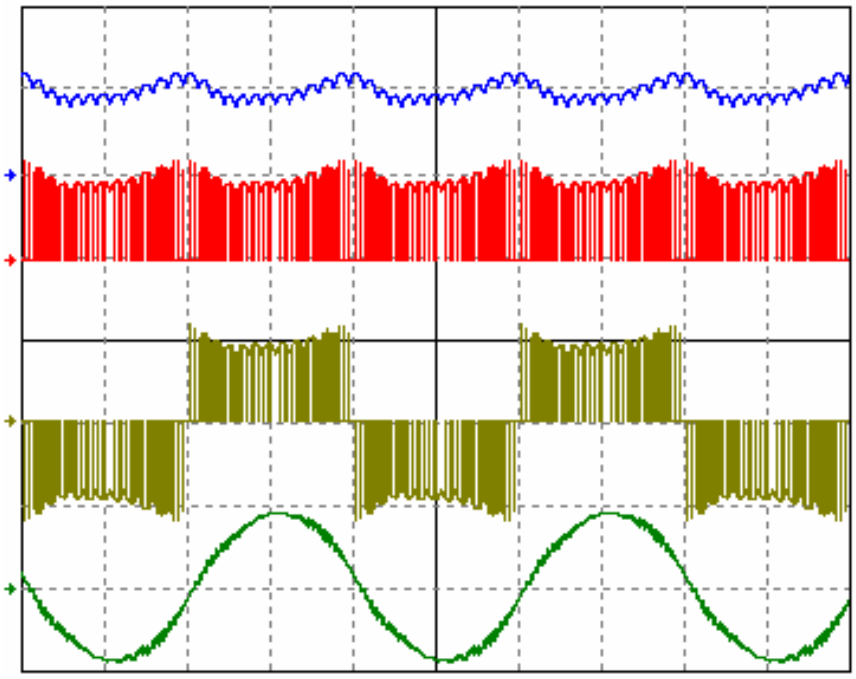


(a) PSIM® simulation

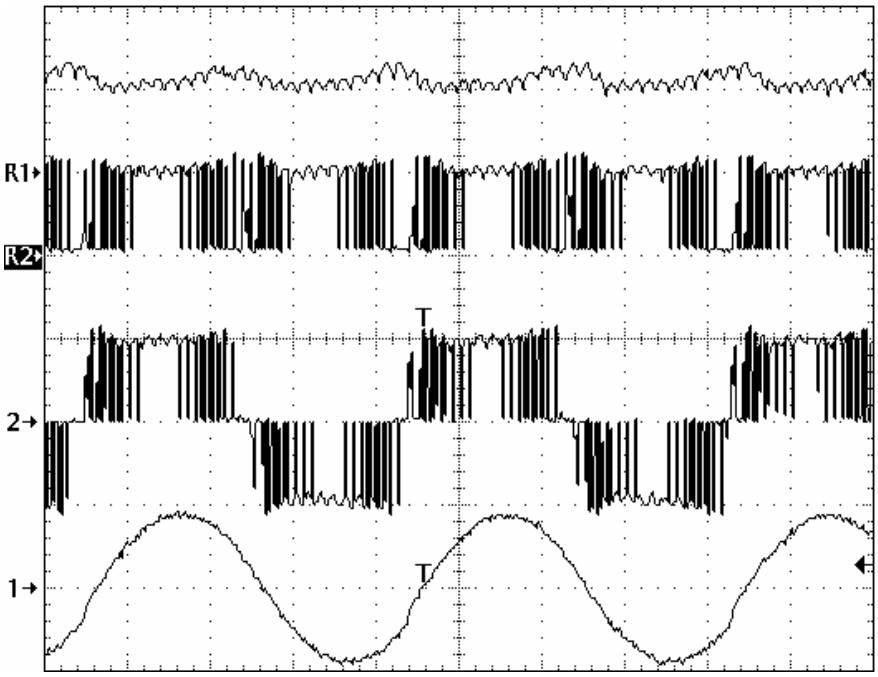


(b) Measured results

Figure 4.21: Proof of inverter concept, showing (a) PSIM® simulation, and (b) measured results, using an ideal current source. The waveforms shown are the power supply, current wave-shaper, unfolding circuit and filter output currents, from top to bottom, respectively. The zero position for each waveform is shown by the small arrow on the left. The vertical and horizontal scales are 2A and 5ms per division, respectively.



(a) PSIM® simulation



(b) Measured results

Figure 4.22: Proof of inverter concept, showing (a) PSIM® simulation, and (b) measured results, using the PM generator as current source. The waveforms shown are the rectifier, current wave-shaper, unfolding circuit and filter output currents, from top to bottom, respectively. The vertical and horizontal scales are 20A and 5ms per division, respectively.

Table 4.4: Simulated and measured resistive load inverter performance.

	DC Power Supply		**PM Generator (500rpm)**	
	Simulated	Measured	Simulated	Measured
Input current (A)	2.05	2.03	19.9	21
Input current ripple (A_{pk-pk})	0.06	0.10	8.15	8.80
Output current (A)	1.43	1.26	13.0	12.8
Output voltage (V)	0.71	0.63	6.50	6.40
Output power (W)	1.02	0.79	84.5	81.9
Output current THD (%)	3.40	3.70	5.97	4.00

The inverter concept has been successfully demonstrated, using both an ideal and the PM generator current sources. It is also tested with various resistive / capacitive loads to investigate the constant current assumption previously made, as discussed below.

4.4.2 Constant Current Assumption

For high quality inverter output current waveforms it is necessary that the input current be relatively constant even at the peak output voltage. This condition is satisfied when the peak output voltage is much less than the rectified open-circuit voltage. This is investigated for three machine speed / load cases, as highlighted on the I-V locus of Figure 4.23. The experimental data from each case is summarised in Table 4.5. Note that that the inverter modulation index is maintained at 100% throughout the testing, and that cases 2 and 3 are bench-marked against case 1.

Case 1 ($n = 500$ rpm, $R_L = 0.5\,\Omega$)

The calculated I-V locus indicates that a minimum peak current of about 19A occurs under this condition, however this will be slightly less, due to the rectifier ripple. Hence the inverter input current will fluctuate between the short-circuit current (21.6A) and about 18A. This is verified by Figure 4.24, which shows the simulated and the measured experimental inverter input current, as well as the resulting resistive load current. The load current contains very little distortion as a filter capacitance of 2,000μF is used. This value results in a filter cutoff frequency of approximately 160Hz, which corresponds to 4% of the PWM switching frequency.

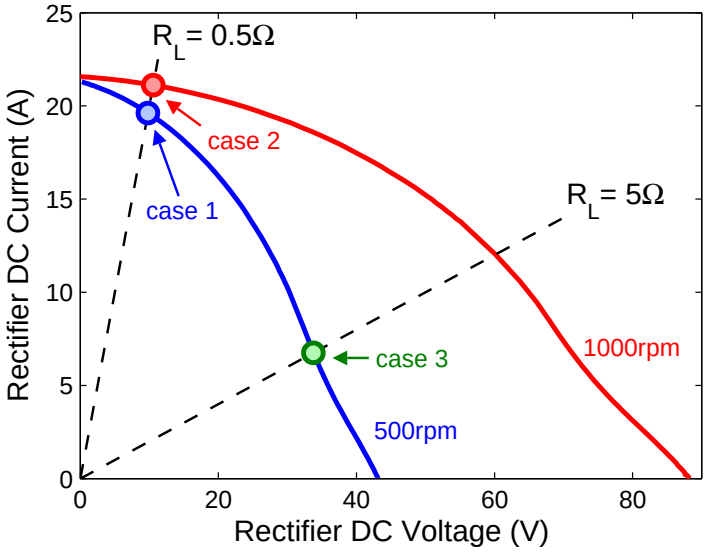
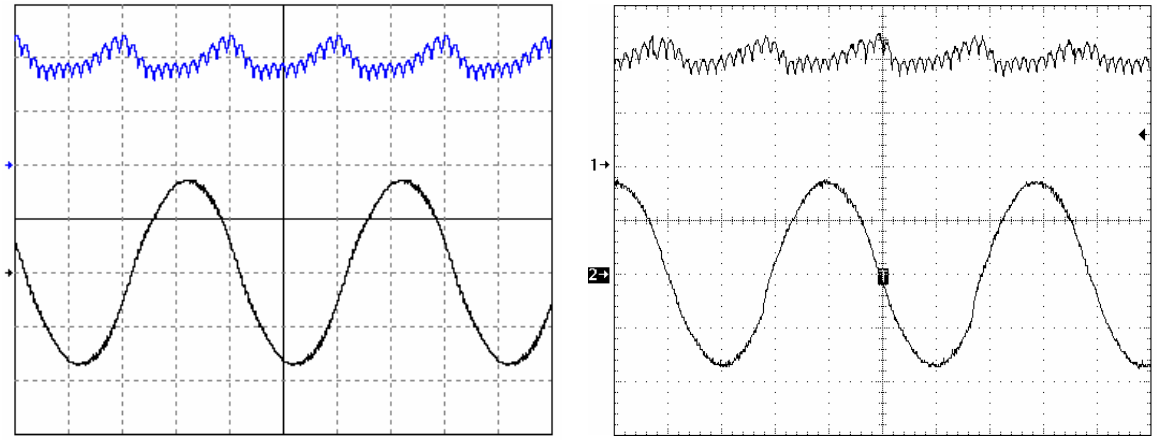


Figure 4.23: Calculated generator I-V locus for 500 and 1,000rpm. The dashed lines represent resistive load lines of 0.5 and 5Ω, and the circles correspond to three test cases.



(a) PSIM® simulation

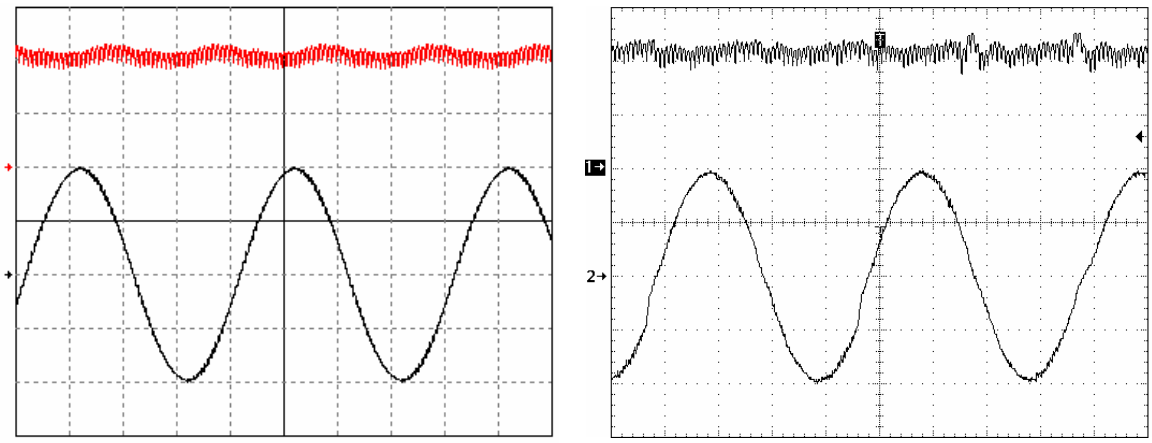
(b) Measured results

Figure 4.24: Simulated (a), and measured experimental (b) inverter currents, for case 1. The waveforms shown are the rectifier (top) and filter (bottom) output currents. The vertical and horizontal scales are 10A and 5ms per division, respectively.

Case 2 ($n = 1000$ rpm, $R_L = 0.5\,\Omega$)

The inverter load remains unchanged, however the generator speed has doubled. Although the open-circuit voltage has doubled (from 45V to 90V), the I-V locus indicates that the peak load current will only slightly increase from 18 to 20A. Hence, the inverter input current is expected to fluctuate between the short-circuit (21.6A) current and about

20A (allowing for the rectifier ripple). This is verified by Figure 4.25, which shows the simulated and experimentally measured inverter input and load currents. The increased speed clearly makes the input current more constant, by reducing the magnitude of the 100Hz ripple. This slightly increases the fundamental of the load current, and significantly improves the measured total harmonic distortion (THD), from 4.0% to 3.0%. Note that the increase in speed also increases the rectifier ripple frequency.



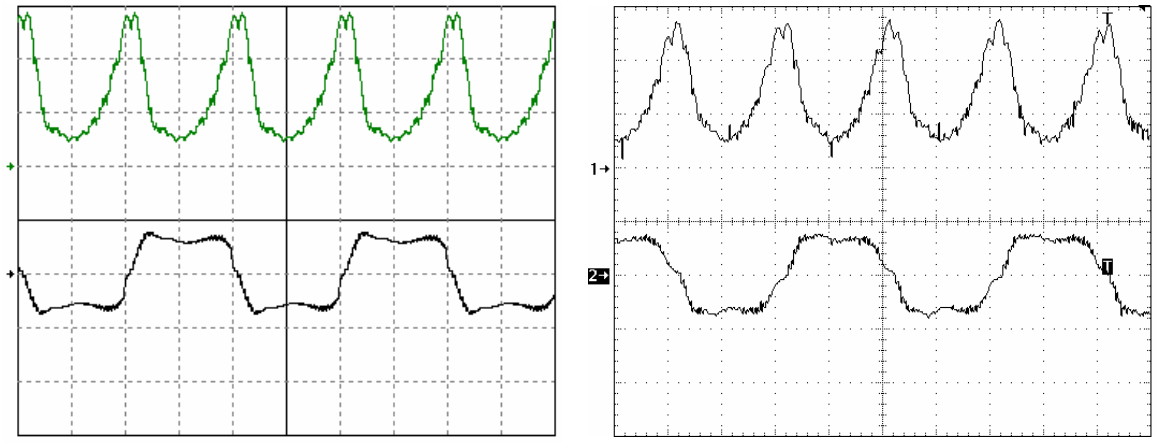
(a) PSIM® simulation (b) Measured results

Figure 4.25: Simulation (a), and measured experimental (b) inverter currents, for case 2. The waveforms shown are the rectifier (top) and filter (bottom) output currents. The vertical and horizontal scales are 10A and 5ms per division, respectively.

Case 3 ($n = 500$ rpm, $R_L = 5\Omega$)

The generator speed is reduced to 500rpm. The load resistance is increased ten-fold (to 5Ω), whilst the filter capacitance is reduced by a factor of 10, to maintain the filter time-constant. With an ideal constant current source input, the peak output voltage should increase by a factor of ten to about 98V. However at 500rpm, the rectified open-circuit voltage is 45V, and so the constant current assumption breaks down. The locus also suggests that the inverter input current will fluctuate between the short-circuit current and about 5.7A (allowing for the rectifier ripple). This is verified by the simulated and measured inverter input and load currents, shown in Figure 4.26. The inverter input current fluctuates significantly and the subsequent load current is highly distorted, i.e. its THD is 35.8%, compared to 4.0% for case 1. Note that the open-loop control algorithm causes the output current to appear trapezoidal, as it is the sinusoidal modulation of the fluctuating input current. In addition, the peak input current now exceeds the SC

current. This is because the SC current seen in the I-V locus is that under steady-state conditions, whilst the inverter input currents seen here are transient waveforms.



(a) PSIM® simulation (b) Measured results

Figure 4.26: Simulation (a), and measured experimental (b) inverter currents, for case 3. The waveforms shown are the rectifier (top) and filter (bottom) output currents. The vertical and horizontal scales are 10A and 5ms per division, respectively.

Table 4.5: Summary of simulated (SIM) and measured (MEAS) inverter performance, for cases 1–3.

	Case 1		Case 2		Case 3	
	SIM	MEAS	SIM	MEAS	SIM	MEAS
Input current (A)	20.0	21.0	21.2	22.0	15.4	15.1
Input current ripple (A_{pk-pk})	8.25	8.80	4.68	5.10	24.1	22.2
Output current (A)	12.5	12.8	14.1	13.8	5.88	5.80
Output voltage (V)	6.49	7.55	7.33	8.20	29.4	31.0
Output power (W)	81.2	85.0	103	98.8	173	168
Output current THD (%)	4.10	4.00	1.90	3.00	35.8	35.8

Comparison of the above input current waveforms shows that it contains two forms of ripple. These are referred to as the low and medium-frequency ripples (relative to the high-frequency PWM frequency). The medium-frequency ripple is caused by the rectifier and is proportional to the generator speed. It does not contribute much to the output current THD, as these frequencies are beyond the filter cutoff frequency, i.e. the filter attenuates these harmonics. In contrast, the low-frequency ripple occurs at frequencies below the cutoff and hence are not attenuated by the low-pass filter.

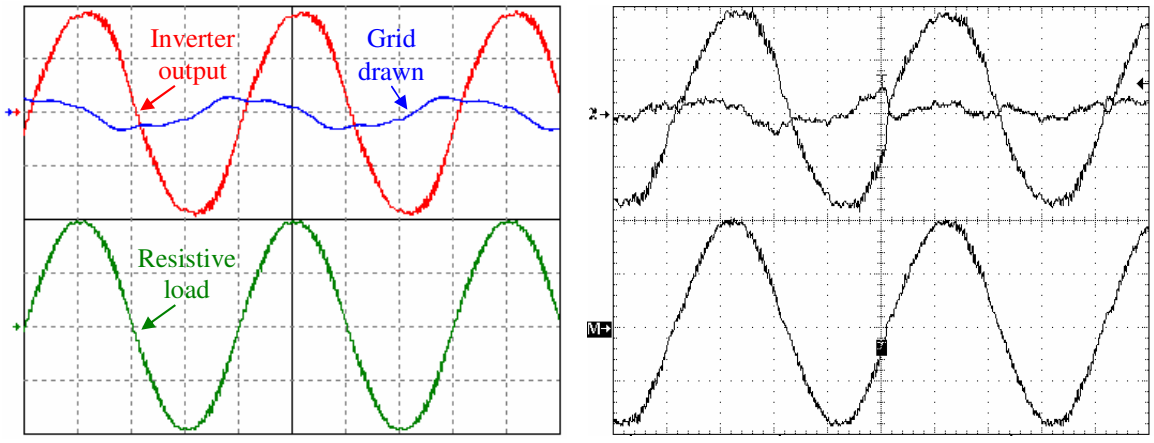
The low-frequency input current ripple is caused by the low-cost inverter design, which avoids a DC link inductor (energy storage device) to improve the overall efficiency. The

consequence of this is that the instantaneous input and output powers must be equal, which implies that the inverter input current and voltage must fluctuate at twice the grid frequency (100 Hz). The magnitude of the peak-to-peak inverter input current ripple is shown to be related to the ratio of the load voltage to the open-circuit voltage (recall Figure 4.23). It is seen that the 100Hz component of the inverter input current ripple decreases as the voltage ratio approaches zero. This implies that the inverter output current distortion can be reduced if the load voltage is much less than the rectifier open-circuit voltage, i.e. the generator operates in the constant current region of its I-V locus. The sources of input and output current harmonics are further discussed in Chapter 5.

4.4.3 Grid-Connected Testing

Proof of Concept - Grid-Connected Operation

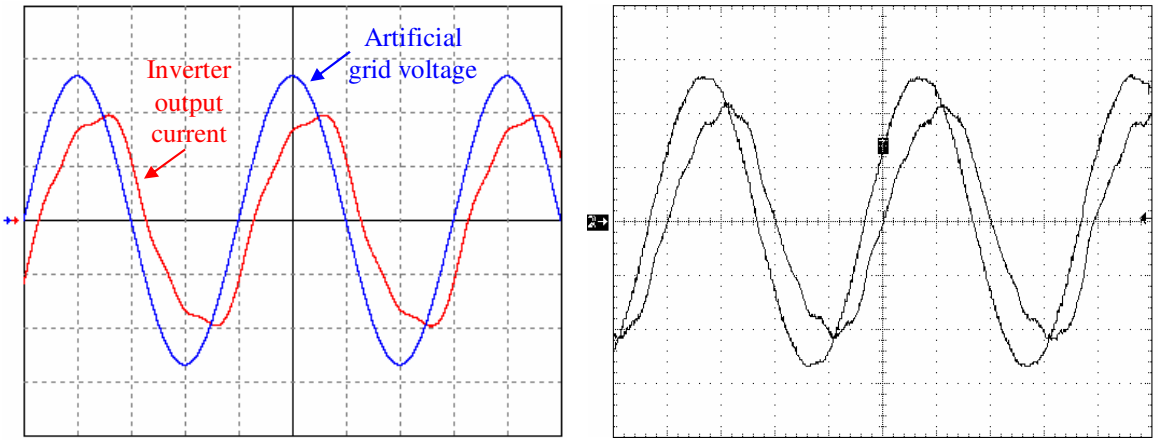
Once the resistive load and grid voltages are synchronised, switch *SW2* is closed and the artificial grid (autotransformer output) is connected in parallel with the resistive load (refer to the synchronisation procedure in Section 4.3.1). In this case, ideally the grid should provide zero current and the output power of the inverter should still be absorbed by the load resistance. The currents for this case are shown in Figure 4.27 and include the inverter output, grid drawn and resistive load currents. Note that the resistive load current is simply the summation of the inverter and grid drawn currents.



(a) PSIM® simulation (b) Measured results

Figure 4.27: Simulated (a), and measured experimental (b) inverter currents, for the intermediate grid-connected stage, i.e. resistive / capacitive load in parallel with the grid. The horizontal and vertical scales are 10A and 5ms per division, respectively.

The pure grid-connected case is obtained by removing the load resistance (opening switch *SW1* of Figure 4.12), which causes the inverter current to flow through the autotransformer's leakage inductance into the mains. The simulated and experimentally measured inverter output current and artificial grid voltage waveforms, for an autotransformer output voltage of 15 V_{RMS}, are shown in Figure 4.28. Note that the simulation is based on the equivalent transformer model shown in Figure 4.12 with equivalent resistance and inductance values taken from Figure 4.13.



(a) PSIM® simulation (b) Measured results

Figure 4.28: Simulated (a), and measured experimental (b) : inverter output current and artificial grid voltage waveforms, for the purely grid-connected stage. The voltage and current vertical scales are 5V and 10A per division, respectively.

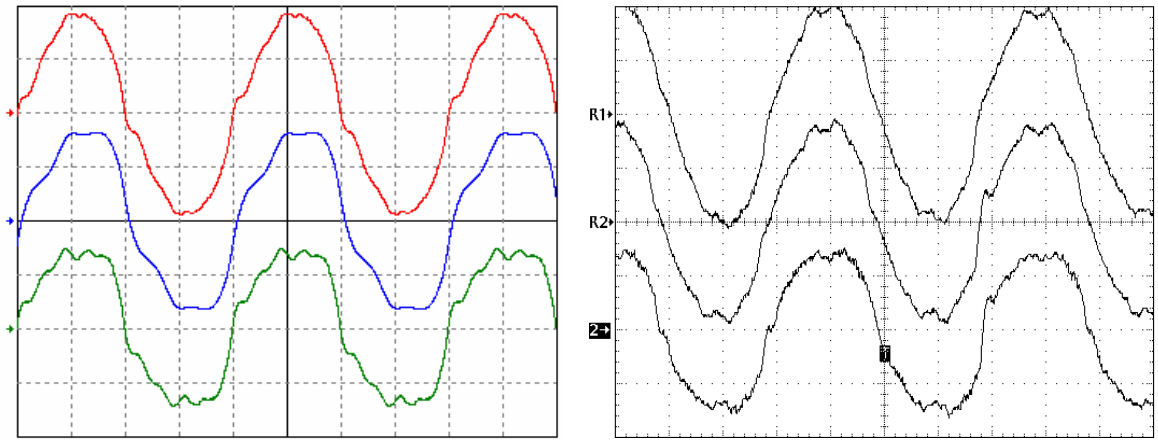
The inverter output current above is shown to lag the grid voltage by about 27°, which equates to a power-factor of approximately 0.89. However, according to the Australian Standards, the inverter must be considered as a load of the grid, hence the inverter current is actually leading the grid voltage. This can also be seen from Figure 4.9, which shows that in the absence of the inverter, the grid feeds an LC network. The high capacitive reactance hence draws a leading current from the grid. Therefore, the inverter is shown to comply with the power factor requirements of the Australian Standards, i.e. 0.95 lag to 0.8 lead.

In contrast, the inverter output current of Figure 4.28 has a THD of about 12.5%, which exceeds the grid THD requirements of 5%. The output current contains more distortion than that for the resistive load case, this is due to i) resonance between the filter capacitor and transformer leakage reactance, and ii) a higher cutoff frequency. The output current THD must be reduced before the inverter can be made commercially

available. Two possible techniques to reduce the output THD are hence investigated, these include the reduction of i) the artificial grid voltage, and ii) the inverter modulation index. Both techniques should push the generator closer to the constant current region of the I-V locus, and hence reduce the input current ripple and output current distortion.

Effect of Grid Voltage Variation

The inverter current was monitored as the artificial grid voltage was varied between RMS voltages of 5 and 20V. This test was performed twice. Initially a fixed filter capacitance of 600μF was used, which caused high amounts of distortion. The test was repeated and the capacitance was varied with grid voltage, in an effort to reduce the output current THD. The filter capacitance ranged from 200 to 2,000μF, and was varied for each grid voltage such that the output current THD was minimised. This was determined by visual inspection of the inverter output current waveform. Examples of simulated and experimentally measured inverter output currents for the three artificial grid voltages are shown in Figure 4.29, for the variable capacitance case. The corresponding values of filter capacitance is shown in Figure 4.30. It is seen in Figure 4.29 (by inspection) that with increasing grid voltage, the output current decreases in magnitude while the THD increases. This occurs as the generator is shifted toward the voltage source region, where the constant current assumption begins to break-down, see Figure 4.23.



(a) PSIM® simulation (b) Measured results

Figure 4.29: Simulated (a), and measured experimental (b) grid-connected inverter currents, for various grid voltages. The currents shown correspond to RMS grid voltages of (top) 6.5V, (middle) 10V, and (bottom) 15V. The vertical and horizontal scales are 10A and 5ms per division, respectively.

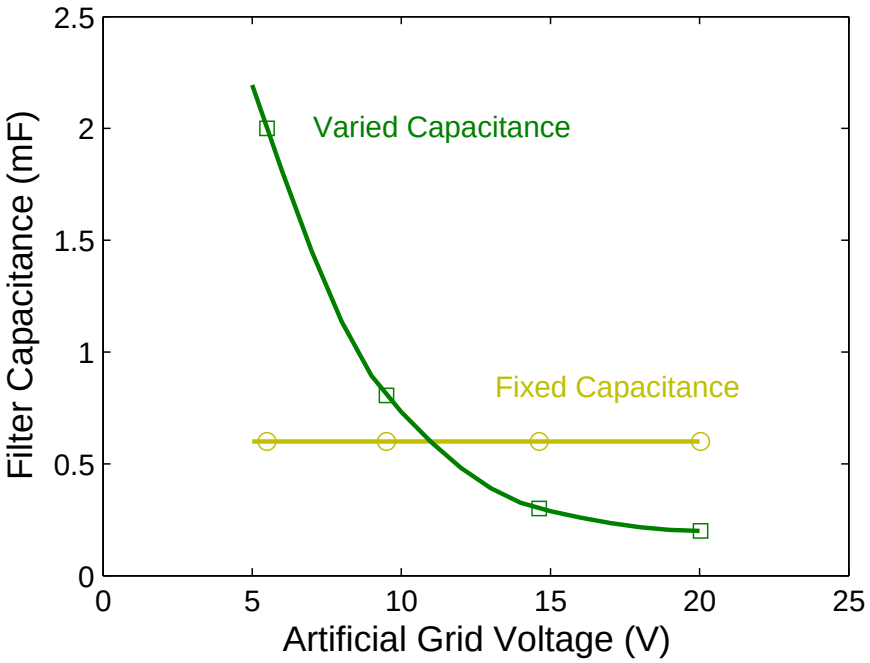
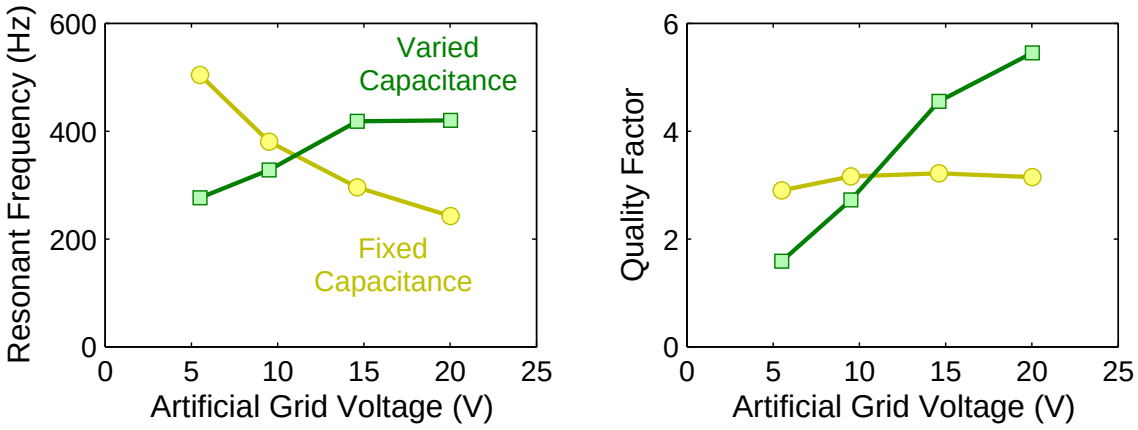


Figure 4.30: Variation of filter capacitance with artificial grid voltage, for both the fixed and varied capacitance tests.

The autotransformer turns ratio and hence its equivalent leakage inductance and resistance increase with grid voltage. These parameters are important as they affect the filter resonant frequency, f_{res}, and its gain at the resonant frequency (quality factor, Q). Therefore harmonics present at the resonant frequency may be potentially amplified, which will increase the overall total harmonic distortion. A summary of the effect of grid voltage variation on the resonant frequency and quality factor is shown in Figure 4.31. Note that the rectifier ripple frequency is 1,200 Hz in this case, and hence the rectifier ripple is attenuated by the filter rather than amplified by the filter resonance.

Figures 4.31(a) and 4.31(b) indicate that the resonant frequency decreases, while the quality factor remains relatively constant for the fixed capacitance case. In contrast, the resonant frequency and quality factor both increase with grid voltage for the variable capacitance case. Both sets of observations indicate that the THD will increase with grid voltage, due to the effects resonance. In addition, the THD will also increase as the constant current assumption breaks down (grid voltage increases), due to increased low order harmonics. This coupled with a quality factor greater than 1 and the decreasing resonant frequency, suggests that the THD for the fixed capacitance case should be greater than that for the variable capacitance case. This is verified by Figure 4.32, which shows the



(a) Resonant frequency

(b) Quality factor

Figure 4.31: Calculated (a) resonant frequency, and (b) quality factor vs. grid voltage, for both the varied and fixed capacitance cases.

simulated and experimentally measured THD for the four different grid voltages mentioned above. Despite the discrepancies between the simulated and measured data, they both verify that the inverter output current THD increases with grid voltage.

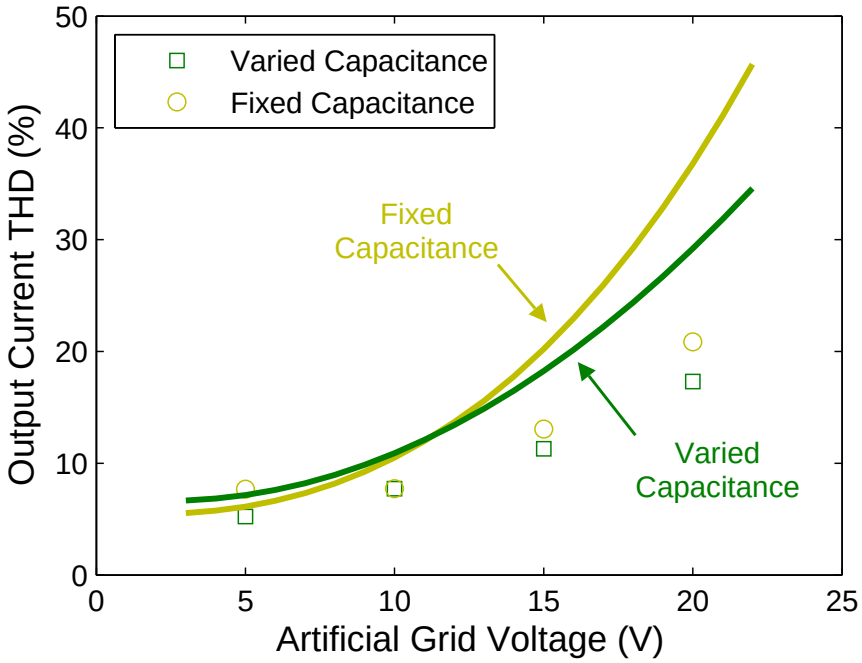
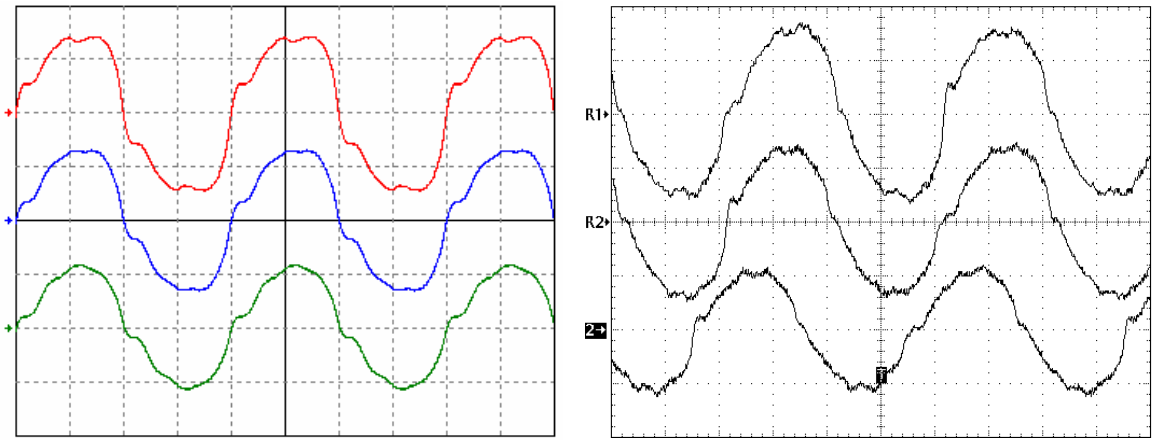


Figure 4.32: Inverter output current THD vs. grid voltage, for both fixed and variable filter capacitance cases. The solid lines represent simulated THD, whilst the points correspond to experimentally measured data.

The discrepancy between the measured and simulated THD data is likely caused by the equivalent transformer modelling. The transformer model is an approximation only, which ignores the magnetising reactance and core loss resistance. Note that this will have an effect on the quality factor, i.e. the gain at the resonant frequency. This appears somewhat valid as the simulated current waveforms show a slight increased effect of resonance on the output current THD, compared to those captured experimentally. Despite this, the close matching simulated and experimentally captured current waveforms of Figure 4.29 give confidence in the PSIM® model.

Effect of Modulation Index Variation

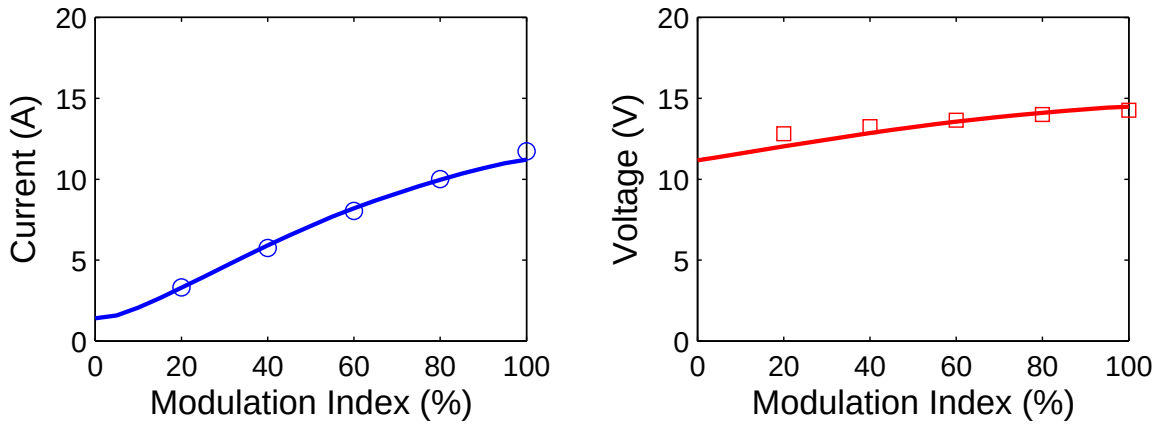
The PWM modulation index was varied for the pure grid-connected case. The artificial grid voltage was set to 15V$_{RMS}$ and a filter capacitance of 400μF was selected to minimise the output current THD, for a m_a of 100%. The effect of modulation index variation on the simulated and measured output current waveforms is shown in Figure 4.33, for modulation indices of 100%, 80% and 60%. The simulated and measured current waveforms indicate that the inverter output current, and hence output power, is linearly proportional to m_a for a fixed grid voltage. This differs from the resistive load case, where the inverter output power is proportional to ${m_a}^2$.



(a) PSIM® simulation (b) Measured results

Figure 4.33: Simulated (a), and measured experimental (b) grid-connected inverter currents, for various modulation indices. The currents shown correspond to modulation indices of (top) 100%, (middle) 80%, and (bottom) 60%. The vertical and horizontal scales are 10A and 5ms per division, respectively.

The inverter output current is expected to vary linearly with modulation index, if supplied by an ideal constant current source and loaded by a resistance. However, the inverter is loaded by the autotransformer secondary winding and is fed by the PM generator and rectifier current source. The (PSIM®) simulated and measured output currents and voltages are shown in Figure 4.34, over a wide range of modulation indices.



(a) Inverter output current

(b) Inverter output voltage

Figure 4.34: Inverter output (a) current, and (b) voltage for the grid-connected case, showing the effect of modulation index variation. The solid lines represent PSIM® simulations, whilst the points correspond to experimentally measured data.

Figure 4.34(a) shows that the inverter output current does not approach zero at low values of m_a. This is the result of the grid-connected filter, which draws a current from the grid when m_a is equal to 0%; the magnitude and power factor depend on the filter reactance. The output current appears to increase linearly at low values of m_a, and then saturate as m_a approaches 100%. This is caused by the non-ideal constant current source, i.e. the inverter pushes the generator further from the constant current region of the I-V locus as the m_a increases. The degree of the saturation varies with grid voltage. For example, if the generator remains in the constant current region for a m_a of 100%, the inverter output current will be linearly proportional to the modulation index over the entire range of m_a, except at low values, where the output current will approach that drawn by the filter.

Figure 4.34(b) shows how the inverter output voltage varies with modulation index. The inverter has a non-zero output voltage for m_a equal to 0%, due to the voltage drop across the (grid-connected) filter capacitance, and the output voltage is shown to increase with modulation index. This is due to the autotransformer regulation, i.e. the voltage drop

across the transformer equivalent inductance increases with the inverter output current (recall Figure 4.12). Therefore, the inverter output voltage must increase with modulation index as this action increases the inverter output current.

It was seen above that the inverter output current saturates as the modulation index approaches 100%, as the PM generator is moved away from the constant current region of the I-V locus. It is hence expected that as the m_a increases, the input current distortion and hence output current distortion will also increase. This is verified by the simulated output current THD in Figure 4.35. The figure also includes experimentally measured THD data, which does not agree with the simulations over the entire range of m_a. The measured THD does decrease with modulation index, until m_a is equal to about 60%, the THD then increases as m_a approaches 0%. The harmonic analysis of the measured current waveforms indicate that resonance causes the increased THD. The measured resonant frequency is 450Hz. PSIM®, however, predicts a resonant frequency of 411Hz, and is likely due to the approximation of the transformer parameters. Despite the discrepancy between the simulated and measured THD, which could be further investigated, the simulated current waveforms closely match those measured throughout this chapter and give confidence in the PSIM® model.

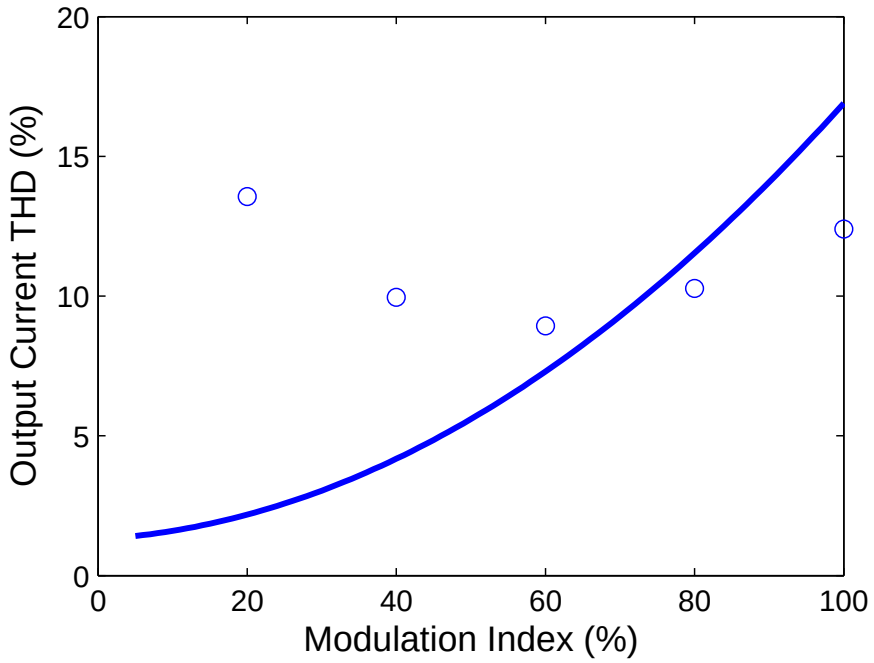


Figure 4.35: Inverter output current THD vs. modulation index. The solid line represents the simulated THD, whilst the points represent the measured data.

4.5 Chapter Summary

The proposed novel grid-connected current-source inverter topology, based on the high-inductance PM generator, uncontrolled rectifier, single-switch current wave-shaper, unfolding circuit (H-bridge inverter) and low-pass filter, has been designed and simulated in PSIM®. The inverter concept was successfully demonstrated using a 150W prototype that was experimentally tested using a dynamometer, and controlled in an open-loop manner. The current wave-shaper switch was modulated to create a rectified sinusoidal output current, which was unfolded and filtered by the H-bridge inverter and low-pass filter, respectively. The measured inverter output current waveforms, for both resistive and grid-connected loads, closely matched the simulation results, which gave confidence in the model.

The use of an open-loop control method meant that variations in the rectifier output current appeared in the inverter output current. The rectifier output current was modulated by the rectifier ripple and the 100Hz instantaneous power fluctuations due to the single-phase output and the lack of input DC link energy storage. The magnitude of the rectifier ripple was fixed and its varied with generator speed. In contrast, the lack of DC link energy storage caused the input current to fluctuate at twice the grid frequency; its ripple magnitude varied with inverter output power. This was experimentally verified by firstly varying the resistance and capacitance values of three RC load combinations (for a fixed load time-constant), and secondly by increasing the effective (artificial) grid voltage seen by the inverter during the grid-loaded testing stage.

The inverter low-pass filter, which utilised the grid transformer leakage reactance and resistance, demonstrated its ability to attenuate the high-frequency current harmonics caused by the unipolar PWM switching. Inspection of the output current, however, revealed a significant ninth-order harmonic, which was caused by resonance between the filter capacitor and transformer inductance. This prevented the inverter from meeting the THD grid requirement.

Chapter 5

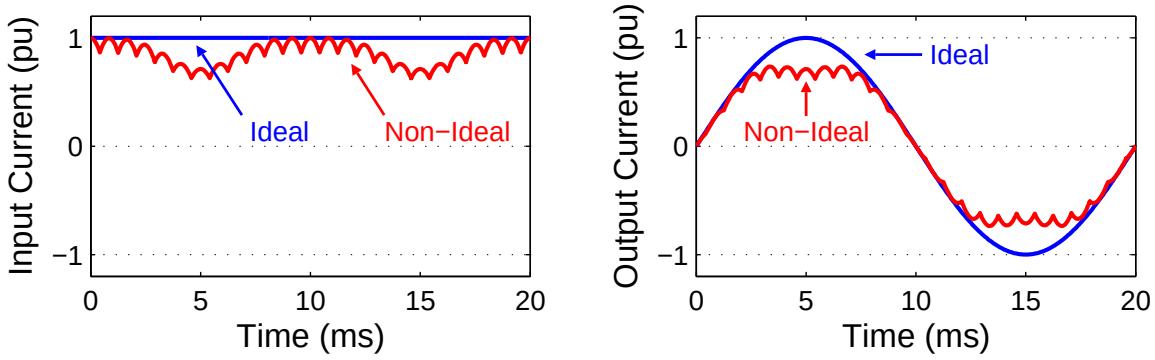
Inverter Analysis and Control

This chapter analyses the proposed grid-connected inverter. The non-ideal input current source, and its effect on the inverter output current is studied. The harmonic distortion of the non-ideal current source and that of the PWM switching is examined. Four techniques to attenuate unwanted harmonics are suggested and briefly examined. Of these, the low-pass filter and feed-forward controller are further discussed. The low-pass filter is analysed and design trade-offs are shown. The feed-forward controller is also designed and its ability to significantly improve the output current THD is demonstrated.

5.1 Analysis of Non-Ideal Constant Current Source

The grid-connected inverter concept assumes that the rectifier ideally provides constant current to the inverter, however, the previous chapter showed that the inverter input current was non-ideal. An example of the ideal and non-ideal inverter input currents is shown in Figure 5.1(a). The figure indicates that the harmonics in the output current are related to the harmonics found in the input current. The large second-order input current harmonics become large third-order output current harmonics, as a result of the sinusoidal modulation.

The input current shows two distinct forms of ripple. The higher frequency ripple is caused by the use of the uncontrolled three-phase rectifier, whilst the low-frequency ripple (twice that of the mains) is caused by the power fluctuations associated with the single-phase inverter design. The lack of an energy storage element implies that the instantaneous inverter input and output powers must be equal. Assuming unity power factor operation, the inverter delivers a time-varying (fluctuating) power that is the square



(a) Input current

(b) Output current

Figure 5.1: Normalised inverter (a) input, and (b) output currents for ideal and non-ideal inverter input currents.

of a sinusoid, whose average power is half that of its peak. This fluctuating input power will cause the generator to vibrate [91] and the inverter input current to vary. Each source of distortion is further discussed below. Note that the effect of the PWM switching and that of the low-pass filter is ignored in this section. In addition, the inverter input and output currents and voltages are expressed as normalised quantities throughout this chapter, i.e. they have peak values of 1pu.

5.1.1 Fluctuating Input Current

Part I showed that the PM generator is able to provide constant current, and hence power, to a battery or resistive load. However, the proposed single-phase inverter delivers a time-varying output power. This, coupled with the energy storage-less inverter design, implies the inverter input power must also vary with time (fluctuate). It follows that the inverter input voltage varies with time. For a practical generator, this voltage variation produces an output current variation. This variation is analysed by considering the time-varying rectifier output (inverter input) voltage, $v_R(t)$, in terms of the current wave-shaper output and the grid voltage, $v_{ws}(t)$ and $v_g(t)$, respectively.

Figure 4.29 previously showed that the inverter output current THD increased with the artificial grid voltage for a fixed modulation index. This occurred as the generator was operated closer to the variable voltage region of the I-V locus, which reduces the machine's ability to provide constant current. This is further analysed in this section. Note that all voltages hereafter are normalised relative to the rectifier open-circuit voltage.

Consider the time-varying inverter output (grid) voltage. Its instantaneous value, relative to that of the rectified open-circuit voltage, is defined as α_0; e.g. a peak α_0 of 0.5pu corresponds to a rectified open-circuit voltage of 679V. The normalised grid voltage is hence expressed in terms of peak α_0 (i.e. $\widehat{\alpha}_0$), as shown in Equation (5.1), where ω_g represents the grid angular frequency. The unfolding circuit input voltage can also be expressed as a function of $\widehat{\alpha}_0$, as it is simply the rectified equivalent of its output voltage. This is shown in Equation (5.2). Note that $\widehat{\alpha}_0$ is a scalar that ranges between 0 and 1.

$$v_g(t) = \widehat{\alpha}_0.\sin(\omega_g t) \quad \text{(pu)} \tag{5.1}$$

$$v_{ws}(t) = |v_g(t)| = \widehat{\alpha}_0.|\sin(\omega_g t)| \quad \text{(pu)} \tag{5.2}$$

The rectifier output voltage can also be expressed in terms of $\widehat{\alpha}_0$, and is derived from the time-varying ideal boost equation shown in Equation (5.3). Note that the duty-cycle, d, was previously kept constant for a battery load. However, it is now time-varying as shown in Equation (5.4), where m_a represents the inverter modulation index. The rectifier voltage is hence expressed by Equations (5.5) and (5.6).

$$v_R(t) = [1 - d(t)]\ v_{ws}(t) \quad \text{(pu)} \tag{5.3}$$

$$d(t) = 1 - m_a.|\sin(\omega_g t)| \quad \text{(pu)} \tag{5.4}$$

$$\begin{aligned} v_R(t) &= m_a.|\sin(\omega_g t)|.v_{ws}(t) && (5.5)\\ &= m_a.\widehat{\alpha}_0.\sin^2(\omega_g t) \quad \text{(pu)} && (5.6) \end{aligned}$$

A graphical summary of the normalised grid, (current) wave-shaper and rectifier output voltages (Equations (5.1), 5.2 and (5.6), respectively) is shown in Figure 5.2. The figure shows that the grid voltage and wave-shaper output voltages are sinusoids with a peak value equal to α_0. The peak rectifier voltage, however, is proportional to the inverter modulation index, and the figure shows normalised voltages for cases where m_a is equal to 100 and 50%. Note that the grid and current wave-shaper output voltage waveforms are independent of m_a, i.e. their magnitudes are set by the grid voltage.

The inverter input current can be derived from the normalised rectifier I-V locus, which is shown in Figure 5.3 along with the locus of an ideal current source. The figure shows both the ideal and the measured (PM machine) loci, where α and β represent the

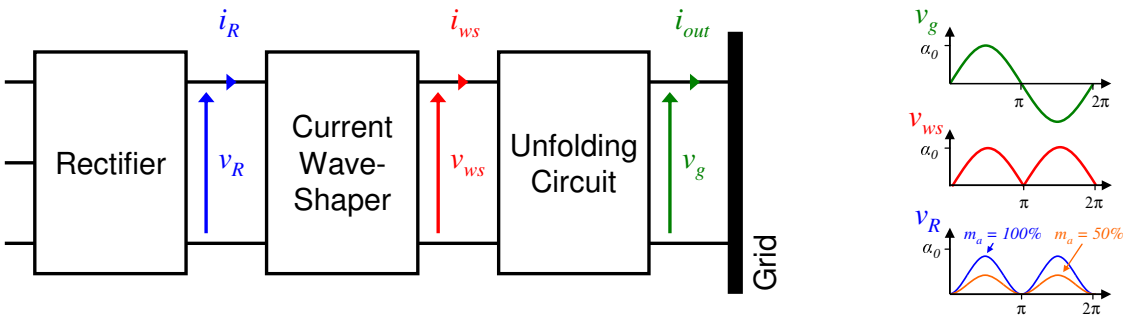


Figure 5.2: Output voltage of various inverter stages, showing the grid, wave-shaper and rectifier output voltages. The rectifier output voltage is a sinusoid squared, and is shown for modulation indices, m_a, of 100 and 50%.

normalised rectifier voltage and current, respectively. Therefore, $\alpha = 1$ pu represents an open-circuit, whilst $\beta = 1$ pu represents a short-circuit. The ideal locus neglects the effect of the rectifier (as described in Section 2.3.1), hence the ideal current, $\beta_{(id)}$, is given by Equation (5.7), which is based on the unit circle equation, i.e. $x^2 + y^2 = r^2$. In contrast, the dashed line, which represents a fitted curve corresponding to the measured data, $\beta_{(exp)}$, is expressed as a quintic function of α, as shown in Equation (5.8).

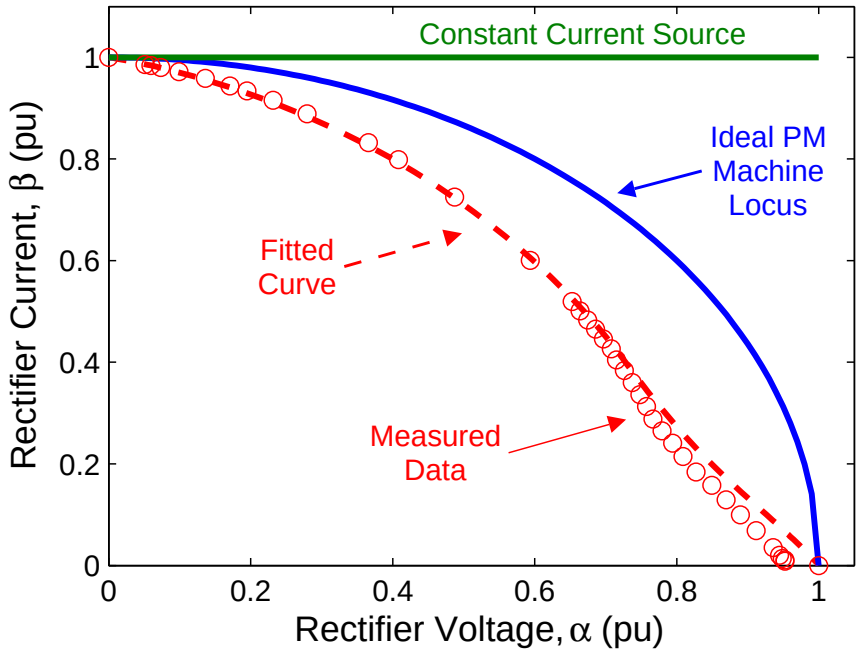


Figure 5.3: Normalised ideal and fitted experimental rectifier I-V loci, where α and β represent the voltage and current, respectively. The points represent measured data.

$$\beta_{(id)} = \sqrt{1-\alpha^2} \tag{5.7}$$

$$\beta_{(exp)} = 3.86\alpha^5 - 7.47\alpha^4 + 4.27\alpha^3 - 1.53\alpha^2 - 0.116\alpha + 1 \tag{5.8}$$

The normalised rectifier current is determined by tracing the time-varying normalised rectifier voltage (from Figure 5.2) on to the rectifier I-V locus, and plotting the corresponding current. This process is demonstrated using the ideal rectifier I-V locus in Figure 5.4 for a peak normalised rectifier voltage ($\widehat{\alpha}$) of 0.8 and 0.6pu, which results in a fluctuating rectifier current, $i_R(t)$, with minima of 0.6 and 0.8, respectively. The experimental inverter input current is obtained similarly and is expected to contain greater harmonic distortion than the ideal case, as it is less effective as a constant current source.

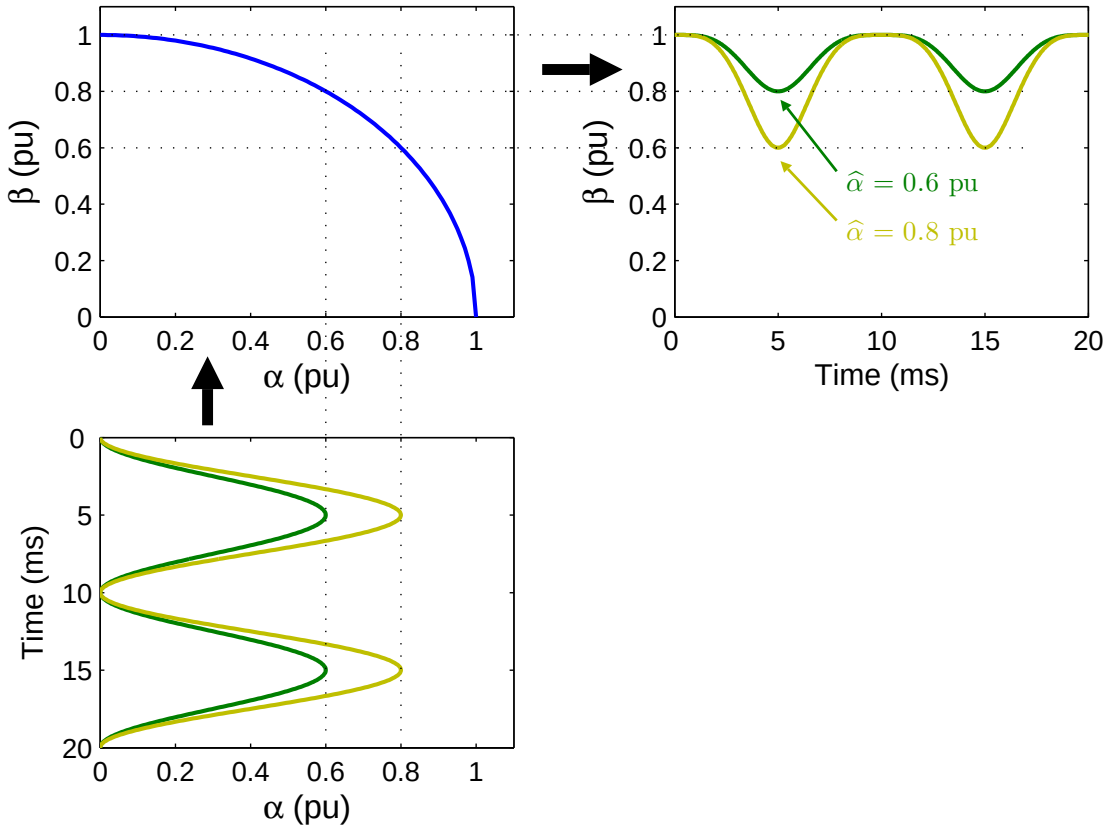


Figure 5.4: Normalised ideal inverter input (rectifier output) current, derived from the rectifier output voltage and the normalised rectifier I-V locus. The inverter input currents shown correspond to the cases where $\widehat{\alpha}$ = 0.6 and 0.8 pu.

The ideal boost equation, shown in Equation (5.9), is used to determine the wave-shaper output current, I_{ws}. Consider the ideal I-V locus case. Using Equations (5.7) and (5.8) and substituting the terms $(1-d)$, I_R and I_{ws} for their time-varying equivalents, allows the ideal wave-shaper output current, $i_{ws\ (id)}(t)$, to be expressed by Equation (5.10). The ideal inverter output current, $i_{out\ (id)}(t)$, is simply the unfolded equivalent of the wave-shaper output current, as given below in Equation (5.11). Examples of the inverter input and subsequent output currents, using both the ideal and experimental loci over a wide range of $\widehat{\alpha}_0$, is shown in Figure 5.5. The m_a is 100% for all cases.

$$I_{ws} = (1-d)\ I_R \tag{5.9}$$

$$i_{ws\ (id)}(t) = m_a.|\sin(\omega_g t)|\ \sqrt{1-\left(m_a.\widehat{\alpha}_0|\sin^2(\omega_g t)|\right)^2} \quad \text{(pu)} \tag{5.10}$$

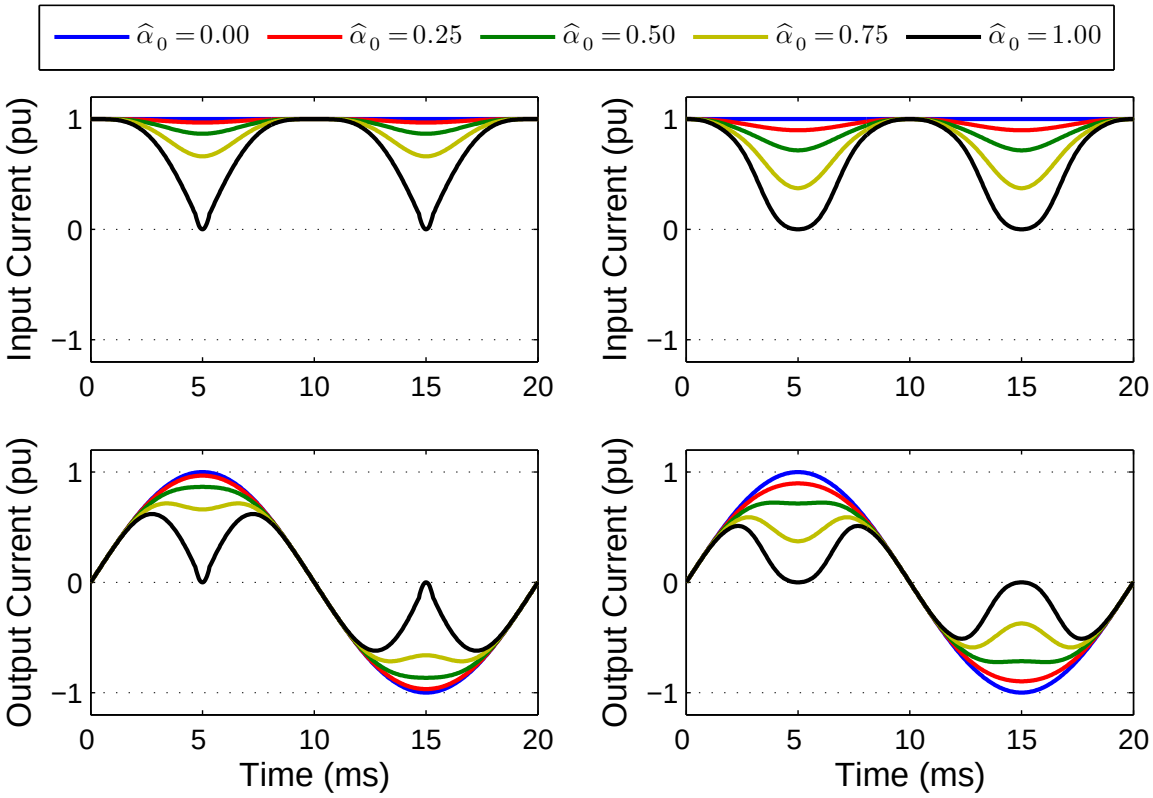
$$i_{out\ (id)}(t) = m_a.\sin(\omega_g t)\ \sqrt{1-\left(m_a.\widehat{\alpha}_0|\sin^2(\omega_g t)|\right)^2} \quad \text{(pu)} \tag{5.11}$$

Figure 5.5 shows the inverter input and output currents for various values of $\widehat{\alpha}_0$ ($m_a = 100\%$) using both the ideal and experimental I-V loci. The importance of a constant input current source is clearly seen. The fluctuating input current is caused by the low-cost single-phase inverter design, and could be reduced by modifying the inverter design, e.g. introducing an energy storage element or outputting three-phase power.

5.1.2 Rectifier Ripple

The uncontrolled full-wave three-phase rectifier is used to convert the generator's AC output currents to a DC current. The drawback is that the rectifier output (inverter input) current contains ripple. This time-varying rectifier ripple, $rect(t)$, fluctuates at six times the generator frequency and has a magnitude of 13.34% $(1-\sqrt{3}/2)$ of the peak AC line current. This is expressed in Equation (5.12), where ω_m is the generator electrical frequency. An example of the effect of the rectifier ripple is shown in Figure 5.6, which shows the distorted input and subsequent inverter output current. Note that only the effect of the rectifier ripple is shown (i.e. $\widehat{\alpha}_0$ is zero).

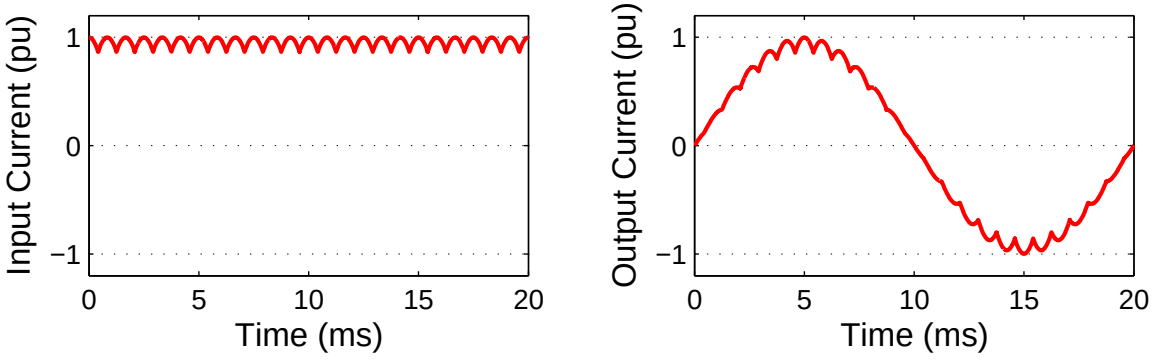
$$rect(t) = \frac{|\sin(\omega_m t)| + |\sin(\omega_m t + \frac{2\pi}{3})| + |\sin(\omega_m t + \frac{4\pi}{3})|}{2} \tag{5.12}$$



(a) Ideal I-V locus

(b) Experimental I-V locus

Figure 5.5: Normalised inverter input (top) and output (bottom) currents, using the ideal (left) and experimental (right) I-V loci. The currents are displayed for $\widehat{\alpha}_0$ ranging from 0 to 1pu, in 0.25 increments. The output current contains the distortion found in the input current. There is greater distortion using the experimental I-V locus.



(a) Input current

(b) Output current

Figure 5.6: Normalised inverter (a) input and (b) output currents, showing the effect of the rectifier ripple ($\widehat{\alpha}_0 = 0$) for a machine frequency of 200Hz (rectifier ripple frequency of 1.2 kHz).

5.1.3 The Resulting Input Current

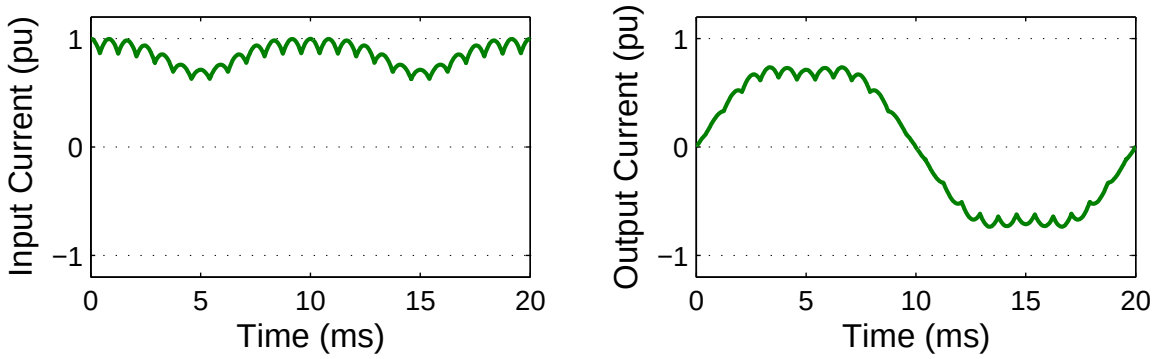
The inverter input current, $i_R(t)$, contains distortion from the rectifier ripple and the fluctuating inverter input power, and is expressed by Equation (5.13). Substituting β with $\beta_{(id)}$ (Equations (5.6) and (5.7)), and the term $rect(t)$ (Equation (5.12)), allows the ideal inverter input current, $i_{R\ (id)}(t)$, to be represented by Equation (5.14). The resulting (simplified) ideal output current, $i_{out\ (id)}(t)$, is shown in Equation (5.15).

$$i_R(t) = rect(t)\,.\,\beta \quad \text{(pu)} \tag{5.13}$$

$$i_{R\ (id)}(t) = \frac{|\sin(\omega_m t)| + |\sin(\omega_m t + \frac{2\pi}{3})| + |\sin(\omega_m t + \frac{4\pi}{3})|}{2} \sqrt{1 - \left(m_a.\widehat{\alpha}_0 |\sin^2(\omega_g t)|\right)^2} \quad \text{(pu)} \tag{5.14}$$

$$i_{out\ (id)}(t) = m_a.\sin(\omega_g t)\,.\,i_{R\ (id)}(t) \tag{5.15}$$

An example of the inverter input and its subsequent output current is shown in Figure 5.7, for the ideal locus, $\widehat{\alpha}$ value of 0.7pu ($\widehat{\alpha}_0 = 0.7$, $m_a = 100\%$) and a machine frequency of 200Hz. Note that these current waveforms are identical to those in Figure 5.1. The input current is mainly caused by the fluctuating input power, however, the rectifier ripple also contributes. It is expected that the rectifier associated distortion will dominate at low values of $\widehat{\alpha}$. This is shown in Figure 5.8, which shows the inverter input and output current for two cases of $\widehat{\alpha} = 0.20$pu ($\alpha = m_a.\alpha_0$). Case one has $\widehat{\alpha}_0 = 0.20$ and $m_a = 100\%$,

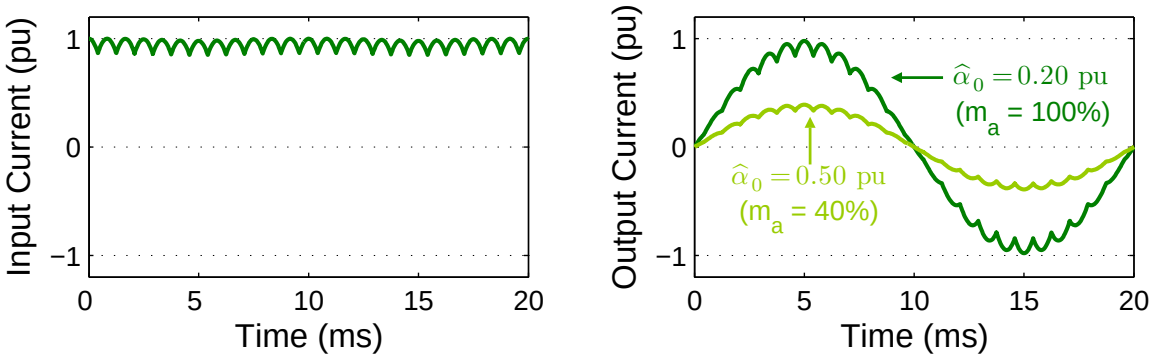


(a) Input current

(b) Output current

Figure 5.7: Normalised ideal inverter (a) input and (b) output currents, showing the combined effect of the rectifier ripple (f_m = 200Hz) and the fluctuating input current ($\widehat{\alpha}_0 = 0.7$pu).

whilst case two has $\widehat{\alpha}_0 = 0.50$ and $m_a = 40\%$. Both input currents are identical. The output currents waveforms are identical in shape, however, differ in magnitude. This highlights that the input current depends on $\widehat{\alpha}$, while the ratio of the output to the input current depends on the m_a.



(a) Input current

(b) Output current

Figure 5.8: Normalised ideal inverter (a) input and (b) output current, for a generator frequency of 200Hz and two cases of $\widehat{\alpha}$ equal to 0.2pu ($\widehat{\alpha}$ =0.2pu, $m_a = 100\%$, and $\widehat{\alpha} = 0.5$pu, $m_a = 40\%$).

The inverter output current distortion is quantified in the next section.

5.2 Total Harmonic Distortion

The amount of distortion in a waveform is quantified by the means of an index called the *total harmonic distortion* (THD) [67]. The THD is a ratio of the total harmonic components, h_{tot}, to the harmonic magnitude of the fundamental frequency, h_1, as shown in Equation (5.16), where h_m specifies the harmonic magnitude found at integer multiples of the fundamental frequency, e.g. h_3 and h_{11} represent the third and 11^{th}-order harmonics, respectively.

$$\text{THD } (\%) = 100 \times \frac{h_{tot}}{h_1} = \frac{\sqrt{\sum_{m\neq 1} {h_m}^2}}{h_1} \tag{5.16}$$

Note that an ideal waveform is a sinusoid, which has zero harmonic components and hence zero distortion. The harmonic content is determined by the *fast Fourier transform* (FFT), which is an efficient algorithm that computes the *discrete Fourier transform* (DFT) [107]. The DFT is a signal processing technique that is used to identify the magnitude and frequency of harmonics that are embedded within signals.

In addition to the rectifier ripple and fluctuating input current, the unipolar PWM switching of the current wave-shaper significantly contributes to the inverter output current THD. Each of these harmonic sources are individually discussed and analysed in the following sections. As previously stated, Australian Standard 4777.2 requires that the output current of a grid-connected inverter must contain less than 5% THD [96].

5.2.1 Fluctuating Input Power

It was previously discussed that the lack of energy storage causes the inverter input current to fluctuate at twice the grid frequency for a single-phase output, recall Figure 5.5. The figure showed the effect of the fluctuating input power on the inverter output current for $\widehat{\alpha}_0$ ranging from from 0 to 1pu. These output current waveforms suggest that the third-order harmonic, h_3, increases and that the fundamental decreases, with increasing $\widehat{\alpha}_0$. This is confirmed by Figure 5.9, which shows the ideal locus output currents for $\widehat{\alpha} = 0.50$ and 0.75pu ($m_a = 100\%$), and the effect of varying $\widehat{\alpha}$ on the fundamental, third, fifth and seventh-order harmonics (h_1, h_3, h_5, h_7). Although higher frequency odd-order harmonics exist, these are ignored as their magnitudes are much less than those of h_{3-7}, and do not significantly affect the THD. It is expected that the THD will rise rapidly with increasing $\widehat{\alpha}$ as the harmonic content increases while the fundamental decreases.

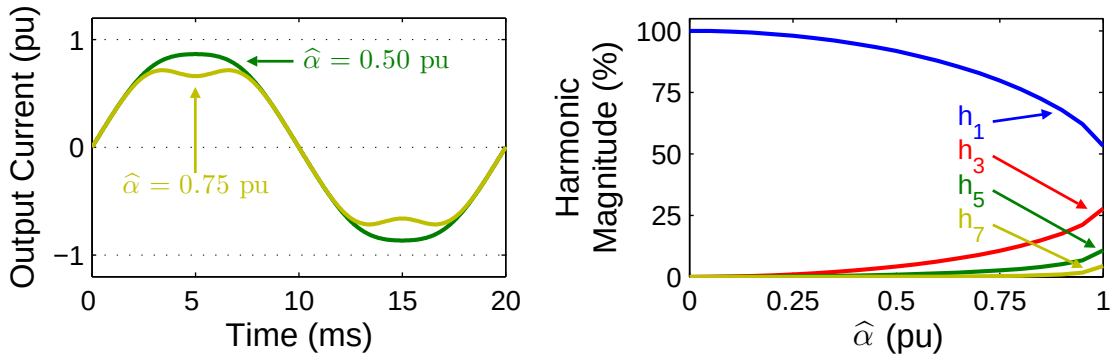


Figure 5.9: Normalised inverter output current for $\widehat{\alpha} = 0.50$ and 0.75 pu (left), and the harmonic response to increasing $\widehat{\alpha}$ (right), using the ideal I-V locus. Note that the output current is shown for $m_a = 100\%$.

Similarly, Figure 5.10 shows the inverter output currents for the same values of $\widehat{\alpha}$, and the harmonic response to increasing $\widehat{\alpha}$, now using the experimental I-V locus. As with the ideal I-V locus, the magnitude of the fundamental decreases, whilst the magnitudes of the third, fifth and seventh-order harmonics increase for increasing $\widehat{\alpha}$. The key differences are that the fundamental falls more rapidly and the third-order harmonic increases more rapidly than that for the ideal case (locus). The fifth and seventh-order harmonics are similar for the ideal and experimental loci. The only difference is for $\widehat{\alpha}$ between 0.9 and 1pu, where the ideal locus harmonics are slightly higher than those corresponding to the experimental locus. Note that the relatively small magnitudes in h_5 and h_7 have little effect on the resulting THD.

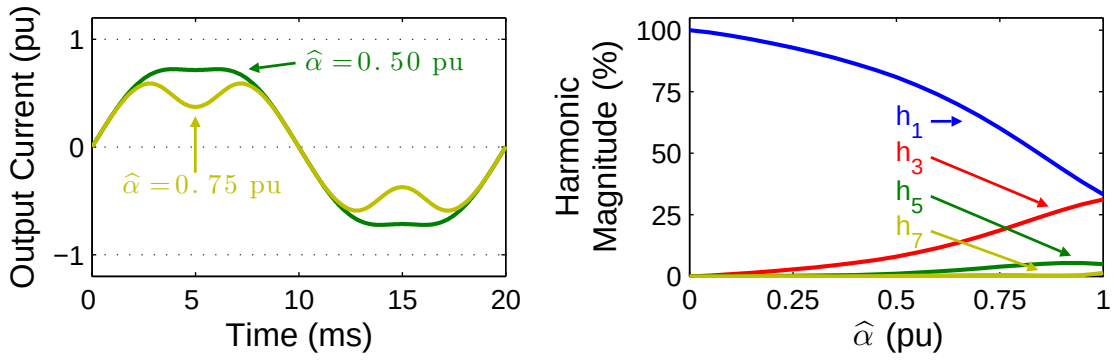


Figure 5.10: Normalised inverter output current for $\widehat{\alpha} = 0.50$ and 0.75 pu (left), and the harmonic response to increasing $\widehat{\alpha}$, (right) using the experimental I-V locus. The output current is shown for $m_a = 100\%$.

The increase in third-order harmonics, together with the decrease in fundamental magnitude, imply that the experimental locus will have a higher value of THD for the entire range of $\widehat{\alpha}$ values. This is confirmed by Figure 5.11, which shows the calculated THD vs. $\widehat{\alpha}$ for both loci, where the dashed line represents the grid THD limit of 5%. Note that the THD values shown here ignore the effect of the rectifier current ripple. The figure suggests that for a DC (fluctuating) input current, the grid THD requirements can be met providing $\widehat{\alpha}$ is limited to 0.52 or 0.34 pu, using the ideal and experimental loci, respectively. Note that the conduction losses of the uncontrolled rectifier cause the experimental I-V locus to differ from the analytical ideal case, and hence show the importance of reducing its losses.

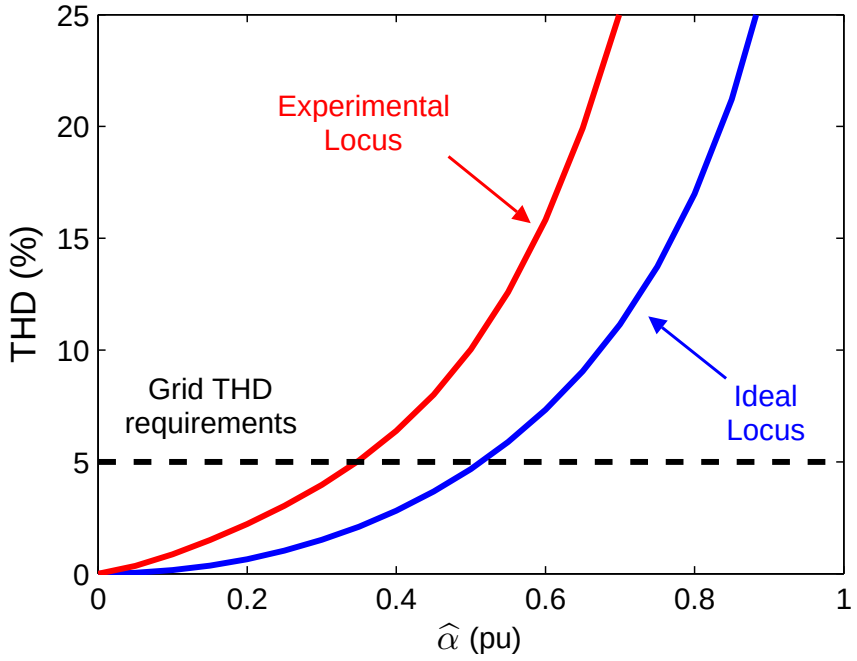


Figure 5.11: Calculated THD vs. $\widehat{\alpha}$ for both the ideal and experiential rectifier I-V loci. The dashed line represents the acceptable THD limit.

5.2.2 Rectifier Ripple

The normalised three-phase rectifier ripple has a fixed magnitude, but varying frequency. This occurs as the turbine operates over a wide range of speeds, and the rectifier ripple frequency is six times the machine frequency, f_m. The inverter output current and the corresponding harmonic spectrum are shown in Figure 5.12 for a grid frequency of 50Hz and a machine frequency of 200Hz.

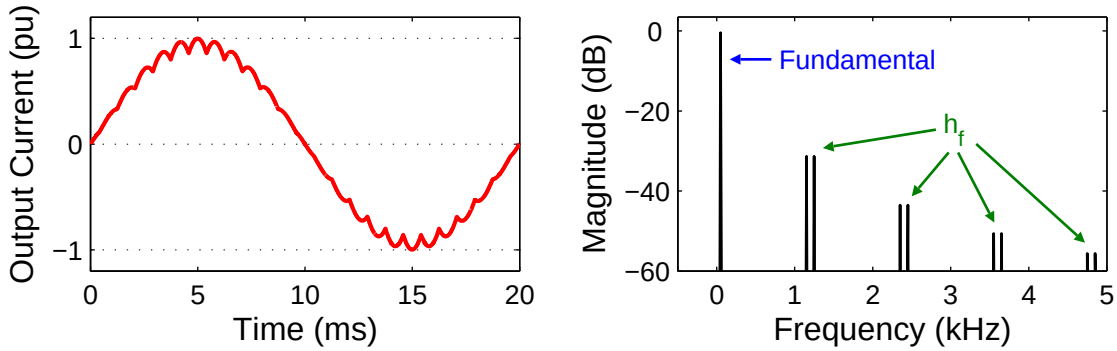


Figure 5.12: Normalised inverter output current showing the effect of the rectifier ripple (left), and its calculated harmonic spectrum (right); h_f represents harmonic frequencies.

The harmonic frequencies, h_f, are given by Equation (5.17), where f_1 is the fundamental frequency, and m is an integer. The output current THD is calculated from the FFT spectrum and is equal to 4.20%. This THD is independent of the machine frequency and the type of generator locus used.

$$h_f = m\,6 f_m \pm f_1 \tag{5.17}$$

5.2.3 The Resulting Input Current

The inverter input current contains distortion from both the rectifier ripple and the fluctuating input current, hence, these should be seen in the output current and the corresponding FFT. This is shown in Figure 5.13 for $\widehat{\alpha} = 0.7$ pu ($\widehat{\alpha}_0 = 0.7$, $m_a = 100\%$), using the ideal I-V locus. The harmonics are identified by their source.

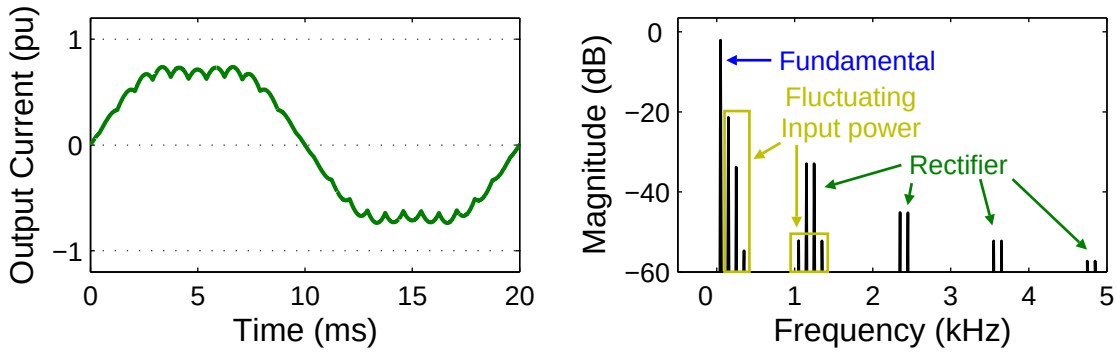


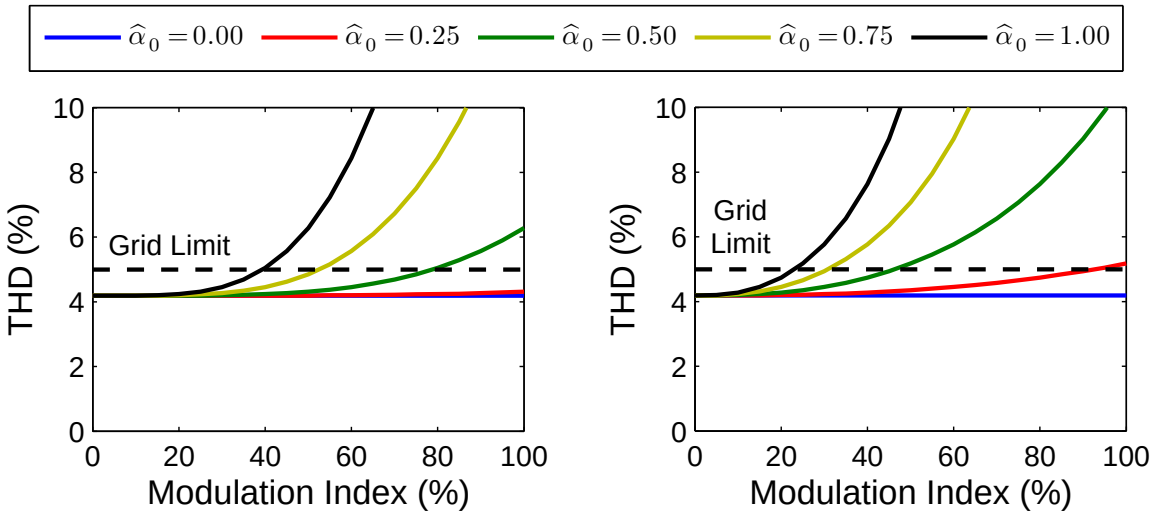
Figure 5.13: Normalised inverter output current showing the effect of the rectifier ripple and the fluctuating input power (left), and the corresponding harmonic spectrum (right).

The harmonic spectrum of the output current shows that the harmonics caused by the fluctuating input current can be found at frequencies expressed by Equation (5.18). In addition, the harmonics caused by the rectifier ripple are expressed by Equation (5.19), where m is an integer and n is an odd integer. Although multiple sidebands now appear centred around $m\,6f_m$, Figure 5.13 shows only two sidebands centred at 1.2kHz and 1 pair thereafter. Sidebands do not appear in this figure for n > 3 or m > 2, as their magnitudes are negligible, i.e. < 0.1% of the fundamental magnitude.

$$h_f = nf_1 \qquad (n > 1) \tag{5.18}$$

$$h_f = m\,6f_m \pm nf_1 \qquad (m, n \geq 1) \tag{5.19}$$

The use of a rectifier causes the inverter output current to contain a minimum of 4.19% THD. The grid limit of 5% hence allows for a 2.71% margin ($\sqrt{5^2 - 4.2^2}$). Therefore, the inverter is able to meet the grid THD requirement, if $\widehat{\alpha}$ is limited to 0.39 and 0.23pu, using the ideal and experimental I-V loci, respectively (see Figure 5.11). Recall that $\widehat{\alpha} = \widehat{\alpha}_0\, m_a$. This implies that as the machine speed decreases, so too does the induced voltage and hence $\widehat{\alpha}_0$. Therefore, the modulation index should be reduced with speed to maintain a constant output current THD. This concept is shown in Figure 5.14 which shows the output current THD as a function of m_a for various values of $\widehat{\alpha}_0$ (pu).

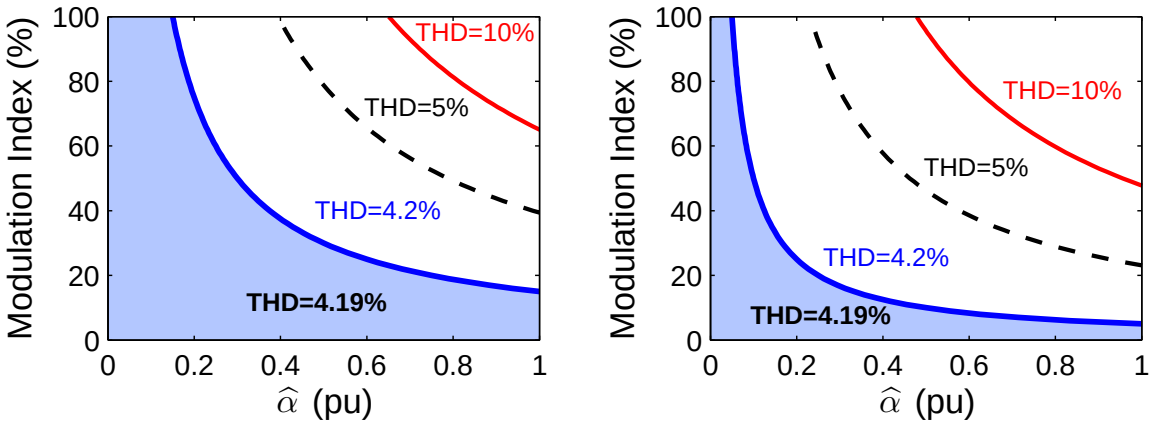


(a) Ideal I-V locus

(b) Experimental I-V locus

Figure 5.14: Output current THD vs. modulation index and $\widehat{\alpha}_0$ (pu), for the (a) ideal, and (b) experimental I-V loci. The dashed line represents the grid THD limit of 5%.

The THD information seen in Figure 5.14 can be rearranged and presented as a contour plot, as shown in Figure 5.15 for THD contours of 4.2, 5 and 10%. These contours represent just over the minimum output current THD (caused by the rectifier ripple), the acceptable grid limit and twice the acceptable limit. The THD contours correspond to fixed values of $\widehat{\alpha}$, e.g. an output current THD of 5% corresponds to $\widehat{\alpha}$ values of 0.394 and 0.231 pu using the ideal and experimental loci, respectively. The figure shows that a constant THD can be maintained by reducing m_a in proportion with the generator speed ($\widehat{\alpha}$). Note that the rectifier ripple distortion occurs for all generator speeds, hence the THD for small values of $\widehat{\alpha}$ is 4.19%, as indicated by the shaded regions.



(a) Ideal I-V locus

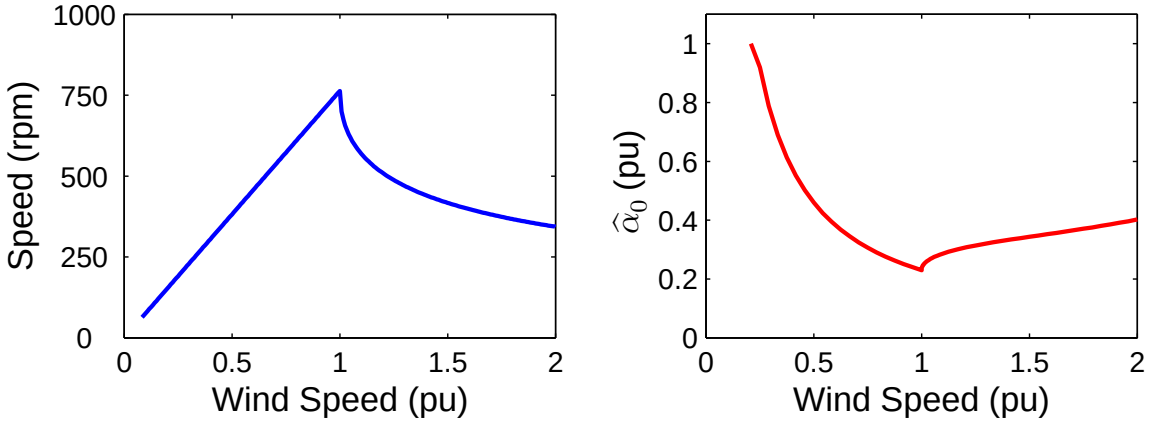
(b) Experimental I-V locus

Figure 5.15: THD vs. $\widehat{\alpha}_0$ and modulation index contour plot, for the (a) ideal, and (b) experimental I-V loci. The shaded regions represents the minimum output THD, caused by the rectifier, while the dashed line represents the grid THD limit of 5%.

Figures 5.15 and 5.14 indicate that the inverter must reduce m_a as the generator speed decreases ($\widehat{\alpha}_0$ increases) to maintain a constant THD. The inverter may reduce the modulation index automatically as the turbine speed and hence power decrease with wind speed. This is further investigated in the following subsection.

Modulation Index and $\widehat{\alpha}_0$ Variation with Wind Speed

Recall that α_0 represents the ratio of the peak grid to rectified open-circuit voltage, and that the peak turbine speed occurs at rated wind speed. This implies that the minimum $\widehat{\alpha}_0$ will occur at rated wind speed and that $\widehat{\alpha}_0$ will be larger at all other wind speeds. This is shown in Figure 5.16, which shows the turbine speed and the resulting $\widehat{\alpha}_0$ as a function of wind speed. Note that Figure 5.16(a) is the normalised equivalent of Figure 1.5(c).

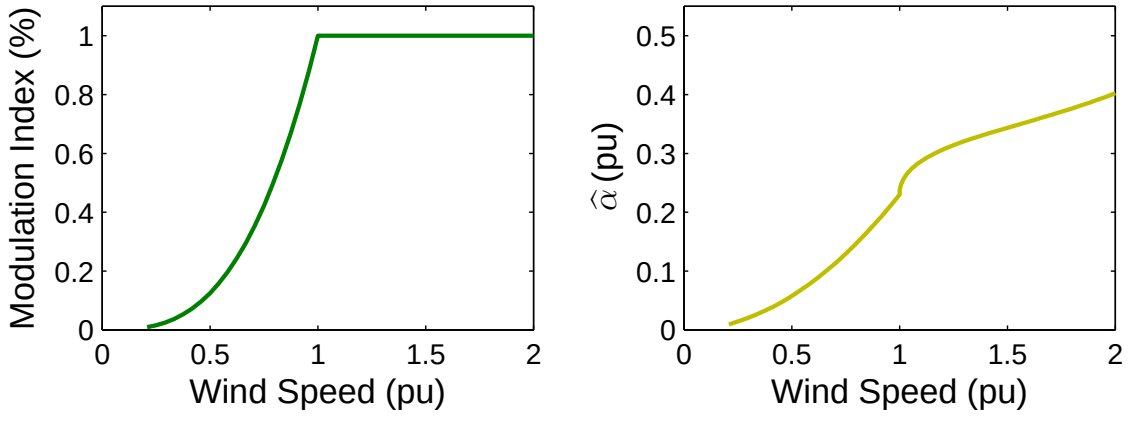


(a) Turbine speed

(b) $\widehat{\alpha}_0$

Figure 5.16: Turbine speed (a) and the resulting $\widehat{\alpha}_0$ (b), as a function of wind speed. Note that $\widehat{\alpha}_0$ is equal to 0.23pu at rated wind speed.

Consider wind speeds below rated. The turbine and inverter output power, and hence the required modulation index increases with the cube of wind speed. Therefore, $\widehat{\alpha}$ must increase with the square of wind speed, as $\widehat{\alpha}_0$ is inversely proportional to wind speed (recall that $\widehat{\alpha} = \widehat{\alpha}_0.m_a$). A summary of the modulation index and the resulting $\widehat{\alpha}$ is shown in Figure 5.17, over a wide range of normalised wind speeds. Note that the modulation index is 100% above rated wind speed as the inverter aims to deliver rated power to grid, and the resulting $\widehat{\alpha}$ is identical to $\widehat{\alpha}_0$ for this range of wind speeds.



(a) Modulation index

(b) $\widehat{\alpha}$

Figure 5.17: Modulation index (a) and the resulting $\widehat{\alpha}$ (b), as a function of wind speed. Note that $\widehat{\alpha}$ is equal to 0.23pu at rated wind speed.

The open-loop inverter output current THD is determined from the above $\widehat{\alpha}$ curve, and the THD vs. $\widehat{\alpha}$ curve (see Figure 5.14(b)). The resulting output current THD is shown in Figure 5.18, as a function of normalised wind speed. The THD is shown to increase from the 4.19% at low wind speeds, which is solely caused by the rectifier ripple, up to the grid requirement at rated wind speed. The THD then increases above the 5% grid requirement, with wind speed, at rate proportional to $\widehat{\alpha}$. The figure highlights that the inverter is able to meet the grid THD requirements below rated wind speed, providing a suitable generator is used ($\widehat{\alpha}_0$). However, the effects of resonance, i.e. input current harmonic amplification, are not considered here. This is examined in Section 5.3.9.

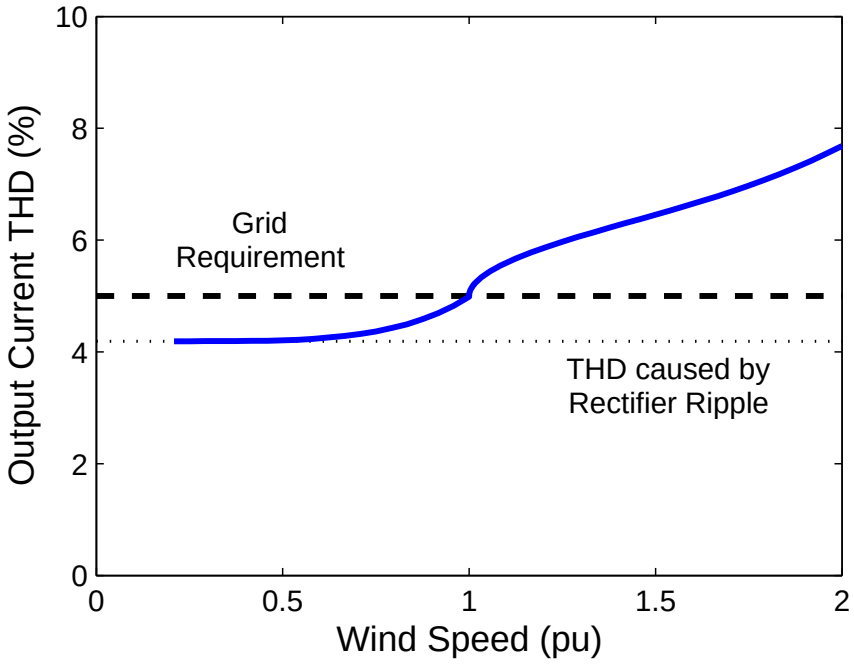
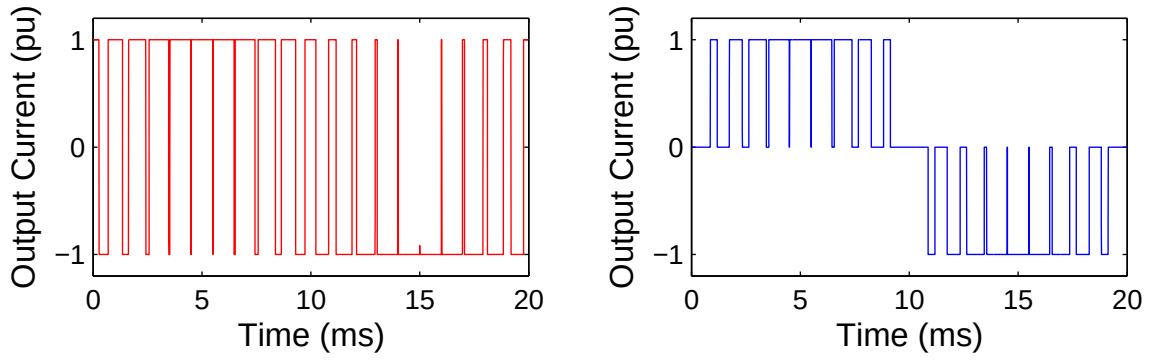


Figure 5.18: Open-loop inverter output current THD vs. wind speed. The dashed line represents the grid THD requirement, whilst the dotted line corresponds to the THD caused by the rectifier ripple.

5.2.4 PWM Switching Schemes

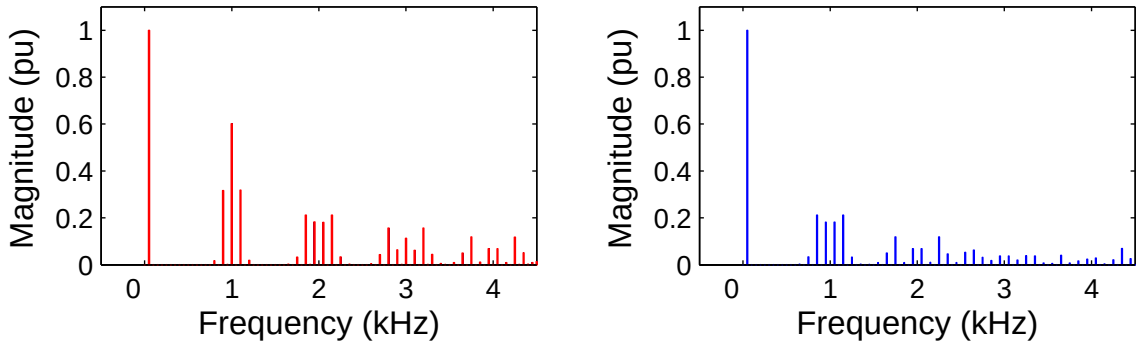
In addition to the input current distortion caused by the non-ideal current source, the PWM switching of the current wave-shaper significantly contributes to the inverter output current THD. Two varieties of PWM switching exist, these are the bipolar and unipolar schemes. An example of each waveform is shown in Figure 5.19, for a modulation index of 100%. Their corresponding harmonic spectra are shown in Figure 5.20.



(a) Bipolar PWM

(b) Unipolar PWM

Figure 5.19: Normalised PWM switching scheme waveforms, showing the (a) Bipolar, and (b) Unipolar varieties, for a switching frequency of 1kHz.



(a) Bipolar PWM spectrum

(b) Unipolar PWM spectrum

Figure 5.20: Harmonic spectra of the (a) bipolar, and (b) unipolar PWM switching scheme waveforms. Note: the harmonic magnitudes now have linear scales, which were logarithmic in earlier figures.

The unipolar PWM waveform has lower harmonics than the bipolar waveform, as it changes polarity at twice the inverter frequency, as does a sinusoid, whereas the bipolar PWM waveform changes polarity at the inverter switching frequency, f_{sw}. The harmonic spectra shows that the harmonics appear as sidebands that are centred at integer multiples of the PWM switching frequency, f_{sw}. These harmonic frequencies, h_f, are expressed by Equation (5.20), where f_1 is the fundamental frequency, m is an integer, and n is an odd integer. Comparison of the harmonic spectra indicate that the unipolar harmonics centred at m f_{sw} have the same amplitude as the bipolar harmonics centred at $2m$ f_{sw}. The unipolar waveform does not contain the bipolar harmonics that are centred at odd multiples of f_{sw}, which is verified in [67]. The reduced harmonic content implies that the

unipolar waveform contains less THD than the bipolar equivalent. Comparison of the calculated THDs confirms this, i.e. the bipolar PWM waveform THD is 96.2%, whilst the unipolar waveform THD is 49.5%. Despite the significant increase in THD, the bipolar PWM switching scheme is used more often than the unipolar alternative [108].

$$h_f = mf_{sw} \pm nf_1 \tag{5.20}$$

Effect of Modulation Index Variation

The bipolar PWM waveform harmonics are further analysed in [67], where the effect of varying the inverter modulation index is also taken into consideration. However, only half of this information applies to the unipolar PWM case, and as such, a detailed harmonic analysis of the unipolar PWM waveform is presented here. Note that the PWM switching frequency is set to 4kHz, as this corresponds to that used experimentally in Chapter 4.

The unipolar PWM waveform was simulated and analysed, over a wide range of modulation indices. It was found that the total harmonic components, h_{tot}, varied somewhat quadratically with modulation index, whilst the fundamental magnitude was directly proportional to m_a. The resulting THD is hence inversely proportional to the inverter modulation index, as shown in Figure 5.21, where the dashed line represents the grid THD limit of 5%. It is clearly seen that the output current fails to meet the THD requirement over the entire range of modulation index.

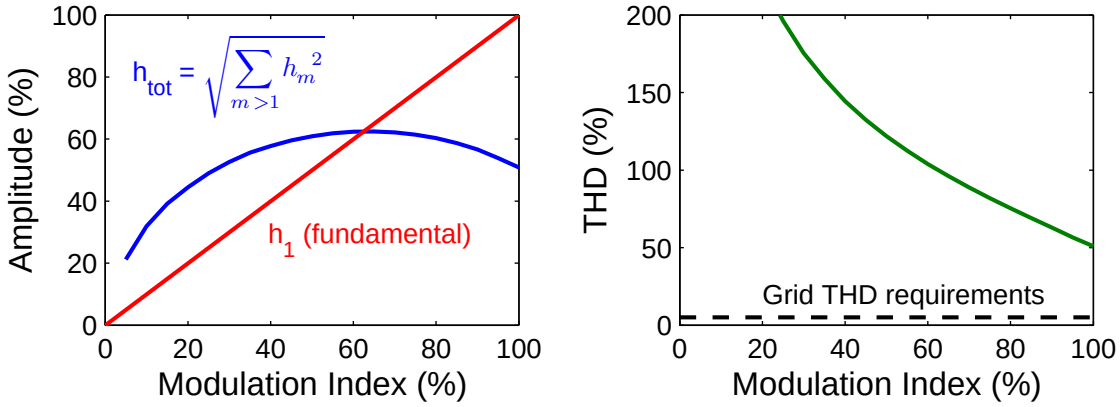


Figure 5.21: Calculated total harmonic amplitude (left), and distortion (right) vs. inverter modulation index, for a unipolar PWM waveform. Note that the fundamental magnitude is also shown with harmonic amplitude, as the THD is inversely proportional to it. The dashed line represents the grid THD limit of 5%.

The harmonic information presented in Figure 5.21 is summarised in Table 5.1. The table identifies the harmonic frequencies, their magnitudes, and the total harmonic distortion for various modulation indices, using an ideal DC input current ($\widehat{\alpha}_0 = 0$).

Table 5.1: Harmonic information regarding the unipolar PWM waveform, for various modulation indices. The harmonic frequencies are expressed as functions of the fundamental and inverter switching frequencies,(f_1 and f_{sw}), whilst the harmonic magnitudes are expressed as percentages relative to the peak of the PWM waveform.

h_f \ m_a	100%	80%	60%	40%	20%
h_1	100	80	60	40	20
$\mathrm{f}_{sw} \pm f_1$	18.15	31.45	37.01	32.58	18.95
$\mathrm{f}_{sw} \pm 3f_1$	21.19	13.92	7.06	2.34	
$\mathrm{f}_{sw} \pm 5f_1$	3.34	1.24			
$2\mathrm{f}_{sw} \pm f_1$	6.75	10.50	0.79	15.75	16.26
$2\mathrm{f}_{sw} \pm 3f_1$	1.07	11.48	13.21	6.93	1.15
$2\mathrm{f}_{sw} \pm 5f_1$	11.88	8.38	3.40	0.64	
$2\mathrm{f}_{sw} \pm 7f_1$	5.08	1.73			
$2\mathrm{f}_{sw} \pm 9f_1$	0.88				
$3\mathrm{f}_{sw} \pm f_1$	3.77	3.04	6.98	0.60	12.33
$3\mathrm{f}_{sw} \pm 3f_1$	1.78	5.58	4.57	8.79	2.31
$3\mathrm{f}_{sw} \pm 5f_1$	3.00	5.91	7.14	2.23	
$3\mathrm{f}_{sw} \pm 7f_1$	6.20	6.07	2.09	0.22	
$3\mathrm{f}_{sw} \pm 9f_1$	5.34	1.93	0.29		
$3\mathrm{f}_{sw} \pm 11f_1$	1.78	0.35			
$3\mathrm{f}_{sw} \pm 13f_1$	0.39				
$4\mathrm{f}_{sw} \pm f_1$	2.46	0.50	2.53	5.25	7.89
$4\mathrm{f}_{sw} \pm 3f_1$	1.53	1.12	4.17	5.77	3.43
$4\mathrm{f}_{sw} \pm 5f_1$	0.72	3.79	4.40	4.22	0.29
$4\mathrm{f}_{sw} \pm 7f_1$	3.55	3.35	4.57	0.87	
$4\mathrm{f}_{sw} \pm 9f_1$	2.39	4.70	1.46		
$4\mathrm{f}_{sw} \pm 11f_1$	4.67	2.00	0.23		
$4\mathrm{f}_{sw} \pm 13f_1$	2.51	0.50			
$4\mathrm{f}_{sw} \pm 15f_1$	0.78				
$4\mathrm{f}_{sw} \pm 17f_1$	0.14				
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
$mf_{sw} \pm nf_1$	$\cdots$	$\cdots$	$\cdots$	$\cdots$	$\cdots$
h_{tot}	50.54	59.98	62.00	57.51	44.31
THD	50.54	74.97	103.34	143.78	221.53

5.2.5 The Inverter Output Current

This section examines the combined effect of all three harmonic sources on the output current. An example of this is shown in Figure 5.22, which shows the distorted inverter input current and the resulting inverter output current. The input current shows the rectifier ripple and fluctuating input current, for a generator frequency of 200Hz, and $\widehat{\alpha}_0 = 0.8$pu, respectively. The unipolar PWM switching operates at 4kHz, with a modulation index of 100%. The FFT of the inverter output current reveals the harmonic spectrum shown in Figure 5.23. The harmonics are grouped and identified by their source.

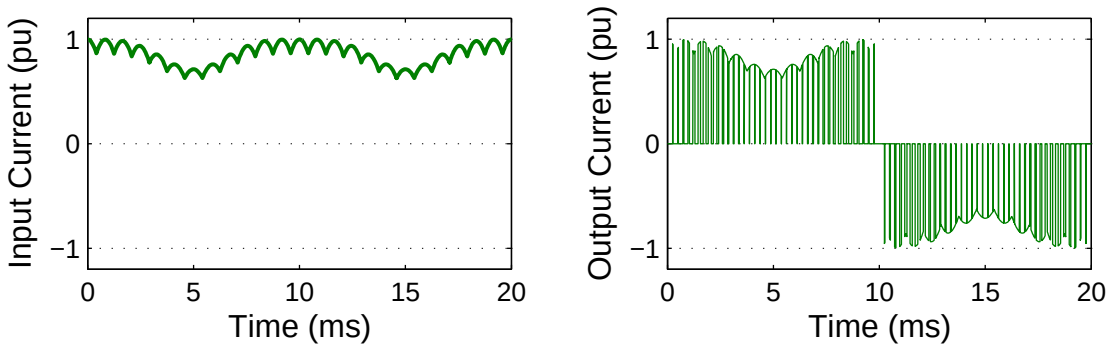


Figure 5.22: The normalised inverter input (left), and output (right) current, showing the effects of the rectifier ripple, fluctuating input power, and the unipolar PWM switching for $\widehat{\alpha} = 0.8$ pu ($\widehat{\alpha}_0 = 0.8$, and $m_a = 100\%$).

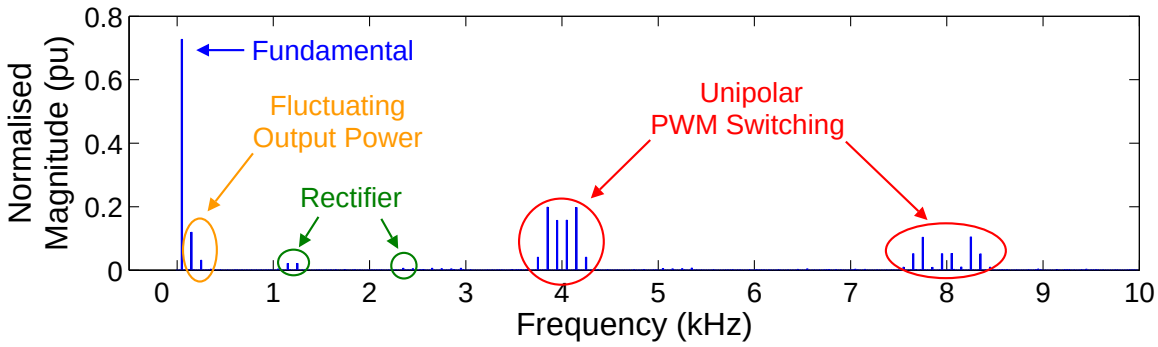


Figure 5.23: Harmonic spectrum of the inverter output current, identifying the harmonics caused by the rectifier, fluctuating input power, and the unipolar PWM switching.

Figures 5.22 and 5.23 indicate that the majority of the output current distortion is associated with the PWM switching. The harmonic spectrum also shows that the harmonics caused by fluctuating input power, rectifier, and PWM switching, occur at low,

medium and high frequencies, respectively. It was previously shown, in Section 5.2.3, that the low-frequency harmonics could be reduced by reducing the modulation index. This action could be applied again, however, it will also reduce the fundamental magnitude and hence increase the overall THD. The effect of modulation index variation on the inverter output current is summarised in Figure 5.24, where the calculated THD includes the harmonic distortion caused by the rectifier, fluctuating input power and the unipolar PWM switching. The reduction of modulation index clearly increases the output current THD, with the exception of $\widehat{\alpha}_0$ greater than 0.75pu, where the output THD can be reduced for modulation indices above about 70%.

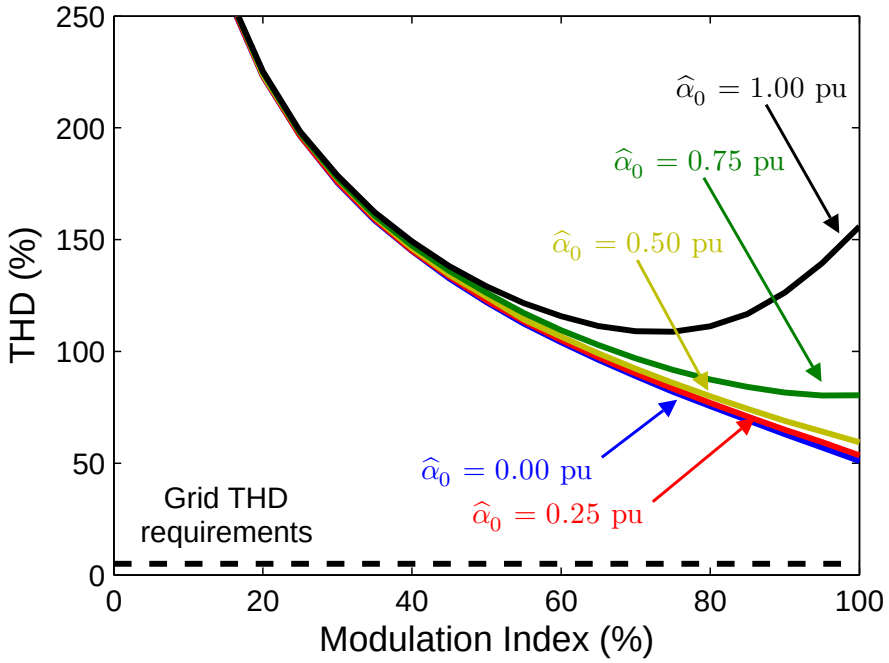


Figure 5.24: Calculated total harmonic distortion vs. modulation index for various values of $\widehat{\alpha}_0$. The THD can be minimised, via modulation index manipulation, for $\widehat{\alpha}_0 > 0.75$pu, however it greatly exceeds the acceptable limit (dashed line).

5.2.6 Reducing Harmonic Distortion

The previous section showed that the inverter output current is unable to meet the grid THD requirement, without some form of harmonic reduction. It is anticipated that the low-pass filter will sufficiently attenuate the PWM switching harmonics, however, the low-frequency harmonics, caused by the fluctuating input power, will be difficult to eliminate, as they occur in the vicinity of the fundamental. In addition, the medium-frequency

harmonics may be difficult to eliminate, as the turbine operates at various speeds, which causes the harmonic frequencies to also vary. This section briefly discusses several techniques to attenuate / eliminate harmonics, these include using: low-pass and notch filters, reducing $\widehat{\alpha}$, and using a feed-froward controller.

Low-Pass Filter

The low-pass filter is extensively used in electronic and communication systems, to attenuate high frequency components whilst allowing low frequencies through. For this application, a second-order CL type low-pass filter is required as this sufficiently couples the current source inverter to the voltage source grid, according to the *impedance mismatch criteria* [105]. An example of this type of filter is shown in Figure 5.25, where R_d is the damping resistor.

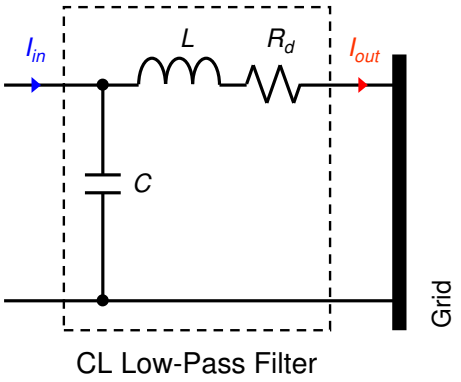


Figure 5.25: CL type low-pass filter, as used to couple the current source inverter to the grid. R_d represents the damping resistor used to control the filter quality factor.

The filter cutoff frequency is commonly referred to as the resonant frequency, f_{res}, as the filter has an infinite gain at that frequency if there is no damping resistance. The gain at the resonant frequency is known as the quality factor, Q, and can be reduced by using a series damping resistor, R_d (seen in the above figure). The resonant frequency and quality factor are given by Equations (5.21) and (5.22), respectively, whilst Figure 5.26 shows the effect that varying the damping resistance has on the quality factor. Note that the filter gain represents the ratio of output to input current, i.e. $I_{out} \,/\, I_{in}$, and that the gain is presented in decibels (dB).

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{5.21}$$

$$Q = \frac{1}{R_d}\sqrt{\frac{L}{C}} \tag{5.22}$$

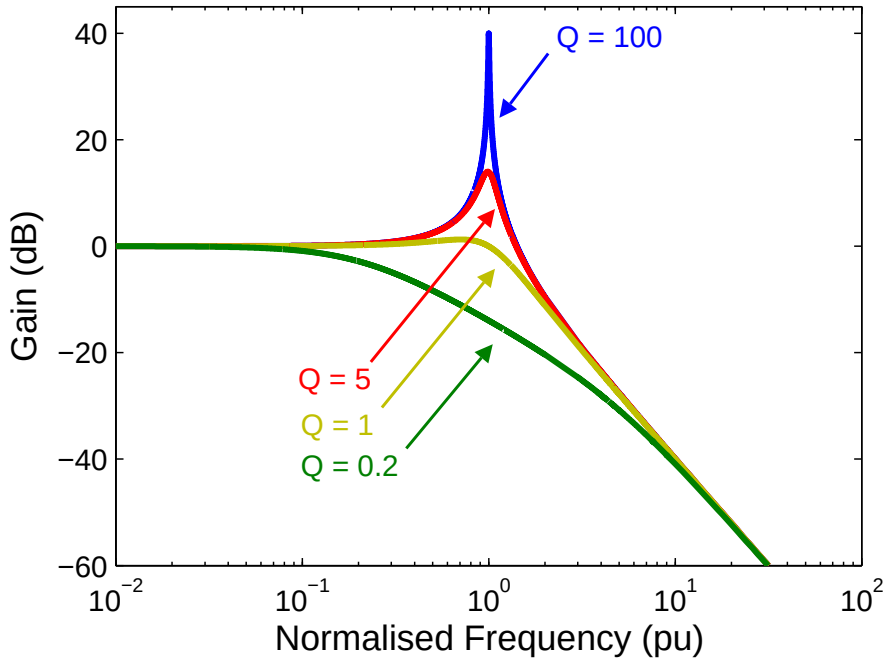


Figure 5.26: Normalised low-pass filter frequency response, showing the effect of varying the filter quality factor, Q.

The CL filter is able to substantially attenuate the high-frequency PWM harmonics if the resonant frequency is selected to be small compared to the PWM switching frequency. Despite this, there are two drawbacks of using this type of low-pass filter. Firstly, the harmonics will be amplified if they occur at the resonant frequency and if the quality factor exceeds 1. The filter will have a fixed resonant frequency and may correspond to the frequency of the rectifier ripple, as the turbine operates over a wide range of speeds. This may amplify the harmonics and increase the output current THD. Secondly, the low-pass filter is unable to attenuate the low-frequency harmonics caused by the fluctuating input power, as these occur close to the fundamental frequency.

Notch Filters

Notch filters are used to eliminate specific frequencies, whilst passing all others. They comprise of a series LC resonant network in a voltage divider configuration [109]. An example of a notch filter and its position, relative to the proposed grid-connected inverter,

is shown in Figure 5.27. The figure includes a series connected damping resistor, R_d, which is used to control the filter quality factor. The effect of varying the quality factor on the normalised filter gain is shown in Figure 5.28.

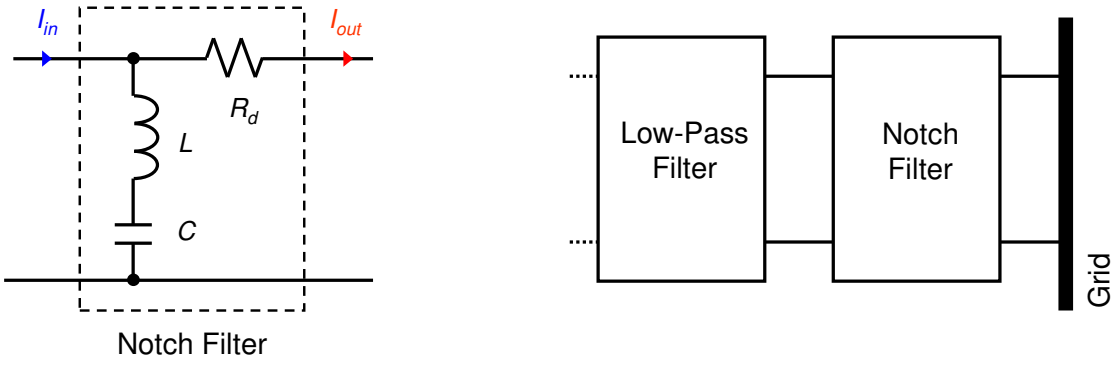


Figure 5.27: Notch filter (left), and its position in the proposed grid-connected inverter system (right).

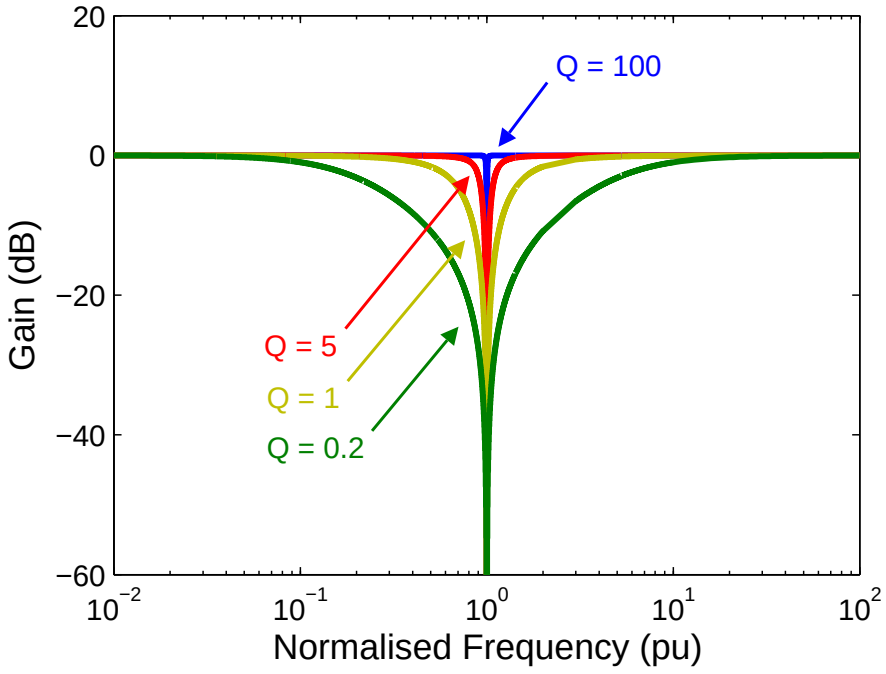


Figure 5.28: Normalised notch filter frequency response, showing the effect of increasing the quality factor, Q.

The above figure shows that the filter shunt impedance approaches zero as the filter input frequency approaches the resonant frequency. This provides a path to ground, which

diverts the input current through the LC network and hence creates the *notch* in the filter frequency response. The notch filter resonant frequency and quality factor are identical to those for the above low-pass filter, see Equations (5.21) and (5.22).

Although notch filters can be used to eliminate fixed frequency harmonics, e.g. the third and fifth-order harmonics of the fundamental, they can not be used to eliminate the harmonics caused by the rectifier ripple, as this harmonic frequency varies with the generator speed. The main drawback of notch filters is that they can potentially become grid harmonic sinks. That is, if tuned to the grid frequency harmonics, notch filters will draw large harmonic currents from the grid, which is undesirable. The Australian Standards also state that the inverter should not significantly sink frequencies used for ripple control (which allows remote grid load optimisation [110]) by the local electrical distributor [96]. Notch filters also attract cost, and hence, are no longer considered.

Reduction of $\widehat{\alpha}$

Section 5.2.1 showed that low frequency harmonics, i.e. h_{3-7}, can be reduced by reducing $\widehat{\alpha}$. This is achieved by reducing either the m_a or $\widehat{\alpha}_0$. The modulation index is easier to adjust, as this is handled by the controller. The drawback is that the output current magnitude is linearly proportional to the m_a, i.e. the output current distortion improves at the expense of the inverter output current magnitude. Hence a distortion / power trade-off exists.

In contrast, the reduction of α_0 does not affect the magnitude of the output current, however, this is more difficult to achieve in practise, as this implies that the generator open-circuit voltage must increase. This can be achieved by:

- increasing the machine speed - It was seen in part I that the turbine speed may be controlled by adjusting the electromagnetic torque, however, to increase its speed the turbine may not operate at its optimal c_p which will reduce the turbine and hence the inverter output power.

- modifying the machine characteristics - The back-EMF is dictated by the electrical frequency, ω_e, and the back-EMF constant, k, hence increasing either k or the number of pole-pairs will reduce $\widehat{\alpha}_0$. The drawback is that the machine must be physically altered for such changes to take effect, e.g. the permanent magnets may be replaced those with a higher energy density.

Although the reduction of $\widehat{\alpha}$ is required to minimise the input current ripple, the drawback of this is that the PM generator operates more in the constant current region of its I-V locus. The higher currents ($\beta \rightarrow 1$) cause higher stator copper losses, and hence reduce the generator efficiency.

Advanced Control

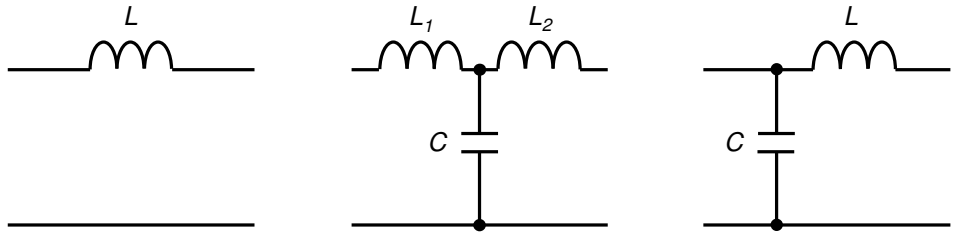
The inverter is presently controlled in an open-loop manner, and hence the output current contains the harmonics found in the input current. The use of a more sophisticated control system, such as a feedback or feed-forward controller would improve the output current waveform. The feedback controller would adjust the current-wave shaper duty-cycle such that the output current would be sinusoidal. This type of controller, however, requires an expensive isolated output current sensor. In contrast, a feed-forward controller would adjust the wave-shaper duty-cycle, based on the sampled input current and the known simple relationship between the duty-cycle and input and output currents. This attracts a lower cost, as the current sensor is not required to be isolated, however, both systems require a fast processor to rapidly sample their respective currents.

In summary, a low-pass filter and a feed-forward controller should allow the grid-connected inverter to deliver high quality power to the grid. These are further discussed in Sections 5.3 and 5.4, respectively.

5.3 Low-Pass Filter Analysis

The low-pass filter is situated between the unfolding circuit and the grid. Its primary role is to attenuate the high-frequency PWM current harmonics, such that the output current THD meets the grid requirements, i.e. THD $< 5\%$. In addition, the choice of filter component can also affect the inverter power factor. This is examined in Section 5.3.6, which emphasises that the inverter power factor must lie between 0.8 leading and 0.95 lagging, for inverter outputs between 20% and 100% of rated volt-amperes.

It was previously mentioned in Section 4.2.5 that the low-pass filter configuration is determined by applying the filter *impedance mismatch criteria* to the inverter input type, i.e. current or voltage source. Voltage source inverters (VSI) make up the majority of commercially available inverters, and use either a single inductive (L) or inductive-capacitive-inductive (LCL) type low-pass filter. The L filter is the simplest and most common filter type amongst VSI [61], and is well suited to high-frequency PWM converters [111]. The drawback, however, is that L type filters attenuate high-frequencies at only 20dB/decade, and so its use is restricted in high-powered low-frequency converter applications [111, 112]. The LCL filter addresses these problems, as it attenuates frequencies at 60dB/decade [61], beyond its resonant frequency, and it so achieves reduced levels of harmonic distortion at lower switching frequencies and with less total inductance [111, 112] and hence less losses. In contrast, a capacitive-inductive (CL) type filter is used with current source inverters (CSI), and attenuates frequencies at 40dB/decade, beyond its resonant frequency. A summary of these low-pass filter configurations is shown in Figure 5.29.



(a) L type (b) LCL type (c) CL type

Figure 5.29: Typical grid-connected inverter low-pass filter varieties, showing the (a) L, (b) LCL and (c) CL types used. The L and LCL filters are used to couple voltage source inverters to the grid, whilst the CL type couples a current source inverter to the grid.

The main drawback of the LCL and CL type filters is resonance, which can potentially increase harmonics if the filter gain at the resonant frequency is greater than 1 and the

resonant frequency, f_{res}, coincides with any low or medium-frequency harmonics. This was seen in the experimental testing stage (Section 4.4.3) where the filter resonated at 450Hz, i.e. the ninth-order harmonic. The effect of resonance can be reduced by limiting the filter gain at the resonant frequency. This, however, requires an understanding of the filter and how it responds to various input frequencies.

5.3.1 Filter Response

The filter response is determined by its transfer function, $H(s)$, which represents the complex ratio of the frequency dependent output to input, where $s = j\omega$. Note that $H(s)$ represents the ratio of the output to input voltage, for an L or LCL filter, and the ratio of output to input current, for a CL type filter. An example of an undamped CL low-pass filter transfer function is shown in Equation (5.23).

$$H(s) = \frac{1}{s^2LC + 1} \tag{5.23}$$

The filter gain, A, is the absolute value of the transfer function, and the phase delay, ϕ, is given by the argument of the transfer function, as summarised by Equations (5.24), and (5.25), respectively.

$$A = |H(s)| \tag{5.24}$$

$$\phi = \arg\left(H(s)\right) \tag{5.25}$$

The gain at the resonant frequency determines the extent of resonance and is commonly referred to as the *quality factor*, Q. Consider the undamped CL filter. The filter has an infinite quality factor, when the denominator of Equation (5.23) is zero. The frequency corresponding to this case, is known as the resonant frequency, f_{res}, and is given by Equation (5.26). The infinite gain would amplify harmonics if found at the resonant frequency, and hence increase the filter output THD. The need to limit the filter quality factor is clearly seen. In practise, this is achieved by adding damping to the filter, and is discussed in the following section. Note that f_{res} is also referred to as the cutoff frequency, f_c, and that both terms are used throughout this chapter.

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \tag{5.26}$$

5.3.2 Filter Damping

The CL low-pass filter can be damped by introducing a damping resistor, R_d, to the circuit. The damping resistor can be connected in one of four ways, as listed below and summarised in Figure 5.30. Note that configuration 4 was previously seen in Section 5.2.6.

1) connected in series with the capacitor,
2) connected in parallel to the capacitor,
3) connected in parallel to the inductor, or
4) connected in series with the inductor.

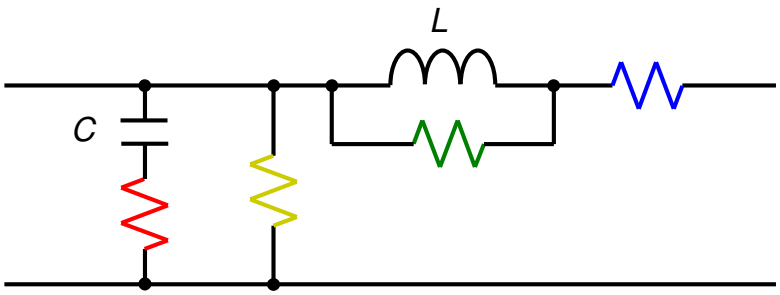


Figure 5.30: Damped CL low-pass filter, showing four configurations.

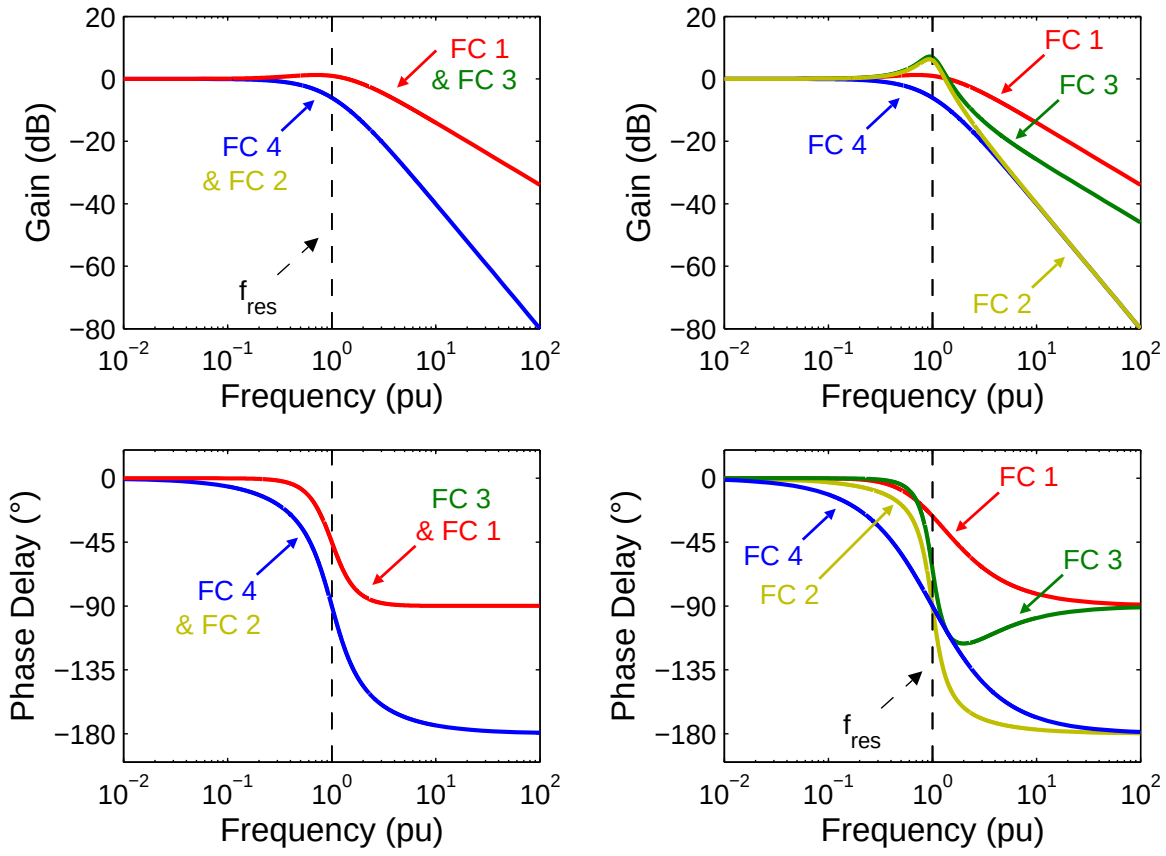
The quality factor is a function of the filter characteristic impedance, Z_0, the damping resistance and the filter configuration; Z_0 is expressed by Equation (5.27). The filter is said to be *over*, *critically* and *under*-damped if Q is less than, equal to and greater than 0.71 $(1/\sqrt{2})$, respectively. Although a quality factor of less than 1 prevents harmonic amplification, it is generally acceptable for a switched-mode power supply filter to be designed with a Q between 2 and 4 [105].

$$Z_0 = \sqrt{\frac{L}{C}} \tag{5.27}$$

5.3.3 Damped Filter Response and Configuration Comparison

Examples of damped low-pass filter responses are shown in Figure 5.31, for each of the four damped filter configurations (FC) 1–4. Figures 5.31(a) and 5.31(b), show the gain and phase delay as a function of input filter frequency, for damping resistances equal to $Z_0\,\Omega$ and $2\,Z_0\,\Omega$, respectively. Note that the filter input frequency is shown on a logarithmic scale, ranges from 0.01 to 100pu and is normalised relative to the resonant frequency.

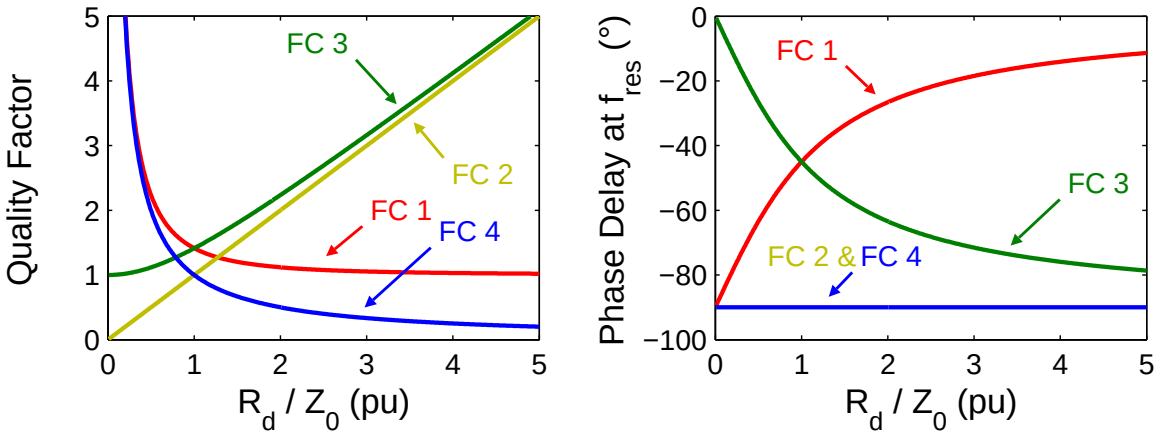
The gain and phase delay plots of FC 1 and FC 3 are identical for a damping resistance equal to the characteristic impedance, as are those of FC 2 and FC 4 (Figure 5.31(a)). As the damping resistance increases, the gain and phase delay plots become unique (see Figure 5.31(b)). In general, FC 1 and FC 3 behave similarly, as do FC 2 and FC 4. Generally, the gain of an n^{th}-order low-pass filter rolls-off at $-20\,n$ dB/decade and the phase delay approaches $-90\,n^{\circ}$ at high frequencies. This indicates that FC 1 and FC 3 behave as first-order low-pass filters, whilst FC 2 and FC 4 act like second-order low-pass filters. This implies that FC 2 and FC 4 will yield a cleaner (lower THD) output current than FC 1 and FC 3.



(a) $R_d = Z_0\,\Omega$ (b) $R_d = 2\,Z_0\,\Omega$

Figure 5.31: Normalised CL low-pass filter gain and phase margin comparison, for (a) $R_d = Z_0\,\Omega$ and (b) $R_d = 2\,Z_0\,\Omega$. Filter configurations (FC) 1 and 3, behave as first-order filters, whilst FC 2 and 4 behave like second-order filters. Note that the frequency is normalised relative to the resonant frequency, f_{res}.

The above figure showed that the filter quality factor and phase delay at the resonant frequency, varies with damping resistance and the selected filter configuration. This is further examined and verified in Figure 5.32, for various values of damping resistance, however, the phase delay of FC 2 and FC 4 is independent of the ratio of R_d to Z_0. This information and other key filter features is summarised in Table 5.2. Note that the damping resistance is normalised, i.e. it is expressed relative to the characteristic impedance.



(a) Quality factor

(b) Phase delay

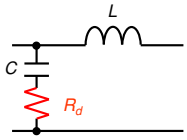
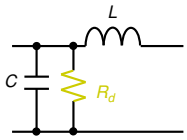
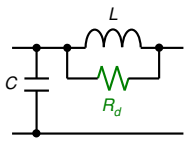
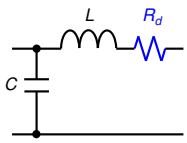
Figure 5.32: Filter gain (a) and phase delay (b), at the resonant frequency, f_{res}, of each filter configuration, as a function of damping resistance, R_d. Note that the damping resistance is normalised, i.e. it is expressed relative to the characteristic impedance, Z_0.

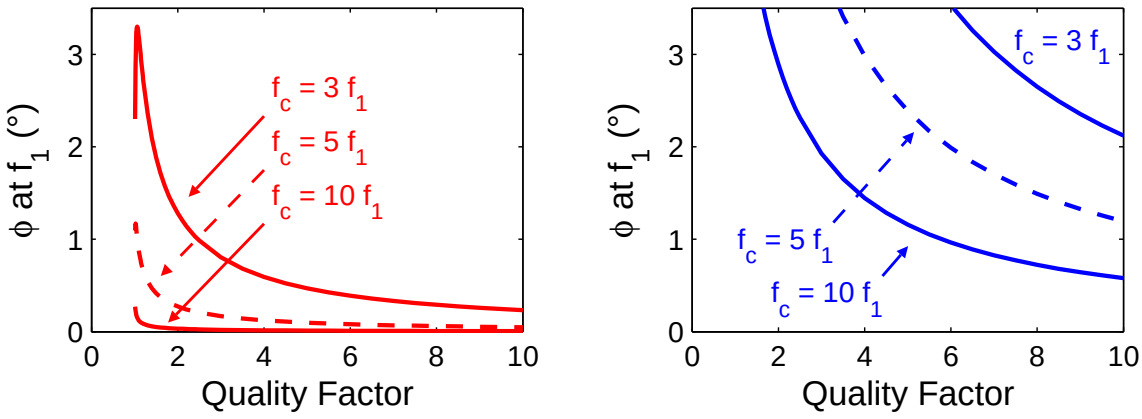
Filter Induced Phase Delay

Although the above figures and table shows that the low-pass filter introduces a phase delay, it is only the phase delay at the fundamental frequency (ϕ at f_1) that is of significance, as this can affect the inverter power factor. Providing the filter Q is greater than 1 and the resonant frequency is significantly greater than the fundamental frequency, the ϕ at f_1 is small and hence negligible. This is shown in Figure 5.33, where the filter delay (at the fundamental frequency) is plotted as a function of Q, for resonant frequencies equal to $3\,f_1$, $5\,f_1$ and $10\,f_1$. It is seen that the filter delay decreases as Q increases, and as the f_{res} increases.

Recall that FC 1 and FC 3 have quality factors greater than one, for all values of R_d. This information, together with the knowledge of low-frequency harmonics, h_{3-7} (from Section 5.2.1), implies that the f_{res} should be designed to be at least 9 times the f_1, to

Table 5.2: Comparison of the key low-pass filter properties, for each of the four damped filter configurations (FC).

FC	Circuit	Transfer function, $H(s)$	Quality Factor, Q	Phase delay at f_{res} (°)	Roll-off rate beyond f_{res}
1		$\frac{sCR_d+1}{s^2CL+sCR_d+1}$	$\sqrt{\left(\frac{Z_0}{R_d}\right)^2+1}$	$90-\tan^{-1}\left(\frac{R_d}{Z_0}\right)$	−20dB/decade
2		$\frac{R_d}{s^2CLR_d+sL+R_d}$	$\frac{R_d}{Z_0}$	−90	−40dB/decade
3		$\frac{sL+R_d}{s^2CLR_d+sL+R_d}$	$\sqrt{\left(\frac{R_d}{Z_0}\right)^2+1}$	$-\tan^{-1}\left(\frac{R_d}{Z_0}\right)$	−20dB/decade
4		$\frac{1}{s^2CL+sCR_d+1}$	$\frac{Z_0}{R_d}$	−90	−40dB/decade



(a) Filter configurations 1 and 3

(b) Filter configurations 2 and 4

Figure 5.33: Filter delay at the fundamental frequency (ϕ at f_1) vs. quality factor for filter configurations (a) 1 and 3, and (b) 2 and 4. The curves represent cutoff frequencies (f_c) equal to 3, 5 and 10 times that of the fundamental.

avoid low-frequency harmonic amplification (as Q > 1). Therefore, as a general guideline, the filter resonant frequency should be selected to be at least one decade above the fundamental, when using the PM generator current source. Using this recommendation, the phase delay at f_1 for FC 1 and FC 3 will be very small, i.e. $< 0.25°$, and is hence negligible. In contrast, the ϕ at f_1 caused by FC 2 and FC 4 will be between 3° and 1° for a Q between 2 and 4, respectively. Despite this, the phase delay of FC 2 and FC 4 is also considered insignificant, i.e. from this point on, it is assumed that the fundamental of the filtered unipolar PWM waveform is in phase with the grid voltage.

5.3.4 Design Considerations

It is well known that a GCI is required to provide high quality (low THD) power to the grid, whilst meeting the necessary power factor. Despite this, the importance of the low-pass filter design is often overlooked. The low-pass filter design influences the harmonic attenuation and affects the inverter power factor. In addition, the filter will have copper losses and hence reduce the overall inverter efficiency. To maintain a high efficiency, a maximum damping resistor power loss, P_d, of 5% rated power is arbitrarily selected. This should also be taken into account when designing a GCI low-pass filter.

Filter Variables

The filter itself has four variables, three of which are circuit parameters, i.e. the capacitance, the inductance and the damping resistance; the remaining variable is the filter configuration. A summary of these filter variables, and the key filter parameters they affect, is summarised in Table 5.3.

Table 5.3: Low-Pass filter variables, and the key parameters they affect.

Variable \ Parameter	Resonant Frequency, f_{res}	Quality Factor, Q	Harmonic Attenuation	Damping Resistor Power Loss, P_d
Inductance, L	✓	✓	✓	✓
Capacitance, C	✓	✓	✓	✓
Damping Resistance, R_d	×	✓	✓	✓
Filter Configuration (FC)	×	✓	✓	✓

Frequency and Filter Component Normalisation

The filter cutoff (or resonant) frequency and filter components are normalised, as this greatly simplifies the analysis and allows the designer to easily select component values for any sized (rated) system. The normalised cutoff frequency, ω_{cn} is expressed relative to the base frequency, ω_B, these are expressed by Equations (5.28) and (5.29), respectively, where f_1 represents the grid (inverter fundamental) frequency.

$$\omega_{cn} \equiv \frac{\omega}{\omega_B} \tag{5.28}$$

$$\omega_B = 2\,\pi\,f_1 \tag{5.29}$$

Consider an inverter designed to deliver rated power, P_B, in to a grid of rated voltage V_B. The resulting base impedance, Z_B, is expressed by Equation (5.30), and is later used to normalise the filter components. Note that the base impedance is defined as the quotient of the base voltage and base current, I_B.

$$Z_B \equiv \frac{V_B}{I_B} = \frac{{V_B}^2}{P_B} \tag{5.30}$$

The normalised filter capacitance, C_n, is shown in Equation (5.31), where C_B represents the base capacitance, which itself is expressed in Equation (5.32).

$$C_n = \frac{C}{C_B} \tag{5.31}$$

$$C_B = \frac{1}{\omega_B Z_B} \tag{5.32}$$

Similarly, the normalised filter inductance, L_n, is expressed relative to the base inductance, L_B; these are summarised in Equations (5.33) and (5.34), respectively.

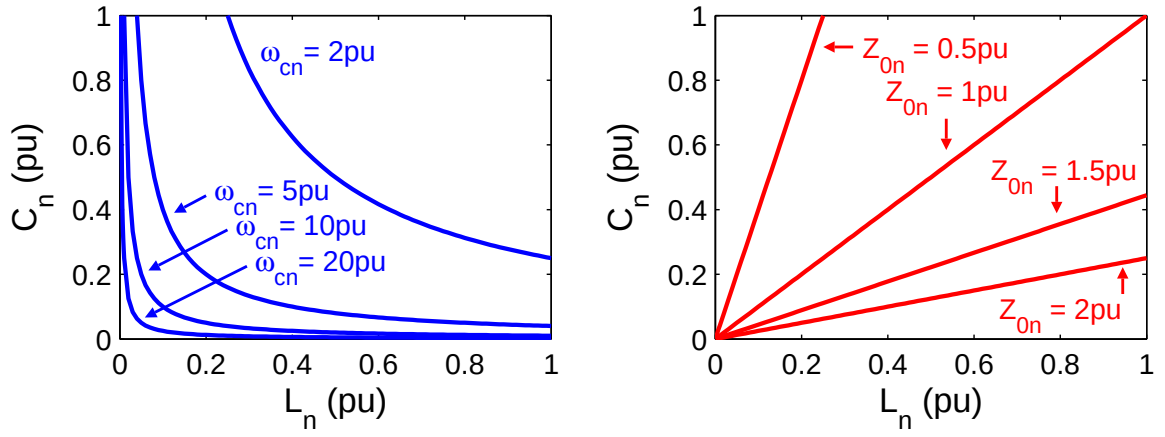
$$L_n = \frac{L}{L_B} \tag{5.33}$$

$$L_B = \frac{Z_B}{\omega_B} \tag{5.34}$$

The filter resonant frequency, which was previously shown in Equation (5.21), is also normalised and simplified. Substitution of C_n and L_n, in to this expression, shows that the product is inversely proportional to the square of filter resonant frequency; this is summarised by Equation (5.35) and Figure 5.34(a), which shows ω_{cn} contours of 1, 5, 10 and 20pu. Similarly, Figure 5.34(b) shows normalised characteristic impedance, Z_{0n}, contours of 0.5, 1, 1.5, 2 and 2.5pu; Z_{0n} is expressed by Equation (5.36).

$$L_n C_n = \frac{1}{\omega_{cn}^{\ 2}} \tag{5.35}$$

$$Z_{0n} = \sqrt{\frac{L_n}{C_n}} = \frac{Z_0}{Z_B} \tag{5.36}$$



(a) Cutoff frequency, ω_{cn}, contours

(b) Characteristic impedance, Z_{0n}, contours

Figure 5.34: Normalised capacitance, C_n, vs. inductance, L_n, plots, showing (a) cutoff frequency, ω_{cn}, and (b) characteristic impedance, , contours. The ω_{cn} contours are equal to 2, 5, 10 and 20pu, whilst those for Z_{0n} are equal to 0.5, 1, 1.5 and 2pu.

Practical Limitations

Although Figure 5.34 suggests that a low-pass filter can be easily designed, based on a desired cutoff frequency or characteristic impedance, it should be noted that components may face practical limitations, such as size, cost, weight etc. For example, consider a 1kW GCI: an inductance of 0.6pu corresponds to approximately 110mH. An inductor this size for this application would be heavy, bulky and costly, due to the inverter current rating (4.2A). Hence, the size, cost and weight of the filter (and hence inverter) can be reduced

by selecting a smaller value of L_n; conversely, this would require a larger capacitance for a given cutoff frequency.

A small capacitance and small inductance can be selected, however, this produces a high cutoff frequency, which requires the inverter to operate at an even higher switching frequency, f_{sw}, to allow the filter to remove the PWM harmonics. This leads to higher inverter switching losses, P_{SW}, as P_{SW} is proportional to the f_{sw}. Hence upper switching and cutoff frequency limits are required. For a 50Hz GCI, a maximum switching frequency of 10kHz is selected (200pu). The upper cutoff frequency depends on the filter configuration, required harmonic attenuation, and the inverter switching frequency. This further investigated in Section 5.3.5, whilst Sections 5.3.6 and 5.3.7 examine the power factor requirements and damping resistor power loss, respectively. Section 5.3.8 summarises with a power factor, power loss and output current THD trade-off.

5.3.5 Harmonic Attenuation and Distortion

This section examines the filter's ability to attenuate harmonic components and hence reduce the THD of an unipolar PWM current. Consider Figure 5.35, it shows the harmonic spectrum of a 4kHz unipolar PWM waveform, and filter gain of FC 1 - 4. The cutoff frequency, f_c, and quality factor are arbitrarily selected as 1kHz and 2, respectively. Note that the filter gain of FC 1 and 3 are indistinguishable, as such, the resulting THD of these filters will be identical. Similarly, the gain and hence THD of FC 2 and 4 are identical.

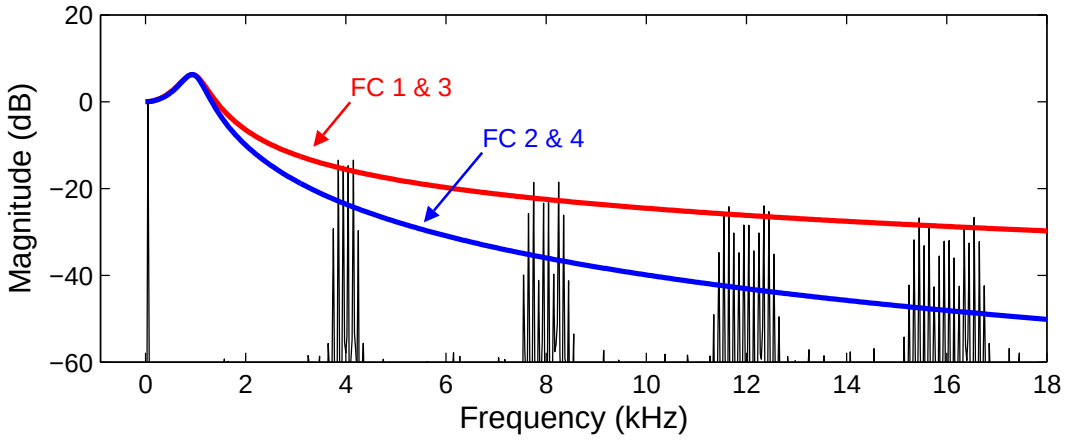
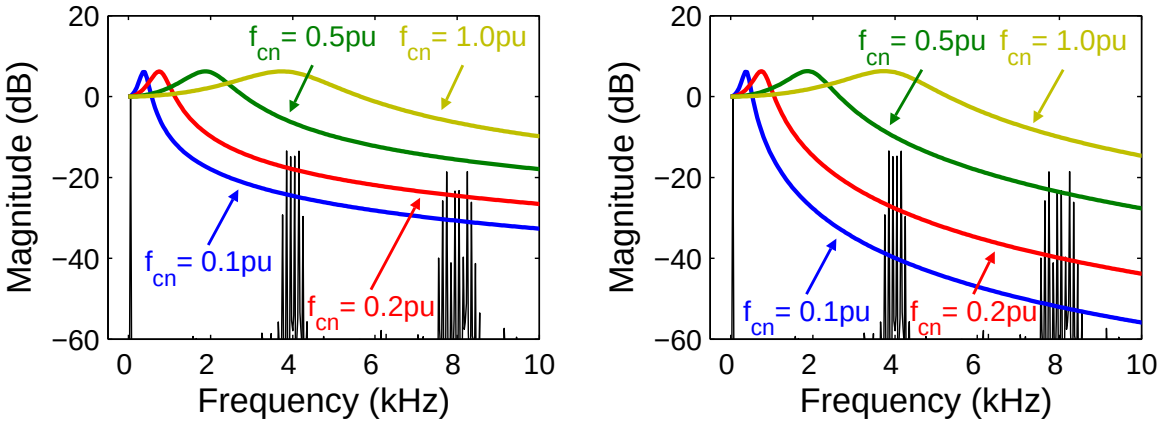


Figure 5.35: Harmonic spectrum of a unipolar PWM waveform, and the gain of filter configurations 1 and 3, and 2 and 4, which represent first and second-order filter responses, respectively. Each filter gain is shown for a quality factor of 2 and a cutoff frequency of 1kHz. Note that the harmonic spectrum is shown for a switching frequency of 4kHz.

Figure 5.35 indicates that filter configurations 2 and 4 offer a greater rate of attenuation than FC 1 and 3. This is expected as FC 1 and 3 behave as first-order filters, i.e. their gains roll-off at $-20\,\text{dB/decade}$, whilst the gains of FC 2 and 4 roll-off at $-40\,\text{dB/decade}$, as they are second-order low-pass filters. In addition to order, other aspects such as quality factor and cutoff frequency also affect the filter gain and hence output current THD. The effect of varying the normalised cutoff frequency, f_c, on the filter gain is shown in Figure 5.36 for a Q of 2, whilst Figure 5.37 shows the effect of varying the quality factor, for a fixed f_c of 800Hz. Note that the PWM switching frequency is maintained at 4kHz.



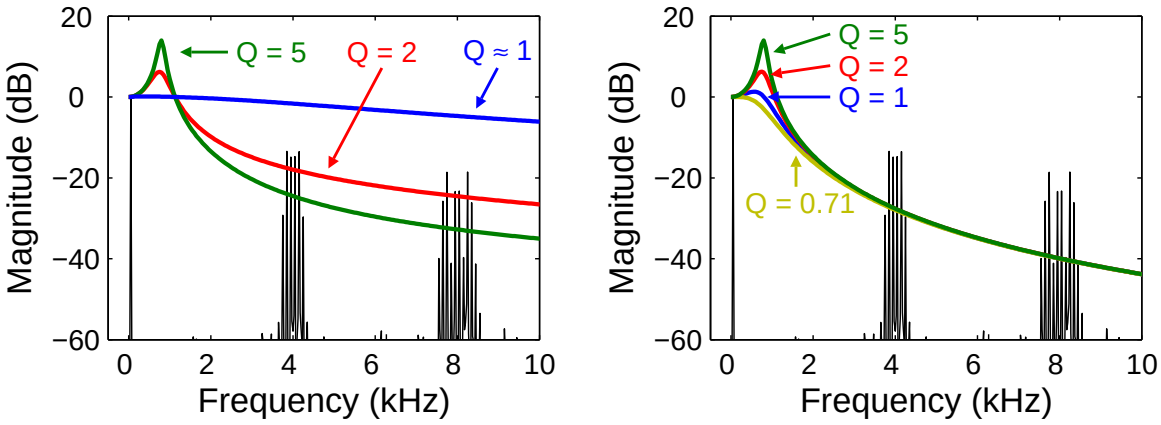
(a) Filter configurations 1 and 3

(b) Filter configurations 2 and 4

Figure 5.36: Filter gain on a 4kHz unipolar PWM harmonic spectrum, showing the effect of varying the filter cutoff frequency, for filter configurations (a) 1 and 3, and (b) 2 and 4. The cutoff frequencies are normalised relative to the switching frequency and are shown equal to 0.1, 0.2, 0.5 and 1pu. Note that the PWM harmonics are now only shown for only two multiples of the switching frequency.

Note that the normalised cutoff frequency, ω_{cn}, seen in Figure 5.34(a), is expressed relative to the fundamental frequency, f_1, whilst the normalised cutoff frequency, f_{cn}, shown in Figures 5.36 and 5.37 are expressed relative to the inverter switching frequency, f_{sw}.

Figure 5.36 implies that the low-pass filters becomes less effective as f_c approaches f_{sw}, as higher magnitude high-frequency components pass through the filter, which ultimately increases the output current THD. In addition, Figure 5.37 suggests the quality factor of FC 1 and 3 also affect the harmonic attenuation and hence the resulting THD. For



(a) Filter configurations 1 and 3

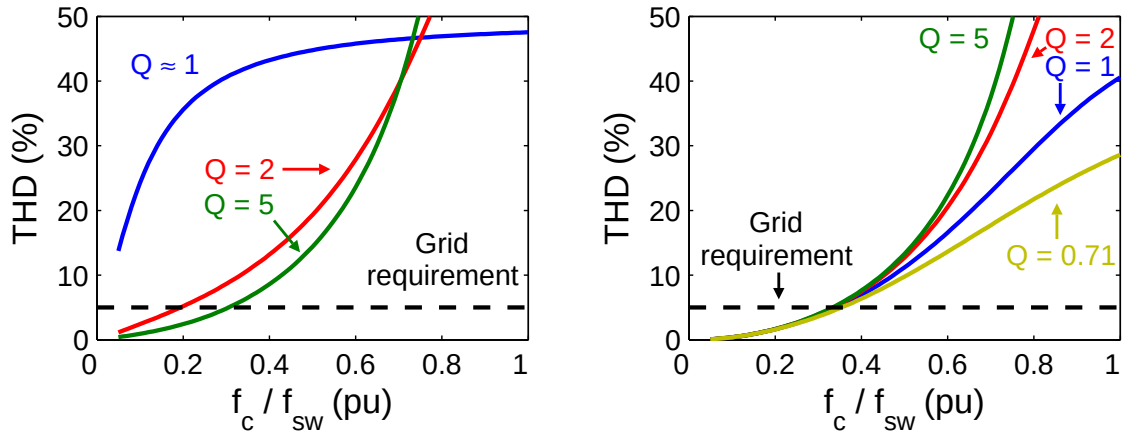
(b) Filter configurations 2 and 4

Figure 5.37: Filter gain on a 4kHz unipolar PWM harmonic spectrum, showing the effect of varying the filter quality factor, for filter configurations (a) 1 and 3, and (b) 2 and 4. Quality factors, of 1, 2 and 5 are shown for each filter configuration; in addition the critically damped case, $Q = 0.71$ ($\frac{1}{\sqrt{2}}$), is shown in (b). Note that the cutoff frequency is 800Hz (0.2pu, relative to the switching frequency).

example a low Q ($\approx$1) provides little attenuation at high frequencies, whilst a higher value Q (e.g. 5) significantly improves the high-frequency attenuation. In contrast, the Q does not affect the output current THD for FC 2 and 4, at low cutoff frequencies, however, it becomes significant as f_c approaches f_{sw}.

The above statements are verified in Figure 5.38, which shows the calculated output current THD for each filter, as a function of both cutoff frequency and quality factor; the dashed line represents the grid THD limit of 5%. The figure indicates that FC 1 and 3 are effective if the Q is above 2 and the f_c is between less than about 0.2 to 0.3pu; this may explain why Nave suggests a Q between 2 and 4 [105]. In addition, the figure shows that the THD of FC 2 and 4 is independent of Q, for f_{cn} less than about 0.3pu, and that each filter configuration is able to meet the grid THD requirement for a Q of 5, and a f_{cn} less than about 0.3pu. Hence, the cutoff frequency is limited to about 0.3pu, such that the filtered current meets the grid THD requirement.

In summary, filter configurations 2 and 4 are able to meet the grid THD specifications over a wider range of Q and f_c, than FC 1 and 3. This knowledge makes the design of the second-order low-pass filters more flexible in terms of cutoff frequency and quality factor, however, the power factor and damping resistor loss should also be considered before selecting a filter configuration.



(a) Filter configurations 1 and 3

(b) Filter configurations 2 and 4

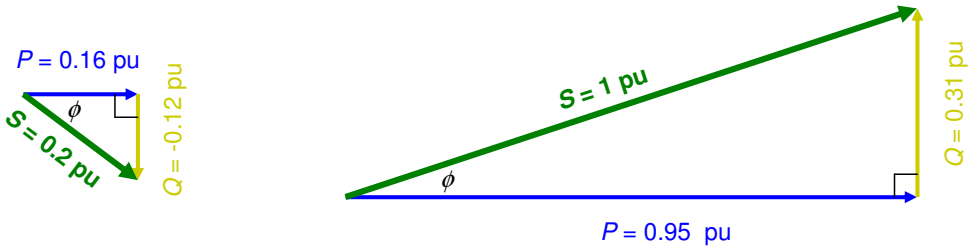
Figure 5.38: Output current THD vs. filter cutoff frequency and quality factor, for filter configurations (a) 1 and 3, and (b) 2 and 4. The curves represent quality factors, Q, of 1, 2 and 5, for filter configurations 1–4. Note that filter configurations 2 and 4 also include the critically damped case, i.e. a Q of 0.71 ($\frac{1}{\sqrt{2}}$).

5.3.6 Power Factor Requirements

This section shows that the inverter power factor is affected by the choice of filter components, and provides a guideline to selecting the filter inductance and capacitance, such that the power factor requirements are met. The Australian Standards consider the inverter as a load from the grid, and requires the inverter to operate between 0.8 lead and 0.95 lag for all output apparent powers between 20 and 100% rated (0.2 to 1 pu) power [96]. A summary of the normalised apparent, real and reactive powers (S, P, and Q, respectively), under these conditions is shown in Table 5.4 and Figure 5.39. Note that it is assumed that the fundamental of the inverter output current is in-phase with the grid voltage.

Table 5.4: Summary of normalised apparent, real and reactive power, and power factor angle (ϕ) under grid power factor requirement extremes.

Power / Grid Extremes	Apparent (S)	Real (P)	Reactive (Q)	ϕ
Power Factor = 0.80 lead	0.20 pu	0.16 pu	−0.12 pu	36.9°
Power Factor = 0.95 lag	1.00 pu	0.95 pu	0.31 pu	−18.2°



(a) Leading power factor

(b) Lagging power factor

Figure 5.39: Real, P, reactive, Q, and apparent power, S, triangle, corresponding to the grid power factor limits, showing (a) 0.8 lead and (b) 0.95 lag.

The reactive power, Q, in the above figure represents the net reactive power that is either delivered to or absorbed by the grid. It is the difference between that which is supplied by the capacitor, Q_C, and that which is absorbed by the inductor, Q_L, and is hence expressed as $Q_L - Q_C$. This reactive power flow, is summarised for an undamped CL low-pass filter in Figure 5.40, which also shows the real power flow, i.e. from the inverter to the grid. Note that the inverter does not produce reactive power as the fundamental output current is assumed to operate at unity power factor, i.e. it is supplied by the capacitor and is absorbed by the inductor and grid.

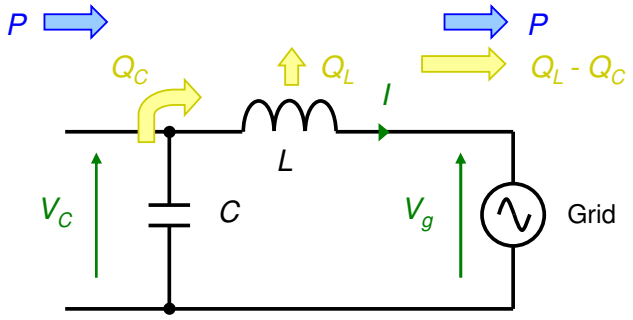


Figure 5.40: Real, P, and reactive, Q, power flow diagram for an undamped CL low-pass filter. Note that the grid supplies / absorbs reactive power that is equal to $Q_L - Q_C$, and that real power is not absorbed in the filter.

The introduction of a damping resistor would simply imply that the net real power, that is fed to the grid, is equal to $P - P_d$, where P_d is the damping resistor power loss. As P_d is set to 0.05pu (5% rated power) at rated current, it is foreseen that a small reduction in real power will not greatly affect the resulting power factor. For example, consider the 0.95 lagging case: if P is reduced from 0.95 to 0.9pu, whilst Q is maintained at 0.31 pu, the power factor changes from 0.95 lag to 0.945 lag.

Reactive Power

The reactive power that is absorbed by the inductor, and generated by the capacitor is determined analytically here. Both Q_L and Q_C are expressed as a normalised quantities. The normalised inverter output current is assumed be equal to 1pu and 0.2pu, for rated and 20% rated volt-amperes operation, respectively.

The inductor absorbs reactive power, Q_L, which is proportional to the square of the normalised current (I_n) and its reactance, X_L. This is summarised by Equation (5.37), and is simplified to Equation (5.38). Hence, at rated current, Q_L is equal to L_n pu, whilst at 20% rated power, it is equal to $0.04\,L_n$ pu.

$$Q_L = I_n^2\, X_L \tag{5.37}$$

$$= I_n^2\, L_n \quad \text{(pu)} \tag{5.38}$$

The capacitor generates reactive power, Q_C, which is proportional to the square of the capacitor voltage, V_C, and inversely proportional to the capacitive reactance, X_C. This is summarised and simplified in Equations (5.39) and (5.40), respectively. Note: $1/X_C$ simplifies to C_n, due to the grid frequency.

$$Q_C = \frac{V_C^2}{X_C} \tag{5.39}$$

$$= V_{Cn}^2\, C_n \quad \text{(pu)} \tag{5.40}$$

The capacitor voltage is the phasor summation of the grid voltage, V_g, and the voltage drop across the inductor, V_L, as summarised by Equation (5.41). This simplifies to Equation (5.42), as V_g is assumed to be equal to 1 pu, and V_L is equal to $j\, I_n\, L_n$ ($\omega_n = 1$pu).

$$V_C = V_g - V_L \tag{5.41}$$

$$= 1 - j\, I_n\, L_n \quad \text{(pu)} \tag{5.42}$$

Filter Component Limitations

The maximum value of C_n and L_n can be determined, such that the power factor requirements are met. Consider the leading power factor case, which allows the maximum value of C_n to be determined. This power factor is most difficult to meet when the inverter operates at 20% rated volt-amperes. Under this condition, the inverter output current is 0.2pu and Q is equal to -0.12pu. As Q is equal to $Q_L - Q_C$, the maximum value of C_n can be calculated as a function of L_n. Hence, for zero inductance, a normalised capacitance of less than 0.12pu is required to meet the power factor standard. This maximum capacitance value is expected to increase with increasing L_n, however, only slightly as Q_L is equal to $0.04\,L_n$ pu (for 20% rated operation). For example, the leading power factor requirement will be met for an inductance of 0.5pu, providing C_n does not exceed 0.124 pu.

This process is repeated for the lagging power factor case, however, the power factor is set to 0.95 (lag) and the inverter output current is set to 1pu. The normalised capacitance is again determined as a function of L_n, such that the power factor is met. In the absence of a capacitor, the maximum inductance is equal to 0.31pu. The introduction of capacitance will supply reactive power to the inductor and effectively allow L_n to increase. Compared to the effect of L_n on C_n in the light-load leading power factor case, the effect of C_n on L_n under full-load conditions is more significant as the V_C is greater than 1pu.

A summary of the inductance and capacitance limits, that allow the filter to meet the lagging and leading grid power factor requirements, respectively, is shown by the dashed lines in Figure 5.41. The figure also shows ω_{cn} contours of 10, 26, and 65pu, which together with the dashed lines, form the boundary of two design regions; these are shaded for convenience. The smaller region, area A, corresponds to a switching frequency of 4kHz, whilst the larger region, areas A and B, represents the design region for a f_{sw} of 10kHz. Hence, filter components selected within a specified design region (based on the f_{sw}) should yield a sinusoidal output current whose fundamental is within the required power factor range. Note that a minimum ω_{cn} of 10pu is selected as this produces a small and insignificant filter phase delay (recall Figure 5.33). Maximum ω_{cn} of 26 and 65pu are selected as these correspond to f_{cn} of about 0.33pu, i.e. the output current waveform will contain less than 5% THD, for switching frequencies of 4 and 10kHz, respectively.

Although the inverter power factor requirements are met by selecting values of C_n and L_n within the design region, other aspects such as the filter characteristic impedance, must also be considered. The Z_{0n} is governed by C_n and L_n (recall Equation (5.36)), and also

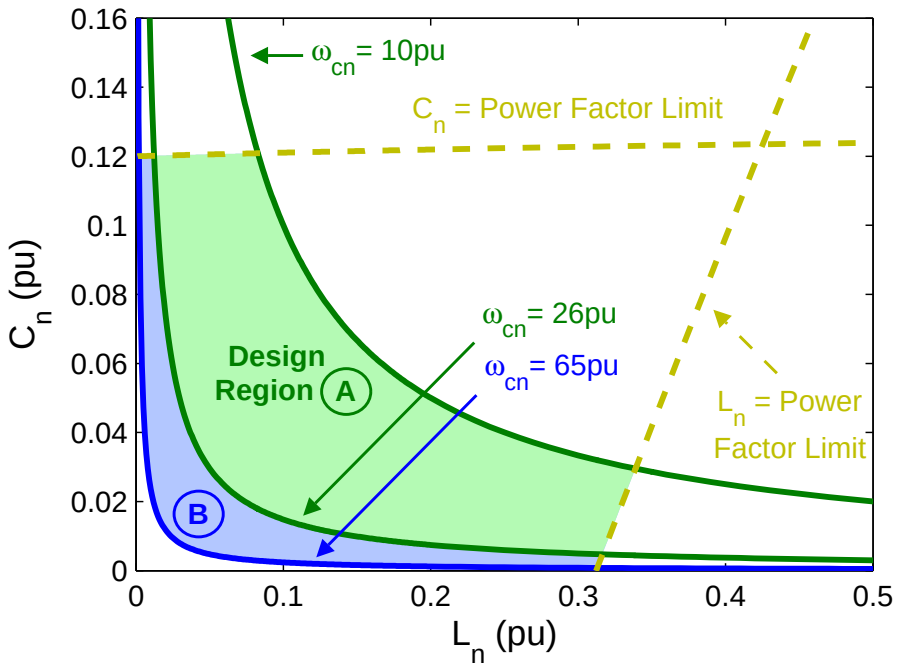


Figure 5.41: Normalised capacitance vs. inductance, showing various cutoff frequencies and characteristic impedances. The shaded area represents the design region, which limits the inverter switching losses, and meets the required power factor standards.

affects the choice of R_d and hence the quality factor. The filter power loss, caused by R_d, is discussed in the following section, whilst the effect of reducing C_n on both the output current THD and power loss is examined in Section 5.3.8, for all filter configurations.

5.3.7 Power Loss

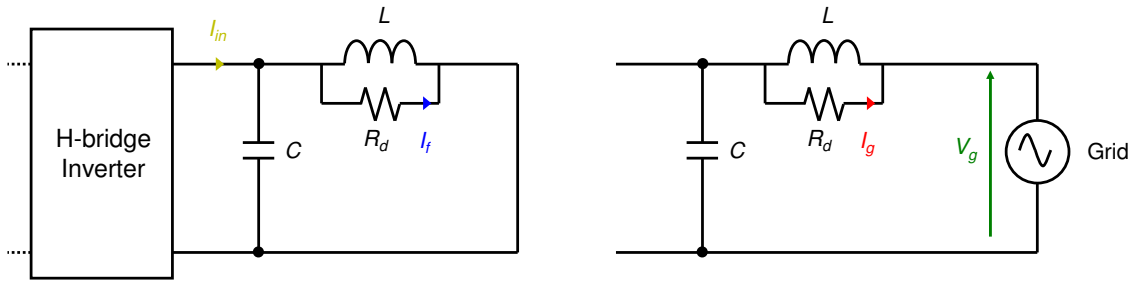
Section 5.3.5 showed that each filter is able to meet the grid THD requirement providing the quality factor is greater than 2 and the cutoff frequency was less than about 0.2pu. The issue is that as Q increases, so too does R_d for a fixed Z_0. Intuitively, the power loss associated with the damping resistance, P_d, should increase with R_d for FC 1 and 4, as these are series connected resistive-inductive-capacitive (RLC) circuits. In contrast, P_d should decrease for FC 2 and 3, as these are parallel damped RLC circuits.

Analytically, the damping resistance power loss is proportional to R_d and the square of the current that flows through it, I_d, as shown in Equation (5.43). The total current that flows through R_d is determined by the theory of *superposition*, i.e. the summation of the currents caused by each source, whilst ignoring the other. The damping resistor current from the inverter, I_f, is determined by shorting the grid, as it is a voltage source.

In contrast, the grid drawn current, I_g, is calculated by removing the inverter, as it is a current source. This process is depicted in Figure 5.42, for FC 3, and is summarised by Equation (5.44).

$$P_d = I_d^2 R_d \tag{5.43}$$

$$|I_d| = |I_f + I_g| \tag{5.44}$$



(a) Current from inverter, I_f

(b) Current from grid, I_g

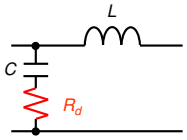
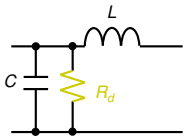
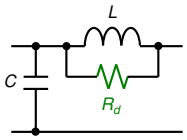
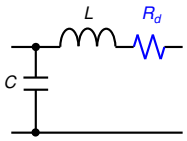
Figure 5.42: Damping resistor current determined by the theory of *superposition*, showing damping resistor current from (a) the inverter, I_f, and (b) the grid, I_g. The theory considers the current from each source, whilst ignoring the other. Note that current and voltage sources are replaced with open and short-circuits, respectively.

The *current divider* rule is used to determine the inverter associated current, I_f. A summary of these currents, along with those caused from the grid, I_g, are shown in Table 5.5, as a function of input frequency ($s = j\,\omega$). The table shows that I_f of FC 2 and 3 are identical, as are I_g of FC 1 and 4. Note that the power loss calculation (see Equation (5.43)) uses the RMS value of I_f, which includes the filtered high-frequency PWM harmonic components up to $7\,f_{sw}$, which contains 118 harmonic sidebands. In contrast, the grid drawn current considers only the fundamental (grid) frequency, i.e. $\omega = \omega_B$.

Power Loss Comparison

The power loss of each filter configuration can be determined by examining each circuit of Table 5.5. Consider FC 1. The high-frequency PWM harmonics will pass through the capacitor and R_d as the capacitor is essentially a short-circuit at high-frequencies. Hence, the high-frequency current harmonics and the subsequent high power loss will be

Table 5.5: Comparison of damping resistor current, for various low-pass filter configurations. The total current is determined from the principle of superposition, i.e it is the summation of the inverter and grid drawn currents, I_{inv} and I_g, respectively.

FC	Circuit	I_f $(\omega \geq \omega_B)$	I_g $(\omega = \omega_B)$
1		$I_{in}\,\frac{s^2\,CL}{s^2CL+sCR_d+1}$	$\frac{V_g\,sC}{s^2CL+sCR_d+1}$
2		$I_{in}\,\frac{sL}{s^2CLR_d+sL+R_d}$	$\frac{V_g}{s^2CLR_d+sC+R_d}$
3		$I_{in}\,\frac{sL}{s^2CLR_d+sL+R_d}$	$\frac{V_g\,s^2CL}{s^2CLR_d+sL+R_d}$
4		$I_{in}\,\frac{1}{s^2CL+sCR_d+1}$	$\frac{V_g\,sC}{s^2CL+sCR_d+1}$

dissipated in R_d. In contrast, the grid-drawn current will be small due to the capacitance limitation, and the resulting power loss will hence be negligible.

Consider FC 2. The high-frequency PWM harmonics currents are assumed to pass through the capacitor. This implies the fundamental current caused by the inverter will pass through R_d, if it is smaller than the inductive reactance. The grid-drawn current will also be large for small R_d, as there is a small and insignificant voltage drop across the inductor, i.e. the voltage drop across the resistor is essentially that of the grid. The resistance must hence must be large to limit P_d. The drawback, however, is that Q is directly proportional to R_d, i.e. a power loss vs. quality factor trade-off exists.

Consider FC 4. The capacitor again shorts the high-frequency components, implying that the fundamental inverter output current passes through R_d. The resulting inverter associated power loss is hence proportional to R_d. The grid-drawn current is once again limited by the capacitance and the resulting power loss is considered negligible.

Consider FC 3. The series-connected capacitor again limits the grid-drawn current to a small amount and hence a negligible power loss. The inverter associated current does

not contain high-frequency harmonics and is small predividing R_d is comparable to (or smaller than) the inductive reactance. Such a case would result in a small Q and hence a large output current THD (recall Figure 5.38(a)). In contrast, a large R_d will increase Q, which will sufficiently attenuate the high-frequency PWM harmonics, whilst reducing the damping resistor power loss.

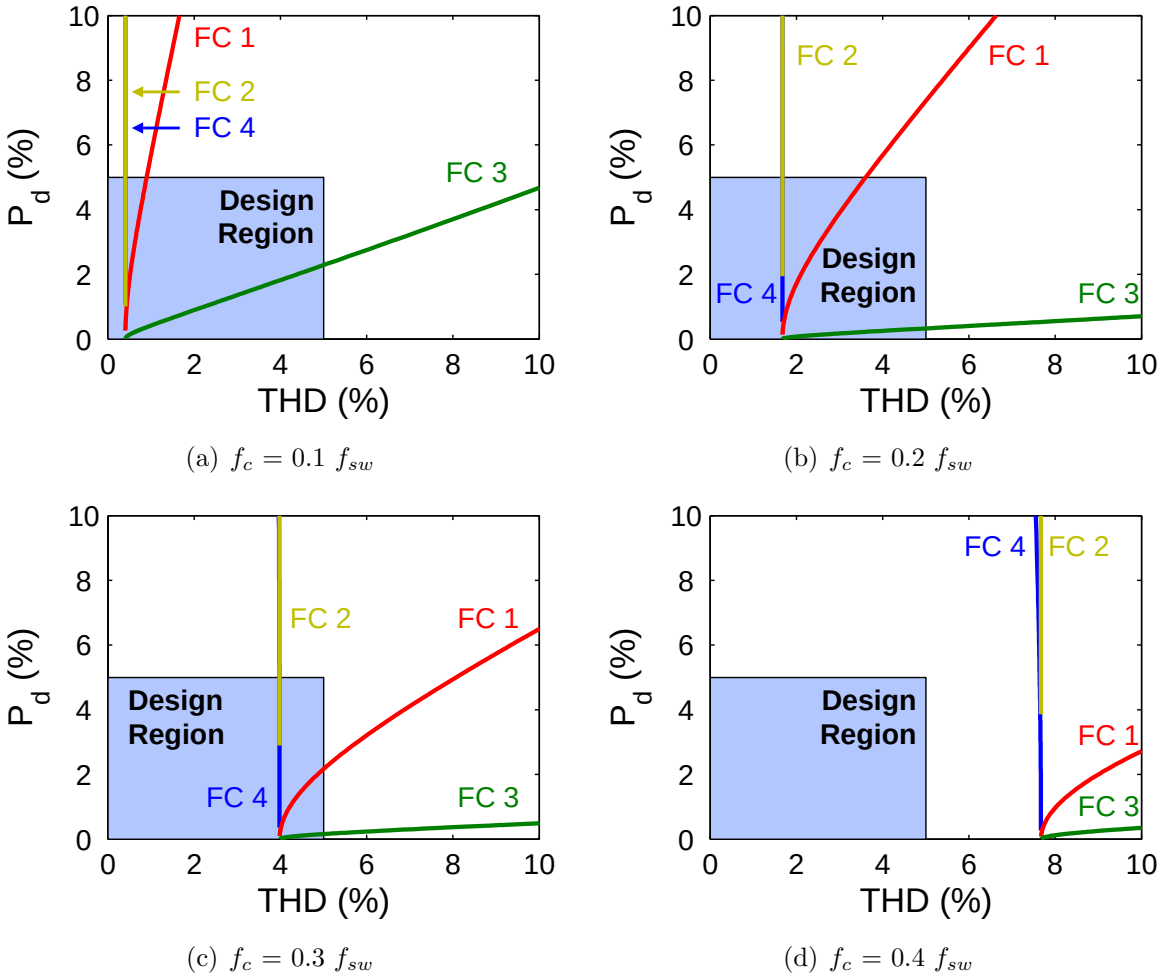
The above information suggests that FC 2 is the least favoured filter configuration, due to high power losses. Nave verifies this by stating that power dissipation problems may render this filter impractical [105]. A similar study by Ahmed et al. compares the simulated damping resistor power loss of several LCL filter configurations for a GCI [112]. Although his work compares seven filter topologies, many of which are fourth-order filters, Ahmed does consider LCL versions of FC 1 and 2 for a 10kVA system. Despite the third-order nature, the simulations show that the parallel damped arrangement (similar to FC 2) produces copper losses of 1.5kW (0.15pu), compared to 6.5W (0.0065pu) for the series damped capacitor (similar to FC 1). Hence, FC 2 produces a power loss of about 230 times than that of FC 1.

Filter configuration 3 is not considered in Ahmed's study, however, it appears to produce the least power loss. The drawback, however, is that FC 3 is only able to attenuate the high-frequency PWM harmonics as a first-order filter, and hence an output current THD vs. power loss trade-off exists. This is further examined in the following section.

5.3.8 Design Trade-Offs - Unipolar PWM Waveform

It is well known that the inverter must meet strict grid power factor and THD requirements in order to operate as a grid-connected inverter. The effect of filter parameter variation, such as cutoff frequency and quality factor, on the both the output current THD and power factor has been examined in Sections 5.3.5 and 5.3.6, respectively. In addition, the damping resistor power loss has also been discussed, albeit separately. The power loss and THD are now considered simultaneously, for a f_{sw} of 4kHz, and C_n of 0.12pu.

Figure 5.43 shows the damping resistor power loss vs. filter output current THD for FC 1–4 and f_c equal to 0.2 and 0.3pu. Simulations over a wider range of f_c can be found in the appendix (Section A.2.1). The shaded area represents the design region, which is bound by power loss and THD limits of 5%. The power loss is determined using the inverter associated current, I_f, which includes the filtered harmonic components up to $7\,f_{sw}$, and the grid drawn current, I_g. The figure shows that each filter is able to limit power loss to 5%, whilst meeting the THD specification, for some value of R_d and hence Q.



(a) $f_c = 0.1\ f_{sw}$

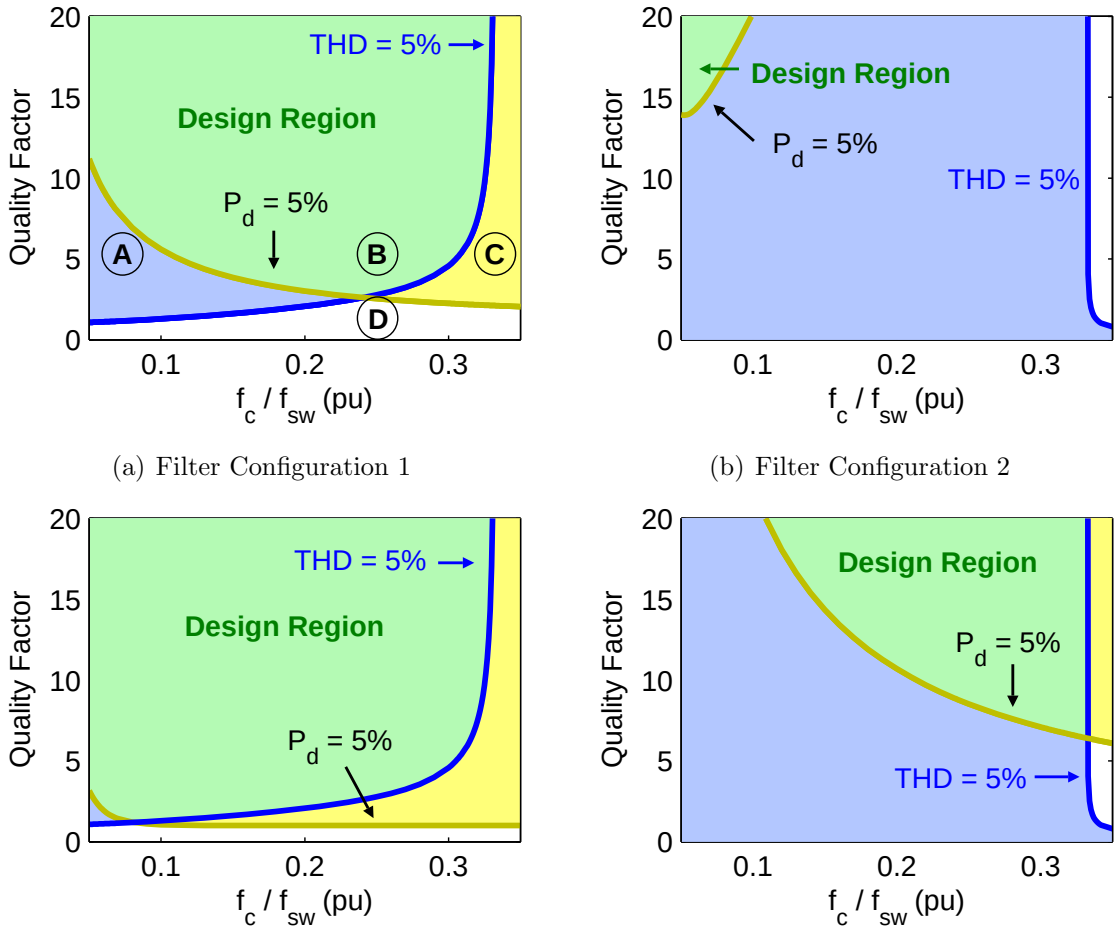
(b) $f_c = 0.2\ f_{sw}$

(c) $f_c = 0.3\ f_{sw}$

(d) $f_c = 0.4\ f_{sw}$

Figure 5.43: Filter power loss, P_d, vs. output current THD for cutoff frequencies, f_c, of (a) 0.2, and (b) 0.3 pu (relative to the inverter switching frequency, f_{sw}). The shaded region indicates the design region, where both the THD and power loss is less than 5%.

Although the output current THD, power factor and filter power loss are of prime importance, the filter quality factor should also be known as this has the potential to amplify harmonics, which ultimately influences the output current THD for a non-ideal input current. Figure 5.44 hence shows the quality factor as a function of normalised cutoff frequency, for each filter configuration (FC). Four shaded regions are shown, these correspond to areas where: A) the THD is less than 5%, B) the THD and power loss are both less than 5%, C) the power loss is less than 5%, and D) both the THD and power loss are greater than 5%; the solid lines represent contours of THD and or power loss equal to 5%. Note that the switching frequency is set to 4kHz and that the filter capacitance is maintained at 0.12pu for each FC, such that the power factor standards are met.



(a) Filter Configuration 1

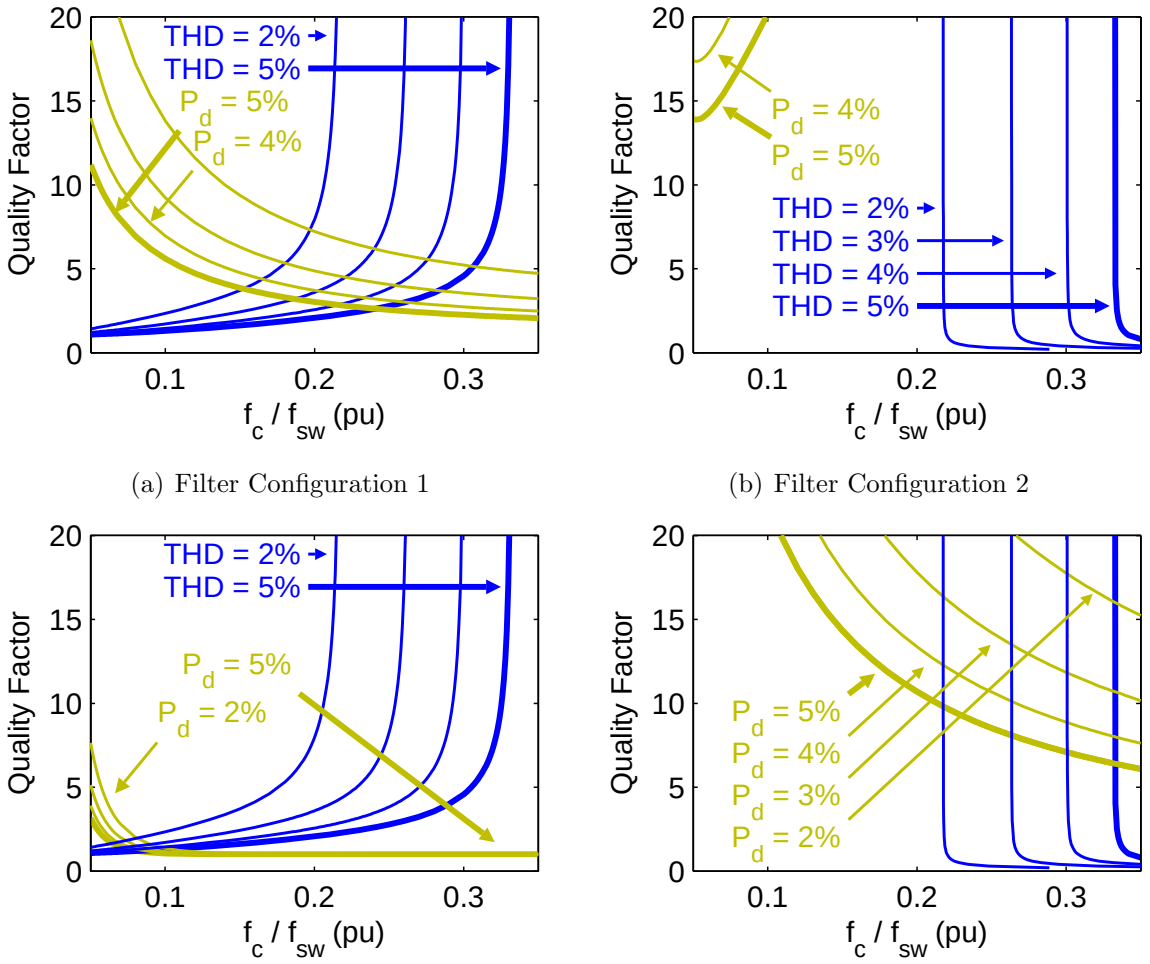
(b) Filter Configuration 2

(c) Filter Configuration 3

(d) Filter Configuration 4

Figure 5.44: Power loss and THD contours of 5%, for filter configurations (a) 1, (b) 2, (c) 3 and (d) 4, for a switching frequency of 4kHz. The solid lines represent contours of THD and damping resistor power loss, P_d, equal to 5%. The resulting shaded regions represent the area where the A) THD, B) THD and damping resistor power loss, and C) power loss, are less than 5%, whilst area D) corresponds to the region where both the THD and power loss exceed 5%. Note that area B is referred to as the *design region*.

The design region allows the inductor to be easily selected, based on a desired cutoff frequency, filter configuration and filter capacitance. Similarly, the damping resistor can also be determined knowing the quality factor and filter configuration. Note that the inverter performance can be improved, i.e. the output current THD and damping resistor power loss can be reduced by increasing the filter quality factor. This is seen in Figure 5.45, which shows THD and power loss contours of 2, 3, 4 and 5% for each filter configuration. Note that the f_{sw} and C_n are maintained at 4kHz and 0.12pu, respectively.



(a) Filter Configuration 1

(b) Filter Configuration 2

(c) Filter Configuration 3

(d) Filter Configuration 4

Figure 5.45: Power loss and THD contours of 2, 3, 4 and 5%, for filter configuration (FC) (a) 1, (b) 2, (c) 3 and (d) 4, for a switching frequency of 4kHz and a capacitance of 0.12pu. The THD and power loss, P_d, of each filter can be reduced by increasing the quality factor, Q, with FC 3 showing the least Q and P_d variance.

Despite being first-order filters, Figures 5.44 and 5.45 show that FC 1 and 3 are the only configurations that meet Nave's recommendation of a Q between 2 and 4. In addition, FC 3 is able to meet this over a wider range of cutoff frequencies, and its P_d is less susceptible to quality factor variations. In contrast, both second-order filters can not meet Nave's suggested Q range; the minimum Q which allows FC 4 to lie within the design region, is 6.5, whilst that of FC 2 is about 20 (for a f_c of 0.1pu). Recall that ω_{cn} should be greater than one decade above ω_B, to prevent a filter phase delay. Hence f_{cn} should exceed 0.125pu for the above 4kHz f_{sw} case.

Effect of Varying C_n

The design regions of Figure 5.44 are shown for a capacitance of 0.12pu, as this value allows the filter to meet the 0.8 leading power factor whilst operating at 20% rated power. In addition, it also restricts L_n to a small range of values (see Figure 5.41), which is desired as larger capacitors are generally cheaper and easier to obtain than large inductances. If desired, the range of L_n can be increased by reducing C_n, however this increases Z_{0n}.

The drawback of increasing Z_{0n} is that R_d must also be increased to maintain a given Q. This action will increase P_d for the series connected RLC filters (FC 1 and 4), and reduce losses for parallel connected RLC filters (FC 2 and 3). Consider FC 1 and 4. Assuming the presence of R_d does not affect the RMS current in the filter, the power loss in both filters is proportional to R_d. In practise, however, the presence of R_d will reduce the current in the part of the circuit where R_d is located and hence the power loss would increase more slowly than R_d.

A summary of the effect of reducing C_n on the filter design region is shown in Table 5.6 for each FC and C_n equal to 0.12, 0.06 and 0.03pu. The table shows that the THD contour of 5% is unaffected by varying Z_{0n}, whilst the power loss contour of 5% is affected (as explained above). Consider the P_d contour equal to 5% for each filter configuration, for a fixed f_{sw}, e.g. 0.2pu. The minimum Q of FC 1 and 4, is shown to be inversely proportional to C_n, whilst it is directly proportional to C_n for FC 2, and is unchanged for FC 3.

Assuming that a variation of C_n and L_n does not affect the filter currents (for a fixed THD), R_d does not change for a fixed P_d. The Z_{0n}, however, is inversely proportional to C_n for a fixed ω_{cn}. Since Q is directly proportional to Z_0 for FC 1 and 4 (series RLC circuits), the minimum Q corresponding to a fixed P_d must also be inversely proportional to C_n. Similarly, the Q of FC 2 is inversely proportional to Z_{0n}, and hence the minimum Q corresponding to a P_d of 5% is directly proportional to C_n.

Effect of Varying f_{sw}

The effect of increasing the f_{sw} on each filter's design region is summarised in Table 5.7, for f_{sw} equal to 4, 7 and 10kHz, and for a fixed C_n of 0.12pu. The table shows that the design region increases with f_{sw} for FC 1, 3 and 4, whilst it decreases for FC 2. This occurs as ω_{cn} increases with f_{sw}, which results in an increase in L_n and hence Z_{0n}. The minimum Q corresponding to a fixed P_d is hence inversely proportional to the f_{sw} for FC 1 and 4. In contrast, the minimum Q for FC 2 is inversely proportional to f_{sw}, whilst that for FC 3 is not affected (for f_c equal to 0.2pu).

Table 5.6: Effect of varying filter capacitance on filter design region, for filter configurations (FC) 1, 2, 3 and 4. The C_n is equal to 0.12 (leading power factor limit), 0.06 and 0.03pu. Note that the design region for FC 4 is not displayed for $C_n = 0.03$pu due to the high quality factor, Q, required.

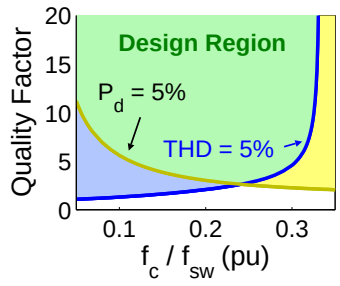
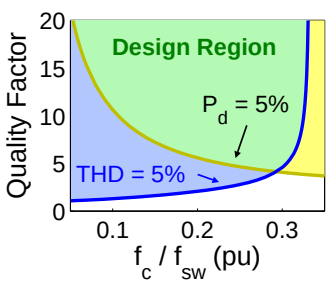
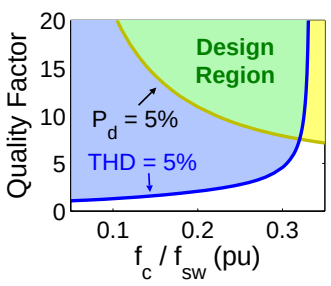
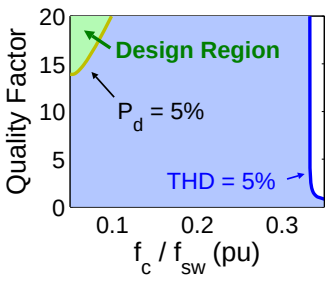
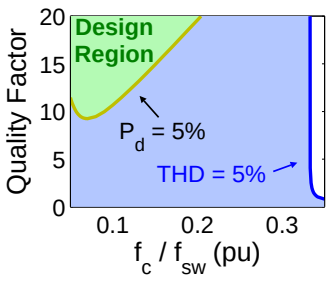
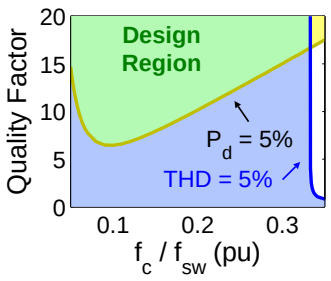
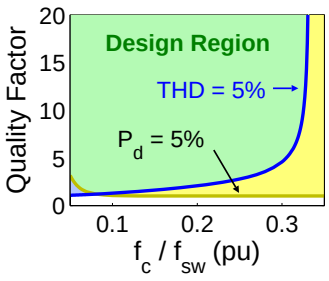
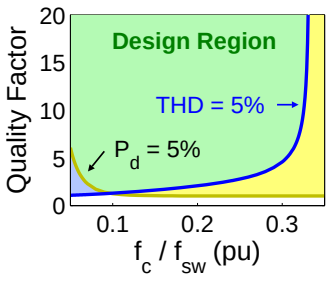
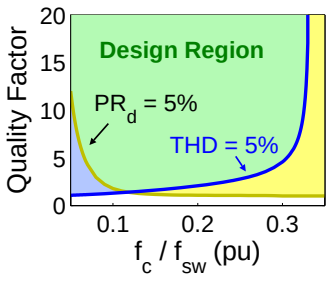
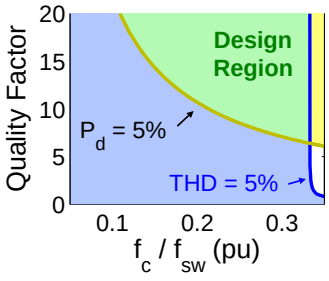
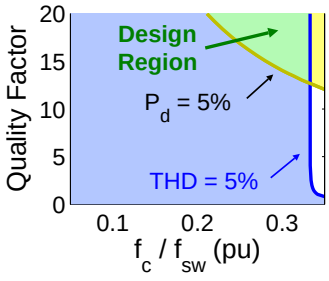
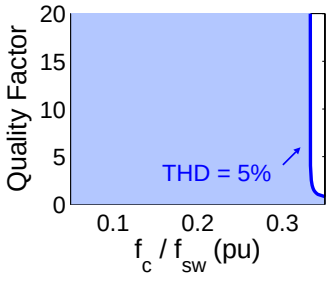
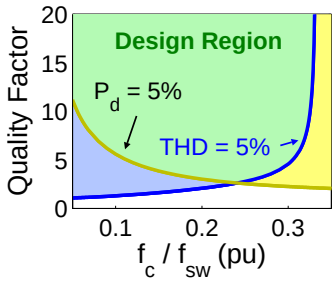
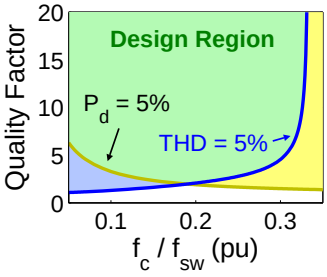
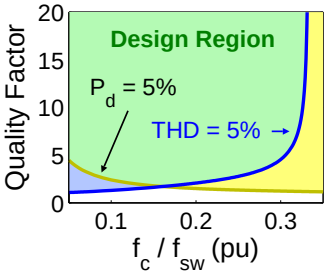
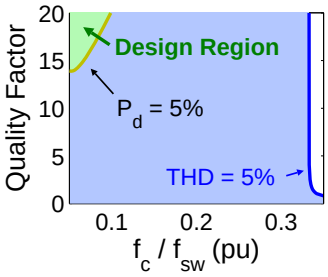
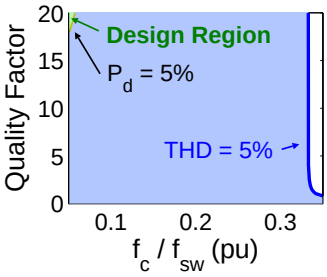
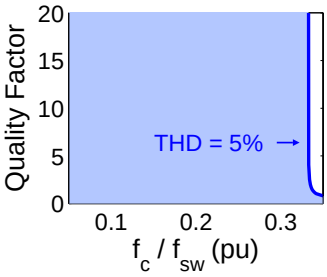
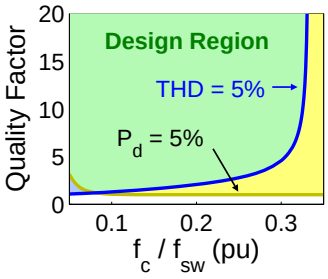
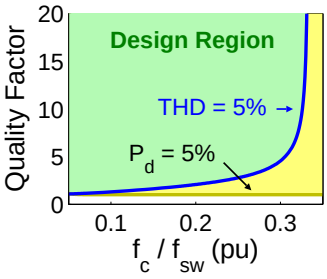
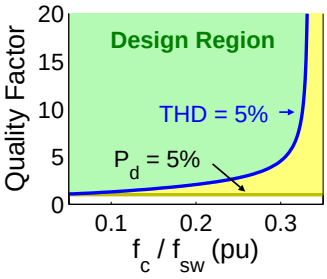
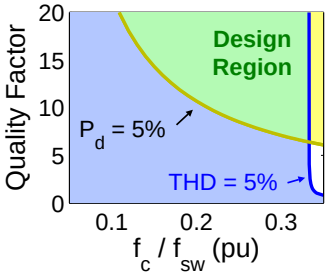
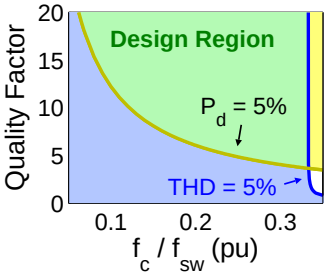
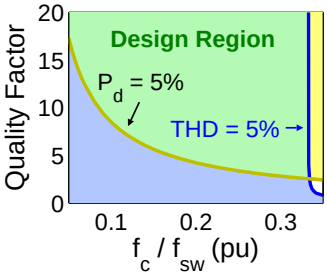
FC	$C_n = 0.12$pu	$C_n = 0.06$pu	$C_n = 0.03$pu
1			
2			
3			
4			

Table 5.7: Effect of varying switching frequency, f_{sw}, on filter design region, for filter configurations (FC) 1, 2, 3 and 4. The f_{sw} is equal to 4, 7 and 10kHz, for a filter capacitance of 0.12pu.

FC	f_{sw} = 4kHz	f_{sw} = 7kHz	f_{sw} = 10kHz
1			
2			
3			
4			

In summary, the design region of FC 1 and 4, is maximised by increasing either C_n (within the leading power factor limit) or the f_{sw}. Conversely,the design region of FC 2 can be maximised by reducing either C_n or the f_{sw}. Filter configuration 3 is shown to be least affected by either C_n or f_{sw} variation, and offers the lowest value of Q. These attributes make FC 3 the filter of choice.

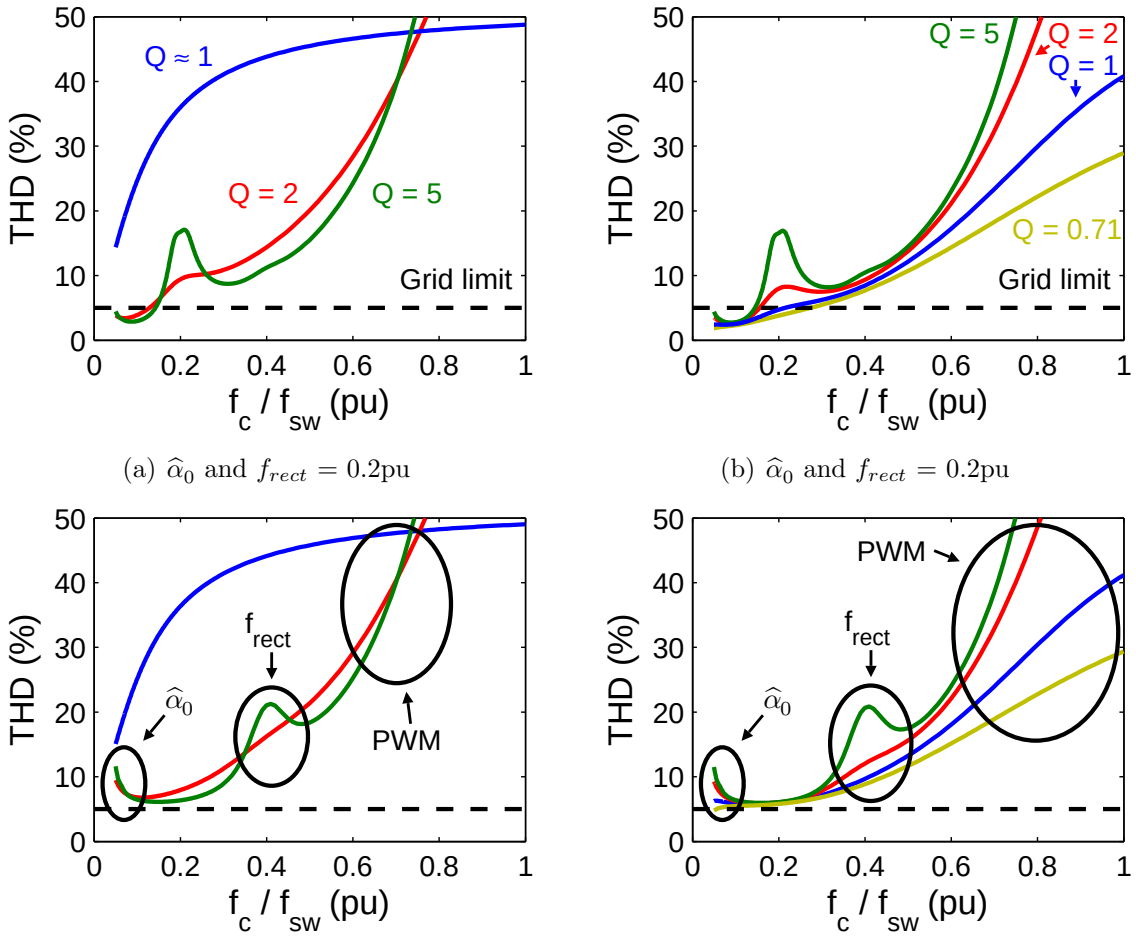
5.3.9 Effect of Non-Ideal Current Source

Thus far, it is assumed that the filter is supplied with a unipolar PWM current that is created using an ideal constant current source, however, the proposed GCI uses a PM generator and uncontrolled rectifier. Therefore, the effects of this non-ideal current source (NICS), are examined here. Unlike the ideal PWM current case, the quality factor becomes important as low and medium-frequency harmonics exist; these are caused by the fluctuating output power (α_0) and the rectifier ripple (f_{rect}), respectively. These harmonics will be amplified if the f_{res} is equal (or close) to the harmonic frequencies, and if Q exceeds 1. This is highly likely, as Figure 5.44 indicates that the Q for FC 1, 2 and 4, must be greater than 4 to meet the THD and power loss design region. In addition, the resonant frequency will be fixed (due to fixed filter components), whilst the rectifier ripple frequency will vary with turbine (wind) speed.

The THD vs. cutoff frequency is shown in Figure 5.46, using the NICS and for cases i) $\widehat{\alpha}_0$ and $f_{rect} = 0.2$pu, and ii) $\widehat{\alpha}_0$ and $f_{rect} = 0.4$pu. The plot appears similar to that of the ideal PWM input current case (Figure 5.38), however, the THD is shown to increase at low and medium cutoff frequencies. This is caused by resonance; the extent of which depends on the quality factor, and value of $\widehat{\alpha}_0$. The figure also identifies the source of harmonics, e.g. those caused by the fluctuating input power ($\widehat{\alpha}_0$), the rectifier ripple (f_{rect}) or the PWM switching (PWM).

The key conclusion from Figure 5.46 is that the NICS significantly reduces the range of f_c, for which the inverter is able to meet the grid THD requirement. The inverter is shown to exceed this 5% requirement if $\widehat{\alpha}_0$ exceeds 0.4pu; α_0 can be reduced by over-sizing the machine (as mentioned in Section 5.2.6), however, this does not remove the rectifier ripple harmonics. The ideal solution is to remove the low and medium-frequency harmonics caused by the NICS, such that the filter must only attenuate the high-frequency (PWM) harmonics, and the effects of resonance can be hence be ignored. The low and medium-frequency harmonics can be effectively removed by incorporating a more sophisticated,

e.g. feedback or feed-forward, controller. A feed-forward control algorithm is investigated in Section 5.4.



(a) $\widehat{\alpha}_0$ and $f_{rect} = 0.2$pu

(b) $\widehat{\alpha}_0$ and $f_{rect} = 0.2$pu

(c) $\widehat{\alpha}_0$ and $f_{rect} = 0.4$pu

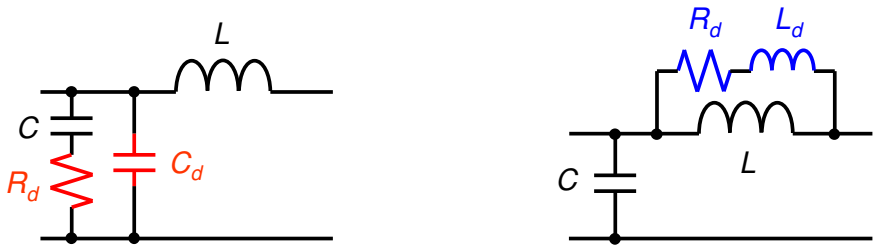
(d) $\widehat{\alpha}_0$ and $f_{rect} = 0.4$pu

Figure 5.46: THD vs. cutoff frequency and quality factor (Q), showing the effects of fluctuating output power ($\widehat{\alpha}_0$) and the rectifier ripple frequency (f_{rect}), for filter configurations (a) 1 and 3, and (b) 2 and 4. The THD is shown for (top) $\widehat{\alpha}_0$ and $f_{rect} = 0.2$pu, and (bottom) $\widehat{\alpha}_0$ and $f_{rect} = 0.4$pu. The harmonics sources are identified in the latter.

5.3.10 Alternative (Third-Order) Filter Configurations

Third-order low pass filters that meet the impedance mismatch criteria are shown in Figure 5.47, these include the *parallel* and *series*-damped third-order filters. Note the term series or parallel-damped refers to the connection of the damping resistor with respect to the reactive elements (either C_d or L_d). Both filters have a roll-off rate of -40dB/decade,

however the parallel-damped filter has lower power losses [105]. These filters are beyond the scope of this work and are further discussed in [105,113]. Given that FC 3 is promising it is not necessary to further investigate third-order filters.



(a) Parallel damped (b) Series damped

Figure 5.47: Third-order variations of the damped LC low-pass filters, including the (a) parallel and (b) series damped configurations.

5.4 Feed-Forward Control

5.4.1 Introduction

A system which shows feed-forward behaviour responds to a measured input disturbance in a pre-defined way; this differs to feedback systems that deal with any deviation from the desired system output behaviour. Feed-forward systems require a system model and are hence sensitive to model inaccuracies. The controlled variable will deviate from the desired output unless all input disturbances are anticipated [114] and are accurately calculable [115]. Feed-forward controllers hence use sophisticated calculations to accurately model input disturbances [114]. Despite this, feed-forward systems are stable and respond quickly [116]. In contrast, feedback systems do not require a system model, as they are based on closed-loop control. They are hence slower to respond, and may become unstable, however, they are able to deal with unique disturbances.

Conventional voltage-source, current-controlled inverters use feedback control based on sampling the output current. The difference between the instantaneous output and reference currents is known as the error. The controller adjusts the inverter switching signals to minimise the error. In contrast, a feed-forward controller would sample an input parameter, e.g. the machine speed or inverter input current, and apply a predetermined control pattern to the inverter. Both controllers require a fast processor for rapid sampling, however, the feed-forward system generally has lower costs, as the required sensors are generally cheaper. The machine speed can be easily measured using a low-cost Hall-effect sensor or the inverter input current can be measured using a low-cost shunt resistor, whilst the equivalent feedback control system requires a more expensive isolated current sensor.

5.4.2 Aim of Proposed Feed-Forward Control

Feed-forward control is investigated here to remove the low and medium-frequency harmonics, due to the fluctuating input power ($\widehat{\alpha}$) and the rectifier ripple, respectively. Section 5.2.3 showed that the low-frequency harmonics, and hence the THD, could be reduced by decreasing the modulation index. However, this also reduced the fundamental component and was unable to reduce the rectifier ripple harmonics. The proposed feed-forward (compensation) scheme aims to remove the low and medium-frequency harmonics, by adjusting the modulation index (and hence duty-cycle) in real-time, such that a sinusoidal output current with zero distortion is obtained. Note that the inverter output current obtained using the feed-forward controller is referred to as the *compensated* current.

An example of the open-loop inverter input and compensated inverter output currents is shown in Figure 5.48, for a rectifier ripple frequency of 1.8kHz, and a $\widehat{\alpha}_0$ of 0.25pu. The compensated output current, $i_c(t)$, has a peak equal to $\beta\sqrt{3}/2$ pu, as this corresponds to the minimum rectifier ripple. Hence a compensated current whose peak is less than or equal to the minimum open-loop inverter input current will not contain harmonic distortion caused by the rectifier ripple or the fluctuating input power ($\widehat{\alpha}_0$).

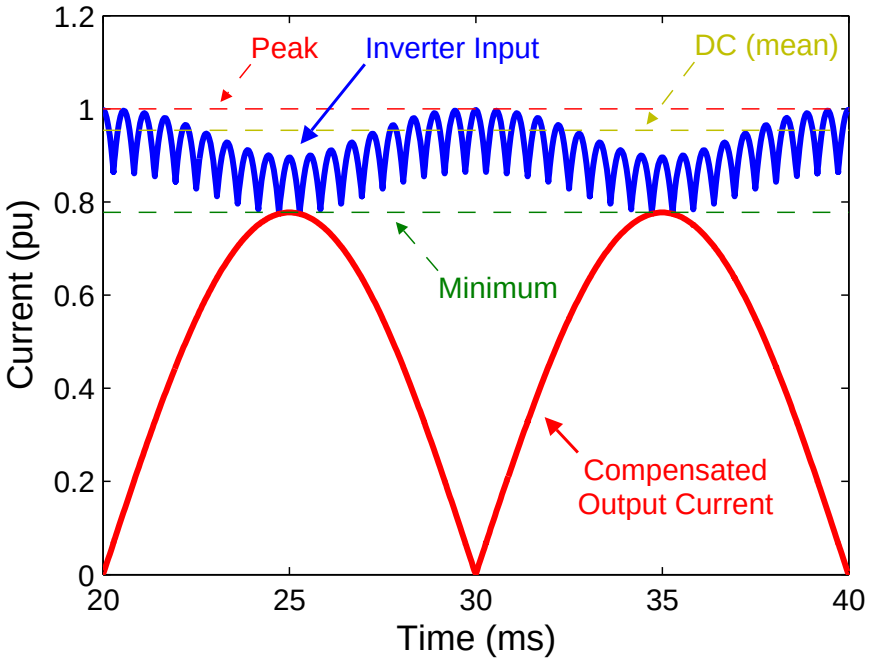


Figure 5.48: Feed-forward current compensation concept, showing the normalised open-loop inverter input current and the rectified compensated inverter output current. The rectifier ripple frequency is shown for 1.8kHz, whilst $\widehat{\alpha}_0$ is equal to 0.25pu. Note that the terms *peak*, *DC (mean)* and *minimum* refer to the open-loop inverter input current.

The ideal compensated output current, $i_{c\ (id)}(t)$, is expressed by Equation (5.45), which substitutes β (from above) by Equation (5.7), for the ideal case. The experimental compensated current, $i_{c\ exp}(t)$, is derived in a similar manner and is shown in Equation (5.46); this is derived by substituting β by Equation (5.8).

$$i_{c\ (id)}(t) = \frac{\sqrt{3}}{2}\sqrt{1-\widehat{\alpha}_0^{\,2}}\,.\sin(\omega_g t) \quad \text{(pu)} \tag{5.45}$$

$$i_{c\ (exp)}(t) = \frac{\sqrt{3}}{2}\left(3.86\,\widehat{\alpha}_0^{\,5} - 7.47\,\widehat{\alpha}_0^{\,4} + 4.27\,\widehat{\alpha}_0^{\,3} - 1.53\,\widehat{\alpha}_0^{\,2} - 0.116\,\widehat{\alpha}_0 + 1\right).\sin(\omega_g t) \quad \text{(pu)} \tag{5.46}$$

Two types of feed-forward control are proposed to obtain a distortion-free output current. The first samples the generator frequency, f_m, whilst the second technique samples the inverter input current, $i_{in}(t)$. Both techniques instantaneously manipulate the inverter modulation index, m_a, (and hence the duty-cycle) such that a sinusoidal inverter output current is obtained.

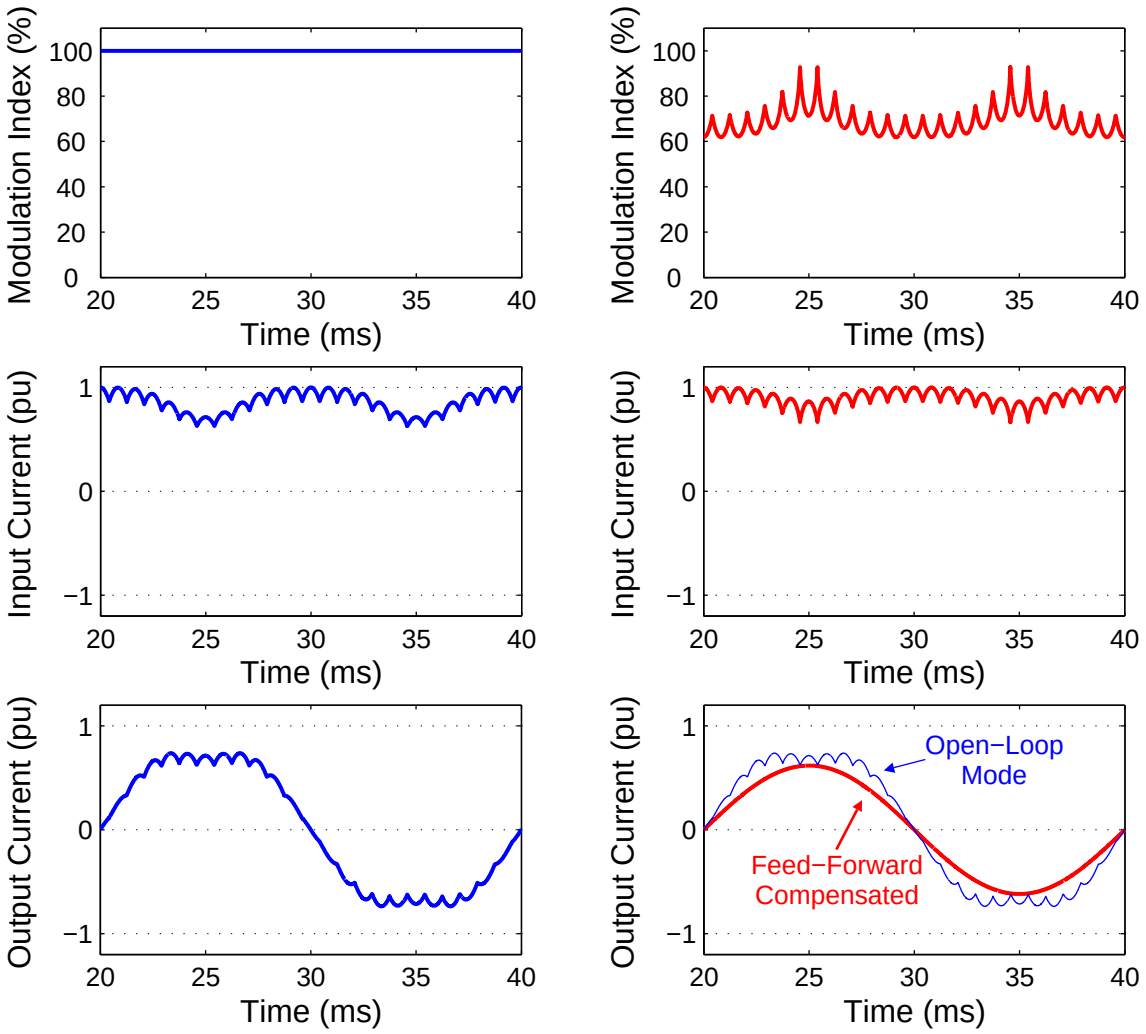
5.4.3 Controller 1 (FFC 1): Sample Machine Frequency

Consider the ideal I-V locus. The resulting ideal inverter output current, which contains input current harmonic distortion, is expressed by Equation (5.15). The feed-forward controller is able to effectively remove the input current distortion if the ideal output current is equal to the ideal compensated current, i.e. Equation (5.45). This is summarised in Equation (5.47), which simplifies the ideal output current (right-hand side of the expression). This equality is rearranged and solved for in terms of m_a; the resulting required time-varying modulation index, $m_a(t)$, is expressed in Equation (5.48), and is shown in Figure 5.49(b). The solution is expressed in terms of $rect(t)$, $\widehat{\alpha}_0$ and $\sin(\omega_g t)$. The sinusoid can be stored in a look-up-table, however both $rect(t)$ and $\widehat{\alpha}_0$ must be calculated in real-time; these parameters can be calculated from the machine frequency, using a Hall-effect sensor.

$$\frac{\sqrt{3}}{2}\sqrt{1-\widehat{\alpha}_0^{\,2}}.sin(\omega_g t) \;=\; rect(t).m_a(t).sin(\omega_g t)\sqrt{1-V_{in}^{\,2}(t)} \tag{5.47}$$

$$m_a(t) = \frac{\sqrt{2}}{2.rect(t).sin(\omega_g t).\widehat{\alpha}_0}\sqrt{rect^2(t) - \sqrt{rect^4(t) - 3.rect^2(t).sin(\omega_g t).\widehat{\alpha}_0^{\,2}\left(1-\widehat{\alpha}_0^{\,2}\right)}} \tag{5.48}$$

A comparison of the inverter performance using both open-loop (uncompensated) and feed-forward compensated control, for the ideal rectifier I-V locus, is shown in Figure 5.49. The figure shows the modulation index and the subsequent inverter input and output currents for $\widehat{\alpha}_0 = 0.7$pu. The benefit of feed-forward inverter control is clearly seen, i.e. the harmonic components are completely removed and the output current THD is ideally zero. Although the feed-forward controller significantly improves the inverter output current THD, its magnitude is now lower than its open-loop equivalent. This is further discussed for the experimental locus case in Section 5.4.5.



(a) Open-Loop Control (b) Feed-Forward Control

Figure 5.49: Comparison of the (a) open-loop and (b) feed-forward control schemes using the **ideal** I-V locus for $\widehat{\alpha}_0 = 0.7$pu. Each control mode shows the modulation index and the resulting inverter input and output currents, from top to bottom, respectively.

Now consider the experimental locus. The time-varying modulation index is determined by a similar approach, however the experimental compensated current (Equation (5.46)) is equated to the experimental inverter output current and rearranged, as summarised by Equation (5.49). Unlike the ideal locus case, a *closed form solution* does not exist; this is verified by *Abel's impossibility theorem* that states that "*polynomial equations higher than fourth degree are incapable of algebraic solution in terms of a finite number of additions, subtractions, multiplications, divisions, and root extractions*" [117].

$$3.86\,\widehat{\alpha}_0^{\,5}.\sin^{10}(\omega_g t).m_a^{\,6}(t) - 7.47\,\widehat{\alpha}_0^{\,4}.\sin^{8}(\omega_g t).m_a^{\,4}(t) + 4.27\,\widehat{\alpha}_0^{\,3}.\sin^{6}(\omega_g t).m_a^{\,3}(t)$$
$$-1.53\,\widehat{\alpha}_0^{\,2}.\sin^{4}(\omega_g t).m_a^{\,2}(t) - 0.116\,\widehat{\alpha}_0.\sin^{2}(\omega_g t).m_a(t) + 1$$
$$-\frac{\sqrt{3}}{2}\sqrt{3.86\,\widehat{\alpha}_0^{\,5} - 7.47\,\widehat{\alpha}_0^{\,4} + 4.27\,\widehat{\alpha}_0^{\,3} - 1.53\,\widehat{\alpha}_0^{\,2} - 0.116.\widehat{\alpha}_0 + 1} = 0 \tag{5.49}$$

The experimental I-V locus must be simplified if a closed-form solution is to be found. It is hence approximated, as shown in Equation (5.50). The resulting I-V locus for $\widehat{\alpha}_0 = 0.7$pu is shown in Figure 5.50; the ideal and experimental loci are shown for reference.

$$\beta_{app} \approx \sqrt{1 - (2 - \alpha_0^{\,2})\,\alpha_0^{\,2}} \tag{5.50}$$

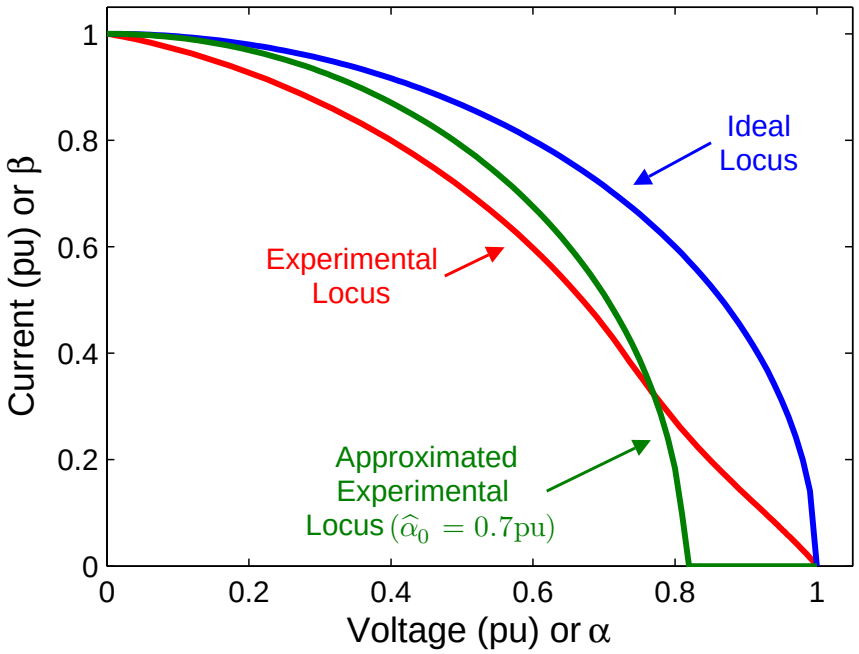
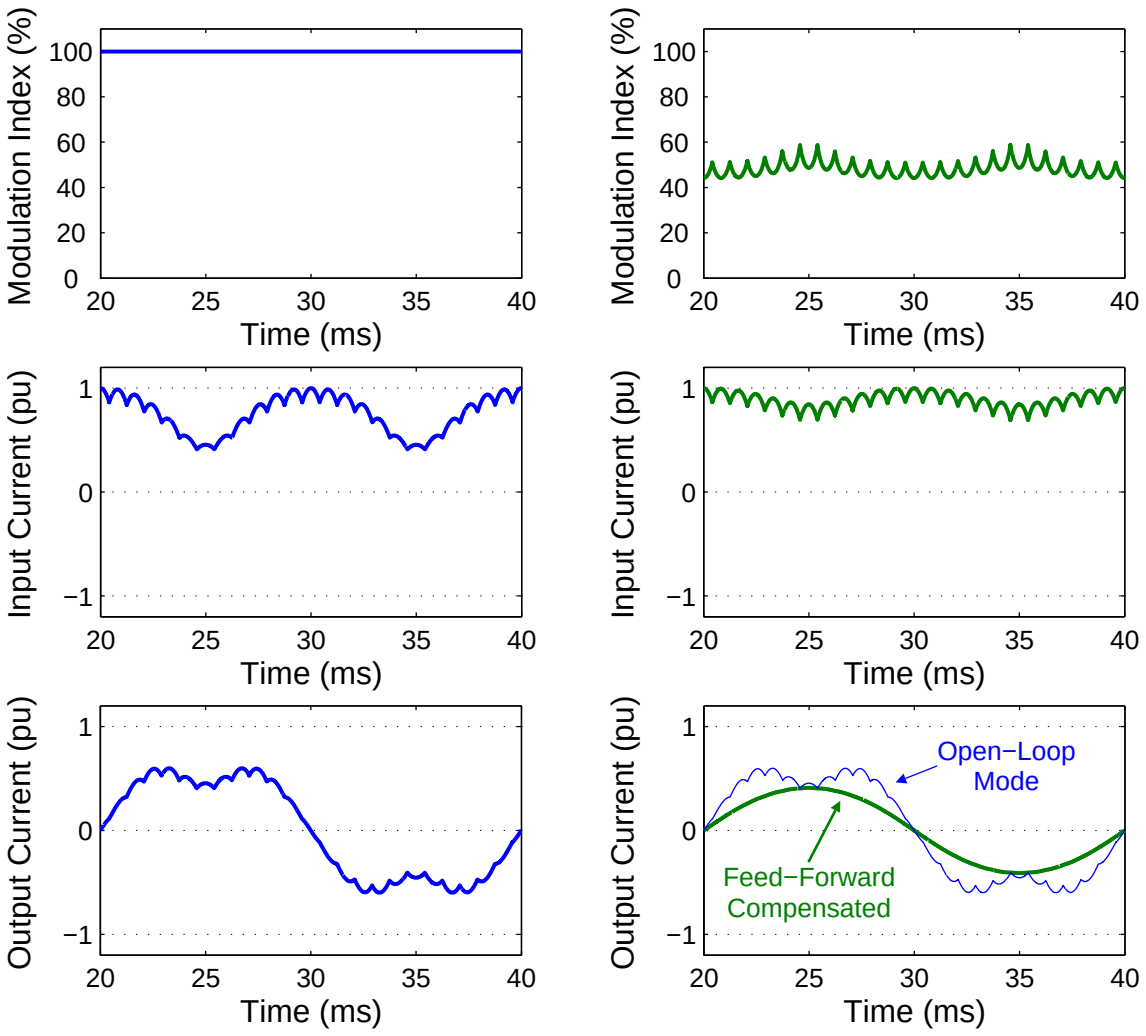


Figure 5.50: Approximated, experimental and ideal rectifier I-V loci.

The small discrepancies between the approximated and measured loci imply that the compensated inverter output current will contain some distortion. This is seen in Figure 5.51, which shows the time-varying modulation index and the resulting inverter input and output currents; the output current contains 1.9% THD. The time-varying m_a is found using the same approach shown for the ideal case, i.e. by using β_{app} (Equation (5.50)) and hence solving Equation (5.51) in terms of $m_a(t)$; the solution is expressed in Equation (5.52).

$$\frac{\sqrt{3}}{2}\sqrt{1-\left(2-\widehat{\alpha}_0^{\,2}\right)\widehat{\alpha}_0^{\,2}}\;.\;sin(\omega_g t) = rect(t).m_a(t).sin(\omega_g t)\sqrt{1-\left(2-\widehat{\alpha}_0^{\,2}\right)V_{in}^{\,2}(t)} \quad (5.51)$$

$$m_a(t) = \frac{\sqrt{2.rect(t).\left(2-\widehat{\alpha}_0^{\,2}\right)\left(rect(t)-\sqrt{rect^2(t)-3.\sin^4(\omega_g t)\,\widehat{\alpha}_0^{\,2}\left(2-5\,\widehat{\alpha}_0^2+4\,\widehat{\alpha}_0^4-\widehat{\alpha}_0^6\right)}\right)}}{2.rect(t).\sin^2(\omega_g t)\,\widehat{\alpha}_0\left(2-\widehat{\alpha}_0^{\,2}\right)} \quad (5.52)$$



(a) Open-Loop Control (b) Feed-Forward Control

Figure 5.51: Comparison of the (a) open-loop and (b) feed-forward control schemes using the approximated experimental I-V locus for $\widehat{\alpha}_0 = 0.7$pu. Each control mode shows the modulation index, inverter input and output currents, from top to bottom, respectively.

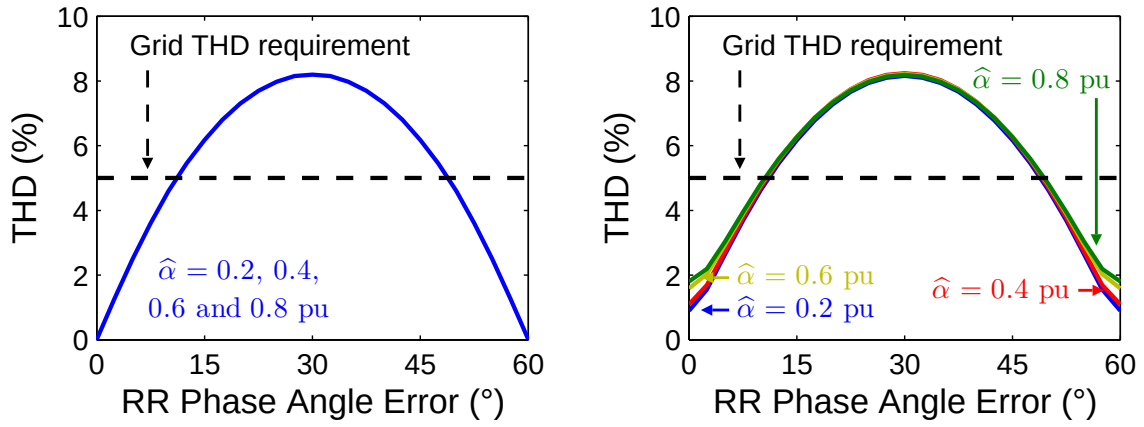
Although this feed-forward control algorithm significantly improves the quality of the inverter output current, it is difficult to implement due to the complexity of the required time-varying m_a solution, which must be calculated in real-time. In addition, the peak compensated inverter output current is less than the peak open-loop current. This is due to the control algorithm that delivers a (compensated) sinusoidal inverter output current whose peak is equal to the minimum inverter input current.

Comparison of Figures 5.49(b) and 5.51(b) show that the peak compensated output current, using the (approximated) experimental I-V locus, is less than that using the ideal locus. This is due to the shape of the approximated experiential locus, which significantly reduces the minimum inverter input current, using open-loop control. Note that the peak experimental compensated output current is also less than the minimum inverter input current (see Figure 5.51(b)). This implies that the fundamental magnitude of the compensated output current can increase without containing distortion providing the peak compensated current is less than the minimum inverter input current. This is further examined in Section 6.3.3.

Rectifier Ripple Phase Angle Errors

Although the feed-forward control concept has been successfully demonstrated, it should be noted that the phase of the rectifier ripple current waveform is assumed to be known. This, however, will require rotor position information which increases the cost of implementation. The effect of the rectifier ripple phase angle error is analysed below.

The rectifier ripple (RR) phase angle error will affect the feed-forward controller's ability to remove the rectifier ripple harmonics, however, it will not affect the controller's ability to remove the low-frequency harmonics. The maximum phase error is 60°, and as such, the most RR distortion and hence compensated current THD is expected to occur for a phase error of 30°. In contrast the least rectifier ripple distortion and hence compensated output current THD is expected to occur when the rectifier ripple phase angle error is 0 or 60°. This is verified in Figure 5.52, which shows the compensated current THD as a function of rectifier phase angle error, using both the ideal and approximated experimental I-V loci. There is little difference between the ideal and experimental THD curves, except at phase angle errors of between 0 and 10°, and 50 and 60°, where the ideal locus produces a lower THD. Note that the peak compensated current THD is 8.2%, which is about twice that caused by the RR (4.19%), and that the THD curves are symmetrical and centred at 30°.



(a) Ideal locus

(b) Experimental locus

Figure 5.52: Compensated inverter output current THD vs. rectifier ripple (RR) phase angle error, for the (a) ideal, and (b) approximated experimental I-V loci. The THD is shown for $\widehat{\alpha}_0$ equal to 0.2, 0.4, 0.6 and 0.8pu. The dashed line represents the grid THD limit of 5%.

The above figure indicates that the feed-forward algorithm will only meet the grid THD requirement over a small range of phase angle errors, i.e. less than $\pm$ 11°. This, coupled with the fact that low-cost microcontrollers may be unable to perform such complex m_a calculations in real-time, justifies the need for a simpler and faster feed-forward control algorithm.

5.4.4 Controller 2 (FFC 2): Sample Inverter Input Current

The second feed-forward controller samples the inverter input current, hence it is not required to be calculated in real-time. This allows the controller to quickly calculate the required duty-cycle and hence modulation, based on the ideal boost equation, as shown in Equation (5.53), which relates the inverter input and output currents, $i_{in}(t)$ and $i_{out}(t)$, respectively. Note that this was previously expressed in terms of the rectifier and wave-shaper output currents (Equation (5.9)).

$$i_{out}(t) = [1 - d(t)] \, . i_{in}(t) \tag{5.53}$$

The term $[1 - d(t)]$, from the above expression, is given by $m_a(t).\sin(\omega_g t)$, as shown in Equation (5.54). The term $i_{out}(t)$ is now replaced by the appropriate expression for the desired (compensated) output current, and hence the time-varying modulation index

can be found. The solution, however, is dependent on the I-V locus used, i.e. Equations (5.55) and (5.56) represent the time-varying modulation indices using the ideal and the experimental I-V loci, respectively.

$$i_{out}(t) = m_a(t).\sin(\omega t).i_{in}(t) \tag{5.54}$$

$$m_a(t) = \frac{\frac{\sqrt{3}}{2}\sqrt{1-\widehat{\alpha}_0^{\,2}}}{i_{in}(t)} \tag{5.55}$$

$$m_a(t) = \frac{\frac{\sqrt{3}}{2}\left(3.86\,\widehat{\alpha}_0^{\,5} - 7.47\,\widehat{\alpha}_0^{\,4} + 4.27\,\widehat{\alpha}_0^{\,3} - 1.53\,\widehat{\alpha}_0^{\,2} - 0.116\,\widehat{\alpha}_0 + 1\right)}{i_{in}(t)} \tag{5.56}$$

The second feed-forward controller is able to calculate the required time-varying modulation index much faster than the first feed-forward scheme, due to the simpler expression for $m_a(t)$. Despite this, α_0 must also be calculated, which hence requires a generator speed sensor and knowledge of the generator (I-V locus) and a gird voltage sensor. Note that the calculation time can be reduced by using look-up-tables to store i) the normalised rectifier I-V locus, i.e. β_0 vs. α_0, and the generator speed vs. α_0 information. The second feed-froward controller is selected over the first type, as it is simpler and does not require rotor position information. A summary of the feed-forward controller is shown in Figure 5.53, it replaces the *Modulation Index* box (on the left-hand side) of Figure 4.17.

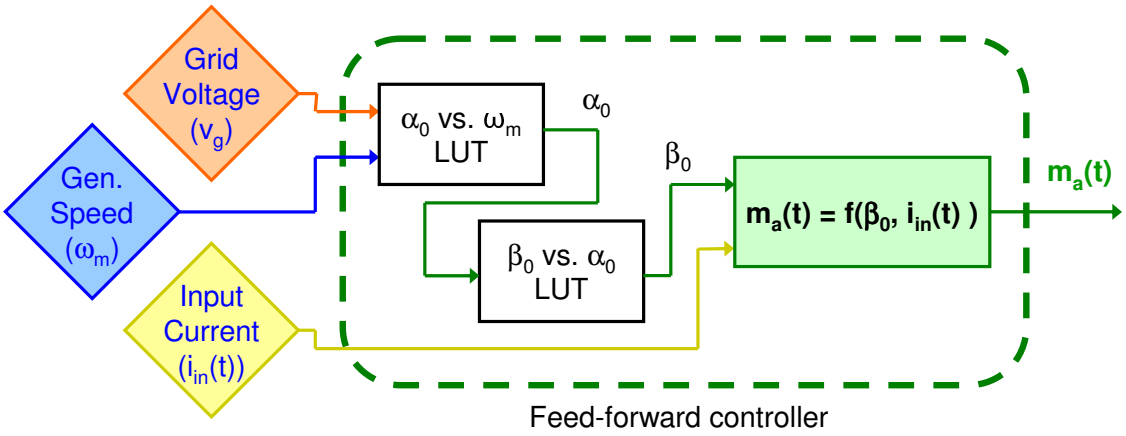
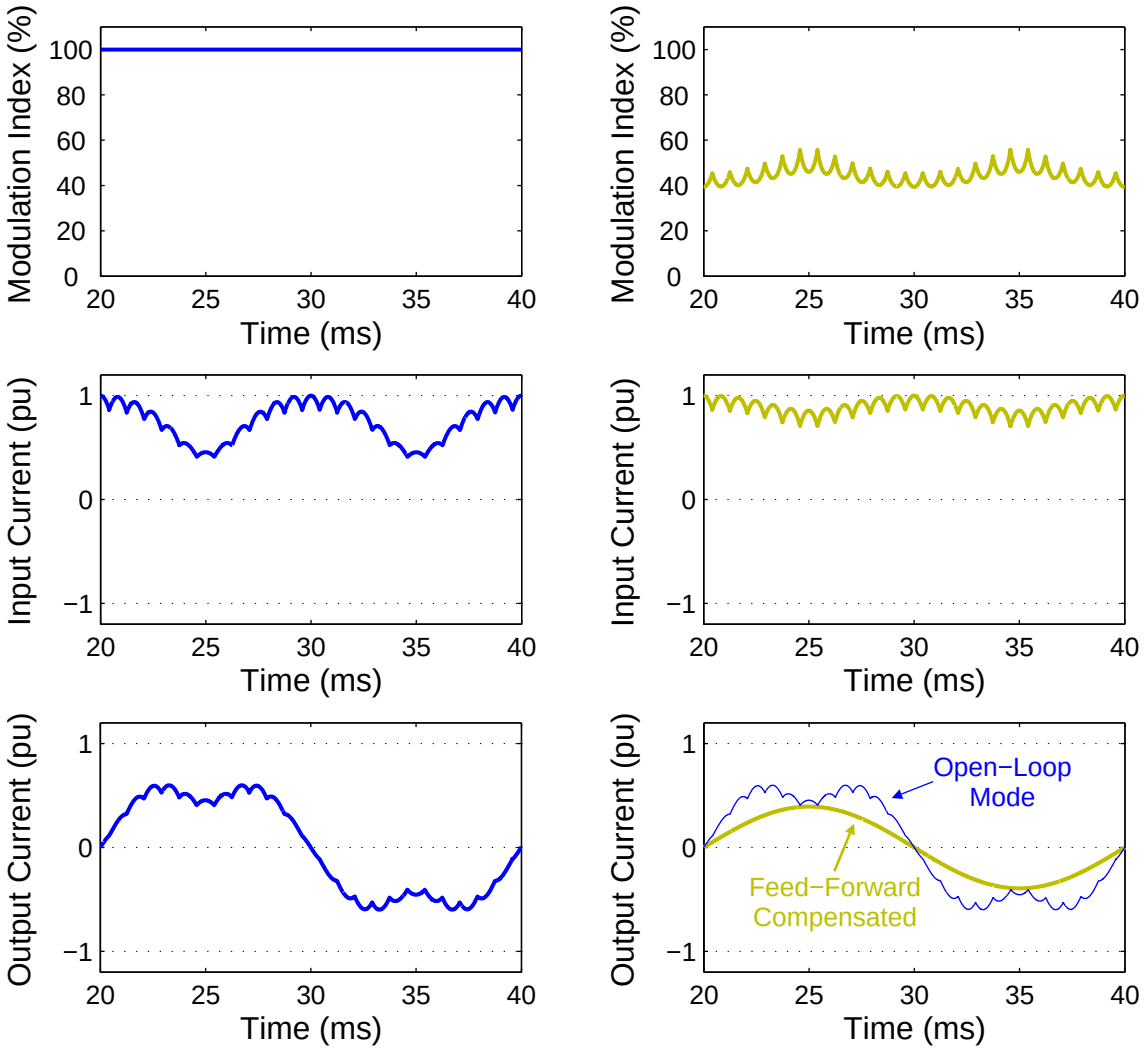


Figure 5.53: Feed-forward controller summary, showing the input and output stages, and the look-up-tables (LUT). The diamonds represent input stages and include the sampled grid voltage, v_g, input current, $i_{in}(t)$, and generator speed, ω_m, whilst the time-varying modulation index, $m_a(t)$, is the controller output.

Figure 5.54 compares the inverter performance using both the open-loop and the second feed-forward controller, for the experimental rectifier I-V locus. The figure shows the calculated modulation index and the subsequent inverter input and output currents for $\widehat{\alpha}_0 = 0.7$pu. The benefit of the feed-forward controller is clearly demonstrated, i.e. the low and medium-frequency harmonics are eliminated. The output current now contains zero THD, irrespective of which I-V locus is used. Note that both feed-forward controllers behave alike when using the ideal I-V locus (see Figure 5.49), hence it is not examined.



(a) Open-Loop Control (b) Feed-Forward Control

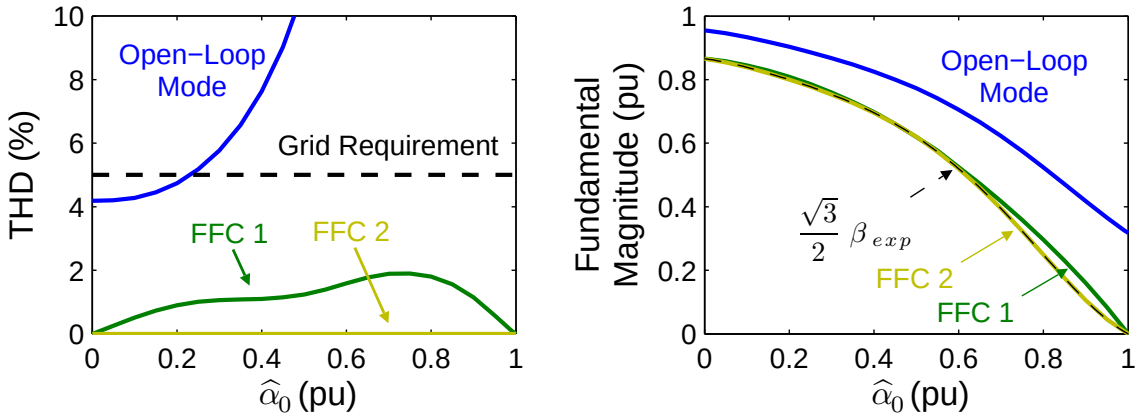
Figure 5.54: Comparison of the (a) open-loop and (b) feed-forward compensated control schemes using the experimental I-V locus for $\widehat{\alpha}_0 = 0.7$pu. Each control mode shows the modulation index, inverter input and output currents, from top to bottom, respectively.

5.4.5 Comparison of Feed-Forward and Open-Loop Control

This section compares the inverter's performance using both open-loop and the two feed-forward controllers. The inverter output current THD and fundamental magnitudes are compared, over a wide range of wind speeds. The THD and fundamental magnitude is first examined as a function of $\widehat{\alpha}_0$, as $\widehat{\alpha}_0$ varies with wind and hence turbine speed.

Inverter Performance vs. $\widehat{\alpha}_0$

This section examines the THD and fundamental magnitude of the inverter output current waveform, when comparing open-loop and both feed-forward controllers, for the experimental locus, over a wide range of $\widehat{\alpha}_0$. Figure 5.55(a) shows that both of the feed-forward control algorithms significantly reduce the inverter output current THD, and allow the inverter to meet the grid THD requirement over a much wider range of $\widehat{\alpha}_0$, compared to that of the open-loop controller. Note that the open-loop case corresponds to a modulation index of 100%, and the phase angle of the rectifier ripple is assumed to be known for FFC 1.



(a) THD

(b) Fundamental magnitude

Figure 5.55: Inverter output current (a) THD, and (b) fundamental magnitude vs. $\widehat{\alpha}_0$ using open-loop and both feed-forward control algorithms. The dashed line in (a) represents the grid THD requirement, whilst in (b) it corresponds to the calculated minimum inverter input current for the experimental locus, $\sqrt{3}/2\ \beta_{exp}$. Note that the open-loop curve corresponds to a modulation index of 100%.

Comparison of the above THD plots, shows that FFC 1 contains some residual distortion ($< 2\%$), whilst FFC 2 is ideally able to eliminate all of the harmonics. The small level of output current distortion, using FFC 1, is caused by the difference in the approximated

and experimental inverter input currents, which itself is a result of the slight discrepancies between the approximated and the experimental I-V loci (recall Figure 5.50). In contrast, the output current THD of FFC 2 is zero, as the inverter input current is measured and not approximated.

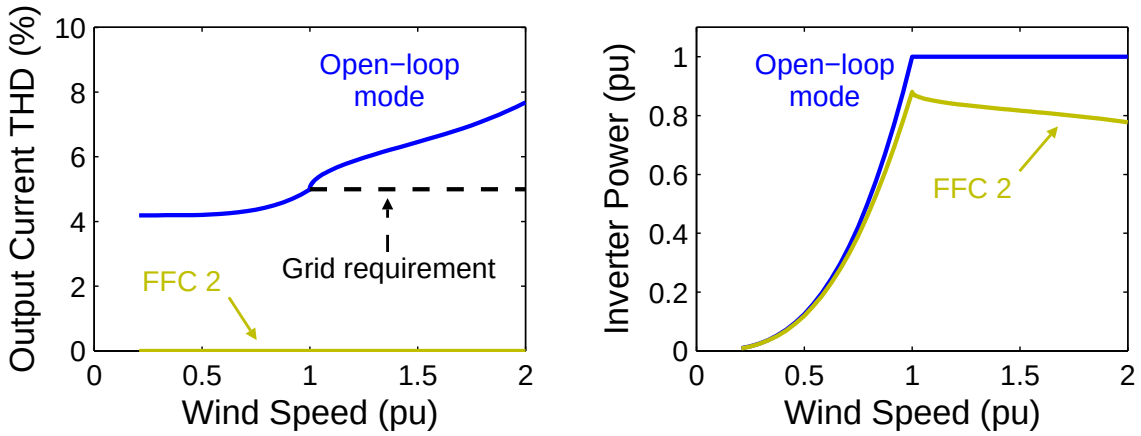
Despite the reduction in output current THD, Figure 5.55 shows that the fundamental magnitude of the compensated output current is lower than its open-loop equivalent. Recall that the compensated current should have a fundamental magnitude less than or equal to $\beta_{exp}\sqrt{3}/2$, in order to effectively eliminate the rectifier ripple associated harmonics; this is shown in Figure 5.55(b) by the dashed line. The figure shows that FFC 1 is able to deliver an output current whose magnitude closely matches that of the expected curve, however, small discrepancies exist at higher values of $\widehat{\alpha}_0$, due to the approximated experimental I-V locus. In contrast, FFC 2 is able to yield a sinusoidal output current whose fundamental is exactly equal to $\beta_{exp}\sqrt{3}/2$, as the inverter input current is measured and not approximated.

Although both feed-forward controllers were demonstrated to effectively reduce the inverter output current THD, the second controller performs better as it yields a purely sinusoidal output current with zero distortion. In addition, this controller uses a much simpler calculation of the time-varying modulation index than FFC 1. As such, only FFC 2 is considered in the following section.

Inverter Performance vs. Wind Speed

The inverter output current THD and normalised output power is examined as a function of normalised wind speed. This is shown in Figure 5.56 for both open-loop and feed-forward controllers. Note that only FFC 2 is examined. The open-loop inverter output power and current THD is obtained from Figures 5.17(a) and 5.18, respectively, whilst those using FFC 2, are determined from $\widehat{\alpha}$ (Figure 5.17) and Figure 5.55.

The feed-forward controller delivers a sinusoidal output current, with zero distortion, to the grid over the entire range of wind speeds. The open-loop controller, however, can only meet the grid THD requirement below rated wind speed, providing the low-pass filter resonant frequency does not coincide with any harmonics. Despite this, the inverter is able to deliver more power to the grid using open-loop control, as the FFC 2 reduces the fundamental magnitude of the output current in order to remove the rectifier ripple harmonics. Hence, a power quality (THD) vs. quantity (power) trade-off exists below rated wind speed, for a given generator, providing the effects of resonance are ignored.



(a) THD

(b) Power

Figure 5.56: Inverter output (a) current THD, and (b) power, vs. wind speed, for both open-loop and feed-froward (FFC 2) controllers. The dashed line in (a) represents the grid THD requirement, which applies at rated output power.

Despite the trade-off, the benefits of the feed-forward controller significantly outweigh its open-loop alternative, i.e. the feed-forward controller delivers high quality current at all wind speeds, and allows the low-pass filter to be designed for any resonant frequency. Note that the open-loop controller only obtains slightly more power than FFC 2 for a given generator. Hence, the inverter can easily deliver rated power to the grid by simply over-sizing the generator.

5.5 Chapter Summary

Open-loop sinusoidal modulation of the current wave-shaper (SMR) switch means that the input current harmonics appear in the output current. The rectifier ripple current by itself causes an output current THD of 4.19%, which is independent of generator speed, whilst that caused by the low-frequency (100Hz power) ripple is proportional to the ratio of the rectifier output voltage under load to its open-circuit voltage and hence inverter output power. This was shown graphically using the I-V locus, as the generator is pushed in to the variable-voltage region, where it is unable to provide constant current.

The grid requires an output current with less than 5% THD, which assuming only low-frequency rectifier ripple are present in the inverter output current, implies the peak inverter output voltage must be less than 23% of the rectified open-circuit voltage. The low-frequency ripple is shown to decrease with modulation index, as this effectively reduces the effective rectifier output voltage and hence output power. Despite the reduced input current ripple, the output current fundamental is also reduced with decreasing modulation index, due to its linear relationship with input current. This causes the output current THD to increase due to the presence of the PWM harmonic components.

A feed-forward controller produces the desired output current waveform despite a varying input current. This is done by either sampling the or accurately calculating the instantaneous inverter input current and adjusting the modulation index (and hence duty-cycle) in real-time.

The high-frequency PWM harmonics of a current-source grid-connected inverter are removed by a capacitive-inductive low-pass grid filter, according to the impedance mismatch criteria. This type of filter is analysed, and it is shown that damping is required to limit the effect of resonance. Four damping resistor locations, and their respective power loss vs. harmonic attenuation (output current THD) trade-offs are discussed. The configuration with the damping resistor connected in parallel to the filter inductor, offers the least power loss, whilst sufficiently attenuating the high-frequency PWM harmonics. In addition, the choice of filter capacitance and inductance is shown to be a trade-off between the cut-off frequency and grid power factor. The analysis shows that a cut-off frequency of at least ten times the fundamental is required to prevent significant filter delay, and that a filter capacitance of less than 0.12pu is required to meet the light-load Australian Standard power factor requirement. A detailed filter design approach is produced, that determines the filter parameters based on the desired cut-off frequency, power loss and ideal output current THD.

Chapter 6

Design and Simulation of 1kW Grid-Connected Inverter System

This chapter uses the principles of wind power and the inverter analysis from Chapter 5 to design a 1kW grid-connected wind turbine that delivers high quality power to the grid over a wide range of wind speeds. The chapter begins with a turbine design that allows the inverter to provide rated power at rated wind speed. This is followed by a low-pass filter design that ensures the inverter complies with the grid specifications, at rated wind speed using an open-loop control mode. Finally, the inverter and turbine are shown to meet the grid requirements over a wide range of wind speeds, by employing a simple and low-cost feed-forward controller.

6.1 Turbine Sizing and Machine Parameter Selection

The wind turbine needs to be designed such that the inverter is able to deliver rated power, 1kW, to the grid at the chosen rated wind speed, 12m/s. The Fisher & Paykel® machine tested in Chapters 2 and 4 is unable to provide the required 1kW+ of power and hence a new generator is required for the proposed 1kW grid-connected inverter. Although electrical machine and turbine blade design is beyond the scope of this work, a suitable turbine and generator can be determined based on a series of assumptions.

6.1.1 System Assumptions

This section lists the assumptions made to calculate the size (power rating) of a suitable generator and wind turbine that delivers 1kW of electrical power to the grid at rated wind speed. Note that the assumptions listed regard the inverter, turbine and generator.

Inverter Assumptions

- the inverter switching frequency is limited to 10kHz, as this limits switching losses,
- the inverter is 95% efficient, based on calculated power loss caused by thyristor and diode voltage drops,
- the maximum damping resistance power loss, P_d, is limited to 50W (0.05pu),

Turbine Assumptions

- the peak c_p is equal to 0.30, for a turbine whose blade radius is about 1m [1],
- a 5 bladed turbine is used, which is identical in shape as that tested in Chapter 3, however, the blade length is changed,
- the blade power coefficient characteristic (c_p vs. λ) is based on that determined experimentally, however, its peak c_p is increased from 0.20 to 0.30, which occurs for a tip-speed ratio, λ, of 7.5; the c_p curve is shown in Section 6.1.2.

Generator Assumptions

- the machine has 24 pole-pairs (the same as a Fisher & Paykel® type outer rotor surface permanent magnet machine),
- the stator is star (wye) connected,
- the machine is 85% efficient at rated wind speed,
- the stator impedance is mainly inductive, such that the high-inductance characteristic is achieved,
- the back-EMF constant selected such that the ratio of the peak grid voltage to the peak generator rectified output voltage under open-circuit conditions, $\widehat{\alpha}_0$, is equal to 0.25pu at rated wind speed.

6.1.2 Turbine Power and Size Calculations

The wind turbine blade radius, r, is calculated based on the wind power required at rated wind speed. The wind power, P_W, is calculated knowing the maximum coeffi-

cient of performance, c_p, and the required wind turbine power, P_{WT}, as summarised in Equation (6.1); where ρ and v represent the air density and wind velocity, respectively.

$$P_W = \frac{P_{WT}}{c_p} = \frac{1}{2}\,\pi\, r^2 \rho\, v^3 \tag{6.1}$$

The wind turbine power is calculated from the total inverter input power, P_{in} and the inverter and generator efficiencies, η_{inv} and η_{gen}, respectively. This is summarised by Equation (6.2), which simplifies the total inverter input power, P_{invin}, as the summation of inverter output power, P_{inv}, and the maximum damping resistance power loss, P_d. Substitution of P_{WT} in to the above equation allows the turbine radius to be simplified, as summarised by Equation (6.3).

$$P_{WT} = \frac{P_{inv\ in}}{\eta_{inv}\,.\,\eta_{gen}} = \frac{P_{inv} + P_d}{\eta_{inv}\,.\,\eta_{gen}} \tag{6.2}$$

$$r = \sqrt{\frac{2\,(P_{inv} + P_d)}{\eta_{inv}.\eta_{gen}.c_p.\pi.\rho.v^3}} \tag{6.3}$$

The turbine speed can be determined once the turbine radius is calculated. The mechanical speed, ω_m, is determined from Equation (6.4), where λ represents the tip-speed ratio. Note that ω_m has units of rad/s, which is converted to a rotational speed with units rpm, n, using Equation (6.5); the turbine c_p curve used here is shown in Figure 6.1.

$$\omega_m = \frac{\lambda\, v}{r} \tag{6.4}$$

$$n = \omega_m\ \frac{60}{2\pi} \tag{6.5}$$

The above equations allow a turbine radius and operating speed to be calculated at rated wind speed, knowing a desired inverter power rating and a turbine blade characteristic (coefficient of performance). A summary of the turbine parameters required for use with the proposed 1kW grid-connected inverter, is summarised in Table 6.1.

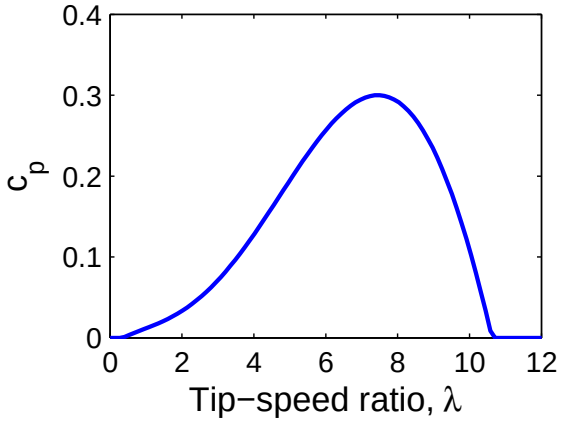


Figure 6.1: Turbine coefficient of performance, c_p, vs. tip-speed ratio, λ, characteristic used to calculate turbine operating speed at rated wind speed. The peak c_p is equal to 0.30 and occurs for a λ of 7.5. Note that the curve is based on the experimentally measured curve, however, it is scaled to achieve a higher peak c_p.

Table 6.1: Summary of calculated turbine properties that allows the proposed grid-connected inverter to deliver 1kW to the grid, at rated wind speed.

Property	Value
Rated Inverter power, P_{inv}	1000 W
Damping resistor power loss, P_d	50 W
Inverter efficiency, η_{inv}	95 %
Generator efficiency, η_{gen}	85 %
Wind turbine power, P_{WT}	1300 W
Peak c_p	0.30
Air density, ρ	1.225 kg/m^3
Blade length (radius), r	1.146 m
Tip-speed ratio, λ, for peak c_p	7.50
Rated Wind Speed, v_r	12m/s
Rated Turbine mechanical speed, ω_m	78.54 rad/s
Rated Turbine mechanical speed, n	750 rpm

6.1.3 Generator Equivalent Circuit Parameter Selection

The generator can be designed, as the turbine size and operating speed, at rated wind speed, has been determined. The design process is listed below:

1. calculate the required back-EMF constant to give $\widehat{\alpha}_0 = 0.25$pu,
2. find the generator short-circuit current that allows the inverter to deliver rated power, using the feed-forward current compensation scheme, to the grid,

3. determine the stator resistance from the assumed generator efficiency and losses, and

4. use the short-circuit current and back-EMF constant to calculate the stator impedance, and hence reactance (knowing the resistance).

Step 1 – Calculate the Back-EMF Constant

The back-EMF constant, k, is determined such that $\widehat{\alpha}_0$ is equal to 0.25pu at rated wind speed. This allows the peak generator rectified output voltage under open-circuit conditions, $V_{R\,pk}$, to be calculated knowing the peak grid voltage, $V_{g\,pk}$; recall that $\widehat{\alpha}_0$ is the ratio of these peaks, as summarised by Equation (6.6). Note that the peak rectifier output voltage is greater than the average DC output voltage, V_{DC}, as shown in Equation (6.7); V_{DC} itself is expressed relative to the peak phase voltage, $V_{ph\,pk}$, in Equation (6.8) [56].

$$\widehat{\alpha}_0 = \frac{V_{g\,pk}}{V_{R\,pk\,OC}} \tag{6.6}$$

$$V_{DC} = 0.9557\,V_{R\,pk} \tag{6.7}$$

$$V_{DC} = \frac{\pi}{2}\,V_{ph\,pk} \tag{6.8}$$

The nominal Australian grid voltage, at the *point of supply*, is $230\,V_{RMS}$, as set by Australian Standard 60038 [118]. Although a tolerance of $+\,10\%$ and $-\,6\%$ exists, the proposed grid-connected inverter will be designed for a rated voltage of 230 V. This, along with Equations (6.6) – (6.8), implies that the generator peak back-EMF voltage must be equal to 866.7 V, at rated wind speed. This allows the back-EMF constant, to be calculated as summarised by Equation (6.9).

$$k = \frac{E}{\omega_m} \tag{6.9}$$

Step 2 – Calculate the Short-Circuit Current

The generator short-circuit (SC) current is calculated knowing the peak compensated inverter output rated current, which is determined using the experimental I-V locus. The peak compensated current must be less than the minimum inverter input current in order

to remove both the rectifier ripple and fluctuating output power harmonics. The minimum rectifier (inverter input) current, I_R, is calculated as the product of β and the minimum rectifier ripple, as summarised in Equation (6.10).

$$\min\left(I_R\right) = \beta\,\frac{\sqrt{3}}{2} \tag{6.10}$$

This concept is illustrated in Figure 5.48 and is again shown in Figure 6.2 for convenience. The open-loop inverter input current is shown for $\widehat{\alpha}_0 = 0.25$pu, which corresponds to a $\breve{\beta}$ of 0.898pu, and a compensated inverter output current with a peak of 0.778pu. The generator peak short-circuit current, $I_{SC\,pk}$, can hence be calculated, as shown by Equation (6.11), where I_B is the inverter base (rated) current. Therefore, the proposed GCI requires a generator peak SC current of 7.91A to deliver rated power to the grid.

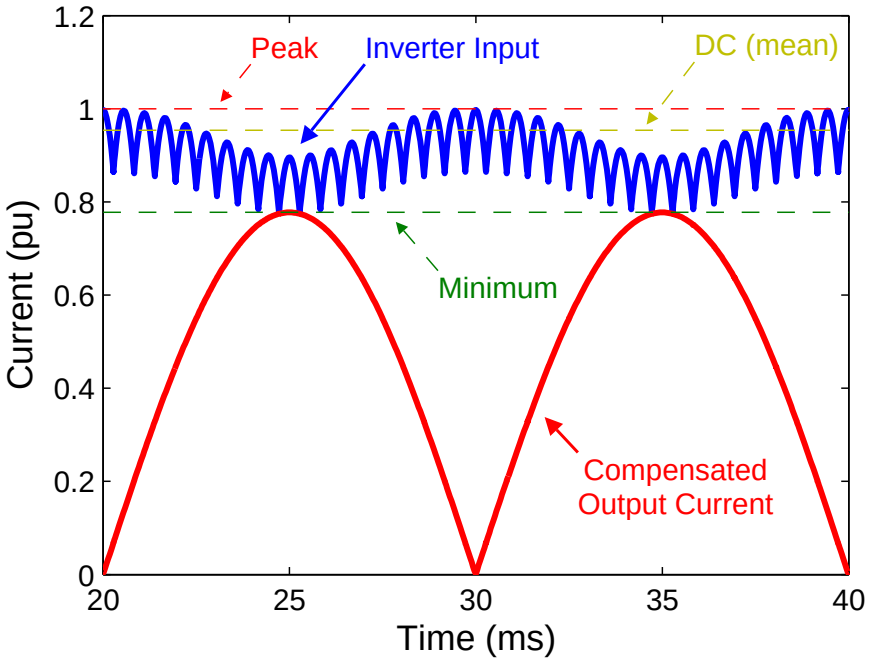


Figure 6.2: Normalised inverter input and peak compensated output current, for $\widehat{\alpha}_0$ 0.25pu. The rectifier ripple frequency is shown for 1.8kHz, as this corresponds to rated turbine speed (750rpm). Note that the terms *peak*, *DC (mean)* and *minimum* refer to the inverter input current waveform.

$$I_{SC\,pk} = \frac{\sqrt{2}\,I_B}{\min\left(I_R\right)} \tag{6.11}$$

Step 3 – Calculate the Stator Resistance

The stator resistance can be determined from the generator copper losses, which is the difference between the assumed generator losses, P_L, and the assumed iron and friction and windage losses under rated operating conditions. This is summarised by Equation (6.12), where P_{IFW} and P_{CU} represent the iron, friction and windage, and copper losses, respectively. Note that P_L is equivalent to the difference in wind turbine and generator output power.

$$P_L = P_{IFW} + P_{CU} \tag{6.12}$$

The assumed total power loss is obtained from Table 6.1, whilst the iron and friction and windage losses are a function of machine speed. These speed dependent losses are assumed identical to those discussed in Chapter 2, as the generator types are assumed similar. The measured iron and friction and windage losses are shown again in Equation (6.13) for convenience, where n_k represents the machine speed in k rpm. Once determined, the copper loss and hence stator resistance, R_s, can be calculated from Equation (6.14), where I_{ph} is the stator phase current. Note that the mean stator phase current is equal to 0.9538 pu, relative to the generator short-circuit current for $\widehat{\alpha}_0 = 0.25$pu.

$$P_{IFW} = 42.88\, {n_k}^2 + 32.54\, n_k \tag{6.13}$$

$$R_s = \frac{P_{CU}}{3\,.\,\text{mean}\,(I_{ph})^2} \tag{6.14}$$

Step 4 – Calculate the Stator Inductance

The stator inductance, L_s, is calculated from the stator reactance, X_s, which itself is determined from the stator impedance, Z_s, and the stator resistance. The later is summarised by Equation (6.15), where Z_s is calculated as the quotient of the phase induced back-EMF voltage and phase short-circuit current, as shown in Equation (6.16).

$$X_s = \sqrt{{Z_s}^2 - {R_s}^2} \tag{6.15}$$

$$|Z_s| = \frac{E}{I_{SC}} \tag{6.16}$$

The stator inductance is calculated from Equation (6.17), where ω_e is the electrical frequency; this is proportional to the machine mechanical speed (in rad/s) and the number of pole-pairs, p, as shown in Equation (6.18).

$$L_s = \frac{X_s}{\omega_e} \tag{6.17}$$

$$\omega_e = n \frac{2\pi}{60} p \tag{6.18}$$

Generator Summary

The above procedure is used to design a PM generator that is suitable for use with the proposed grid-connected inverter. Hence, the machine must provide the inverter with sufficient current, at rated wind speed, such that high quality rated power is delivered to the grid. A summary of the calculated generator properties, at rated wind speed, is shown in Table 6.2.

Table 6.2: Calculated generator parameters for the proposed 1kW grid-connected inverter system. Note that all stator parameters are listed as phase quantities at rated wind speed.

Property	Value
Generator speed, n	750 rpm
Mechanical speed, ω_m	78.54 rad/s
Pole-pairs, p	24
Mechanical frequency, f_m	300 Hz
Rectifier ripple frequency, f_{rect}	1.80 kHz
Electrical frequency, ω_e	1885 rad/s
Back-EMF constant, k	7.127 $V/(rad/s)$
Induced phase voltage, E	559.7 V
Short-circuit current, I_{SC}	5.60 A
Phase resistance, R_s	1.708 Ω
Phase impedance, Z_s	99.94 Ω
Phase reactance, X_s	1.708 Ω
Phase inductance, L_s	53.0 mH

The resulting rectifier I-V locus is shown in Figure 6.3, which shows the rectifier output current vs. rectifier output voltage. The locus shows current and voltage as peak, DC (average), and minimum quantities; recall the inverter input current of Figure 6.2.

The dashed lines represent the peak grid voltage and the minimum peak current for compensation to be achieved. The figure indicates that the feed-forward compensation scheme will effectively remove the input current harmonic distortion, as the minimum peak current, at the grid peak voltage, exceeds that required.

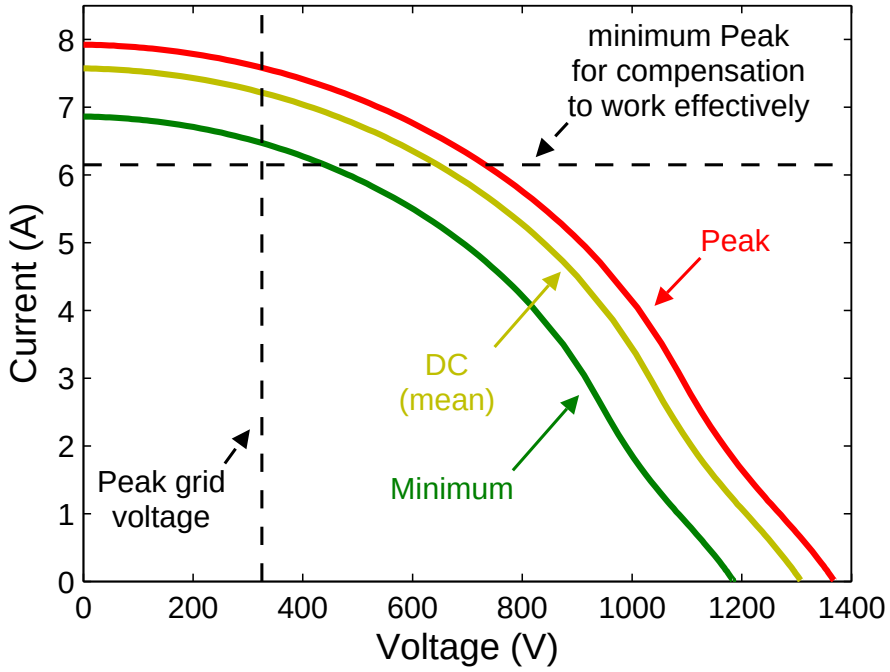


Figure 6.3: Designed generator rectifier output I-V locus, showing the peak, DC (average), and the minimum peak current vs. voltage. The vertical dashed lines represents the peak grid voltage, whilst the horizontal dashed line represents the minimum peak current required to compensate (remove the input current harmonic distortion) the output current. The compensation scheme is shown to be effective at the peak grid voltage.

6.2 Low-Pass Filter Design

6.2.1 Design Criteria

The filter is designed according to the selection criteria discussed in Chapter 5; these are listed below:

- power factor between 0.8 lead and 0.95 lag between 20% and rated operation,
- output current THD less than 5% at rated operation,
- peak damping resistance power loss of 0.05pu or less (relative to rated power),
- inverter switching frequency less than 10kHz, and
- filter cutoff frequency between 10 and 65pu (relative to the fundamental frequency).

6.2.2 Component Selection

The filter components are selected using the normalised low-pass filter analysis of Chapter 5. The procedure is listed below, and yields normalised filter component values. These are used in conjunction with the filter base quantities, to determine actual component values. A list of filter component base quantities is summarised in Table 6.3, for the proposed (1kW) grid-connected inverter.

Output Filter Design Procedure

1. select the inverter switching frequency,
2. select the low-pass filter configuration,
3. select the value of normalised capacitance, C_n, that meets the leading power factor requirement, i.e. $C_n \leq 0.12$pu,
4. use the P_d and THD vs. quality factor and cutoff frequency contour plot to determine a desired power loss and THD, i.e. THD and $P_d \leq 5\%$,
5. determine the inductance to match the desired cutoff frequency, and
6. calculate the damping resistance that allow the desired quality factor to be achieved.

Table 6.3: Low-pass filter base quantities.

Property	Value
Base power, P_B	1000 W
Base grid voltage, V_B	230 V_{RMS}
Base impedance, Z_B	52.9 Ω
Base current, I_B	4.348 A_{RMS}
Fundamental frequency, f_1	50 Hz
Base frequency, ω_B	314.2 rad/s
Base capacitance, C_B	60.17 μF
Base inductance, L_B	168.4 mH

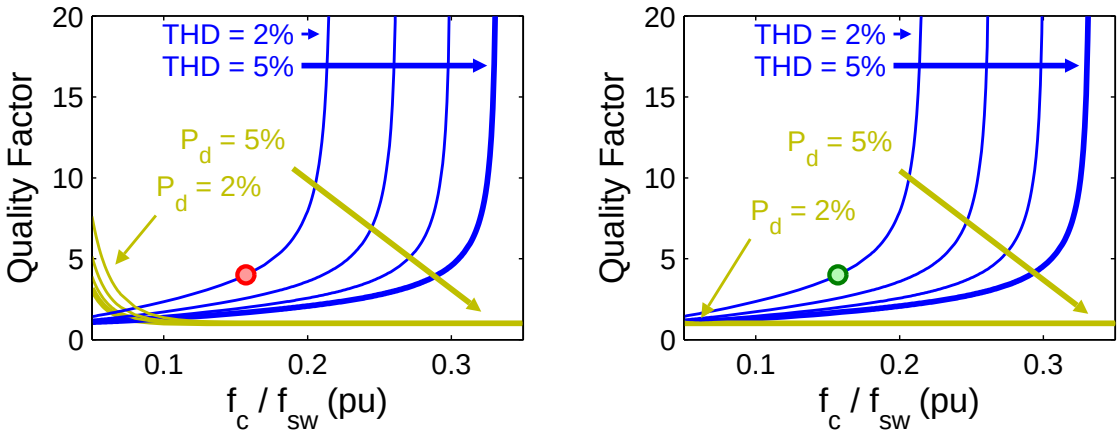
The above design procedure is used to design two CL low-pass filters, to show the effect of varying the switching frequency, f_{sw}, on the filter performance. The first filter is designed for a f_{sw} of 4 kHz, as this corresponds to that of the concept demonstration inverter tested in Chapter 4. The second filter is designed for 10kHz operation, as this corresponds to the maximum allowable f_{sw} (see Section 5.3.4).

Filter configuration 3 was selected for the proposed inverter; the damping resistor of this filter arrangement is connected in parallel to the filter inductor. Though this configuration offers only a first-order attenuation rate beyond the resonant frequency, it can still meet the grid THD requirement and offers the lowest damping resistor power loss, P_d, as seen in Section 5.3.8.

The normalised filter capacitance is the next parameter to be determined. The inverter is designed to meet the leading power factor requirement of 0.8 at 20% rated volt-amperes. This condition is met for an undamped CL filter when the normalised capacitance is equal to 0.12pu. The introduction of a damping resistor will affect the power factor as some real power will be dissipated in R_d, however, the power loss is limited to 0.05pu at rated operation. The small power loss only slightly adjusts the inverter power factor, as mentioned in Section 5.3.6, and is hence ignored.

The required filter cutoff frequency is determined using the quality factor, Q, vs. power loss, P_d, vs. THD tradeoff curves of Section 5.3.8. For convenience these are shown in Figure 6.4 for a normalised filter capacitance of 0.12pu. Figure 6.4(a) shows the tradeoff curve for a switching frequency of 4 kHz, whilst Figure 6.4(b) shows that for f_{sw} equal to 10 kHz. Each trade-off curve show the chosen filter design point (shaded circle) which corresponds to a Q of 4, based on Nave's recommendation, and an output current THD of 2%, which implies a normalised cutoff frequency of 0.155pu. The resulting filter power loss,

under rated conditions, is 0.2% and 0.38% of the rated power, for switching frequencies of 4 and 10kHz, respectively. Note that the THD curves shown assume an ideal current source input and a modulation index, m_a, of 100% is used with the inverter. It is hence expected that either using the PM generator (non-ideal) current source, or reducing the m_a, will increase the output current THD.



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.4: Quality factor, THD, power loss and cutoff frequency tradeoff curves, used to design the 1kW grid-connected inverter, for switching frequencies of (a) 4 kHz, and (b) 10 kHz. The shaded circle represent the chosen filter parameters, i.e. a cutoff frequency of 0.155pu, a quality factor of 4, an output current THD of 2%, a filter power loss of less than 2%.

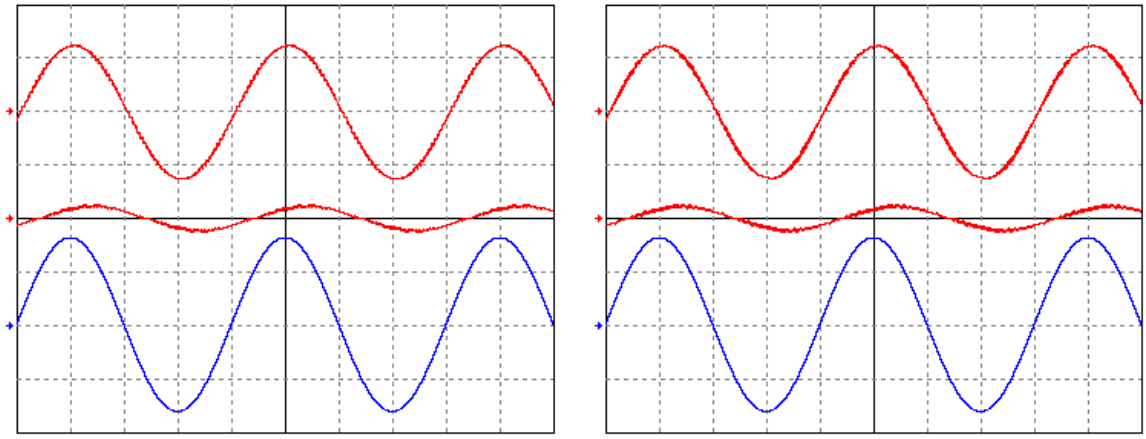
The above trade-off curves allow the normalised filter components to be evaluated, from which, the filter inductance and damping resistance is calculated using the appropriate equations from Chapter 5. A summary of the filter components, for both switching frequencies, is seen in Table 6.4.

Table 6.4: Output filter component values and corresponding filter parameters for the proposed 1kW grid-connected inverter, for both 4 and 10kHz inverter operation.

Component / Parameter	Switching Frequency	
	4 kHz	10 kHz
Capacitance, C	7.22 μF	7.22 μF
Inductance, L	9.1 mH	1.5 mH
Damping Resistance, R_d	137.7 Ω	55.08 Ω
Resonant Frequency, f_{res}	620 Hz	1.55 kHz
Quality Factor, Q	4	4

6.2.3 Filter Simulation - Ideal Current Source

Each low-pass filter is simulated, using PSIM®, in an open-loop manner using an ideal current source. The resulting inverter output current and voltage, at rated and 20% rated operation, is shown in Figure 6.5, for each switching frequency. Note that the power levels are set by adjusted the m_a. A summary of the inverter performance is shown in Table 6.5. The output current THD and damping resistor power loss is equal to that predicted by Figure 6.4, at rated operation. Note that the THD considers only the PWM harmonics due to the ideal current source input.



(a) $f_{sw} = 4\,\text{kHz}$ (b) $f_{sw} = 10\,\text{kHz}$

Figure 6.5: Simulated ideal inverter output current and voltage at rated and 20% rated volt-amperes, for switching frequencies of (a) 4, and (b) 10kHz. The waveforms shown are the rated current, the 20% rated current, and the inverter output voltage, from top to bottom, respectively. The zero position for each waveform is shown by the arrow on the left. The vertical current and voltage scales are 5A and 200V per division, respectively, whilst the horizontal scale is 5ms/div.

Table 6.5: Simulated inverter performance using an ideal current source.

Switching Frequency	Apparent Power (pu)	Power Factor (lead)	Current THD (%)	Power Loss in R_d (W)	Modulation Index (%)
4 kHz	0.201	0.800	6.36	0.323 W	16.0
	1.013	0.993	1.97	1.909 W	100
10 kHz	0.199	0.796	8.65	0.120 W	16.0
	1.006	0.993	2.11	0.383 W	100

The table indicates that the power factor, THD, and the (self imposed) power loss requirements are met at rated current. In contrast, the inverter output current falls

marginally short of the 0.8 leading power factor requirement, for the 10 kHz case. In addition, the output current THD at 20% rated operation is slightly higher than 5%, for each case. This is not an issue as the 5% requirement only applies at rated power. The THD appears to be inversely proportional to the fundamental magnitude, which implies the harmonic components are relatively constant.

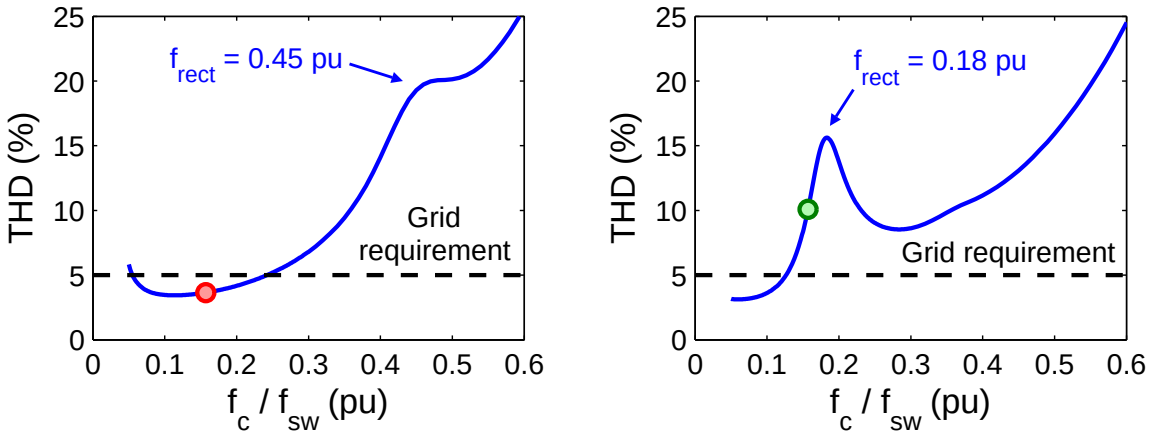
Although the current of Figure 6.5 appears to be lagging the grid voltage (more clearly seen for the 20% rated current), it is leading, according to Standards Australia, who specify the power factor must consider the inverter as a load with respect to the grid. Hence, an inverter that supplies a lagging current is equivalent to one drawing a leading current. This convention is used throughout the remainder of the thesis. In addition, the inverter output voltage is simply the grid voltage, which remains unchanged irrespective of the inverter output current. It is hence not seen in the subsequent simulations.

6.2.4 Filter Simulation - PM Generator Current Source

The output current of each filter has been shown to meet the grid requirements using an ideal current source. Each filter is hence simulated using the PM generator current source in an open-loop manner; the generator properties are listed in Table 6.2. The filter output current hence contains distortion caused by the rectifier ripple and the fluctuating input current. These aspects, together with the effects of resonance, i.e. harmonic amplification, are taken into consideration when calculating the filter output current THD (see Section 5.3.9).

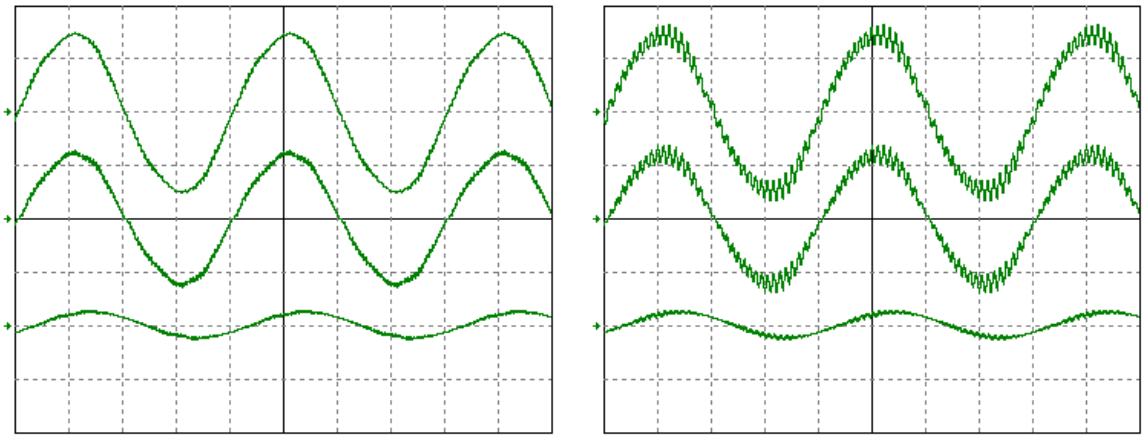
Figure 6.6 shows the calculated output current THD of each filter, as a function of cutoff frequency, for a modulation index of 100%. The shaded circles represent the calculated THD for each filter. The 4kHz case produces an output current THD of 3.65%, whilst that for the 10kHz case is 10.1%. The THD of the latter is significantly higher than the required 5%. This is due to the effects of resonance, i.e. the rectifier ripple harmonics are amplified, as these lie in close proximity to the cutoff (resonant) frequency.

The simulated inverter output currents, for switching frequencies of 4 and 10kHz, are shown in Figure 6.7. Each subfigure shows three currents, these correspond to the maximum, rated and 20% rated cases, from top to bottom respectively. Recall that the generator is designed to provide a compensated rated current of magnitude 1pu, i.e. it is oversized. Hence, operating the inverter in open-loop control mode, with a modulation index of 100% yields an output current greater than 1pu; in this case the peak current is equal to 1.207pu. Note that the effect of resonance is clearly seen for the 10kHz case.



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.6: Output current THD prediction using the PM generator current source, for switching frequencies of (a) 4, and (b) 10 kHz. The points represent the calculated THD for a modulation index of 100%.



(a) f_{sw} = 4 kHz (b) f_{sw} = 10 kHz

Figure 6.7: Various simulated inverter output currents, using the PM generator current source and open-loop control, for switching frequencies of (a) 4kHz, and (b) 10kHz. The currents shown are the maximum, rated and 20% rated currents, from top to bottom, respectively. The zero position for each waveform is shown by the arrow on the left. The vertical scales are 5A/div, and the horizontal scale is 5ms per division.

The oversized generator implies that the inverter modulation index must be reduced to obtain rated current. In this case, rated current is delivered to the grid for a m_a of 81.8%. Similarly, the 20% rated current is obtained when the modulation index is set to 12.9%. This is summarised in Table 6.6, along with power factor and THD information of

each current waveform. The power factor is shown to fall marginally short at 20% rated power, whilst meeting the requirement at rated and maximum powers. The THD is again shown to be high for the 20% rated current case, which decreases with increasing power for the 4 kHz switching case. In contrast, the THD is shown to be relatively constant with power for the 10 kHz case. This is expected as the filter cutoff frequency is close to the rectifier ripple frequency (0.155 vs. 0.18pu, respectively). Hence, the harmonics found in the rectifier ripple are amplified, due to resonance ($Q = 4$), and so the major distortion component of the output current is the rectifier ripple. The rectifier ripple is a constant fraction of the fundamental, due to the action of the current wave-shaper, and hence the THD is expected to be relatively constant.

Note that the rectifier ripple and resonant frequencies were deliberately selected to show the effects of resonance. In addition, the calculated and simulated THD values match closely, i.e. only a small error of 0.6 and 0.2% exist for the 4 kHz and 10 kHz cases, respectively.

Table 6.6: Simulated inverter performance, using the (non-ideal) PM generator current source with open-loop control. Data is provided for switching frequencies of 4 and 10 kHz, and for 20, 100 and 121% rated power conditions.

Switching Frequency	Apparent Power (pu)	Power Factor	Current THD	Power Loss in R_d	Modulation Index (%)
4 kHz	0.201	0.793 lead	6.78 %	0.334 W	12.9 %
	1.001	0.990 lead	4.52 %	2.831 W	81.8 %
	1.207	0.992 lead	4.24 %	2.877 W	100 %
10 kHz	0.200	0.796 lead	9.17 %	0.134 W	12.9 %
	1.000	0.990 lead	10.2 %	1.498 W	81.8 %
	1.207	0.992 lead	10.3 %	1.721 W	100 %

In addition, the above table also shows the filter power loss, due to the damping resistance. The power loss is shown to decrease as the switching frequency increases. This is expected as the filters have a fixed normalised cutoff frequency, and by increasing the f_{sw}, the inductance must decrease. To maintain a constant Q, the damping resistance must also decrease; the power loss is proportional to the damping resistance, and hence must also decrease.

Suitability of Open-Loop Controller

The current waveforms of Figure 6.7 and the THD information of Table 6.6 suggest that operating the proposed grid-connected inverter in open-loop control mode is suitable only for the 4 kHz switching case at rated wind speed. Recall Figure 5.18, which shows that the open-loop THD will decrease with wind speed (due to $\widehat{\alpha}_0$ decreasing with wind speed). Note that this is valid if the rectifier ripple frequency does not approach the low-pass filter resonant frequency. This can not be guaranteed as the rectifier ripple frequency varies with turbine and hence wind speed.

Consider the 10kHz case. The output current THD is significantly higher than the 5% requirement, at rated wind speed. It is foreseen that the inverter THD will initially increase and then decrease with wind speed. This occurs as the rectifier ripple frequency varies with speed, and that the rectifier ripple at rated wind speed is greater than the resonant frequency, i.e. the rectifier ripple harmonics will be further amplified below rated wind speed. The effects of resonance, however, should be less evident at low wind speeds.

Open-loop operation of the proposed grid-connected inverter is hence deemed unsuitable for both switching frequencies, due to the effects of resonance. The inverter must incorporate a feedback or feed-forward controller to eliminate the open-loop inverter input current (and hence output current) harmonic distortion.

6.3 Demonstration of Feed-Forward Control

Two feed-forward control algorithms that effectively removed the open-loop inverter input current harmonics (fluctuating output power and rectifier ripple), were examined in Section 5.4. The first controller (FFC 1) sampled the generator speed, and calculated the distorted input current and hence the required modulation index to remove the harmonics. This was deemed unsuitable as the controller was required to calculated several complex functions in real time. Hence, a second controller (FFC 2) that sampled the inverter input current was investigated. This algorithm also adjusts the modulation index in real-time, however, it is much simpler and faster and hence appropriate for real-time calculations.

6.3.1 Control Implementation

The feed-forward controller was implemented in PSIM® using a current sensor and current reference command, as summarised by Figure 6.8. Note that the current wave-shaper diode (seen in Figure 4.18) has been removed due to the reverse-blocking capability of the thyristors. The time-varying normalised modulation index is simply the reference current divided by the time-varying inverter input current. The current command, I^*, must be expressed as a peak quantity, e.g. to obtain a sinusoidal RMS current of 3A, the current reference must be $4.24\,\mathrm{A}_{pk}$. Note that the m_a will exceed 1pu, if I^* exceeds the peak inverter input current; this is further discussed in Section 6.3.3.

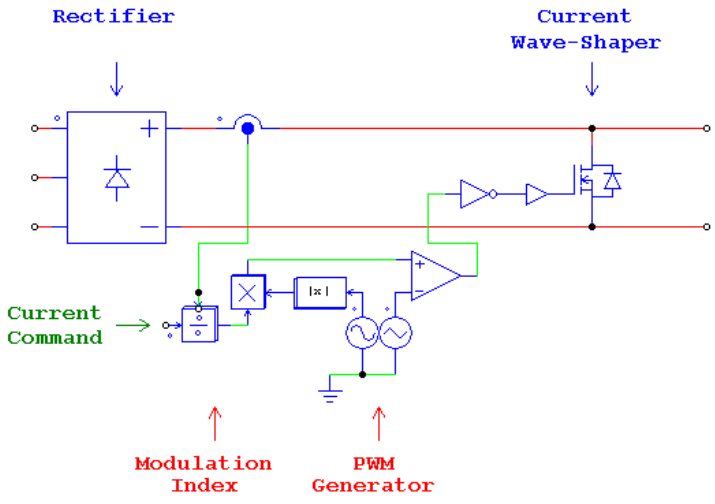
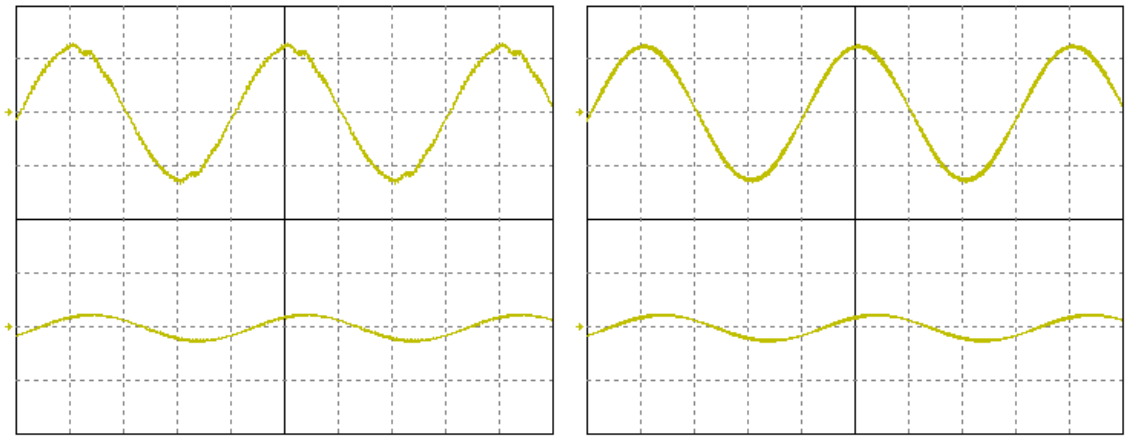


Figure 6.8: Partial PSIM® inverter circuit showing the relevant feed-forward controller implementation. The time-varying normalised modulation index is the quotient of the current command (reference) and sampled rectifier output current.

6.3.2 Proof of Concept at Rated Wind Speed

The feed-forward concept is demonstrated for both the 4 and 10 kHz switching cases, in Figure 6.9, which shows the compensated output currents for both the rated and 20% rated cases. This illustrates that the feed-forward control algorithm effectively removes the inverter input current harmonic distortion, this is more clearly seen for the 10 kHz case, where the rectifier ripple component is no longer visible. A summary of the current waveforms, including the THD, power factor and filter power loss is seen in Table 6.7.



(a) $f_{sw} = 4\,\text{kHz}$ (b) $f_{sw} = 10\,\text{kHz}$

Figure 6.9: Simulated compensated inverter output current for (top) rated, and (bottom) 20% rated current, for switching frequencies of (left) 4kHz and (right) 10kHz. The zero position for each waveform is shown by the arrow on the left. The vertical and horizontal scales are 5A and 5ms per division, respectively.

Table 6.7: Current compensated inverter performance summary, using the (non-ideal) PM generator current source and feed-forward controller.

Switching Frequency	Apparent Power (pu)	Power Factor	Current THD	Power Loss in R_d
4 kHz	0.201	0.798 lead	5.93 %	0.330 W
	1.000	0.993 lead	3.69 %	2.777 W
10 kHz	0.200	0.800 lead	5.93 %	0.118 W
	1.008	0.993 lead	2.81 %	0.697 W

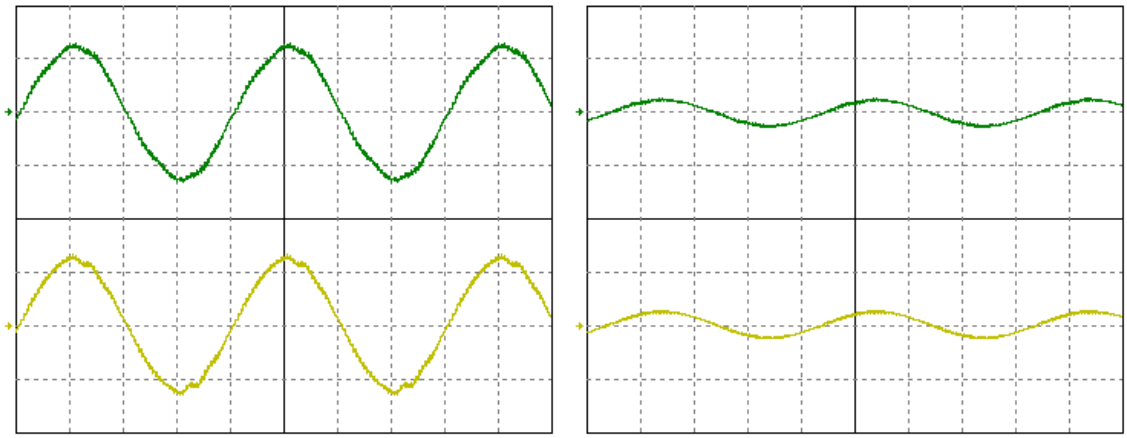
The above table indicates that the use of the feed-forward controller allows both inverters to meet the THD and power factor requirements at rated power, whilst both inverters meet the applicable power factor requirements for the 20% rated case (assume

that 0.798 $\sim$ 0.8). Although both rated current cases produce a THD less than 5%, it is the 10 kHz case that has the lower THD; this is despite it having a cutoff frequency close to the rectifier ripple frequency. This result hence verifies that the feed-forward controller is able to effectively remove the rectifier ripple harmonics.

In addition, the rated compensated output current THD, of both cases, is larger than the designed 2% of Figure 6.4. This occurs as the desired 2% THD is calculated assuming an ideal current source and for a modulation index of 100%, whereas the somewhat oversized generator delivers rated current for an average modulation index of about 80% (see Table 6.6). The resulting compensated current THD is expected to be larger than the desired 2%, as a reduction in m_a increases the PWM harmonic components whilst decreasing the fundamental magnitude (see Section 5.2.4).

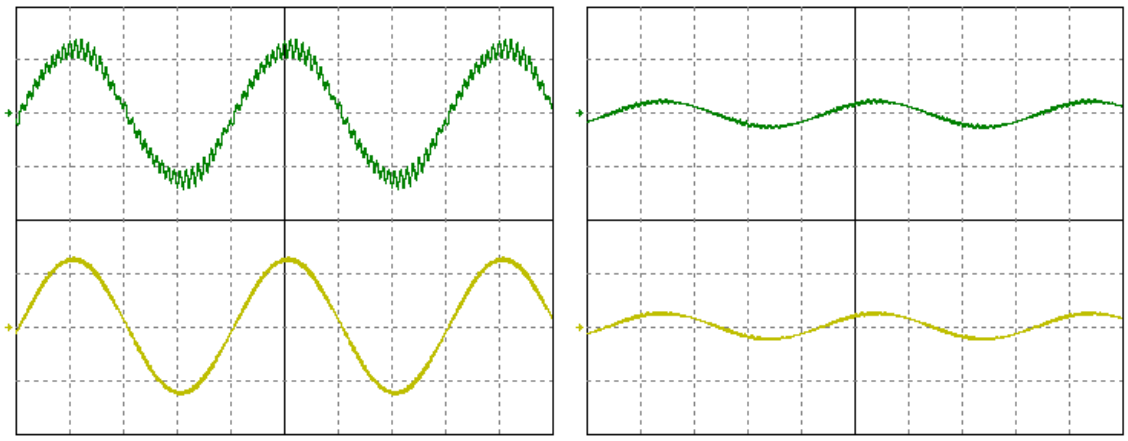
Comparison to Open-Loop Control Mode

The improvement made by the feed-forward controller is best seen when comparing the compensated and open-loop equivalent currents. This is seen for both the 4 and 10 kHz inverter cases, in Figures 6.10 and 6.11, respectively. The most significant improvement is seen for the rated current, using the 10 kHz case, as the effect of resonance (amplified rectifier ripple harmonics) is removed. A summary of the open-loop and feed-forward compensated currents is also shown in Table 6.8; the compensated cases are highlighted.



(a) I_{inv} = 1.00 pu (b) I_{inv} = 0.20 pu

Figure 6.10: Simulated inverter output currents for (a) rated, and (b) 20% rated operation, for a switching frequency of **4 kHz**. The waveforms represent currents using (top) open-loop, and (bottom) feed-forward controllers. The vertical and horizontal scales are 5A and 5ms per division, respectively.



(a) I_{inv} = 1.00 pu (b) I_{inv} = 0.20 pu

Figure 6.11: Simulated inverter output currents for (a) rated, and (b) 20% rated operation, for a switching frequency of **10 kHz**. The waveforms represent currents using (top) open-loop, and (bottom) feed-forward controllers. The vertical and horizontal scales are 5A and 5ms per division, respectively.

Table 6.8: Comparison of open-loop (OL) and feed-forward (FF) compensated inverter performance. Current information is provided for rated and 20% rated power, for switching frequencies of 4 and 10 kHz; the compensated cases are highlighted.

Switching Frequency	Apparent Power (pu)	Control Mode	Power Factor (lead)	Current THD (%)	Power Loss in R_d (W)
4 kHz	0.200	OL	0.793	6.78	0.334
		FF	0.798	5.93	0.330
	1.000	OL	0.990	4.52	2.831
		FF	0.993	3.69	2.777
10 kHz	0.200	OL	0.796	9.17	0.134
		FF	0.800	5.93	0.118
	1.000	OL	0.990	10.2	1.498
		FF	0.993	2.81	0.697

6.3.3 Current Command Variation at Rated Wind Speed

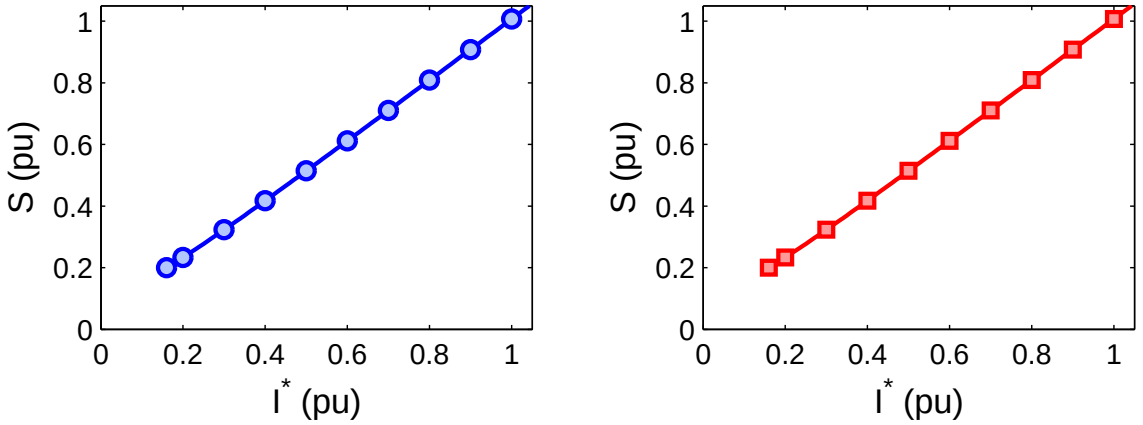
Although the benefit of the feed-forward controller has been clearly demonstrated at rated power, it is also important to investigate the inverter performance over a wide range of powers, as the inverter will operate at sub-rated power levels during periods of low wind speeds. The current command, I^*, is used to adjust the real and hence apparent output

power. Recall that the apparent power is the complex summation of the real and reactive powers, and that the filter capacitor will draw a current of 0.12pu from the grid (for $C_n = 0.12$pu). Hence, a current command of 0.16pu is required for the inverter to operate at 20% (0.2pu) rated apparent power.

The current command is varied in two stages, the first investigates the inverter performance for current and hence output powers less than rated, whilst the second stage attempts to extract more than rated power from the generator.

Linear Modulation Region ($m_a \leq 100\%$)

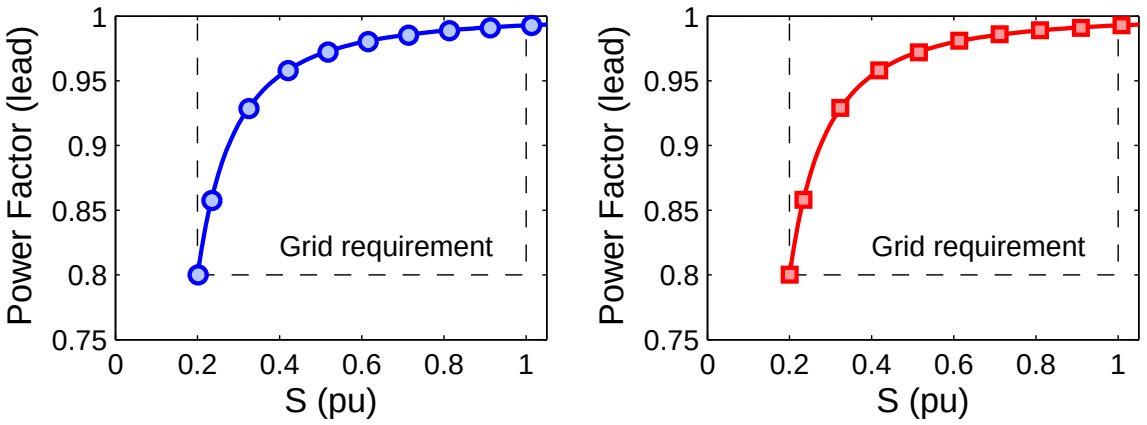
The inverter performance is first examined for apparent power ratings between 0.2 and 1pu, as the inverter is required to meet strict power factor standards over this operating range. As mentioned above, the apparent power is set by adjusting the current command and hence real power. This is highlighted in Figure 6.12, which shows the ideal analytical (using the equations from Section 5.3.6) and (PSIM®) simulated apparent power as a function of normalised current command, for switching frequencies of 4 and 10 kHz.



(a) $f_{sw} = 4$kHz (b) $f_{sw} = 10$kHz

Figure 6.12: Apparent power, S, vs. normalised current command, I^*, for switching frequencies of (a) 4, and (b) 10 kHz. The solid lines represent the ideal analytical power, whilst the points correspond to simulated data.

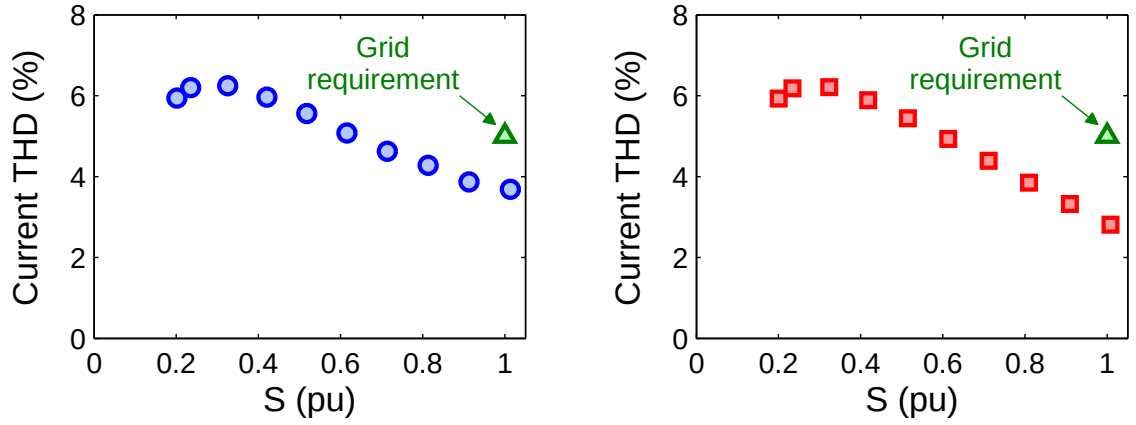
The inverter power factor is displayed in Figure 6.13, as a function of normalised apparent power, for both switching frequencies. The figure shows the ideal analytical and simulated data, as well as the grid requirements; the latter is represented by the dashed lines. The inverter is shown to meet the grid power factor requirements between 20% and rated apparent power, and has a leading power factor over the entire range of S.



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.13: Inverter power factor vs. normalised apparent power, S, for switching frequencies of (a) 4, and (b) 10 kHz. The solid lines and points represent analytical and simulated data, respectively, whilst the dashed lines correspond to the grid requirements.

The current THD is now examined, as the power factor requirements are met. Figure 6.14 shows the simulated inverter output current THD as a function of normalised apparent power. Note that the predicted THD is not shown due to the complexity of the calculation. The grid THD requirement is shown at rated power. power. The inverter is shown to meet the 5% THD requirement for both 4 and 10 kHz switching frequencies; the 10 kHz case has the lowest THD.

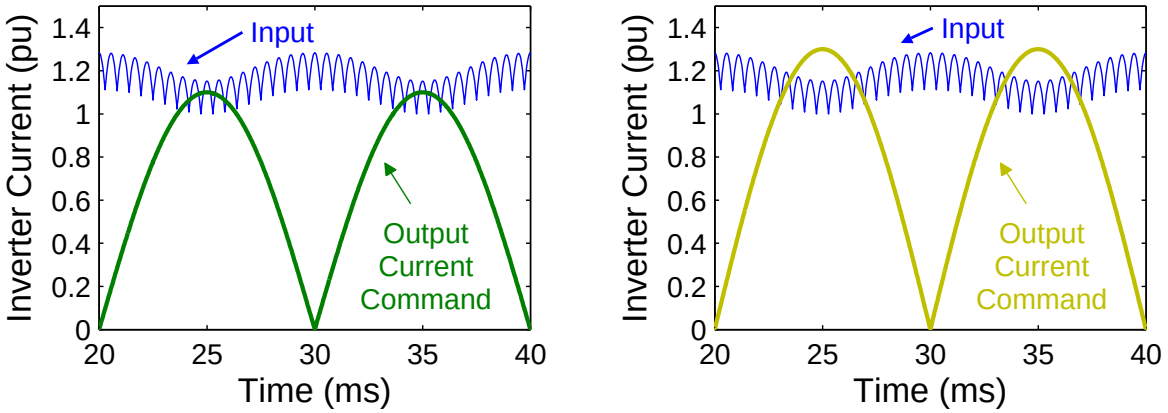


(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.14: Simulated inverter output current THD vs. normalised apparent power, S, for switching frequencies of (a) 4, and (b) 10 kHz. The points represent the simulated data, whilst the triangle correspond to the grid requirement at rated power.

Over-Modulation Region (m_a > 100%)

Increasing the current command beyond 1pu is likely to cause output current distortion, as the peak output current will be greater than the minimum value of the rectifier current ripple. This is illustrated in Figure 6.15, for current commands of 1.1 and 1.3pu for $\widehat{\alpha}_0 = 0.25$pu. Note that that the current scale is normalised, i.e. it is expressed relative to rated inverter current. The figure shows that the maximum compensated current of about 1.15pu should be achievable, however, the input current will contain some of the rectifier ripple harmonics and hence the output current THD will increase. In practise, the output current THD increases, if the I^* is greater than about 1.1pu (for $\widehat{\alpha}_0 = 0.25\,$pu).

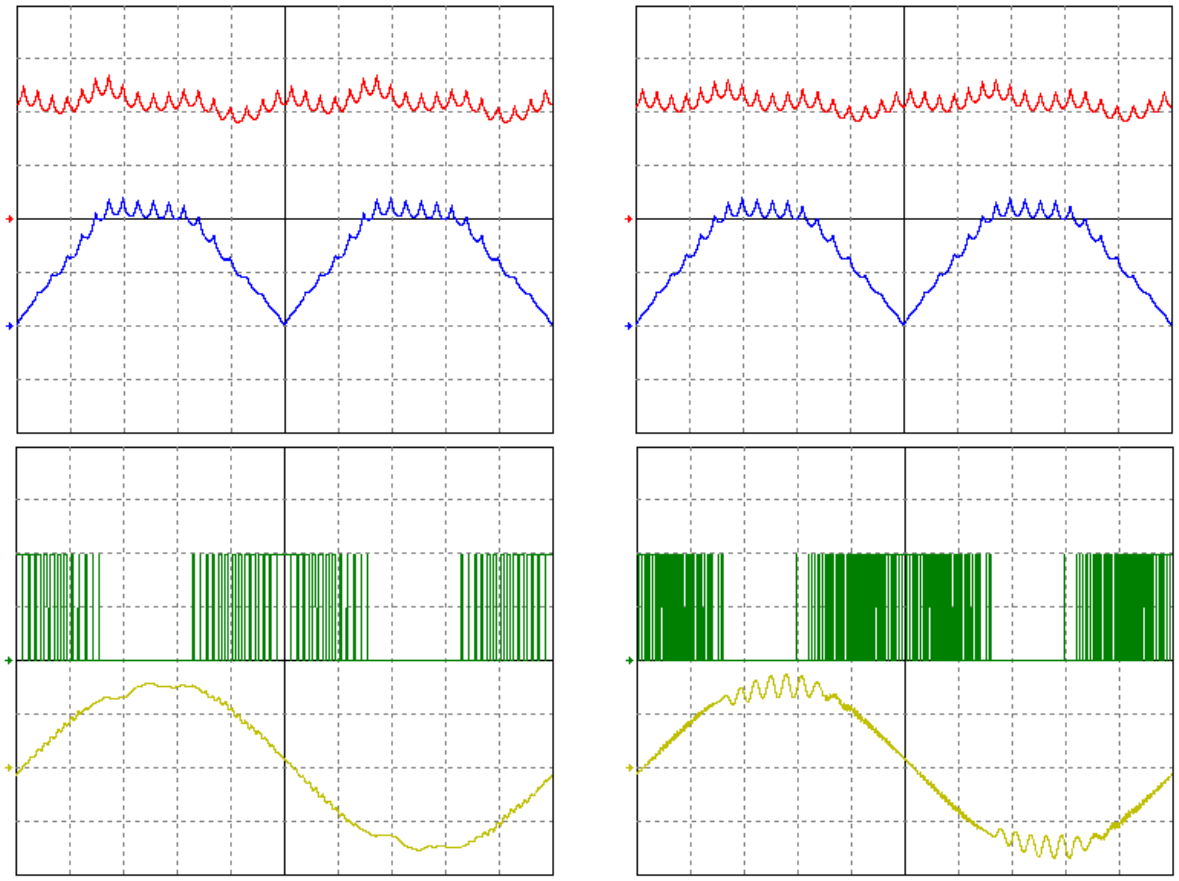


(a) $I^* = 1.1pu$ (b) $I^* = 1.3pu$

Figure 6.15: Normalised inverter input and commanded output currents for current command, I^*, equal to (a) 1.1 and (b) 1.3pu.

Consider Figure 6.15(b). The peak current command is shown to exceed the peak rectifier ripple current. The feed-forward control algorithm will attempt to extract the desired power, under this condition, however, it will fail at the peaks of the sinusoid. This is best understood by revisiting the PWM derivation. Recall that the current wave-shaper PWM duty-cycle command (DCC) is determined by comparing the product of a normalised rectified grid-frequency sinusoid and the time-varying modulation index (sinewave reference), with a normalised switching frequency triangular wave. Hence, a modulation index greater than 1pu, implies that the duty-cycle command (actually $1-d$) will also exceed 1pu. This occurs around the peaks of the compensated current, and implies that the current wave-shaper (CWS) switch will remain continuously open until the duty-cycle command falls below 1pu. The inverter behaves similar to open-loop mode in this situation, i.e. the effects of resonance are seen in the output current.

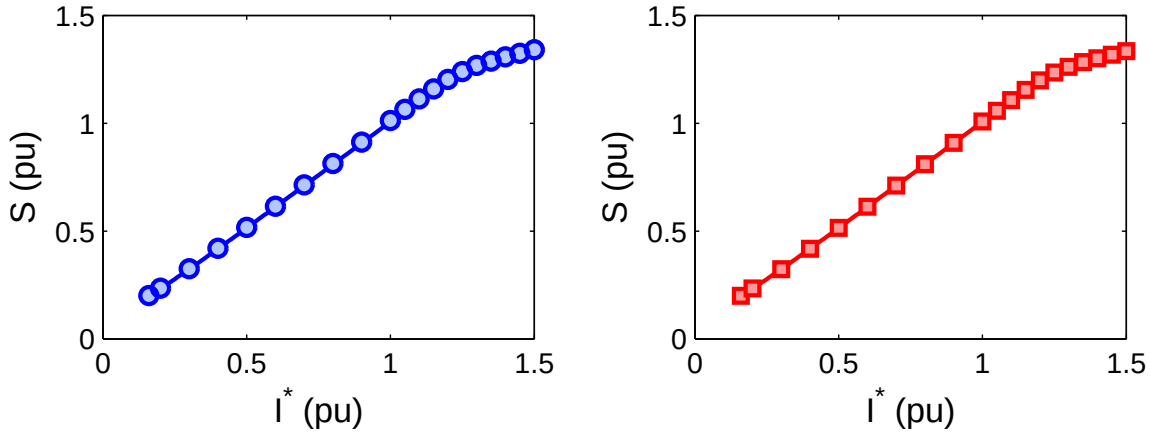
An example of the compensation failure, caused by over-modulation, is seen in Figure 6.16, for a I^* of 1.3pu. The figure shows the time-varying m_a, and the resulting: DCC, CWS gate signal and the filtered output current, for f_{sw} of 4 and 10 kHz. The figure illustrates that the CWS switch remains continuously open if the DCC exceeds 1pu, during which time the input current harmonics pass directly to the output where they can be amplified by the output filter resonance. This is clearly seen in the output currents, particularly for the 10 kHz case. In addition, the output current also shows a some oscillations once the DDC falls below 1pu; this is caused by the filter step response.



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.16: Inverter control signals and filter output current for a current command of 1.3pu, for switching frequencies of (a) 4kHz, and (b) 10kHz. The waveforms shown are the time-varying modulation index, duty-cycle command, current wave-shaper gate signal, and filter output current, from top to bottom, respectively. The output current shows the effect of resonance when the duty-cycle command exceeds 1 pu. The vertical scales are 0.5pu per division for the top three waveforms, and 5A per division for the output current (bottom waveform); the horizontal scale is 2ms per division.

The feed-forward current compensation control algorithm has been shown to fail for current commands that exceed approximately 1.1pu. It is hence expected that as the I^* increases beyond this value, the compensated current (and hence apparent power) will begin to saturate. This is seen in Figure 6.17, which shows the apparent power as a function of current command up to 1.5pu.

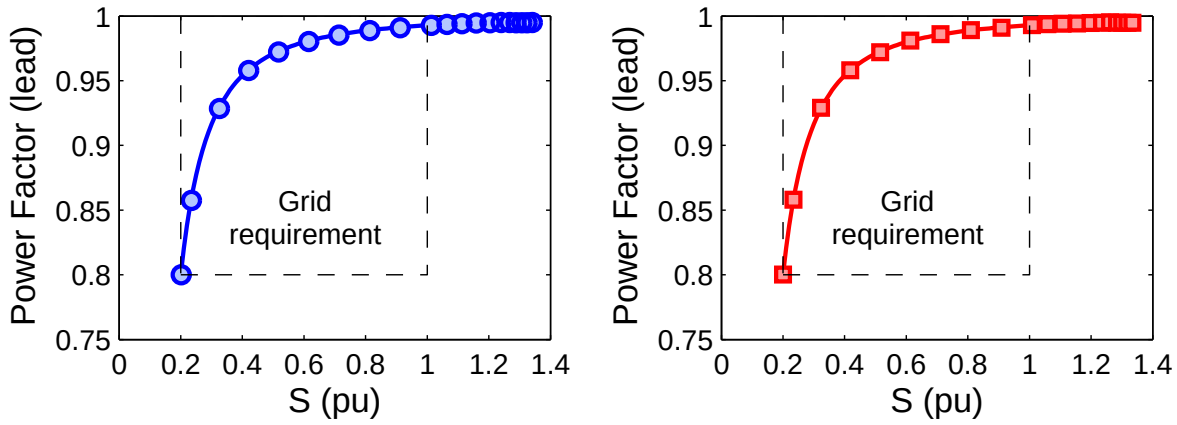


(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.17: Apparent power, S, vs. normalised current command, I^*, over a wide range of values, for switching frequencies of (a) 4, and (b) 10 kHz. The solid lines represent analytical data, whilst the points correspond to simulated data. The apparent power begins to saturate beyond current current commands of approximately 1.1pu.

The resulting (displacement) power factor is expected to approach unity for increasing S, as the unity power factor inverter output current dominates the 0.12pu leading current drawn by the capacitor. This is seen in Figure 6.18, which shows the analytical and simulated power factor as a function of normalised apparent power. This is shown for both switching frequencies, and for current commands up to 1.5pu. The power factor is shown to remain within the grid specifications, i.e. between 0.8 lead and 0.95 lag for inverter power ratings between 20% rated and rated, despite the output current distortion. Note that the displacement power factor considers only the phase angle of the fundamental, whilst the true RMS power factor also considers the output current THD, hence, output current distortion will slightly reduce the true RMS power factor.

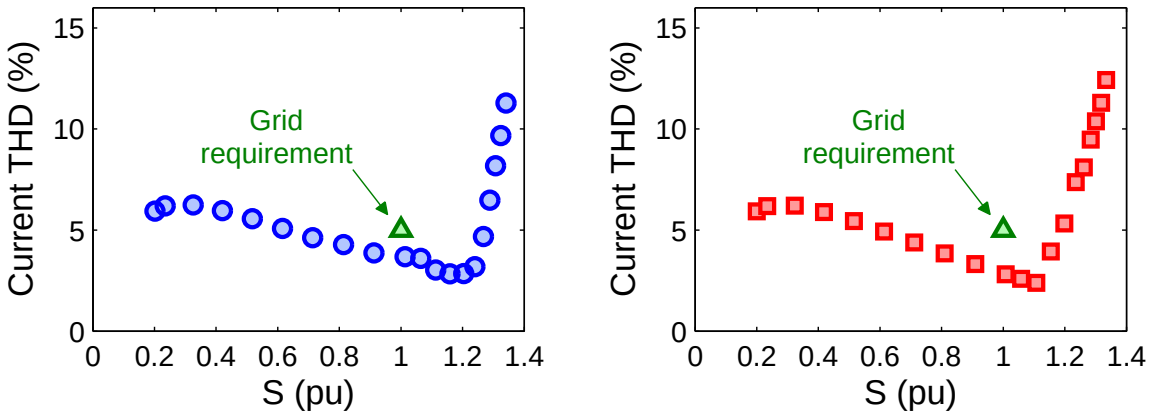
In contrast, the output current THD is expected to sharply increase with increasing apparent power; beyond about 1.1pu. The rise in THD is caused by two factors, firstly the clipping of the peaks of the output current, due to the limited input current, causes third-order harmonic distortion. Secondly, the saturation of the feed-forward control algorithm allows the rectifier current ripple to appear on the output which can be amplified by the



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.18: Inverter power factor vs. normalised apparent power, S, over a wide range S, for switching frequencies of (a) 4, and (b) 10 kHz. The solid lines represent calculated data, whilst the points correspond to simulated data. The power factor is shown to approach unity as the apparent power increases.

output filter. This was previously seen in Figure 6.16. The output current THD is plotted in Figure 6.19, as a function of S, for both inverter switching frequencies. The THD of the 10 kHz case is shown to increase at a faster rate than that for the 4 kHz case, as the rectifier ripple frequency and output filter resonant frequency are close to each other.



(a) f_{sw} = 4kHz (b) f_{sw} = 10kHz

Figure 6.19: Simulated inverter output current THD vs. apparent power, S, for switching frequencies of (a) 4, and (b) 10 kHz, over a wide range of S. The THD sharply increases for $S \geq 1.1$pu, and at a faster rate for the 10 kHz switching case.

The above results suggest that in order to comply with the grid THD requirement, the rated current command should be defined as less than 1.1pu.

6.4 Inverter Simulation for Wide Wind Speed Range

The inverter has been shown to meet the grid power factor requirements at 20% rated and rated apparent powers, and the THD requirement at rated power. However, this is valid only for rated wind speed, and hence the inverter is examined over a wide range of wind speeds, to determine its suitability for grid-connected applications.

6.4.1 Turbine Characteristics

The wind turbine, whose properties are listed in Table 6.1, is simulated over a wide range of wind speeds, as seen in Figure 6.20. The figure shows inverter, generator and turbine output and wind power, as a function of wind speed, v, and assumes a constant inverter efficiency of 95%, a constant generator efficiency of 85%, and a peak c_p of 0.30. The desired inverter power increases with the cube of v until rated wind speed, after which, the power is maintained at rated power. Note that an S of 0.2pu occurs at $v = 6.5$m/s, where the real power is 0.16pu; recall the capacitor draws 0.12pu reactive power for all v.

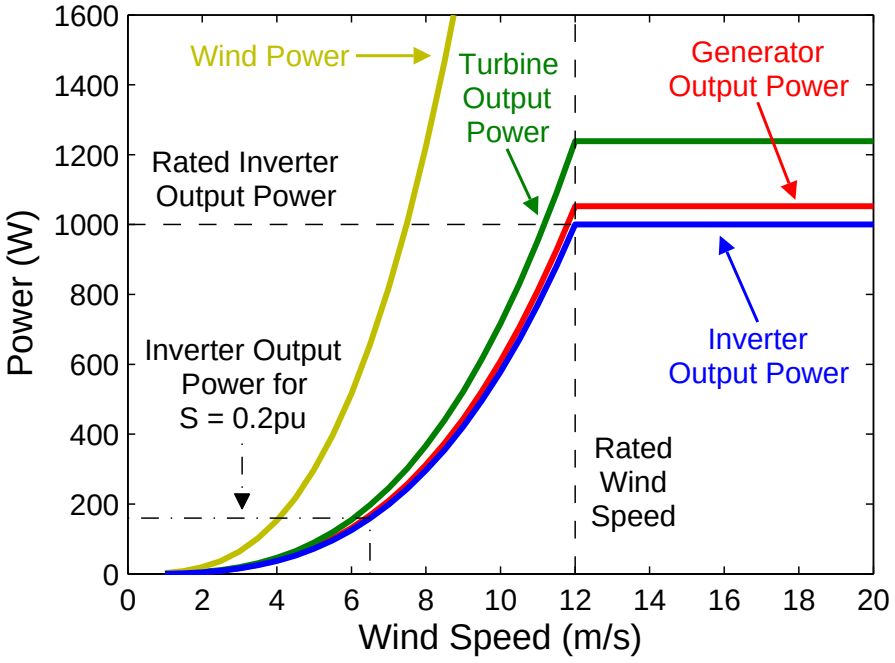
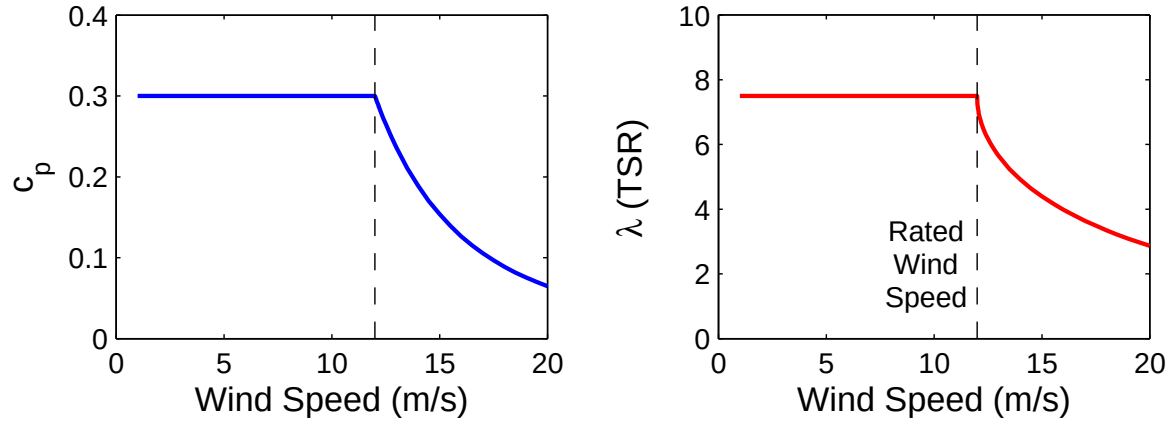


Figure 6.20: Calculated inverter, generator and turbine output power, and total wind power vs. wind speed characteristic, based on assumed efficiencies. The dashed lines represent rated inverter power and wind speed, whilst the dashed-dotted lines correspond to 20% rated power ($v = 6.5$m/s, $P = 160$W).

The inverter, and hence turbine, operate such that the output power is maximised below rated wind speed and maintained at its rated value above rated wind speed. The turbine coefficient of performance, c_p, and tip-speed ratio, λ, should be kept constant at their optimal values below rated wind speed, and must decrease as v increases beyond rated. This implies the generator speed increases linearly with v up to rated, and must also decrease beyond rated wind speed. This action results in an a high $\widehat{\alpha}_0$ for low wind speeds, as the peak grid voltage is fixed. The value of $\widehat{\alpha}_0$ decreases to the desired 0.25pu at rated wind speed, and increases with v beyond rated. This information is summarised in Figure 6.21; the dashed lines represent rated wind speed.



(a) Coefficient of performance

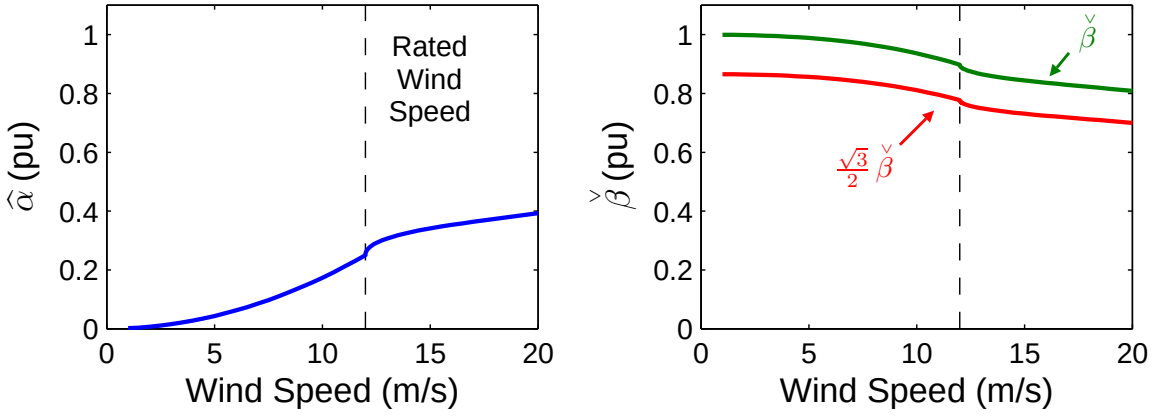
(b) Tip-speed ratio

(c) Turbine speed

(d) $\widehat{\alpha}_0$

Figure 6.21: Turbine and generator operating characteristics vs. wind speed characteristic. The curves shown include the turbine (a) coefficient of performance, c_p, and (b) tip-speed ratio, λ, and the generator (c) speed, and (d) value of $\widehat{\alpha}_0$. The dashed lines represent rated wind speed.

Figure 6.22 shows the resulting $\widehat{\alpha}$ and the normalised minimum inverter input current, $\breve{\beta}$, as a function of wind speed. Recall that the modulation index increases with the cube of wind speed (see Figure 5.17(a)). As such, $\widehat{\alpha}$ increases with the square of wind speed, until rated; it then increases beyond rated, as the turbine and hence generator speed decreases (see Figure 6.21(c)). Note that Figure 6.22(b) also shows $\sqrt{3}/2\,\breve{\beta}$, as this corresponds to the peak compensated inverter output current that contains zero low and medium-frequency harmonics. The compensated output current has a peak of 0.778pu at rated wind speed (as seen in Figure 6.2), which corresponds to rated inverter current.



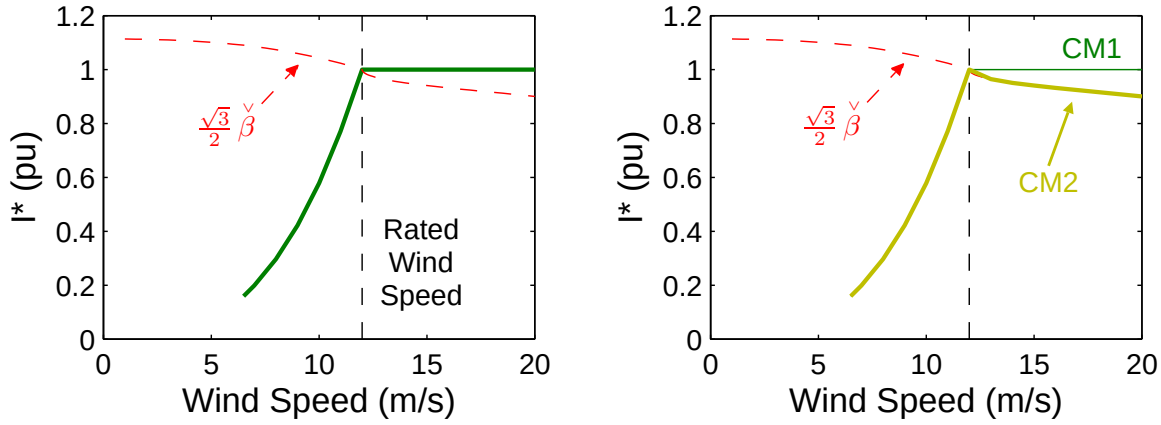
(a) $\widehat{\alpha}$ (b) $\breve{\beta}$

Figure 6.22: Generator (a) $\widehat{\alpha}$, and (b) $\breve{\beta}$ vs. wind speed. Note that $\sqrt{3}/2\,\breve{\beta}$ is also shown in (b) as this corresponds to the peak compensated output current; $\breve{\beta}$ is equal to 0.778pu at rated wind speed, which corresponds to rated inverter output current. The dashed line represents rated wind speed.

6.4.2 Power Control Modes

Although Figure 6.22(b) shows that the inverter can obtain rated current (and hence power) at rated wind speed, the figure suggests that the magnitude of the compensated output current must decrease above rated wind speed, in order to obtain distortion free output current. The modulation index and hence inverter output power, however, are ideally maintained at 1pu above rated wind speed to obtain rated inverter output power. It is hence foreseen that the compensated output current will contain some harmonic distortion above rated wind speed, unless the current command, I^*, is reduced above rated wind speed. This concept is illustrated in Figure 6.23, which shows the current commands for two control modes. Both control modes increase power, with the cube of

wind speed, below rated wind speed, however, differ above rated wind speed. The first control mode (CM) attempts to maintain rated power, whilst the second mode reduces power above rated wind speed, by matching it to $\check{\beta}$, shown as the dashed line, such that the compensated current contains zero distortion. Note the I^* is only shown beyond a wind speed of 6.5m/s as this corresponds to the 20% rated apparent power wind speed.



(a) Control Mode 1

(b) Control Mode 2

Figure 6.23: Current command, I^*, vs. wind speed for control modes (a) 1, and (b) 2. The control modes differ beyond rated wind speed, where control mode 1 maintains rated output power, whilst mode 2 reduces the output power. The dashed and vertical dashed lines represent the maximum current command, and rated wind speed, respectively.

The inverter is simulated using both control modes in Section 6.4.4, where the effects of each control mode on the output current THD and magnitude, are examined above rated wind speed.

6.4.3 Optimised Component Selection

The components for the high power grid-connected inverter are carefully selected to optimise the overall inverter efficiency. Hence, components with low forward voltage drops and *on resistance* are selected to reduce conduction losses, whilst components with short *on* and *off* times are selected to reduce switching losses. A summary of the key inverter components is shown in Table 6.9. Note that the thyristors selected are designed for phase control applications and as such have a turn-off time, t_q, of 100μs, which effectively limits the inverter switching frequency to 10 kHz. Commutation at the zero-crossings is ensured, for the 10 kHz case, as discussed in Section 4.3.3.

Table 6.9: Optimised inverter semiconductor properties.

Component / Property	Bridge Rectifier	MOSFET	Thyristors
Manufacturer	SEMIKRON	ST	IR
Part Number	DBI 25-14	STP25NM60N	12TTS08PbF
Rating	25A, 1400V	12.8A, 600V	12.5A, 800V
Voltage Drop	1V (per diode)	-	1.2V
On Resistance	-	0.17Ω	-
Latching Current	-	-	50mA
Holding Current	-	-	30mA

Note: IR and ST denote *International Rectifier*, and *STMicroelectronics NV*, respectively.

An equivalent IGBT (STP25NM60N) was also considered for the current wave-shaper switch, however, the *turn on* and *turn off* times were significantly longer than those of the MOSFET and it hence had a higher switching loss. Though the IGBT has slightly lower conduction losses compared with the MOSFET, the IGBT produces the higher overall power (switching + conduction) loss. This, along with each device turn on and off times, is summarised in Table 6.10, for a switching frequency of 10kHz.

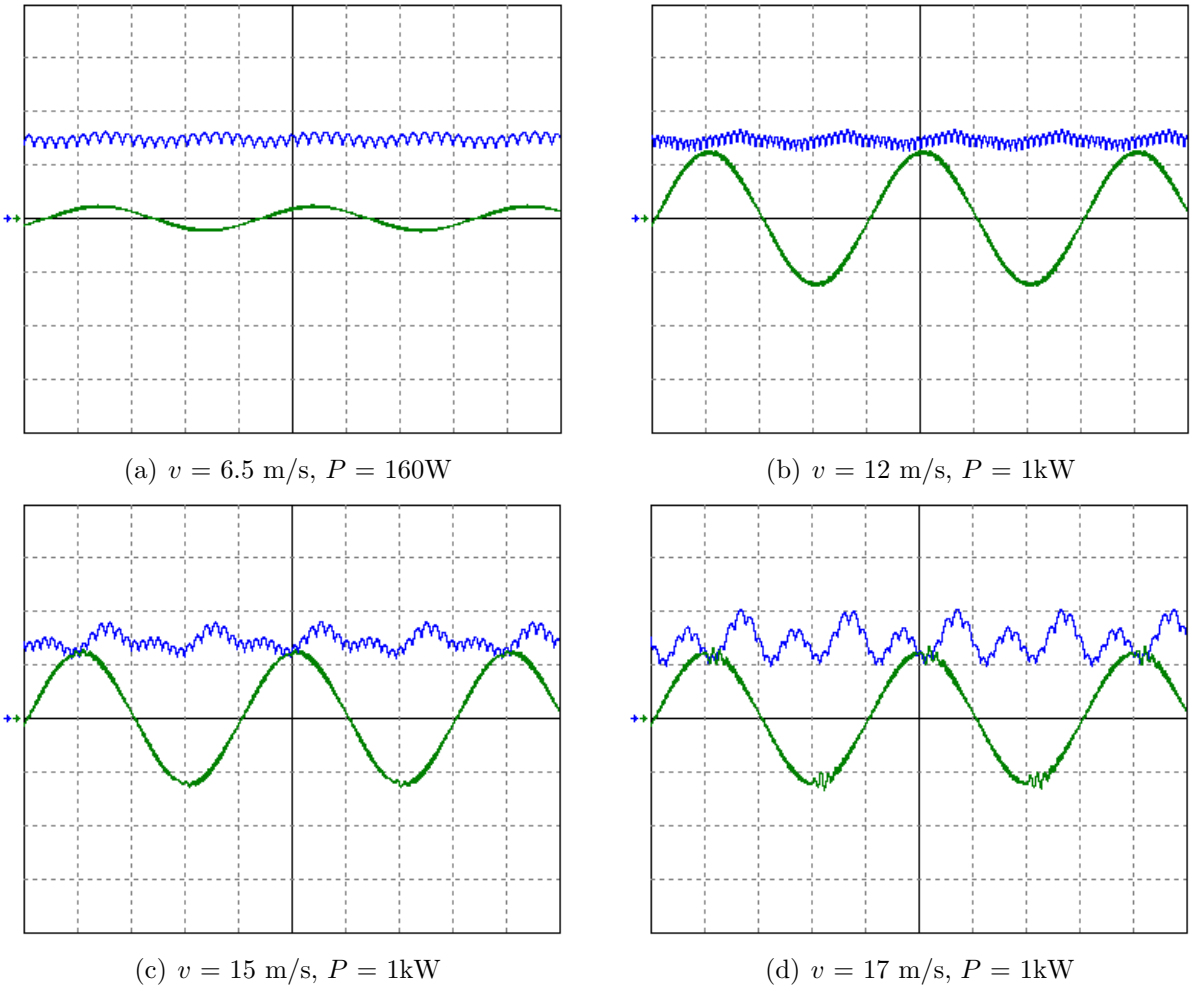
Table 6.10: MOSFET vs. IGBT turn on and off times, and maximum calculated losses, for a switching frequency of 10kHz.

Property	MOSFET	IGBT
On Time	18ns	70ns
Off Time	24ns	790ns
Switching Loss	0.21W	4.3W
Conduction Loss	8.6W	7.4W
Total Loss	**8.8W**	**11.7W**

6.4.4 Inverter Simulations

The inverter using feed-forward compensation is now simulated using both control modes, at four wind speeds of interest: 6.5, 12, 15 and 17m/s. The former corresponds to 20% rated power, whilst the remaining wind speeds correspond to rated power (at and beyond rated v). The inverter input and output currents are shown for these cases in Figure 6.24, using power control mode 1 (CM 1). The output current is shown to have low distortion for 20% and rated powers, however, the cases beyond rated wind speed show increasing current distortion as at times the command current exceeds the input current (as

expected); this is more clearly seen at the wind speed of 17m/s.



(a) $v = 6.5$ m/s, $P = 160$W

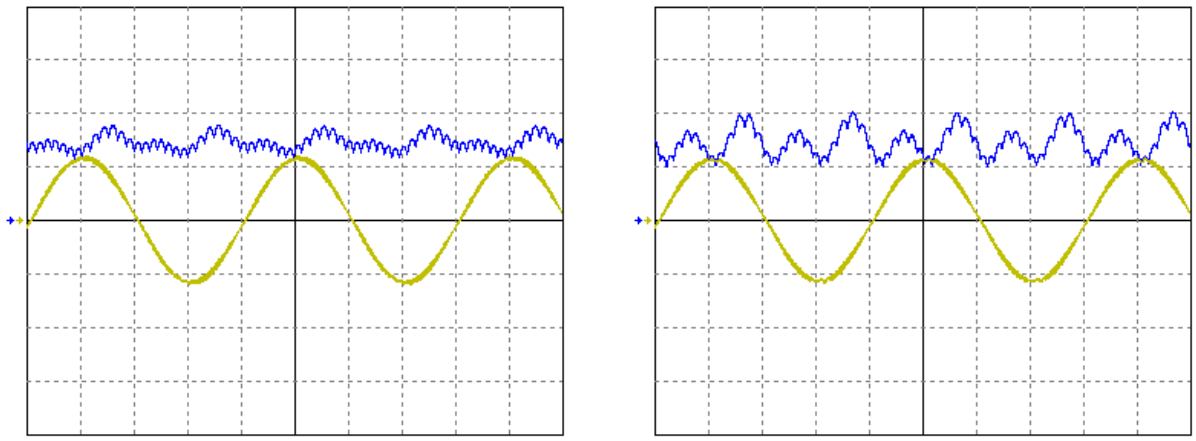
(b) $v = 12$ m/s, $P = 1$kW

(c) $v = 15$ m/s, $P = 1$kW

(d) $v = 17$ m/s, $P = 1$kW

Figure 6.24: Simulated inverter input and filtered output currents, using power control mode 1, for wind speeds of (a) 6.5, (b) 12, (c) 15, and (d) 17m/s. The zero position for each waveform is shown by the arrow on the left. The vertical and horizontal scales are 5A and 5ms per division, respectively.

The inverter is next simulated using power control mode 2 (CM 2), which for wind speeds that exceed rated, reduces the inverter output power to the maximum value while maintaining a low output current THD. The simulated inverter input and output currents are shown in Figure 6.25, for wind speeds of 15 and 17m/s only; this is due to identical current commands, and hence output currents, below rated wind speed.

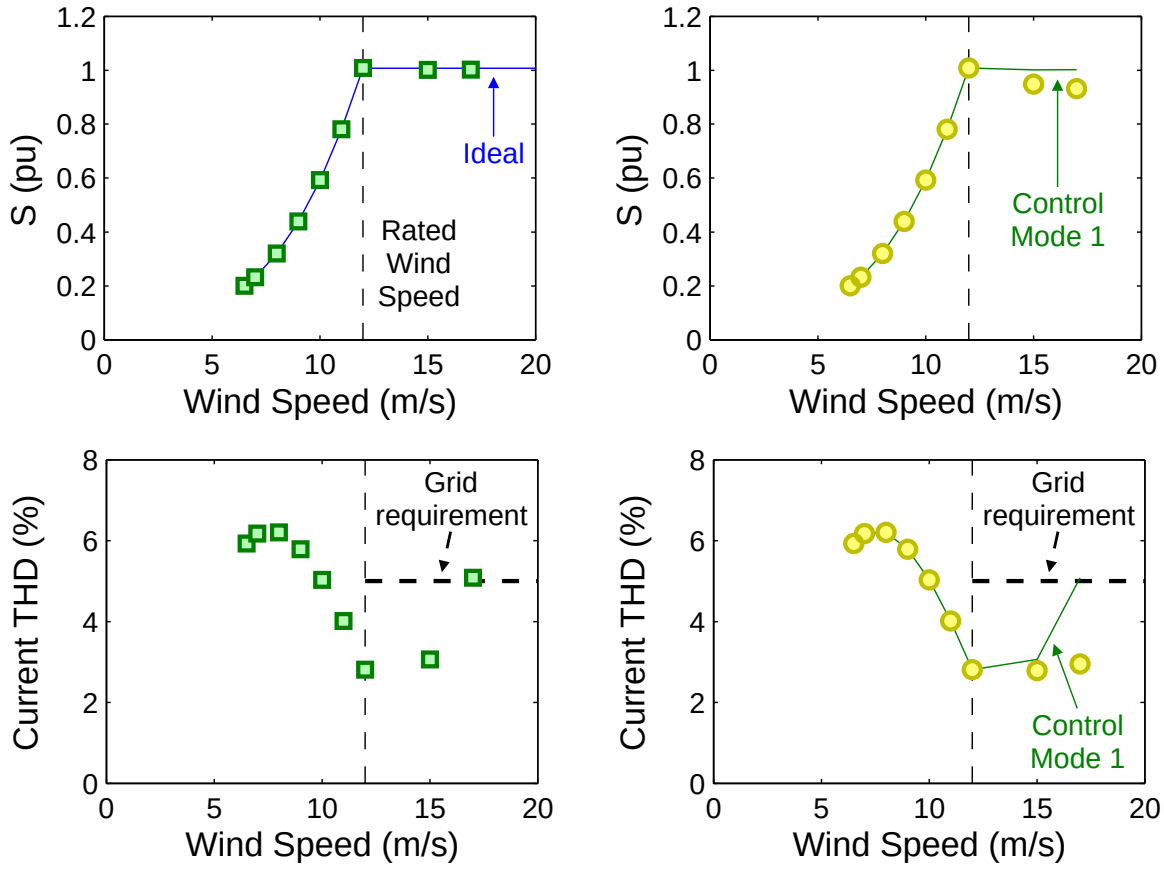


(a) $v = 15$ m/s, $P = 941$W (b) $v = 17$ m/s, $P = 924$W

Figure 6.25: Simulated inverter input and filtered output currents, using power control mode 2, for wind speeds of (a) 15, and (b) 17m/s. The zero position for each waveform is shown by the arrow on the left. The vertical and horizontal scales are 5A and 5ms per division, respectively.

The compensated output currents, of the above figure, show a greatly reduced amount of output current distortion compared to those obtained using CM 1. This is due to the reduced current command, which is equal to the minimum inverter input (rectifier output) current; this action slightly reduces the turbine power and hence speed. Therefore, the output current THD is reduced at the expense of the output current (and hence output power), i.e. a power vs. current THD trade-off exists beyond rated wind speed. This is summarised in Figure 6.26, which shows the apparent power and output current THD as a function of wind speed, for both control modes. Note that the apparent power curve of Figure 6.26(a) also shows the ideal power vs. wind speed relationship, i.e. maximum power below and rated power above rated wind speed. In contrast, Figure 6.26(b) compares the inverter output apparent power and current THD of CM 1, for comparison.

The output current THD of CM 1 and 2 is identical to that previously seen in Figure 6.14, which also varies the current command between 0.16 to 1pu. Beyond rated wind speed, the current THD rapidly increases for CM 1 in a similar fashion to that previously shown in Figure 6.19, where the current command increased beyond 1pu. This is similar to control mode 1, however, the current command remains at 1pu, whilst the minimum rectifier current falls below 1pu. Despite the difference in current commands, the effects of increasing the I^* or reducing the turbine and hence generator speed, are identical. In contrast, the output current THD, using CM 2 only marginally increases beyond rated wind speed, and is hence selected for use with the proposed grid-connected inverter.



(a) Control Mode 1

(b) Control Mode 2

Figure 6.26: Inverter (top) apparent power, S, and (bottom) output current THD, vs. wind speed, for control modes (a) 1, and (b) 2. The vertical and horizontal dashed lines represent rated wind speed, and the grid THD requirement at rated power; the latter is hence only shown at and beyond rated wind speed. Subfigure (a) also compares the ideal inverter power, with that obtained using control mode 1 (points). Similarly, subfigure (b) compares the inverter power and output current THD obtained using control modes 1 for reference; this is shown as a solid line.

6.4.5 Efficiency Analysis

The inverter is shown to meet the grid requirements, over a wide range of wind speeds, using control mode 2. The inverter efficiency, using this control mode, is hence examined. The inverter power-loss breakdown is shown in Figure 6.27, which shows the simulated power loss of various stages of the grid-connected inverter, including the three-phase uncontrolled rectifier, the current wave-shaper (CWS), the unfolding circuit and the output low-pass filter.

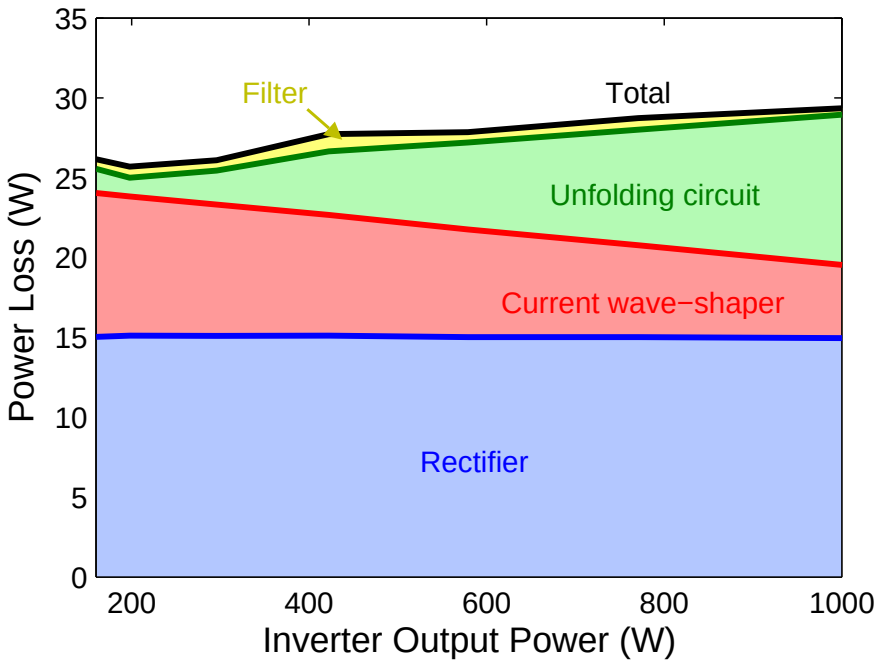


Figure 6.27: Break-down of inverter power loss vs. inverter output power, showing the rectifier, current wave-shaper,unfolding circuit, filter and hence total power loss.

The rectifier power loss of the above figure is shown to be relatively constant. This occurs as the PM generator operates in the constant current region of the I-V locus, over the wide range of inverter output power, which essentially maintains a constant inverter input current. The resulting rectifier power loss is proportional to the current and fixed diode voltage drops. The CWS power loss, which is proportional to the square of the RMS MOSFET current, is shown to decrease with increasing inverter output power. This occurs as the average MOSFET duty-cycle decreases as the current command (and hence inverter output current and power) increase. In contrast, the power loss of the unfolding circuit and low-pass filter increases with inverter output power. This occurs as the unfolding circuit and filter power loss is proportional to the inverter output current and hence power. Note that the filter power loss appears constant, as it is small in magnitude compared to the inverter output power, however, it slightly increases with inverter output power.

The constant and decreasing power loss of the rectifier and CWS imply that their respective efficiencies will increase with inverter output power. In contrast, the increasing output filter and unfolding circuit power losses imply that their respective efficiencies are approximately constant. This is seen in Figure 6.28, which shows the simulated efficiency

of the rectifier, CWS, unfolding circuit and the low-pass filter. In addition, the figure also shows the overall inverter efficiency, which is simply the product of the efficiency of each stage of the inverter. As such, the inverter efficiency increases with inverter output power.

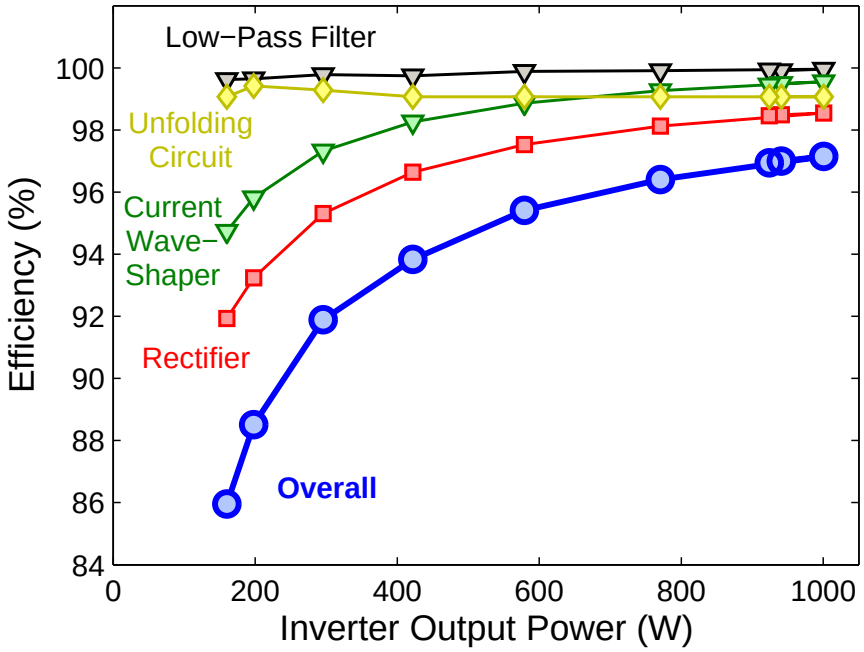


Figure 6.28: Inverter efficiency analysis, showing the rectifier, current wave-shaper, unfolding circuit, filter and overall inverter efficiency vs. output power.

The overall efficiency increases from about 86%, at 20% rated apparent power (real output power of 160W), to about 97.1% at rated power. This peak efficiency of 97.1% is slightly higher than other transformerless grid-connected inverter topologies (recall Table 1.5), and is mainly due to its lack of a DC link inductor and output transformer, which avoid copper and iron losses associated with each.

6.5 Chapter Summary

A 1kW grid-connected inverter based on the proposed topology was designed and simulated. The low-pass filter was designed based on the detailed analysis procedure described in Chapter 5. It was designed to ideally deliver a current with 2% THD to the grid, whilst meeting the light-load leading power factor requirements. Simulations were used to show that the inverter could meet the grid THD and power factor requirements with an ideal current source. However, it was unable to meet the grid THD requirement using the proposed generator. This was due to the use of open-loop sinusoidal modulation, which caused low-frequency and rectifier ripple input current harmonics to appear in the output current.

The introduction of feed-forward input current compensation, based on sampling the inverter input current, eliminated the effect of the low-frequency and rectifier ripple harmonics. The inverter demonstrated its ability to reduce output power, at rated wind speed, by reducing the reference current, whilst meeting the required power factor and THD standards. The inverter also showed it could increase its power, beyond its rated value, by increasing the current reference, i.e. by over-modulating the inverter. This, however, increased the output current distortion, as the current wave-shaper switch remained open for a certain time, which allowed the effects of resonance to manifest itself around the peaks of the compensated current.

The turbine was simulated over a wide range of wind speeds from 6.5–12m/s, corresponding to 20% to 100% of rated output power. The inverter showed it can maximise the turbine and hence inverter power below rated wind speed. The turbine was also simulated up to wind speeds of 20m/s and the inverter was shown to be able to control the generator to keep the turbine speed below its rated value. Under these conditions with the standard control algorithm, the inverter can still produce useful output power but is not able to maintain rated output power without exceeding the THD limit, due to the reduced turbine speed.

The output current distortion, at high wind speeds, occurred as a result of over-modulation. This was resolved by introducing a new control concept that maximised the current reference and hence power whilst meeting grid THD standards. This resulted in a small reduction of current reference, i.e. an output current of 0.93pu was delivered to the grid whilst meeting the grid requirements for a wind speed of 17m/s. Despite the slight power reduction, the turbine was operated in this mode to meet the grid THD standards.

Chapter 7

Conclusions and Future Work

7.1 Summary and Conclusions

This thesis examined and validated the use of a low-cost power converter topology to control a small-scale wind turbine, for both standalone and grid-connected applications. The proposed system used a switched-mode rectifier (SMR) together with a high-inductance permanent magnet (PM) generator to produce a controlled output current. The high-inductance characteristic allows the PM generator to operate as a speed-dependent constant-current source, unlike traditional low-inductance generators that act as speed-dependent constant-voltage sources.

The proposed topology has the following advantages: i) it offers simple output current control, ii) avoids the size, cost, loss and reliability issues associated with energy storage elements, such as DC link inductors or capacitors, and iii) is able to extract power at low speeds. The low-speed generator output power capability with the SMR, however, was shown to be only half of that attainable using an inverter, which thus may require over-sizing the generator for a particular wind turbine. Despite this limitation, the SMR was shown to obtain the same output power at high speeds, and is significantly cheaper and simpler than the inverter.

The turbine speed was controlled by adjusting the SMR duty-cycle, which controlled the generator output current, and hence torque and speed. This method was shown to provide adequate control flexibility for a small-scale wind turbine, based on simulation and experimental testing. The turbine could be controlled such that i) the turbine output power is maximised below rated wind speed, ii) the turbine output power is maintained at its rated value above rated wind speed, and iii) the turbine speed is reduced at high

wind speeds to prevent turbine damage.

The thesis is divided into two main parts. The first part examines the use of the SMR as a DC-DC converter to charge a battery, where the duty-cycle is kept constant under steady-state conditions, and is only adjusted to maximise or reduce power as the wind speed changes. The converter's ability to control the generator power and speed are simulated and experimentally verified using a dynamometer and a small wind tunnel. It was also shown that the SMR can deliver a controllable output current into a fixed voltage-source load making it suitable for a standalone system, such as a battery charger.

The second part of the thesis examined the design, construction, and testing of a novel grid-connected inverter (GCI) topology based on a sinusoidally modulated SMR and line-frequency commutated unfolding circuit. The topology was simulated and a 150W prototype was tested using a dynamometer. The output power was controlled by adjusting the modulation index in an open-loop manner. It was found that the topology was initially unable to meet the grid THD requirement, due to low-order current harmonics caused by resonance in the output CL filter. Each of the key parts of the inverter, including the generator acting as a non-ideal current source, the PWM switching scheme, and the low-pass filter were analysed in detail. A feed-forward control algorithm was also investigated and was shown to be able to remove the effect of the input current harmonics caused by the PM generator and rectifier current source.

The inverter analysis results were used to design a high-powered (1kW) grid-connected inverter to meet the Australian Standards. This involved selecting a suitable turbine diameter, equivalent-circuit parameters for the generator, and configuration and component values for the low-pass filter. The 1kW inverter was simulated over a wide range of wind speeds, and was shown to adequately control the small-scale wind turbine, whilst meeting the appropriate grid requirements.

7.2 Original Contributions

This work contains significant original contributions, all of which result from the investigation of controlling a small-scale wind turbine using the SMR topology together with a non-salient high-inductance PM generator. The SMR topology is simulated and tested for the DC-DC power converter case, whilst a novel GCI topology is designed, simulated, analysed and experimentally tested for the grid-connected inverter. A summary of the key original contributions is shown below; these are separated into their respective parts.

Part I: Investigation of Switched-Mode Rectifier for Standalone Power Converter

- The high-inductance PM test machine was characterised, via open-circuit, short-circuit and DC stator resistance tests. Its open and short-circuit iron, friction and windage losses were also analysed.

- The generator's ability to operate in the constant-current region for prolonged periods of time, without the stator temperature significantly increasing, was demonstrated.

- The generator was modelled and its I-V and P-V loci were simulated and experimentally verified for a wide range of generator speeds. The fixed ratio of the rectifier's AC input current to DC current output was experimentally verified, whilst the ratio of AC input voltage to the DC output voltage was investigated and shown to vary with rectifier input voltage.

- The SMR's ability to control the high-inductance PM generator using a dynamometer and fixed voltage-source load, was simulated and experimentally demonstrated, i.e. the SMR output current and hence output power and torque were controlled by adjusting the duty-cycle.

- The coefficient of performance curve for a small-scale wind turbine was estimated using tests in a wind tunnel.

- The SMR's ability to control a small-scale wind turbine, using a small wind tunnel and a fixed voltage-source load, was simulated and experimentally verified, i.e. the

SMR output current and hence turbine power and torque were controlled by adjusting the duty-cycle. The principles of maximum power point tracking and over-speed protection was demonstrated.

Part II: Investigation of Grid-Connected Inverter based on Switched-Mode Rectifier Topology

- A novel low-cost grid-connected inverter topology was designed and simulated.
- A 150W prototype inverter was constructed and tested, for both resistive and grid-connected loads, using a dynamometer test rig.
- The non-ideal inverter input current was analysed, which identified and quantified the harmonic distortion caused by the rectifier ripple and the 100Hz grid power fluctuation.
- The required CL output low-pass filter and its various damped configurations were thoroughly analysed.
- A normalised filter design approach based on the power loss vs. harmonic attenuation vs. power factor trade-off, was developed, and it was shown that the parallel-damped inductor configuration offered the best performance.
- Two feed-forward control algorithms were analysed and shown to effectively remove the output current harmonic distortion caused by the non-ideal current source.
- A high-powered (1kW) grid-connected inverter was designed. This was based on the Australian Standard grid requirements, and the non-ideal PM generator current source, low-pass filter, and feed-forward controller analyses.
- The final 1kW grid-connected inverter design, which contains an optimised low-pass filter and a feed-forward controller, was simulated and its performance was characterised. Its ability to adequately control a small-scale wind turbine over a wide range of wind speeds was demonstrated.

7.3 Recommendations for Future Work

Despite the successful demonstration of small-scale wind turbine control, using a low-cost high-inductance PM generator and a low-cost SMR power converter topology, for both standalone and grid-connected applications, some areas of this work require further investigation. These are discussed in the paragraphs below.

The DC analytical model requires refinement, as it is currently unable to accurately predict the rectifier output current vs. voltage locus. This is due to simplifying assumptions, such as the use of a loss less rectifier, and the presence of sinusoidal machine phase currents and voltages. It is recommended that the ratio of DC to AC rectifier voltages be further examined, and that the machine voltage and current waveforms are compared for various generator speeds and load conditions.

It is recommended that the small-scale wind turbine, high-inductance PM generator and the SMR be tested at higher wind speeds, using a larger wind tunnel. This is required to further validate the SMR's ability to adequately control a small-scale wind turbine over a wide range of wind speeds.

The experimentally measured and simulated open-loop inverter output current THD should be further examined for the artificially grid-connected case, as these values do not agree, despite the close matching output current waveforms. The series-connected isolation and autotransformers can be modelled more accurately, such that the simulated harmonics, caused by resonance, better match those measured experimentally.

The high-powered (1kW) grid-connected inverter, including the optimised low-pass CL filter and feed-forward controller should be constructed and tested to verify operation. The inverter, combined with a suitable wind turbine and high-inductance generator, should be tested over a wide range of wind speeds using a wind tunnel, to confirm its performance.

Finally, a closed-loop controller should be designed such that the inverter operates in both power maximisation and constant power modes autonomously.

Appendix A

PWM Control Strategies and Low-Pass Filter Design Trade-Offs

A.1 PWM Switching Schemes

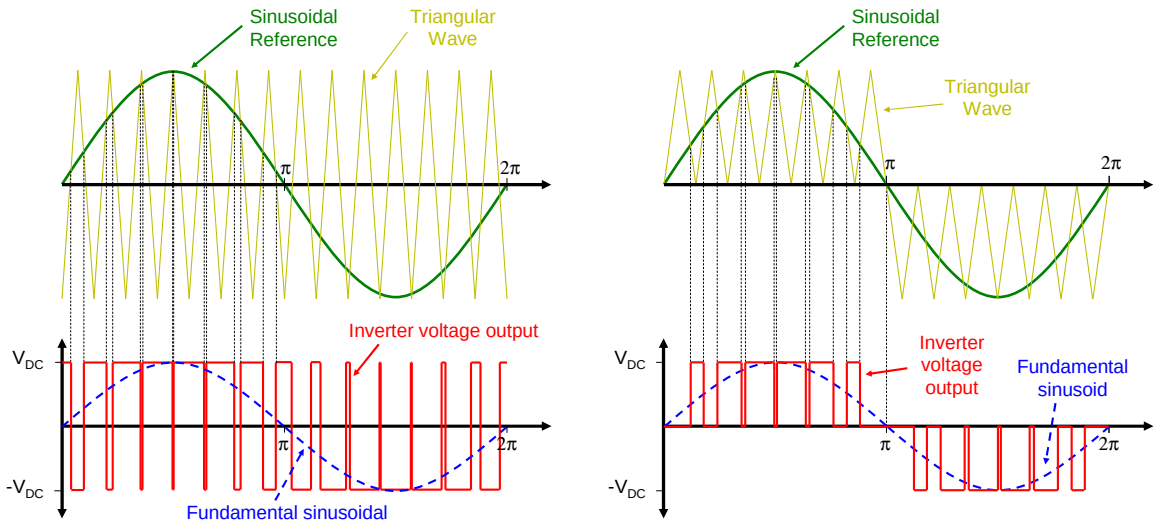
PWM control signals are applied to semiconductor switches at high-frequencies to converter DC voltages / currents to AC voltages / currents. Many PWM schemes exist, these include both *bipolar* and *unipolar sinusoidal*, *selective harmonic elimination*, and *current hysteresis* PWM schemes.

A.1.1 Bipolar and Unipolar Pulse-Width Modulation

Bipolar and Unipolar schemes are used to generate a pulse-width modulated signal, whose fundamentals resembles low-frequency sinusoids. The PWM signals are derived by comparing a sinusoidal reference with a triangular wave of at least seven times the fundamental frequency. Examples of the derivation, actual control signal and fundamental waveforms are shown in Figure A.1. The fundamental is obtained by using a low-pass filter filtering.

A.1.2 Selective Harmonic Elimination

This scheme uses a simple hardware and software structure to delivers a PWM control signal, as seen in Figure A.2. The signal has five notches and five triggering angles, $\alpha_1 ... \alpha_5$. By careful selection of five angles, a desired fundamental component can be determined which eliminates four harmonics, based on fourier analysis. Typically the 5^{th}, 7^{th}, 11^{th} and 13^{th} order harmonics are removed, which increases the magnitude of higher



(a) Bipolar PWM (b) Unipolar PWM

Figure A.1: Principle of sinusoidal pulse-width modulation, showing (a) bipolar, and (b) unipolar inverter output voltages. Each subfigure also shows the sinusoidal reference, the triangular, and the fundamental output sinusoidal waveforms.

order harmonics. This scheme is based on a feed-forward control, where the values of α_i are stored in a look-up-table.

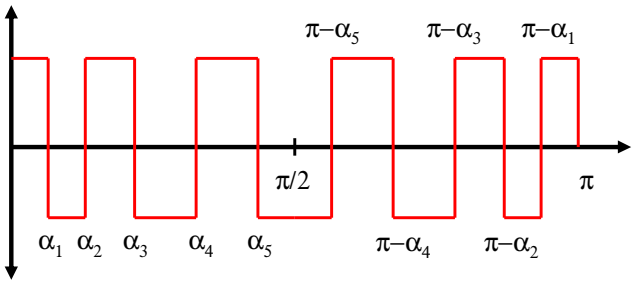


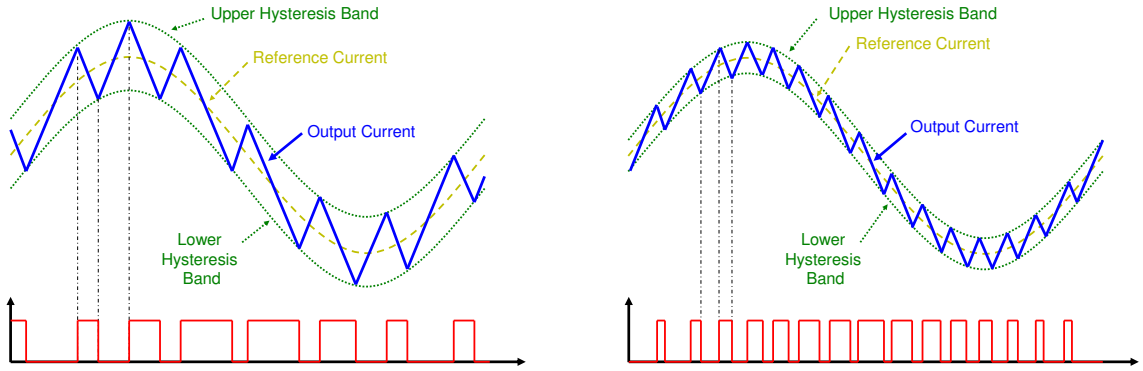
Figure A.2: Harmonic elimination PWM control signal.

A.1.3 Current Hysteresis

This control scheme confines the inverter output current within a hysteresis band, as seen in Figure A.3, for a large and small hysteresis band. The output current is detected and compared to a reference current waveform. If the output current exceeds the hysteresis band, the switch control is changed to reduce the output current. Similarly, when the output current reaches the lower hysteresis band, the control signal is adjusted to increase

output current. The result is a zig-zag type output current, with the deviation from the reference controlled by the height of the hysteresis band. Note that the switching frequency increases as the hysteresis band decreases.

The grid voltage is used as a current reference, however, harmonics found in the grid voltage are hence found in the output current. The cost of a hysteresis current controller is high due to the use of a closed-loop feedback controller, which requires current sensors and a fast analogue-to-digital (AD) converter.



(a) Large hysteresis band

(b) Small hysteresis band

Figure A.3: Principle of current hysteresis control scheme, showing output current of (a) large, and (b) small hysteresis band width.

A.1.4 Space Vector Modulation

This feedback control scheme is based on the current hysteresis scheme. Each phase current error is considered simultaneously, and the controller produces the switch signal that delivers the smallest change in current with respect to time.

A.2 Low-Pass Filter Design

A.2.1 Power Loss vs. THD Trade-Off - Unipolar PWM Case

The filter design power loss vs. output current THD trade-off, for filter configurations (FC) 1–4, was discussed in Section 5.3.8. It is desired to design a filter in the design region, in which the power loss and current THD are less than 5% each. Examples of the operating points, and the design region, is represented by the shaded box, were earlier seen in Figure 5.43, for FCs 1–4 and cutoff frequencies of 0.2 and 0.3pu (relative to the PWM switching frequency). The cutoff frequency, and design region is again shown in Figure A.4, however, the cutoff frequencies now range from 0.10 to 0.45pu. The figure indicates that the filter can be designed with greater flexibility for lower cutoff frequencies. The figure also shows that the design region is only met providing the cutoff frequency is less than 0.3pu.

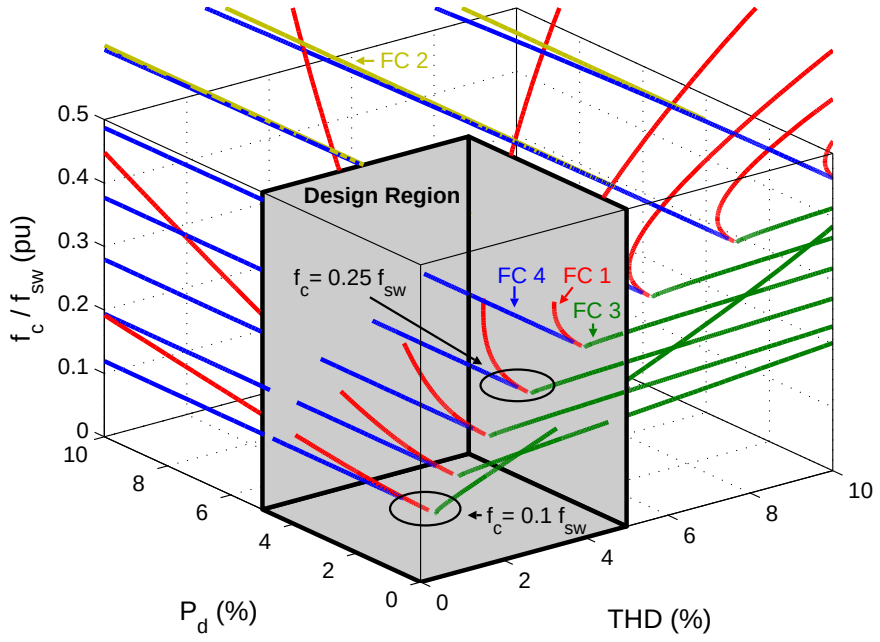


Figure A.4: Filter output current THD vs. damping resistor power loss, P_d, vs. filter cut-off frequency, f_c. The shaded region indicates the design region, where both the THD and the power loss is limited to 5%. Note that the cut-off frequency is expressed relative to the PWM switching frequency, f_{sw}, and ranges from 0.1 to 0.45pu, at increments of 0.05pu.

Appendix B

Relevant Publications

This appendix contains reprints of the two conference papers which summarise the main points of this thesis.

B.1 Wind Turbine Control using SMR Paper

This paper entitled "Investigation of Switched-Mode Rectifier for Control of Small-Scale Wind Turbines" was presented at the IEEE Industry Applications Conference in Hong Kong, October 2005, and appears in pages 2849 – 2856 of the conference proceedings.

Investigation of Switched-Mode Rectifier for Control of Small-Scale Wind Turbines

D.M. Whaley, W.L. Soong and N. Ertugrul
School of Electrical and Electronic Engineering
University of Adelaide
Adelaide, Australia

Whaley, D.M., Soong, W.L. & Ertugrul, N. (2005) Investigation of switched-mode rectifier for control of small-scale wind turbines.
Conference Proceedings, IEEE Industry Applications Conference, Fortieth IAS Annual Meeting, Conference Record of the 2005 IEEE, Hong Kong, v. 4, pp. 2849-2856

B.2 Novel Low-Cost Grid-Connected Inverter Paper

This paper entitled "Investigation of a Low-Cost Grid-Connected Inverter for Small-Scale Wind Turbines Based on a Constant-Current Source PM Generator" was presented at the IEEE Industry Electronics Conference in Paris, November 2006, and appears in pages 4297 – 4302 of the conference proceedings.

Investigation of a Low-Cost Grid-Connected Inverter for Small-Scale Wind Turbines Based on a Constant-Current Source PM Generator

David M. Whaley[1 *], Gurhan Ertasgin[1], Wen L. Soong[1], Nesimi Ertugrul[1], James Darbyshire[2], Hooman Dehbonei[2], Chem V. Nayar[2]

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Whaley, D.M., Ertasgin, G., Soong, W.L., Ertugrul, N., Darbyshire, J. Dehbonei, H. & Nayar, C.V. (2006) Investigation of a low-cost grid-connected inverter for small-scale wind turbines based on a constant-current source PM generator.
Conference Proceedings, IEEE Industrial Electronics Conference, IECON 2006, 32nd Annual Conference of IEEE , Paris, pp. 4297-4302

Appendix C

Microcontroller Code

C.1 Switched-Mode Rectifier

The *C* code listed below is that used by the microcontroller to output a fixed duty-cycle PWM signal, for a switching frequency of 4 kHz. The code makes use of both software and hardware, the latter is used to adjust the duty-cycle in increments of 1%.

```
/*********************************************************/
/*      SAMPLE PROGRAM 1 FOR MSA0654-MEAUST BOARD        */
/*      FILENAME: PWM-percentage.c                       */
/*      WRITTEN BY: David M Whaley  04-05-2004           */
/*      DESCRIPTION:                                     */
/*      -- Demonstrates the use if INT0 and INT1 to      */
/*      increase or decrease a percentage                */
/*      -- Exercises port P0 and P1 to turn display      */
/*      this percentage on LED1 and LED2.                */
/*      -- uses timer A2 to refresh LED's at 100Hz       */
/*      -- uses timers A1 and A2 to make a PWM signal    */
/*      the duty cycle is the displayed percentage,      */
/*      the same as on the LED's                         */
/*                                                       */
/*      *** NOTE: there is a 14mV offset with the        */
/*      PWM signal (output pin)                          */
/*                                                       */
/*      Copyright 2004 by DM WHALEY                      */
/*      All rights reserved. See Terms and Conditions    */
/*      document regarding the use of this sample        */
/*      program.                                         */
/*********************************************************/

#include "sfr62.h"
#include "leddata.h"

void main(void);
void initimerA0(void);
void initport(void);
void INT0int(void);
void INT1int(void);
void timerA2int(void);

#pragma INTERRUPT INT0int
#pragma INTERRUPT INT1int
#pragma INTERRUPT timerA2int
```

```
unsigned char counter = 0;
unsigned int sw_freq = 4;                // set switching frequency (in kHz)
unsigned int sw_cycles;

void main(void)
{
        sw_cycles = 16000 / sw_freq;     // sets timer using f00
        initimerA0();
        initport();
        int0ic = 0x02;                   // set int0 to level 2
        int1ic = 0x02;                   // set int1 to level 1

        ta2mr = 0x80;                    // set up timerA0 for
        ta2 = 0x1388;                    // for 100Hz LED refresh rate
        ta2ic =0x01;                     // set interrupt level for update (=1)
        tabsr |= 0x04;                   // starts timerA2 counting

        while(1);
}


void initimerA0(void)
{
        ta0mr = 0x00;           // set timer A0 for f1 use
        ta0 = sw_cycles;        // set reload register for appropriate period / frequency
        ta1mr = 0x16;           // set timer A1 for f1 use and one-shot timer mode
        trgsr = 0x02;           // timer A1 event/trigger select bit - TA0 overflow selected
        tabsr |= 0x01;          // starts timerA0

        ta1 = 0;                // set timer A1 register for 0 cycles => 0.0ms ie 0% duty
        tabsr |= 0x02;          // timerA1 starts counting
}


void initport(void)
{
        pd0 = 0xFF;             // output mode
        pd1 = 0xFF;             // output mode
        pu00 = 0;               // no pull up for P0_0 to P0_3
        pu01 = 0;               // no pull up for P0_4 to P0_7
        pu02 = 0;               // no pull up for P1_0 to P1_3
        p0 = 0x00;              // initial data to Port 0
        p1 = 0xFF;              // initial data to Port 1
        p0 = 0x00;
}


void INT0int(void)
{
        unsigned int newtimervalue;

        if (counter < 100)
        {
                counter++;
        }                       // increase PWM duty-cycle by 1%
        else                    // or make duty-cycle 0% if already 100%
        {
                counter = 0;
        }

        newtimervalue = (sw_cycles/100)*counter;

        ta1 = newtimervalue;    // set timer A1 register for counter % duty
        tabsr |= 0x02;          // timerA1 starts counting

}
```

```
void INT1int(void)
{
        unsigned int newtimervalue;

        if (counter > 0)
        {
                counter--;
        }                       // decrease PWM duty-cycle by 1%
        else                    // or make duty-cycle 100% if already 0%
        {
                counter = 100;
        }

        newtimervalue =(sw_cycles/100)*counter;

        ta1 = newtimervalue;    // set timer A1 register for counter % duty
        tabsr |= 0x02;          // timerA1 starts counting

}


void timerA2int(void)
{
        static unsigned char led_number = 0;
        unsigned char offset;

        asm("fset I");                          // enable interrupts

        if (led_number == 0)
        {
                led_number = 1;
                p0 = 0xFF;
                p1 = 0xFD;                      // disable LED 1 and enable LED2

                if (counter == 100)
                {                               // displays '1H' for 100% duty cycle
                        p0 = 0x89;              // displays 'H' on LED 2
                }                               // displays '1' on LED 1
                else
                {
                        offset = counter % 10;
                        p0 = leddigit[offset];  // display remainder (1's figure) on LED 2
                }
        }
        else
        {
                led_number = 0;
                p0 = 0xFF;
                p1 = 0xFE;                      // disable LED 2 and enable LED1

                if (counter == 100)
                {                               // displays '1H' for 100% duty cycle
                        p0 = leddigit[1];       // displays '1' on LED 1
                }                               // displays 'H' on LED 2
                else
                {
                        offset = counter / 10;
                        p0 = leddigit[offset];  // display quotient (10's figure) on LED 1
                }
        }
}
```

C.2 Grid-Connected Inverter

The *C* code listed below is that used by the microcontroller to control the grid-connected inverter in open-loop mode. It makes use of both software and hardware interrupts to synchronise the inverter output current to the grid, whilst allowing the user to control the magnitude by adjusting the modulation index.

```
/*********************************************************/
/*      FILENAME: PWM_csi_unf.c                          */
/*      WRITTEN BY: David M. Whaley  08-03-2006          */
/*      DESCRIPTION:                                     */
/*      -- Demonstrates the use if timer B0 to           */
/*      interrupt and increase a PWM duty-cycle,         */
/*      -- Exercises port P0 and P1 to turn display      */
/*      this percentage on LED1 and LED2.                */
/*      -- uses timer B1 to refresh LED's at 100Hz       */
/*      -- uses timers A1 and B2 to make a PWM signal    */
/*      -- uses timers A4 & A3 to fire thyristors on     */
/*      -- uses INT0 abd INT1 to increase and decrease   */
/*      the modulation index, respectively               */
/*      -- the modulation index is the displayed         */
/*      on the LED's                                     */
/*                                                       */
/*      *** NOTE: there is a 14mV offset with the        */
/*      PWM signal (output pin)                          */
/*                                                       */
/*      Copyright 2006 by David M. WHALEY                */
/*      All rights reserved. See Terms and Conditions    */
/*      document regarding the use of this sample        */
/*      program.                                         */
/*********************************************************/

#include "sfr62.h"
#include "leddata.h"

void main(void);
void initimers(void);
void initport(void);
void INT0int(void);
void INT1int(void);
void INT3int(void);
void timerB1int(void);
void timerB0int(void);

#pragma INTERRUPT INT0int
#pragma INTERRUPT INT1int
#pragma INTERRUPT INT3int
#pragma INTERRUPT timerB1int
#pragma INTERRUPT timerB0int

unsigned char d = 100;
unsigned int sw_freq = 4;               // set switching frequency (in kHz)
unsigned int sw_cycles;
unsigned int thyristorfiring = 2;
unsigned int hundredduty = 2;
unsigned int ma = 100;
unsigned int da = 100;
unsigned int anothercounter = 0;
```

```
void main(void)
{
        sw_cycles = 16000 / sw_freq;     // sets timer using f00
        initimers();
        initport();
        int0ic = 0x02;                   // set int0 to level 2
        int1ic = 0x02;          // set int1 to level 2
        int3ic = 0x13;          // set int3 to level 3 (i.e. highest) rising edge

        while(1);
}

void initimers(void)
{
        tb2mr = 0x00;           // set timer B2 for f1 use
        tb2 = sw_cycles;        // set reload register for apprproate period / frequency

        tb1mr = 0x80;           // set up timerB1 for
        tb1 = 0x1388;           // for 100Hz LED refresh rate
        tb1ic =0x02;            // set interrupt level for update (=1)
        tb0mr = 0x80;           // set up timerB0 for
        tb0 = 0xFA;             // for 2kHz interrupt rate

        tb0ic =0x01;            // set interrupt level for update (=1)

        ta1mr = 0x16;           // set up timerA0 to use overflow trigger, and pulse TA1 output pin
        ta4mr = 0x16;           // set up timerA0 to use overflow trigger, and pulse TA2 output pin
                                // used to control thyristor gate fring pulses for opposite devices
        ta3mr = 0x16;           // set up timerA0 to use overflow trigger, and pulse TA3 output pin
                                // used to control THY gate fring pulses for opposite devices to TA2

        trgsr = 0x01;           // set timerA1 TB2 overflow, TA3 & TA4 use falling edge of TA1
        tabsr = 0xFA;           // start timersA1-3 & timerB0-2

        ta1 = 0;                // set timerA1 register for 0 cycles => 0.0ms ie 0% duty
        ta4 = 0;                // set all thyristors off
        ta3 = 0;                // set all thyristors off
}

void initport(void)
{
        pd0 = 0xFF;             // output mode
        pd1 = 0xFF;             // output mode
        pu00 = 0;               // no pull up for P0_0 to P0_3
        pu01 = 0;               // no pull up for P0_4 to P0_7
        pu02 = 0;               // no pull up for P1_0 to P1_3
        p0 = 0x00;              // initial data to Port 0
        p1 = 0xFF;              // initial data to Port 1
        p0 = 0x00;
}



void INT0int(void)
{
        asm("fset I");          // enable interrupts

        if (ma < 100)
        {
                ma++;           // increase modulation
        }                       // index by 1% (if < 100%)
        else
        {
                ma = 0;         // otherwise set it to 0%
        }
}
```

```
void INT1int(void)
{
        asm("fset I");          // enable interrupts

        if (ma > 0)
        {
                ma--;           // decrease modulation
        }                       // index by 1% (if > 0%)
        else
        {
                ma = 100;       // otherwise set it to 100%
        }
}

void INT3int(void)
{
        int3ic = 0x00;          // disbale int3 interrupt as zero-crosing
                                // detection circuit output contains noise
                                // and can interrupt accidentally
        d = 100;                // resets LUT vlaue
        thyristorfiring = 1;    // *** USED TO SET +VE OR -VE OUPUT
                                // CURRENT POLARITY ***
                                // *** set to 1 or 2 ***
                                // when set to 1, white pulses at zero volts
                                // when set to 2, white pulses at rising edge trigger
        anothercounter=0;
}

void timerB1int(void)
{
        static unsigned char led_number = 0;
        unsigned char offset;

        asm("fset I");                          // enable interrupts

        if (led_number == 0)
        {
                led_number = 1;
                p0 = 0xFF;
                p1 = 0xFD;                      // disable LED 1 and enable LED2

                if (ma == 100)
                {                               // displays '1H' for 100% duty cycle
                        p0 = 0x89;              // displays 'H' on LED 2
                }                               // displays '1' on LED 1
                else
                {
                        offset = ma % 10;
                        p0 = leddigit[offset];  // display remainder (1's figure) on LED 2
                }
        }
        else
        {
                led_number = 0;
                p0 = 0xFF;
                p1 = 0xFE;                      // disable LED 2 and enable LED1

                if (ma == 100)
                {                               // displays '1H' for 100% duty cycle
                        p0 = leddigit[1];       // displays '1' on LED 1
                }                               // displays 'H' on LED 2
                else
                {
                        offset = ma / 10;
                        p0 = leddigit[offset];  // display quotient (10's figure) on LED 1
                }
        }
}
```

```
void timerB0int(void)
{
        unsigned int newtimervalue;
        unsigned int newtimervalue2;

        asm("fset I");                          // enable interrupts
        anothercounter++;
        switch(d)
        {
                case 100: d = 84;

                        if(thyristorfiring == 2)
                        {
                                thyristorfiring = 1;            // identify which thyristors
                                                                // are conducting
                                ta3 = 0;                        // turn thyristor 1 & 3 pair off
                                ta4 = (sw_cycles/100)*15;       // turn thyristor 2 & 4 on
                        }
                        else
                        {
                                thyristorfiring = 2;
                                ta4 = 0;                        // turn thyristor 2 & 4 off
                                ta3 = (sw_cycles/100)*15;       // turn thyristor 1 & 3 pair on
                        }
                break;

                case 84: d = 69; break;
                case 69: d = 55; break;
                case 55: d = 41; break;
                case 41: d = 29; break;
                case 29: d = 19; break;
                case 19: d = 11; break;
                case 11: d = 5; break;
                case 5: d = 1; break;
                case 1: d = 0; break;
                case 0: d = 2; break;
                case 2: d = 6; break;
                case 6: d = 12; break;
                case 12: d = 20; break;
                case 20: d = 30; break;
                case 30: d = 42; break;
                case 42: d = 56; break;
                case 56: d = 70; break;
                case 70: d = 85; break;
                case 85: d = 100;
                         ta3 = 0;
                         ta4 = 0; break;
        }

        if(anothercounter > 38)
        {
                int3ic = 0x13;                  // set int3 to level 3 (i.e. highest) rising edge
        }                                       // as this is close to 1 period of grid frequency


        da = 100 - ma + (ma*d)/100;             // adjusted duty-cycle
        newtimervalue = (sw_cycles/100)*da;
        ta1 = newtimervalue;                    // set timer A1 register for da % duty
}
```

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