



High Performance RF CMOS VCOs for Wireless Communication

By

Tae Youn Kim

B.E. (EEE, Hons), The University of Adelaide, 2000

A Thesis

Submitted to the School of Electrical and Electronic Engineering

in Fulfillment of the Requirements

for the Degree of

Doctor of Philosophy

Department of Electrical and Electronic Engineering

The University of Adelaide

Australia

©Copyright by Tae Youn Kim, October 2004

All rights reserved

ABSTRACT

This thesis is dedicated to develop a set of general and systematic techniques to design and produce high performance monolithic CMOS VCOs to use in modern wireless front-end chips.

In general, there are four topics covered in this research work. First, existing oscillator phase noise estimation theories are discussed. Some of these theories lead to simple and rough estimation of the phase noise, while some forms the basis for more complicated and accurate phase noise estimation performed by modern CAD tools.

Second, the operation and noise performance of a number of differential *LC* tuned VCO topologies are investigated in detail. Some common misconceptions associated with cross-coupled oscillators, including the incorrect linear oscillation amplitude expressions, nonexistence of a VCO bias region called voltage-limited region, and the non-apparent topological advantage of the complementary topology are addressed. Also, the noise sources associated with differential *LC* tuned VCOs are identified and investigated. Upconversion processes of low frequency flicker noise through various upconversion processes are discussed.

Third, based on the understandings acquired from the differential *LC* tuned oscillator analyses, a set of new optimization techniques is developed. These techniques allow for design of the best performing VCO realizable for a given process technology, chip area, and power budget. A new geometric monolithic planar spiral inductor optimization technique, an efficient way to trade between power consumption and phase

noise performance via L/C ratio scaling, appropriate sizing of the cross-coupled transistors, and a low-power, low-noise current biasing technique are among the VCO optimization techniques developed in this research work.

Lastly, the VCO optimization techniques developed are tested and validated by fabricating a number of VCOs using two different modern CMOS process technologies and analyzing their performances. The performances of these VCOs are then compared against the state-of-the-art monolithic VCOs reported in the literature. The comparison is not limited to CMOS VCOs, but extends to other competing process technologies such as bipolar technology. The comparison clearly shows the superiority of some of the VCOs designed and fabricated in this research work.

TABLE OF CONTENTS

ABSTRACT	III
STATEMENT OF ORIGINALITY	V
ACKNOWLEDGMENTS	VI
TABLE OF CONTENTS	VII
LIST OF FIGURES	XI
LIST OF TABLES	XVII
LIST OF ACRONYMS	XVIII
LIST OF SYMBOLS	XXII
LIST OF CONSTANTS	XXIV
CHAPTER1: INTRODUCTION	1
1.1 WIRELESS COMMUNICATIONS	1
1.2 MODERN RADIO TRANSCEIVER	2
1.2.1 Reciprocal Mixing	4
1.2.2 OFDM and Phase Noise	7
1.3 VOLTAGE-CONTROLLED OSCILLATORS	9
1.3.1 Monolithic CMOS VCOs	11
1.3.2 Current Monolithic VCO Performances	14
1.4 OBJECTIVES	15
1.5 SCOPES	16
1.6 MAJOR CONTRIBUTIONS	18
1.7 THESIS ORGANIZATION	19
CHPATER2: V	22
2.1 INTRODUCTION	22

2.2 PHASE NOISE	24
2.3 LINEAR OSCILLATORS	26
2.3.1 Linear <i>LC</i> Tuned Oscillator Analysis	28
2.3.2 Ring Oscillator Analysis	32
2.3.3 Limitations of the LTI Model	34
2.3.4 Figure of Merit	34
2.4 NONLINEAR OSCILLATORS	36
2.4.1 Linear Time-Varying Oscillator Model	38
2.4.2 Phase Noise Simulator	42
2.4.3 Limitations of Simulator	44
2.5 CONCLUSIONS	47
CHAPTER3: DIFFERENTIAL <i>LC</i> TUNED OSCILLATORS	49
3.1 INTRODUCTION	49
3.2 CROSS-COUPLED OSCILLATORS	50
3.2.1 NMOS-Only Topology	55
3.2.2 Other Cross-Coupled Topologies	70
3.3 FREQUENCY TUNING METHODS	76
3.3.1 Varactors	77
3.3.2 Continuous Tuning	88
3.3.3 Discrete Tuning	91
3.4 PHASE NOISE SOURCES	96
3.4.1 Passive Resonator Noise	98
3.4.2 Tail Transistor Noise	100
3.4.3 Cross-Coupled Pair Noise	103
3.4.4 External Noise Sources	106
3.5 CONCLUSIONS	109
CHAPTER4: OPTIMIZATION TECHNIQUES	111
4.1 INTRODUCTION	111
4.2 MONOLITHIC INDUCTORS	112

4.2.1 Active Inductors	113
4.2.2 Bond-Wire Inductors	115
4.2.3 Planar Spiral Inductors	116
4.2.4 MEMS Inductors	118
4.3 SPIRAL INDUCTOR OPTIMIZATION	120
4.3.1 Simple Inductor Expressions	120
4.3.2 High Frequency Inductors	122
4.3.3 Geometric Inductor Optimization	130
4.4 L/C RATIO OPTIMIZATION	135
4.5 TRANSISTOR SIZE OPTIMIZATION	140
4.5.1 Tail Transistor Size	140
4.5.2 Cross-Coupled Oscillator Noise Analysis	141
4.5.3 Cross-Coupled Pair Optimization	153
4.6 OTHER OPTIMIZATION MEASURES	157
4.6.1 Bypass Capacitors	157
4.6.2 Low-Power, Low-Noise Current Biasing	159
4.7 CONCLUSIONS	162
CHAPTER5: HIGH PERFORMANCE SOI CMOS VCOS	164
5.1 INTRODUCTION	164
5.2 0.5 μ m SOS CMOS PROCESS	165
5.3 EXPERIMENTAL 5GHZ VCOS	167
5.3.1 VCO Designs	168
5.3.2 Inductor Designs	173
5.3.3 Results	177
5.4 EXPERIMENTAL 17GHZ VCOS	189
5.4.1 VCO Designs	190
5.4.2 Inductor Designs	192
5.4.3 Results	193
5.5 LOW-NOISE 5GHZ VCOS	199
5.5.1 VCO Designs	200

5.5.2 Tank Design	203
5.5.3 Low Noise Measures	206
5.5.4 Results	208
5.6 CONCLUSIONS	214
CHAPTER6: HIGH PERFORMANCE BULK CMOS VCOS	218
6.1 INTRODUCTION	218
6.2 0.18 μ m BULK CMOS PROCESS	219
6.3 LOW-NOISE 5GHZ VCO	221
6.3.1 Inductor Design	222
6.3.2 VCO Design	224
6.3.3 Results	228
6.4 INDUSTRIAL QUALITY 5GHZ VCO	232
6.4.1 Specifications	233
6.4.2 Tank Design	235
6.4.3 VCO Design	238
6.4.4 Bias Current Generator	241
6.4.5 Amplitude Detector	245
6.4.6 Results	246
6.5 VCO PERFORMANCE COMPARISON	257
6.6 CONCLUSIONS	259
CHAPTER7: CONCLUSIONS AND RECOMMENDATIONS	260
7.1 CONCLUSIONS	260
7.2 RECOMMENDATIONS	264
REFERENCES	266
APPENDIX	277