High Performance RF CMOS VCOs for Wireless Communication

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ABSTRACT

This thesis is dedicated to develop a set of general and systematic techniques to design and produce high performance monolithic CMOS VCOs to use in modern wireless front-end chips.

In general, there are four topics covered in this research work. First, existing oscillator phase noise estimation theories are discussed. Some of these theories lead to simple and rough estimation of the phase noise, while some forms the basis for more complicated and accurate phase noise estimation performed by modern CAD tools.

Second, the operation and noise performance of a number of differential *LC* tuned VCO topologies are investigated in detail. Some common misconceptions associated with cross-coupled oscillators, including the incorrect linear oscillation amplitude expressions, nonexistence of a VCO bias region called voltage-limited region, and the non-apparent topological advantage of the complementary topology are addressed. Also, the noise sources associated with differential *LC* tuned VCOs are identified and investigated. Upconversion processes of low frequency flicker noise through various upconversion processes are discussed.

Third, based on the understandings acquired from the differential *LC* tuned oscillator analyses, a set of new optimization techniques is developed. These techniques allow for design of the best performing VCO realizable for a given process technology, chip area, and power budget. A new geometric monolithic planar spiral inductor optimization technique, an efficient way to trade between power consumption and phase

noise performance via L/C ratio scaling, appropriate sizing of the cross-coupled transistors, and a low-power, low-noise current biasing technique are among the VCO optimization techniques developed in this research work.

Lastly, the VCO optimization techniques developed are tested and validated by fabricating a number of VCOs using two different modern CMOS process technologies and analyzing their performances. The performances of these VCOs are then compared against the state-of-the-art monolithic VCOs reported in the literature. The comparison is not limited to CMOS VCOs, but extends to other competing process technologies such as bipolar technology. The comparison clearly shows the superiority of some of the VCOs designed and fabricated in this research work.

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