High Performance RF CMOS VCOs for Wireless Communication

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ABSTRACT

This thesis is dedicated to develop a set of general and systematic techniques to design and produce high performance monolithic CMOS VCOs to use in modern wireless front-end chips.

In general, there are four topics covered in this research work. First, existing oscillator phase noise estimation theories are discussed. Some of these theories lead to simple and rough estimation of the phase noise, while some forms the basis for more complicated and accurate phase noise estimation performed by modern CAD tools.

Second, the operation and noise performance of a number of differential LC tuned VCO topologies are investigated in detail. Some common misconceptions associated with cross-coupled oscillators, including the incorrect linear oscillation amplitude expressions, nonexistence of a VCO bias region called voltage-limited region, and the non-apparent topological advantage of the complementary topology are addressed. Also, the noise sources associated with differential LC tuned VCOs are identified and investigated. Upconversion processes of low frequency flicker noise through various upconversion processes are discussed.

Third, based on the understandings acquired from the differential LC tuned oscillator analyses, a set of new optimization techniques is developed. These techniques allow for design of the best performing VCO realizable for a given process technology, chip area, and power budget. A new geometric monolithic planar spiral inductor optimization technique, an efficient way to trade between power consumption and phase

noise performance via *L/C* ratio scaling, appropriate sizing of the cross-coupled transistors, and a low-power, low-noise current biasing technique are among the VCO optimization techniques developed in this research work.

Lastly, the VCO optimization techniques developed are tested and validated by fabricating a number of VCOs using two different modern CMOS process technologies and analyzing their performances. The performances of these VCOs are then compared against the state-of-the-art monolithic VCOs reported in the literature. The comparison is not limited to CMOS VCOs, but extends to other competing process technologies such as bipolar technology. The comparison clearly shows the superiority of some of the VCOs designed and fabricated in this research work.

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ACKNOWLEDGMENTS

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LIST OF ACRONYMS

AC	Alternate Current
ADS	Advanced Design Systems
AGC	Automatic Gain Control
AM	Amplitude Modulation
AP	Access Point
ASITIC	Analysis and Simulation of Inductors and Transformers in Integrated Circuits
BiCMOS	Bipolar CMOS
BP	Band-Pass
BSIM	Berkeley Short-Channel IGFET Model
CAD	Computer Aided Design
CCP	Cross-Coupled Pair
CMM	Common Mode Modulation
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DCR	Data Clock Recovery
FET	Field-Effect Transistor
FM	Frequency Modulation
FOM	Figure of Merit
GPIB	General Purpose Interface Bus
HBT	Heterojunction Bipolar Transistor
HiPERLAN	High Performance Radio Local Area Network
HiPERLINK	High Performance Radio Link
IC	Integrated Circuit
ICI	Inter-Carrier Interference
IEEE	Institute of Electrical and Electronic Engineering
IF	Intermediate Frequency

ISF	Impulse Sensitivity Function
LNA	Low Noise Amplifier
LO	Local Oscillator
LP	Low-Pass
LTI	Linear Time Invariant
LTV	Linear Time Varying
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	N-type Metal Oxide Semiconductor
OFDM	Orthogonal Frequency Division Multiplex
PA	Power Amplifier
PC	Personal Computer
PCM	Process Control Monitor
PGS	Patterned Ground Shield
PMOS	P-type Metal Oxide Semiconductor
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
RF	Radio Frequency
SAW	Surface Acoustic Wave
SER	Symbol Error Rate
SNR	Signal to Noise Ratio
SOC	System On Chip
SOI	Silicon On Insulator
SOS	Silicon On Sapphire
SPICE	Simulation Program with Integrated Circuit Emphasis
SS	Single-Sided
SSB	Single Side Band
STI	Shallow Trench Isolation
TSMC	Taiwanese Semiconductor Manufacturing Company

VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
WLAN	Wireless Local Area Network
WNBU	Wireless Networking Business Unit

LIST OF SYMBOLS

σ	Conductivity (S/m)
ξ	$C_{v.max}$ to $C_{v.min}$ ratio
Γ	Impulse sensitivity function
γ	Transistor channel noise factor
ΔC_v	$C_{v.max}-C_{v.min}$ (F)
δ_s	Skin depth (m)
A_0	Single-ended oscillation amplitude (V)
C_{fix}	Fixed capacitance (F)
C_{ov}	Gate overlap capacitance (F)
C_{ox}	Unit gate oxide capacitance
C_v	Varactor capacitance (F)
$C_{v.eff}$	Effective varactor capacitance (F)
$C_{v.max}$	Maximum varactor capacitance (F)
$C_{v.min}$	Minimum varactor capacitance (F)
D_{in}	Inner diameter of a spiral (μm)
D_{out}	Outer diameter of a spiral (μm)
F	Oscillator Noise factor
f_0, ω_0	Frequency of oscillation (Hz, rad/s)
$f_{1/f}$, $\omega_{1/f}$	Flicker noise corner frequency (Hz, rad/s)
f_m, ω_m	Frequency offset from carrier (Hz, rad/s)
f_{max}, ω_{max}	Unit power gain frequency of transistor (Hz, rad/s)
f_{self}	Self-resonant frequency (Hz)
f_T	Transition frequency, where current gain falls to unity (Hz)
f_T, ω_T	Unit current gain frequency of transistor (Hz, rad/s)
G_{DS}	Average transistor drain-source conductance (S)
g_{ds}	Transistor drain-source conductance (S)
$G_{ds.eff}$	Effective drain-source conductance of cross-coupled pair (S)

g_{ds0}	Small-signal transistor drain-source conductance at $V_{DS}=0$ (S)
g_m	Transistor transconductance (S)
i_n	Noise current ($A/\sqrt{Hz}$)
I_{ref}	Reference current for tail bias current (A)
I_{tail}	Cross-coupled LC tuned oscillator bias current (A)
K_V	VCO constant, or VCO gain (Hz/V)
$\mathcal{L}\{\omega_m\}, \mathcal{L}\{f_m\}$	Phase noise (dBc/Hz @ ω_m, f_m offset from carrier)
L_{CCP}	Cross-coupled pair transistor length (μm)
N, n	Number of spiral turns
N_{ot}	Transistor gate oxide trap density (units/m^2)
P_{DC}	DC power
P_{SBC}	Oscillator sideband noise power with respect to carrier (W/Hz)
P_{sig}	Single-ended oscillation power (W)
Q	Quality factor
Q_C	Capacitor quality factor
Q_L	Inductor quality factor
Q_{tank}	Loaded Q of LC tuned circuit
r_{DS}	Transistor drain-source resistance (Ω)
$R_{ds,eff}$	Effective drain-source resistance of cross-coupled pair (Ω)
R_{tank}	Parallel equivalent resistance of lossy LC tuned circuit (Ω)
s	Gap between spiral turns (μm)
S_i	Noise current (A^2/Hz)
$S_{i_d^2,1/f}$	Transistor flicker noise current density (A^2/Hz)
S_v	Noise voltage (V^2/Hz)
T	Absolute Temperature (K)
V_B	Transistor bulk potential (V)
V_{CCP}	Cross-coupled pair bias potential (V)
V_{ctl}	Frequency control voltage (V)
V_{DD}	Supply voltage (V)

v_{DS}	Transistor drain-source voltage (V)
V_G	Transistor gate potential (V)
v_{GS}	Transistor gate-source voltage (V)
v_{out+}, v_{out-}	Differential oscillator output signals (V)
V_{tail}	Cross-coupled VCO tail transistor gate bias potential (V)
V_{TH}	Transistor threshold voltage (V)
w	Spiral inductor conductor width (μm)
ω_{1/f^3}	Corner frequency between -30dB/decade region and -20dB/decade region in a plot of oscillator phase noise.
W_{CCP}	Cross-coupled pair transistor width (μm)
υ_n	Noise voltage ($V/\sqrt{Hz}$)

LIST OF CONSTANTS

$k=1.381\times10^{25}$ J/K $\qquad$ Boltzmann's constant

$\mu_0=1.257\times10^{-6}$ H/m $\qquad$ Magnetic permeability of free space

Chapter 1

INTRODUCTION

1.1 WIRELESS COMMUNICATIONS

Beginning in the late 1890s, Italian scientist Guglielmo Marconi successively sent and detected electromagnetic waves across a room. Marconi gradually increased the range, and in 1901, he was able to demonstrate successfully sending the letter 'S' in Morse code over the Atlantic Ocean without wires. Ever since, many other players, namely Lee de Forest, the inventor of the vacuum tube, and Edwin Armstrong, the inventor of superheterodyne system and FM radio competed in the wireless communications race. Like many other industries propelled by wars, the First and the Second World War had accelerated the progress of wireless technology.

The first generation solid-state semiconductor named the transistor, invented by Schockley, Brittain, and Bardeen of the Bell Labs in 1947, opened a new era for the radio industry. Much smaller, efficient, and reliable transistors replaced vacuum tubes. This subsequently reduced the cost and dimensions of the primary power supply, cooling, and equipment accommodation.

Another major step in the semiconductor technology was the development of the technique that came to be known as an Integrated Circuit (IC) by Jack Kilby of Texas Instruments in 1958. IC technology made it possible to integrate transistors and other passive devices like resistors and capacitors all on the same substrate. This did not have immediate impact on the advancement of the wireless technology until Very Large Scale Integration (VLSI) technique gained sufficient momentum starting from the late 1960s. Towards the early 1980s, Monolithic Microwave Integrated Circuits (MMIC) started to appear. MMIC chips integrate much of the radio circuit modules, namely RF amplifier, mixer, and Local Oscillator (LO). Later in the 1990s, monolithic implementation of radio circuit modules was made possible using digital processes, which integrated digital circuit modules for controlling, sampling, and processing of data all in a single chip. This System-On-Chip (SOC) approach allowed for reduction in system form factor and cost.

1.2 MODERN RADIO TRANSCEIVER

Since the birth of superheterodyne system in 1917 by Edwin Armstrong, virtually every wireless communication systems employed the superheterodyne principle to date. A tunable oscillator or a frequency synthesizer is one of the compulsory building blocks in a superheterodyne system along with RF amplifiers and mixers.

The superheterodyne system is able to tune to the frequency under interest, and up or downconvert to frequencies where subsequent filtering or

modulation/demodulation can be performed easily. The frequency translation property of the superheterodyne system is what makes it popular and essential in modern wireless communication systems.

In a superheterodyne receiver shown in Fig. 1.1(a), the received radio frequency (RF) signal through the antenna is often weak, and needs significant boost before it can be processed any further. The low-noise-amplifier (LNA) provides much of the required amplification while minimizing the noise figure.

(a)

(b)
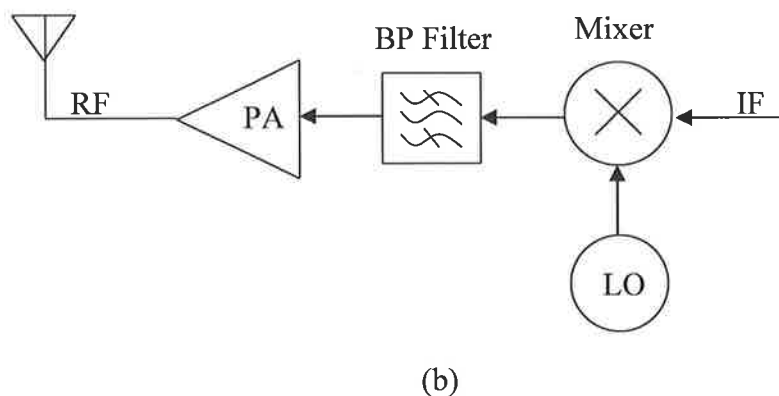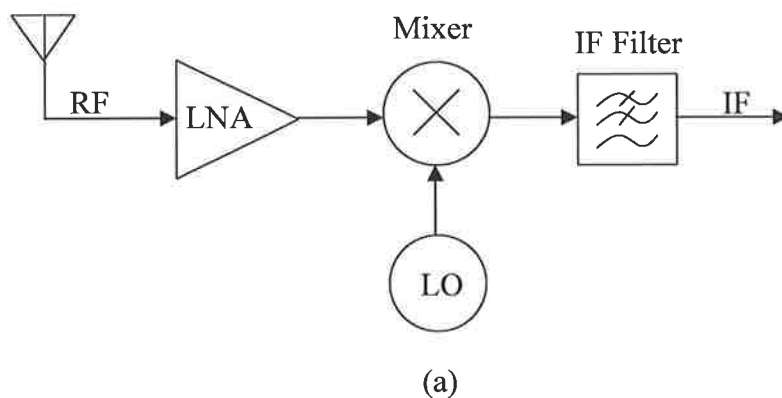
Fig. 1.1: Superheterodyne (a) receiver and (b) transmitter.

A mixer accepts two separate input signals (RF+LO) and outputs the sum or difference of the two input signals (RF–LO, RF+LO,) in the frequency domain. The mixer can be either active or passive. In either case, a mixer usually has a high noise figure compared to an LNA. Nonetheless, as long as the LNA provides sufficient amplification, use of a mixer with relatively poor noise figure can be tolerated.

The IF filter at the output of the mixer is there to filter out unwanted frequency components of the mixer output.

In the transmit path, as shown in Fig. 1.1(b), the intermediate frequency (IF) signal is given sufficient signal-to-noise ratio (SNR) to prepare for degradation of its SNR after passing through the mixer.

The band-pass (BP) filter selectively passes the desired signal from the mixer output to the power-amplifier (PA) for transmitting via the antenna.

By being able to vary the frequency of the LO, the receiver can selectively downconvert the desired signal received via the antenna, and the transmitter can transmit the signal on the desired frequency channel.

1.2.1 Reciprocal Mixing

Noise introduced by an LNA or a mixer is usually amplified thermal noise. Therefore, its noise spectral density characteristic is flat within the pass-band. However, noise introduced by an LO is somewhat different. What contributes to the LO noise are not only the thermal noise, but also the pink noise ($1/f$ noise or flicker noise near DC) of active devices, as well as the spurs from the frequency reference source. The LO

noise near the carrier frequency is considerably larger in magnitude compared to the thermal noise floor of other RF circuit modules.

Ideally, the Fourier representation of a sinusoidal LO signal is represented by a pair of delta functions in the frequency domain. RF/IF signals mixed in the time domain or convoluted in the frequency domain at the mixer with an ideal LO signal is replicated at IF/RF with appropriate amplification. For example, LO signal

$$s(t) = A_0 \cos(\omega_0 t) \tag{1.1}$$

mixed with a pair of RF signals

$$r_1(t) = M_1 \cos(\omega_1 t) \tag{1.2}$$

and

$$r_2(t) = M_2 \cos(\omega_2 t) \tag{1.3}$$

would produces two pairs of IF signals

$$
\begin{aligned}
m_1(t) + m_2(t) &= s(t)\left[r_1(t) + r_2(t)\right] \\
&= A_0 \cos(\omega_0 t)\left[M_1 \cos(\omega_1 t) + M_2 \cos(\omega_2 t)\right] \\
&= \frac{1}{2} A_0 M_1 \left[\cos(\omega_0 + \omega_1)t + \cos(\omega_0 - \omega_1)t\right] \\
&\quad + \frac{1}{2} A_0 M_2 \left[\cos(\omega_0 + \omega_2)t + \cos(\omega_0 - \omega_2)t\right]
\end{aligned}
\tag{1.4}
$$

A low-pass (LP) filter placed at the output of the mixer filters out the frequency components above ω_0, and the resulting IF signals become

$$m_1(t) = \frac{1}{2} A_0 M_1 \cos(\omega_1 - \omega_0)t \tag{1.5}$$

and

$$m_2(t) = \frac{1}{2} A_0 M_2 \cos(\omega_2 - \omega_0)t \tag{1.6}$$

Fig. 1.2(a) illustrates this ideal downconversion process in the frequency domain. $r_1(t)$ and $r_2(t)$ represent received signals adjacent to each other. They can have different levels of power depending on the locations of their transmitters or the modulation scheme used.

When a noisy LO is used, a problem may arise when $r_1(t)$ and $r_2(t)$ are closely spaced and one is much stronger than the other. Phase noise of an oscillator has a symmetric skirt shape centered about the carrier frequency. The shape of the noise skirt near the carrier is affected by the frequency locking technique employed. For the time being, a simple noise skirt shape as shown in Fig. 1.2(b) is assumed.
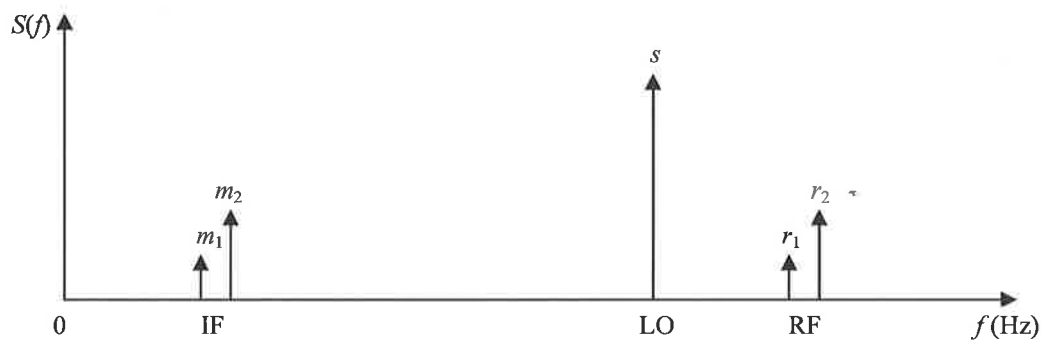
(a)
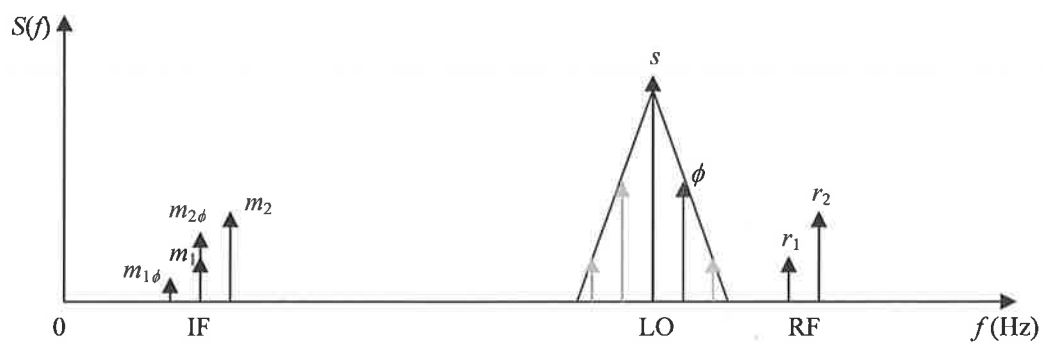
(b)

Fig. 1.2: Downconversion with (a) noiseless LO and (b) noisy LO.

During the downconversion process of $r_1(t)$ and $r_2(t)$, the phase noise frequency component $\phi(t)$ mixes with $r_1(t)$ and $r_2(t)$, just as the carrier $s(t)$ does, and produces IF components $m_{1\phi}(t)$ and $m_{2\phi}(t)$. $m_{2\phi}(t)$ superimposed on top of $m_1(t)$ is considered as noise or interference. The consequence is degraded SNR of the received signal $m_1(t)$.

This is called reciprocal mixing [1]. It can be a serious problem for both upconverters and downconverters, because it desensitizes the receiver and degrades the transmitted signal integrity. The effect of reciprocal mixing can be reduced either by lowering the oscillator phase noise or increasing the signal spacing in the frequency domain. The latter approach is counterintuitive in the sense that spectral efficiency decreases. Because of the ever-increasing number of wireless devices, efficient use of the RF spectrum is highly desired to accommodate as many wireless devices as possible. Therefore the reduction of the phase noise of the LO should be pursued fervently.

1.2.2 OFDM and Phase Noise

The Orthogonal Frequency Division Multiplexing (OFDM) modulation scheme employed in IEEE 802.11a and HiPERLAN Type 2 standards utilizes 52 sub-carriers per channel. Each channel is 20MHz wide and sub-carrier spacing (Δf) is 312.5kHz. Both standards support Binary Phase Shift Keying (BPSK), Quadrature Phase Shift Keying (QPSK), 16-bit Quadrature Amplitude Modulation (QAM), and 64-bit QAM [2], [3].

For example, when 64-bit QAM is selected for the maximum bit rate of 54Mbits/s, adjacent sub-carriers can have a maximum of $20\log(7/1)\approx16.9$dB difference in their power levels as the maximum amplitude is 7 times the minimum. This is illustrated in the 64-bit QAM constellation diagram in Fig. 1.3.
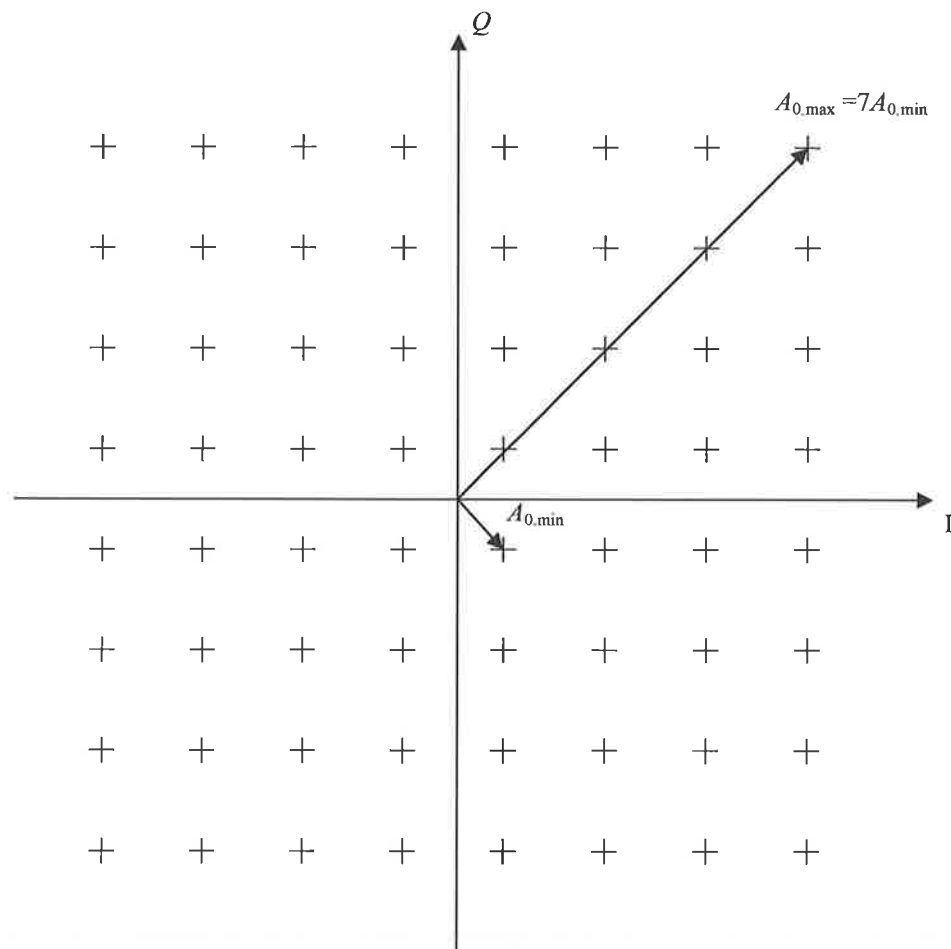
Fig. 1.3: Maximum to minimum amplitude ratio in 64-bit QAM constellation.

Due to the relatively close spacing and the large amplitude difference of sub-carriers in the 64-bit QAM OFDM signal, the system is highly susceptible to the phase noise of the LO. The LO phase noise components at different frequency offsets mix

with all 52 sub-carriers, and through reciprocal mixing, superimpose on top of the up or downconverted sub-carriers as interferences or noise. The interference resulting from the phase noise components less than Δf away from the carrier frequency mostly results in common phase error [4]. Since this is constant for all sub-carriers, and the result is a phase rotation of the constellation, it can be corrected by observing the 4 pilot tones among the 52 sub-carriers [4].

However, phase noise components at around or outside of Δf offset from the carrier result in inter-carrier interference (ICI), which has the appearance of random Gaussian noise [4]. ICI causes loss of orthogonality, resulting in increased symbol error rate (SER). Unfortunately, ICI cannot be corrected due to its random nature, unlike the common phase error [4]. Therefore, in order to minimize the SER and maximize the data throughput, the LO should exhibit low phase noise, especially at frequency offsets around and beyond Δf from the carrier frequency.

1.3 VOLTAGE CONTROLLED OSCILLATORS

A Voltage Controlled Oscillator (VCO) is a circuit module used in a system whose oscillating output frequency is monotonically determined by its input voltage over a finite range. The frequency control signal is in the form of electric potential, and hence the name VCO. A VCO is a very popular choice for the implementation of the LO in a wireless communication system. A typical frequency tuning curve of a VCO is shown in Fig. 1.4.

A VCO is usually used in a phase-locked loop (PLL) rather than on its own to continually correct for its output phase error accumulated over time, and also to be able to tune the VCO to a desired frequency of oscillation.

High performance wireless communication systems often demand a more stringent set of requirements on the VCOs than digital processors. This is because performance of wireless communication systems depends on the spectral purity of signals transmitted or received, and this purity is directly related to the spectral purity of the VCOs used, which is illustrated in the previous section.
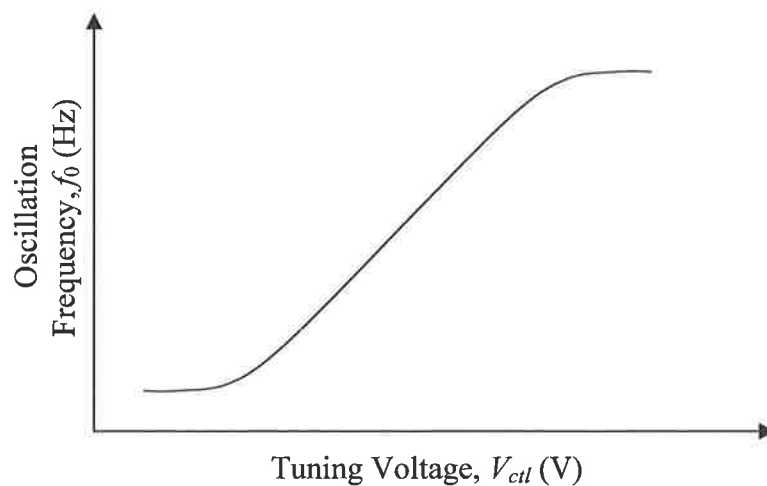
Fig. 1.4: Typical frequency tuning curve of a VCO.

1.3.1 Monolithic CMOS VCOs

Higher levels of integration help to reduce the system production cost, especially when a mass production is needed. This is how VLSI technology overtook discrete component implementations of digital circuits in the past.

As mentioned in the first section, the SOC technology of the modern processes have given designers the ability to integrate a complete or a near complete wireless communication system on a single chip. Monolithic implementation of a VCO along with other RF circuit modules using the SOC technology, without having to compromise the specifications, is highly desirable to lower the production cost of the system.

Complementary-Metal-Oxide-Semiconductor (CMOS) technology is the cheapest brew of VLSI technology available nowadays, and modern CMOS technologies can be used to realize SOC. Therefore, CMOS is the choice of technology for this work despite some difficulties it posses for implementation of high performance analog/RF circuits such as the VCO.

Historically the primary driving forces behind the CMOS industry have been digital VLSI circuits. The majority of CMOS processes have been optimized to implement digital circuits, where all transistors are considered as switches. Speed, size, yield and power dissipation are the prime interests for digital designers. For analog/RF designers however, noise, process variation, gain, linearity, dynamic range, and individual device characteristics are considered equal, if not more important.

Analog/RF circuits make use of on-chip passive devices much more extensively than the digital circuits. Often detailed characterizations of passive elements are not

readily available to designers. Although many modern digital CMOS processes do provide some support for analog/RF circuit designers, the level of support is considered second priority. This makes it even more difficult to design high quality analog/RF circuits in CMOS technology.

Despite the disadvantages of CMOS processes for analog/RF circuits, CMOS is often the choice of technology for many SOC solutions. Their mass productivity at low cost is one of the best selling points. Another attractive aspect of CMOS is their natural ability to integrate high quality digital circuits on the same chip, that work with the analog/RF circuits. This provides the basis for a complete system-on-chip solution, and drastically reduces the cost of the system due to the high level of integration.

Most of analog/RF circuit modules such as amplifiers, mixers, and filters can be integrated relatively easily. Exceptions to this would be circuits that require very large passive components, such as an LP filter with very low cutoff frequency (often used as the loop filter in a PLL), or circuits that require materials that are not available on-chip, such as the surface acoustic wave (SAW) filters that provide excellent frequency selectivity. Some high gain PAs have also proven to be difficult to implement in CMOS due to the insufficient gain of CMOS transistors for the intended application.

A VCO is easy to implement in a CMOS process. There is nothing fundamentally difficult about generating oscillation at the frequency of interest as long as the transistors are sufficiently fast. However, implementing a low-noise, low-power VCO in a CMOS process is a very challenging task. This is because most CMOS processes are optimized with digital circuits in mind and not as much consideration is given for a low-noise operation, critical to the VCO phase noise performance. Therefore, it is left to designers to work around the problems, and the monolithic implementation

of VCOs in CMOS processes has become a very active research area over the past few decades.

Nonetheless, not every VCO known to exist could easily be integrated cost effectively. For example, various cavity, dielectric or SAW resonators require their sizes to be of the order of half-wavelength of the frequency under interest. For 5GHz operation, a half-wavelength is around 30mm in free space. Even with a help of a dielectric to slow down the speed of propagation by the square root of the relative dielectric constant, the required geometry of the resonator would be still too large for a compact integration. Furthermore, use of non-standard materials or processing steps increases the cost of wafer production. For example, cavity resonators would require extra processing steps such as micromachining to create the cavity and metallization of the internal walls. Integration of physical resonator structures would become feasible once the frequency of operation exceeds 100GHz or more [5], unless chip area efficiency or cost is considered unimportant [6].

Monolithic VCOs in CMOS processes that have proven to be area efficient, and cost effective, are digital ring oscillators and inductor-capacitor (*LC*) tuned circuit based oscillators [7]-[12]. Ring oscillators are often used as clock signal generators in digital circuits or in communication systems with relatively relaxed clock jitter or phase noise requirements [8], [11], [12]. Although a typical ring oscillator features relatively large tuning range and smaller chip area compared to tuned circuit based oscillators, in general they cannot be used for high performance communication applications, where system performance depends on the quality of the LO signal. On the other hand, especially for microwave frequencies, the *LC* tuned circuit based oscillators are superior

in terms of phase noise performance, and widely used in high performance wireless communication systems [9], [14], [15].

1.3.2 Current Monolithic VCO Performances

As mentioned in the previous section, VCOs used in high performance wireless communication systems are of the *LC* tuned circuit type. Table 1.1 shows a list of high performance multigigahertz monolithic VCOs reported in the literature to date. It should be noted that the list is not limited to CMOS VCOs, but includes VCOs from other competing technologies such as bipolar technology.

While the phase noise values cannot be directly compared, the figure-of-merit (FOM) should give a rough indication as to how they compare one another. It is clear from Table 1.1 that in general, the *LC* tuned oscillators have better phase noise performance than the ring oscillators listed at the end of the table.

Table 1.1: Comparison of monolithically implemented modern VCOs.

Reference	Process Technology	f_0 (MHz)	Tuning Range (MHz)	P_{DC} (mW)	Phase Noise (dBc/Hz @1MHz)	FOM (dBc/Hz)
[26]	0.25μm CMOS	3945	350	4.08	−99.2	−165.1
[16]	0.5μm BiCMOS	4900	310	57.2	−107.0	−163.2
[26]	0.35μm CMOS	4887	500	9.00	−107.3	−171.5
[17]	Si Bipolar	5765	350	255	−110.0	−161.2
[18]	0.12μm CMOS	3980	1060	1.50	−113.0	−183.2
[17]	SiGe HBT	4765	330	132	−114.0	−166.4
[19]	SiGe HBT	3910	350	17.5	−114.0	−173.4
[20]	0.13μm SOI CMOS	5612	2600	2.50	−114.5	−185.5

[21]	0.35μm BiCMOS	4700	1000	25.0	−115.5	−174.9
[10]	0.25μm CMOS	5462	285	6.90	−116.0	−182.4
[22]	0.25μm CMOS	5230	310	7.05	−116.5	−182.4
[23]	0.25μm CMOS	4000	990	18.8	−117.0	−176.3
[24]	0.25μm CMOS	5000	1100	7.25	−117.0	−182.4
[22]	0.25μm CMOS	5350	354	7.05	−117.0	−183.1
[25]	0.25μm CMOS	4600	230	9.40	−118.1	−181.6
[15]	0.5μm BiCMOS	4405	620	21.6	−119.0	−178.5
[17]	SiGe HBT	4765	270	32.0	−120.0	−178.5
[27]	0.25μm CMOS	4880	780	21.9	−124.5	−184.9
*[28]	0.6μm BiCMOS	2200	100	1.30	−75	−141
*[29]	0.5μm CMOS	2200	N/A	11.8	−94	−150
*[30]	0.25μm CMOS	4595	1470	40.0	−95.3	−153.3

* Ring oscillators

1.4 OBJECTIVES

The ultimate goal of this thesis is to develop a systematic way to design and produce high performance monolithic CMOS VCOs to use in modern wireless front-end chipsets. High performance in the context of this thesis is defined as reliable, high frequency, low cost, low power, low noise, and temperature/process variation tolerant.

In general, there are four topics presented in this research work. First, existing VCO phase noise theories are to be reviewed. Their properties and usefulness in predicting the phase noise of a VCO are to be discussed. In addition, the limitations of some of the modern computer aided design (CAD) tools in predicting the VCO phase noise will be discussed.

Second, the workings of various differential *LC* tuned VCO topologies are to be thoroughly investigated. Some of the common misunderstandings of cross-coupled *LC* tuned oscillators found in the literature are addressed. This includes the commonly accepted oscillation amplitude expressions, the so-called 'voltage-limited region' of a VCO bias region, and the topological superiority of the complementary topology over other topologies often claimed in the literature.

Third, a set of optimization techniques is to be developed to design the best performing VCO realizable for a given process technology, die area, and power budget. A monolithic planar spiral inductor optimization technique, efficient tradeoff between power and noise via *L/C* ratio scaling, appropriate sizing of the cross-coupled transistors, and a low-power, low-noise current biasing technique are among the VCO optimization techniques to be developed.

Lastly, the VCO optimization techniques developed are to be tested and validated by fabricating a number of VCOs and analyzing their measurement results. Also, the performances of these VCOs are to be compared against the leading monolithic VCO designs reported in the literature. That is deemed to be the only reliable and accurate way to prove the effectiveness of the optimization techniques developed in this research work.

1.5 SCOPES

The type of oscillators studied in this thesis is cross-coupled *LC* tuned negative conductance oscillator with differential outputs.

Fabrication technologies used are a Silicon-On-Insulator (SOI) CMOS process and a bulk silicon substrate CMOS process.

VCO topologies covered include, N-type Metal Oxide Semiconductor (NMOS) only topology, complementary topology, where both cross-coupled NMOS and P-type Metal Oxide Semiconductor (PMOS) devices are used in complementary fashion, and other variants of the two aforementioned topologies.

IEEE 802.11b/g

2.412GHz   2.484GHz f

(a)

HiPERLAN II

IEEE 802.11a   HiPERLAN II   IEEE 802.11a

5.15GHz   5.35GHz   5.47 GHz   5.725 GHz   5.825GHz f

(b)

HiPERLINK

17.1GHz   17.3GHz f

(c)
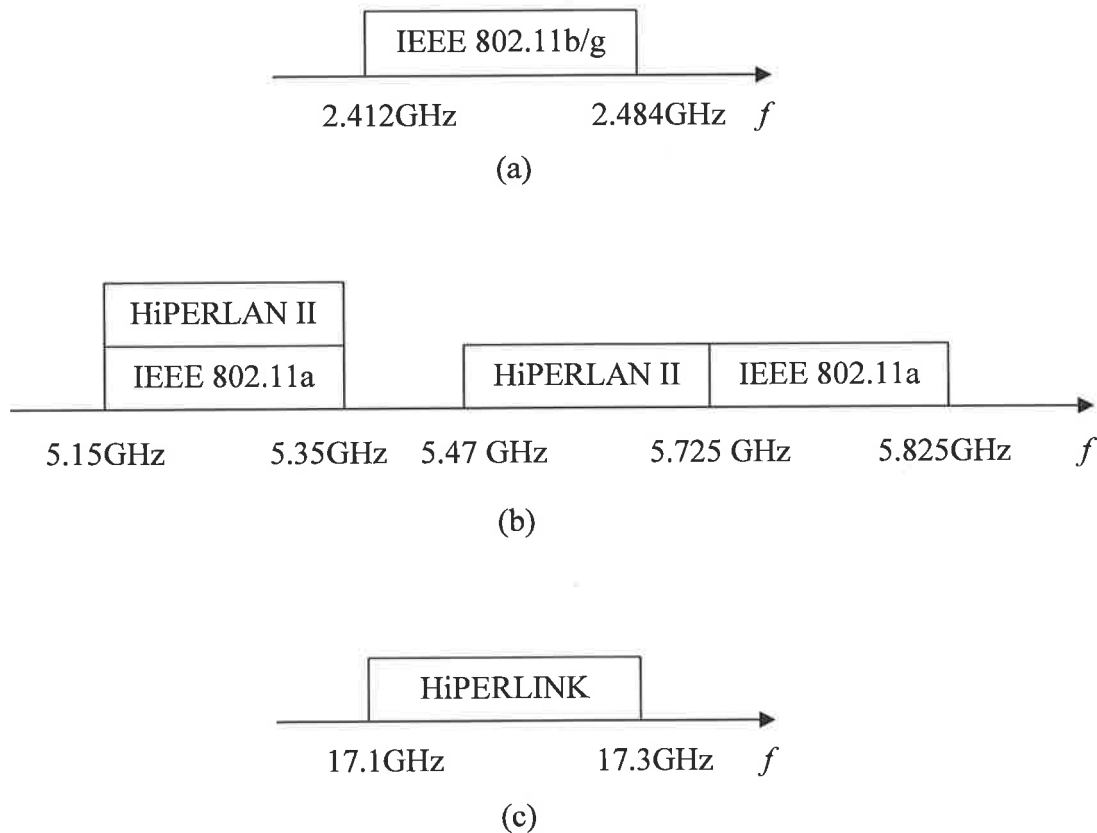
Fig. 1.5: Frequency bands allocations for (a) IEEE 802.11b/g, (b) IEEE 802.11a and HiPERLAN II, and (c) HiPERLINK wireless communication standards.

Target applications for VCOs studied in this thesis include wireless communication systems operating with the IEEE 802.11b/g or IEEE 802.11a or High Performance Radio Local Area Network Type 2 (HiPERLAN II) or High Performance

Radio Link (HiPERLINK) standards. Their operating frequency ranges from 2.412GHz to 2.484GHz for IEEE 802.11b/g standards, 5.15GHz to 5.825GHz for IEEE 802.11a and HiPERLAN II standards, and 17.1GHz to 17.3GHz for HiPERLINK standard [2], [3], [13], [32]. Fig. 1.5 shows spectrum allocations for the three standards.

1.6 MAJOR CONTRIBUTIONS

The VCO optimization techniques newly developed in this research work allow for the design of the best performing monolithic VCO for a given CMOS process technology, power consumption, and chip area. Thorough understanding of the cross-coupled LC tuned VCOs acquired in Chapter 2 and 3 lead to the development of a number of new optimization techniques for monolithic CMOS VCOs in Chapter 4. The techniques are applied to nine experimental VCOs presented in Chapter 5 and 6 to verify the effectiveness of the techniques. The tenth VCO presented in Chapter 6 is an industrial quality, high performance, CMOS VCO designed with the new optimization techniques. This VCO outperforms all VCOs listed in Table 1.1, and it is a tangible proof that the newly developed VCO optimization techniques have advanced the performance barrier of modern monolithic CMOS VCOs.

The following list summarizes the major contributions made by this thesis.

1) Commonly used linear oscillation amplitude estimation equations for cross-coupled LC tuned oscillators are proven to be largely in error (section 3.2.1).

2) The voltage-limited region frequently and unsuspectingly mentioned in the literature is proven to be nonexistent for cross-coupled *LC* tuned oscillators (section 3.2.1).

3) Topological superiority of the complementary topology over NMOS-only topology claimed in the literature is proven to be misleading (section 3.2.2).

4) A new geometric optimization technique for monolithic planar spiral inductors is developed (section 4.3).

5) A new and efficient tradeoff technique that involves a tradeoff between power consumption and phase noise performance through *L/C* ratio scaling is developed (section 4.4).

6) A new cross-coupled transistor size optimization technique is developed (section 4.5).

7) A new low-power, low-noise VCO current biasing technique is implemented and tested (section 4.6.2).

8) A new accurate RF oscillation amplitude detector is devised and tested (section 6.4).

1.7 THESIS ORGANIZATION

The thesis consists of six chapters. Chapter 1 has described the motive and the objectives of this research work, followed by the scope of the work, list of major contributions and the organization of the thesis.

Chapter 2 reviews two different VCO phase noise theories from the literature, and discusses their validity, accuracy, and limitations. Also, the limitations of modern CAD tools in estimating phase noise performance are discussed.

Chapter 3 studies various differential LC tuned oscillator topologies. The workings of cross-coupled oscillators are thoroughly investigated and, through this process, a better understanding on how the oscillation amplitude can be determined is acquired. Also, some common misunderstandings associated with cross-coupled oscillators frequently described in the literature are addressed.

Then various frequency-tuning methods available in modern CMOS processes are investigated.

After that, noise sources that contribute to the VCO phase noise are identified. Also, the important flicker noise upconversion processes are investigated. Understandings acquired from these investigations provide solid grounds for the development of the VCO optimization techniques described in Chapter 4.

Chapter 4 develops various VCO optimization techniques to assist design of high performance VCOs. A monolithic planar spiral inductor is identified as the most cost effective way to implement the inductance required by a tuned circuit. Also, a new geometric optimization technique has been developed for the implementation of the highest quality inductors realizable for a given area budget and process technology.

After that, a technique that efficiently trades increased power consumption for improved phase noise performance through L/C ratio scaling is developed. Also, an optimal cross-coupled transistor sizing technique is developed.

A new low-power, low-noise VCO current biasing technique has been developed to reduce the power consumption in the bias circuit while not compromising the phase noise performance.

Chapter 5 presents eight experimental VCOs, designed and fabricated using a Silicon-On-Insulator (SOI) CMOS process technology. Of these, two are designed to operate at 17GHz and the rest at 5GHz.

The various ideas developed in Chapter 3 and Chapter 4, namely the multi layer inductor effects, *L/C* ratio scaling, switched capacitor bank feasibility, topological advantages and the adequacy of the process technology used are tested and validated.

Chapter 6 presents one experimental and one industrial quality 5GHz VCOs. The experimental VCO is aimed to push the boundary of the phase noise performance of monolithic 5GHz VCOs and demonstrates the feasibility of integrating 2a VCO into a high performance Access Point (AP) quality radio front-end chip.

The industrial quality VCO is designed with a stringent set of specifications to meet the requirements of a monolithic high performance CMOS VCO needed for the high performance dual-band wireless AP equipped product lines of Cisco Systems.

The performances of some of the VCOs developed in this research work are compared against other state-of-the-art monolithic VCOs reported in the literature to date.

Lastly, Chapter 7 concludes the thesis and presents few recommendations for the future work.

Chapter 2

VCO PHASE NOISE

2.1 INTRODUCTION

Since the invention of the triode vacuum tube by Lee de Forest in 1907 [33], studies on electronic oscillators were commenced. Development of electronic oscillators was led by the wireless communications industry. The quality of oscillator was under constant demand for improvement. However, it was only over the past few decades or so, integrated oscillators have seen significant advance in phase noise theory and performance. This was to meet the often-stringent specifications of modulation techniques used in the explosively growing digital wireless communication industry of today.

As pointed out in the previous chapter, the data throughput of a wireless communication system depends on the spectral purity of the LO. Ability to estimate the phase noise of an oscillator allows designers to predict achievable SER or data throughput of the system and estimate its overall performance.

An accurate and reliable way of estimating the phase noise of a VCO to be integrated in the system is to actually fabricate a prototype VCO and measure its

performance with a spectrum analyzer or phase noise measurement instrument set such as the EUROPTEST PN9000. The downsides of this approach are lengthy turn-around period of fabrication processes and high cost involved in producing the prototype.

Usually there are a number of circuit parameters affecting VCO noise performance. Circuit designers are able to optimize the circuit for optimal performance by experimenting with these parameters liberally. However, fabricating and measuring phase noise for every parameter change would be simply not be viable.

Fabrication of prototypes is a sensible design practice in many cases. However, the number of prototype fabrication runs should be minimized in order to lower development time and cost. Instead, maximum utilization of simulations and performance estimates based on theory should be practiced.

Over the years, researchers have derived different phase noise estimation theories and equations. Earlier phase noise analysis often over simplified practical oscillators to a simple linear time-invariant (LTI) system [34]-[36]. Limitations with this model were soon realized by many and replaced with a more sophisticated linear time-varying (LTV) model [9], [37], [38]. Investigation of nonlinear properties of practical oscillators have led to identification of upconversion or downconversion processes of noise in oscillators [9], [29], [37]-[44].

To help designers to estimate VCO performance from as early as the design stage, modern CAD tools such as SpectreRF from Cadence Design Systems are equipped with a sophisticated nonlinear phase noise simulator [45].

In this chapter, a brief description of oscillator phase noise is presented first. After that, the pros and cons of LTI and LTV models, and the limitations of modern SPICE circuit simulators are discussed.

2.2 PHASE NOISE

Due to the unavoidable noise present in every electronic circuit building blocks, output signal of a VCO is noisy like any real electrical signal. The spectral power density of an oscillator output consists of the carrier power mostly concentrated at the frequency of oscillation, and noise components spread out symmetrically about the carrier frequency as side skirts for small frequency offsets ($f_m \ll f_0$) as shown in Fig. 2.1.
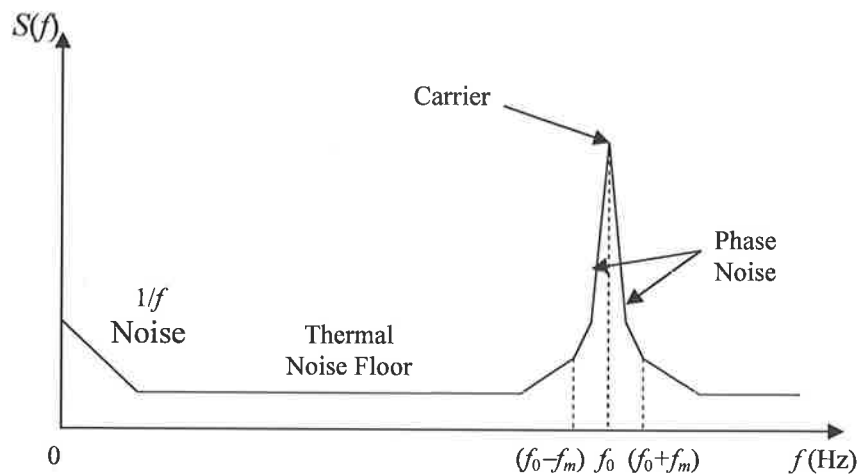
Fig. 2.1: Power spectral density of a VCO output.

An oscillator tuned at frequency f_0 can be represented by

$$s(t) = \left[A_0 + \alpha(t)\right]\cos\left[\omega_o t + \theta(t)\right] \tag{2.1}$$

where A_0 is the oscillation amplitude, and $\alpha(t)$ and $\theta(t)$ represent amplitude noise and phase noise respectively.

The equipartition theorem of thermodynamics states that each independent degree of freedom of a system in equilibrium at temperature T has a mean energy of $0.5kT$, where k is the Boltzmann constant [46]. Assuming oscillator amplitude and phase noise have the same thermal origin, the oscillator noise energy is equally divided between the two. However, because any practical oscillator has some sort of amplitude limiting mechanism built in to limit the amplitude from growing without a bound, the amplitude noise component at the output is suppressed ($\alpha(t) \rightarrow 0$).

On the other hand, there is no equivalent self-limiting mechanism that exists for the phase noise. Therefore, most practical VCOs exhibit only the phase noise component on their output [33].

Suppose a amplitude limited carrier is frequency modulated by a sine wave with frequency f_m. Then (2.1) is then written as

$$s(t) = A_0 \cos\left(\omega_0 t + \theta_p \sin \omega_m t\right) \tag{2.2}$$

where $\theta_p = \Delta f / f_m$ is the peak phase deviation. (2.2) expands to

$$s(t) = A_0\left[\cos(\omega_0 t)\cos\left(\theta_p \sin \omega_m t\right) - \sin(\omega_0 t)\sin\left(\theta_p \sin \omega_m t\right)\right] \tag{2.3}$$

For the peak phase deviation or θ_p much less than 1 ($\theta_p \ll 1$),

$$\cos\left(\theta_p \sin \omega_m t\right) \approx 1 \tag{2.4}$$

and

$$\sin\left(\theta_p \sin \omega_m t\right) \approx \theta_p \sin \omega_m t \tag{2.5}$$

Therefore, $s(t)$ can be written as

$$s(t) = A\left[\cos(\omega_o t) - \sin(\omega_o t)\theta_p \sin\omega_m t\right]$$
$$= A\left\{\cos(\omega_o t) - \frac{\theta_p}{2}\left[\cos(\omega_o + \omega_m)t - \cos(\omega_o - \omega_m)t\right]\right\} \quad (2.6)$$

This means, any small phase variation with frequency f_m and peak amplitude θ_p results in two frequency components on both sides of the carrier with an equal magnitude of $\theta_p/2$ and frequency offset of f_m from the carrier. This is why the phase noise appears symmetrically about the frequency of oscillation for small frequency offsets [47].

Phase noise of an oscillator ($\mathcal{L}\{f_m\}$) is most commonly represented as a ratio of single sideband (SSB) oscillator noise power at f_m offset from the carrier in 1Hz bandwidth to the total oscillator carrier power [48]. The unit is given in dBc/Hz, meaning the noise is in dB below the carrier per Hz of bandwidth. Also, because phase noise is a measure of noise power at a given frequency offset from the carrier, stating a phase noise of an oscillator must accompany the offset frequency where the measurement is made.

2.3 LINEAR OSCILLATORS

In 1966, D. B. Leeson published the first generation phase noise model of *LC* tuned feedback oscillators. This was a heuristic derivation of short-term stability or phase noise behavior of oscillators without formal proof [34]. Leeson's phase noise equation acknowledged the –30dB/decade and –20dB/decade slopes and flat regions in

single-sided (SS) oscillator output power spectral density (PSD) when plotted against

the offset frequency, ω_m from the carrier frequency, ω_0 as illustrated in Fig. 2.2.
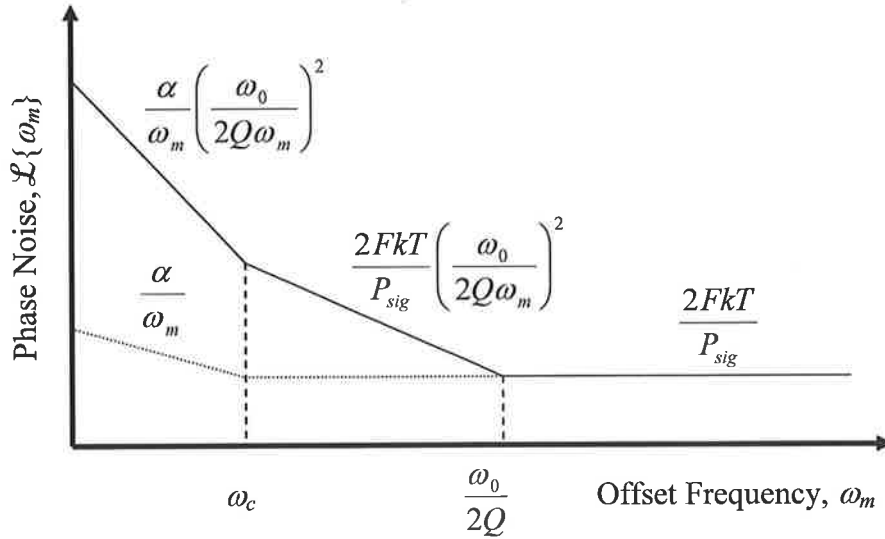
Fig. 2.2: Phase noise plot of a typical electronic oscillator.

$$\mathcal{L}\{\omega_m\} = \left(\frac{\alpha}{\omega_m} + \frac{2FkT}{P_{sig}} \right) \left[\left(\frac{\omega_0}{2Q\omega_m} \right)^2 + 1 \right]$$

$$= \frac{\alpha}{\omega_m} \left(\frac{\omega_0}{2Q\omega_m} \right)^2 + \frac{2FkT}{P_{sig}} \left(\frac{\omega_0}{2Q\omega_m} \right)^2 + \frac{\alpha}{\omega_m} + \frac{2FkT}{P_{sig}} \qquad (2.7)$$

In Leeson's equation (2.7), k is the Boltzmann's constant, T is absolute

temperature, Q is the loaded quality factor of the resonator, F is an empirical noise

factor of the oscillator, α is another empirical parameter 1that joins the ω^{-3} region to the

ω^{-2} region of the phase noise plot at ω_c, which is the flicker noise corner frequency of

the amplifier, P_{sig} is the average power of oscillation, and $\omega_0/(2Q)$ is the half-bandwidth

or the 3dB attenuation frequency offset of the resonator.

Leeson's model qualitatively describes the shape of phase noise close to the

carrier. It looks as if the flicker noise component, $\left(\dfrac{\alpha}{\omega_m}\right)$ and the white noise component,

$\left(\dfrac{2FkT}{P_{sig}}\right)$ of oscillator noise sources are given additional -20dB/decade slope,

$\left(\dfrac{\omega_0}{2Q\omega_m}\right)^2$ within the pass-band, $\left(\dfrac{\omega_0}{2Q}\right)$ of the resonator. The empirical fitting

parameter F determines the vertical displacement of the phase noise curves based on

actual measurement of the phase noise in the -20dB/decade slope region.

Although Leeson's equation acknowledges the appearance of flicker noise near

the carrier, no explanation was provided as to how this low frequency noise was

upconverted to the high frequencies of oscillation.

2.3.1 Linear *LC* Tuned Oscillator Analysis

Others [35], [49], [50] have reproduced Leeson's equation in an attempt to

mathematically estimate the noise factor, F. In their analyses, the phase noise

component resulting from upconversion of flicker noise was considered not as

important since it often appeared with very small offset frequency. Instead, emphases

were given on the prediction of F that determined the vertical displacement of the $-$

20dB/decade slope, which was often the dominant phase noise component in the output

phase noise PSD plot.

The linear parallel *RLC* circuit view of an *LC* tuned oscillator is the starting point in the linear oscillator analysis. Fig. 2.3 shows a simplified linear *LC* tuned oscillator circuit model.

In Fig. 2.3, a resonant circuit is formed by a parallel combination of an ideal *L* and *C*. *R* is the equivalent parallel resistance representing losses associated with the passive *LC* resonator or tank. In order to compensate for losses in the lossy resonator and sustain continuous oscillation, −*R* is added in parallel to the circuit to cancel the lossy term *R*. This negative resistance is assumed to be a noiseless and linear transconductor.
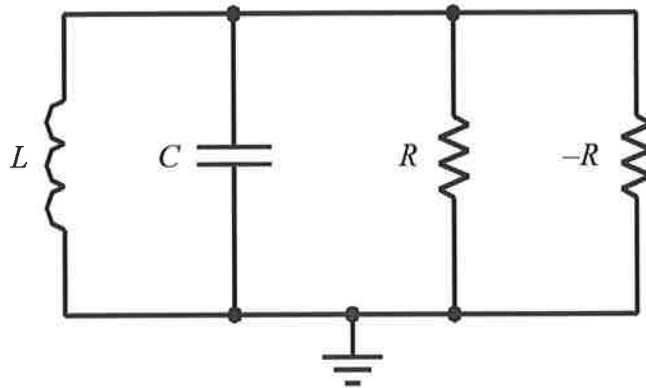
Fig. 2.3: Simple negative resistance *LC* tuned oscillator.

A current-to-voltage noise transfer function associated with above circuit after linearization around the resonant frequency, $\omega_0 + \omega_m$ is given as

$$|H(\omega_0 + \omega_m)|^2 \approx \frac{1}{4(\omega_0 C)^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \tag{2.8}$$

where $\omega_m \ll \omega_0$ [35]. The resulting output noise for a thermally induced noise current in *R* equals to

$$S_v(\omega_0 + \omega_m) = \left|H(\omega_0 + \omega_m)\right|^2 S_i(\omega_0 + \omega_m)$$

$$= \frac{kTR}{Q^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \qquad (2.9)$$

where the noise current $S_i(\omega_0 + \omega_m) = 4kT/R$, and the resonator quality factor, $Q = R\omega_0 C$.

As mentioned in section 2.2, noise of an oscillator is given as the noise power density below the carrier power at a certain frequency offset. Therefore, (2.9) is divided by the oscillator power, $A_0^2/2$ to give the oscillator noise equation (2.10).

$$\mathcal{L}\{\omega_m\} = \frac{8kTR}{A_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \qquad (2.10)$$

This equation is only valid for $\omega_m \ll \omega_0$, where the linearization of the transfer function $|H(\omega)|^2$ is valid. Note that this equation is a factor of 2 larger than the part of Leeson's equation that represents –20dB/decade region, if the noise factor in (2.7) is assumed to be 1 or the amplifier is assumed to be noiseless. This discrepancy between (2.7) and (2.10) is attributed to the fact that above simple linear analysis did not distinguish the phase noise from the amplitude noise. If the loss-compensating active device in the oscillator were purely linear, there would be just as much amplitude noise as the phase noise, and above analysis would be valid. In other words, if the negative resistance perfectly cancelled out the lossy component R, the circuit would be left with pure L and C, resulting in unbounded amplitude and phase responses. Perturbations introduced would therefore accumulate indefinitely [45].

However, all practical oscillators have some sort of amplitude limiting mechanism in the circuit. Oscillation amplitude is often controlled by the amount of bias current and is ultimately limited by the supply voltage, V_{DD}. The fact that amplitude is limited by some circuit parameter implies the amplification is compressive at the

oscillation amplitude and prevents it from growing larger. This compressive nature of the amplifier indicates nonlinearity. Hence, all practical oscillators are nonlinear [45].

The nonlinearity in oscillators basically prevents accumulation of amplitude uncertainty in oscillation. However, there exists no equivalent limiting mechanism for phase perturbation. Therefore, phase perturbation accumulates in an unbounded fashion. This makes oscillator noise close to the carrier virtually all phase-related noise, not amplitude-related noise. Oscillator noise equation given in (2.10) assumes the presence of both amplitude and phase noise. However, since the amplitude noise and phase noise are two independent degrees of freedom, and the amplitude noise is suppressed by the nonlinearity, the resulting phase noise for a real oscillator should be halved, resulting in (2.11) [43], [45], [51].

$$\mathcal{L}\{\omega_m\} = \frac{4kTR}{A_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \qquad (2.11)$$

Although, practical oscillators are conceived as nonlinear, owing to the simplicity of the LTI system, this model was used to estimate F of various LC tuned oscillators over the past decade. The linearity was assumed to be approximately ensured by preventing amplifiers from saturating [49], [50], or by using automatic gain control (AGC) [35].

When a noisy active element is employed to compensate for losses in the tank, as is the case for all real oscillators, the current noise source associated with the active device is added in parallel with the tank resistance R. In a CMOS process, the active element is a FET. The FET channel noise current is given as $4kT\gamma g_{ds0}$, where γ is the transistor channel noise factor, and g_{ds0} is the drain-source conductance at zero drain-source bias potential [33]. This is similar to the noise current of a resistor, except it has

an additional noise factor γ and $1/R$ is replaced with g_{ds0}. Taking the transistor channel

noise into account, the input noise current in (2.9) becomes $S_i(\omega_0+\omega_m)=4kT(1+\gamma)/R$ and

the resulting phase noise equation is

$$\mathcal{L}\{\omega_m\} = \frac{4kTR(1+\gamma)}{A_0^2}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \qquad (2.12)$$

By comparing (2.12) and the second term in (2.7), F is found as $1+\gamma$. $F=1+\gamma$ is

referred to as the fundamental minimum noise factor of an LC tuned oscillator [43], [44],

[50], [52], [53],

The strength of this linear analysis is in the derivation of the phase noise

dependency close to the carrier, which is given as $\left(\dfrac{\omega_0}{2Q\omega_m}\right)^2$. It implies oscillator noise

increases linearly with the square of oscillation frequency, and falls linearly with the

square of Q at a given frequency offset. Since ω_0 is an application specific parameter,

designers should concentrate on increasing Q as high as possible to lower the phase

noise. Although the LTI model lacks quantitative accuracy, it is qualitatively correct in

the –20dB/decade region of phase noise.

2.3.2 Ring Oscillator Analysis

A ring oscillator is formed by connecting a multiple number of inverters in a

closed loop or ring such that the sum of phase delay is an integer multiple of 2π.

Although a ring oscillator lacks a resonator, their phase noise spectrum shape resembles

that of an oscillator with a resonator. This is because the active elements used in ring

oscillators have the same kind of noise components as in tuned oscillators, namely the

thermal noise and the flicker noise. Also, a ring oscillator like any other oscillators

worth investigating has the frequency restoring force against perturbations and is able to

concentrate the signal power within a very narrow frequency band centered at

oscillation frequency. This frequency restoring force shapes the noise around the

frequency of oscillation.

Similar to the linear LC tuned oscillator case, where the LTI analysis yielded the

phase noise expression describing the shaping of the thermal noise around the carrier,

the LTI analysis for ring oscillators reported in [29] successfully describes the shaping

of additive thermal noise around the carrier. With a different set of arguments for the

definition of Q, and a similar linearization approximation, the resulting current-to-

voltage transfer function for a ring oscillator (2.13) is identical to that of an LC tuned

oscillator.

$$|H(\omega_0 + \omega_m)|^2 \approx \frac{1}{4Q^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \qquad (2.13)$$

where the loaded Q for a ring oscillator is defined as

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA(\omega)}{d\omega}\right)^2 + \left(\frac{d\Phi(\omega)}{d\omega}\right)^2} \qquad (2.14)$$

where $A(\omega)=|H(\omega)|$ and $\Phi(\omega)=\angle H(\omega)$.

The ring oscillator Q evaluated in [29], using (2.14) is around 1.3 for a three-

stage ring oscillator. Compared to the relatively high Q of 5 or more often observed in

LC tuned oscillators, the ring oscillator suffers from low Q, because it dissipates all of

its stored energy over each cycle. Hence the relatively poor phase noise performance.

Therefore, ring oscillators are found only in the most noncritical applications, or inside a wide-band PLL that cleans up the noisy spectrum near the carrier [9].

2.3.3 Limitations of the LTI Model

Despite the simplicity in the LTI model, it does not capture the upconversion process of the low-frequency flicker noise that results in the -30dB/decade slope close to the carrier [29], [37], nor does it accurately estimation the practical value of F. Measured F is often larger than the theoretical minimum, $1+\gamma$ [43], [50]. Also, the assumption that the amplifier flicker noise corner frequency coincides with the corner frequency between the ω^{-3} and the ω^{-2} regions in the phase noise plot has no theoretical basis [37], [53], [54].

The neglect of the nonlinear effects is the most significant limitation of the LTI model. The phase noise predictive power of the LTI model diminishes rapidly with oscillator nonlinearity [9].

2.3.4 Figure of Merit

Various communication systems employ different oscillator designs with different circuit parameters implemented in different processes, because the frequency planning and required oscillator quality for each system is different. In order to compare the quality of each design, a figure of merit (FOM) needs to be defined. It is not

meaningful to merely compare the absolute values of the phase noise for every oscillator, due to wide spread of frequencies of oscillation, DC power consumption, and the offset frequencies where the phase noise was measured. However, it is possible to normalize aforementioned parameters for each oscillator, and compare the resulting figure of merit, using (2.15) [20], [50], [51], [55].

$$\text{FOM} = 10\log_{10}\left[\left(\frac{\omega_m}{\omega_0}\right)^2 P_{DC}\right] + \mathcal{L}\{\omega_m\} \qquad (2.15)$$

Here P_{DC} is given in milliwatts. This is the most widely used FOM expression given in dBc/Hz. It is only valid over the –20dB/decade region. This normalization of phase noise basically compares the loaded quality factor of the oscillators, the oscillator noise factors, and the power efficiencies between different VCO designs. The lower the FOM the better the design. However, in some cases, the inverse of the FOM is reported [44], [54]. In which case, the larger the FOM, the better the design.

Some argued that the tuning range of a VCO is a just as important circuit parameter and there should be another definition of FOM that incorporates tuning range [51]. However, unlike the loaded Q or the oscillator noise factor, the tuning range is not a direct measure of the quality of a resonator. Also, it is a very flexible parameter that depends on the tuning scheme used, which may not affect the resonator quality significantly [57]. Therefore, the FOM taking tuning range into account is not widely used.

2.4 NONLINEAR OSCILLATORS

All practical oscillators are intrinsically nonlinear because the oscillation amplitude can only be controlled by a nonlinear system [29], [45]. The degree of nonlinearity varies depending on the design and the operation bias condition. A weakly nonlinear *LC* tuned oscillator example in [36] estimates the error in phase noise between the linear model and the nonlinear model to be about 30%, which corresponds to just over 1dB difference in phase noise. However, this accuracy is only applicable to resonators with exceptionally high loaded *Q*, which require relatively small compensation from the nonlinear active devices to sustain oscillation. The off-chip resonator used in [36] had loaded *Q* of 140 at around 1GHz. Unfortunately, to date, such a high *Q* resonator has not been demonstrated monolithically in a CMOS process.

The consequences of strong nonlinearity of loss-compensating amplifiers in oscillators are:

- Oscillation amplitude is defined and the amplitude noise is suppressed [29], [43], [45].

- Low frequency flicker noise is upconverted to the frequency of oscillation [24], [35], [37], [38], [43]-[45], [50], [52], [58].

- White noise components around the harmonics of the oscillation frequency are downconverted to the frequency of oscillation, [37], [38], [40], [45], [50].

The empirical flicker noise expression of a FET in saturation is given as

$$S_{i_d^2, 1/f} = \frac{M g_m^2}{C_{ox}^2 WL} \frac{1}{f^\beta} \tag{2.16}$$

It contains the empirical parameter M. By comparing (2.16) to a physical flicker noise expression (2.17), M equates to $q^2 N_{ot}$, where q is the charge of electron and N_{ot} is oxide trap density in the channel [59].

$$S_{i_d^2, 1/f} = \frac{q^2 N_{ot} g_m^2}{C_{ox}^2 WL} \frac{1}{f} \qquad (2.17)$$

As technology scales down, the minimum transistor gate width, W and length, L scales down while the unit gate oxide capacitance C_{ox} scales up with thinning gate oxide. Designers may take advantage of increasing unit gate oxide capacitance by making transistor geometry larger than the minimum required to lower the overall flicker noise PSD. The oxide trap density on the other hand, does not necessarily scale with the process feature size but depends on the gate oxidation and subsequent implantation methods used for the process. In fact, in the deep-submicrometer regime, the conventional thermal gate oxide is replaced with nitrided oxide in order to provide sufficient device reliability. However, in doing so, it increases the oxide interface trap density and increases the flicker noise [60]. This increased trap density in conjunction with reduced gate area may worsen the device flicker noise in the deep-submicrometer CMOS processes [61]. Therefore, the flicker noise contribution to the VCO phase noise in the −30dB/decade region is gaining significance as processes scale and can no longer be neglected from the phase noise analysis in high performance systems.

The FET channel thermal noise is often given as $4kT \gamma g_{ds0}$. The value of noise factor γ is 2/3 for long channel devices [62]. For deep-submicrometer devices, this value of γ can increase considerably larger than the long channel estimate [33]. Although γ is considered constant in the long channel regime, in the short channel regime, γ is a function of V_{DS}, and V_{GS}. Varying V_{DS} or V_{GS} causes channel length modulation and that

affects the electrical length of the channel where the carrier velocity is lower than the saturation velocity. This effect becomes more pronounced as the physical channel length shrinks [63].

Depending on the bias condition, the typical value of γ can be around 2 or more in deep-submicrometer CMOS processes [33], [63]. Therefore, the thermal noise contribution from the active devices is larger than that from the passive resonator. This is easily seen from the theoretical minimum oscillator noise factor, $F=1+\gamma$ from the linear oscillator analysis. Furthermore, spectrum folding of thermal noise from the harmonics of the frequency of oscillation increases the contribution of active device thermal noise to the phase noise in the −20dB/decade region [37], [38], [40], [45], [50].

2.4.1 Linear Time-Varying Oscillator Model

In 1998, Hajimiri and Lee published a general theory of phase noise in electrical oscillators. Their work acknowledged the true periodically time-varying nature of all electrical oscillators. The processes of the flicker noise upconversion and the white noise downconversion were also explained [9], [37].

The transfer function of a purely linear LC circuit looks similar to that of an oscillator. However, the difference is that an LC circuit is LTI whereas a practical oscillator is linear time-varying (LTV). Oscillators are intrinsically time-varying because the loss-compensating amplifier gain varies over a full cycle in a way that its gain is excessive during low amplitude parts of the cycle and compressive around the

peaks of amplitude. This is how a practical oscillator is able to maintain constant amplitude of oscillation. Hence, this property is generic [45].

Ref. [37] asserts that current-to-phase transfer function is practically linear for both *LC* oscillators and ring oscillators although the devices are nonlinear. However, this linear transfer function varies with time because the amplifier gain varies periodically with time. In order to mathematically describe this property, Hajimiri and Lee defined an impulse sensitivity function (ISF). It is a dimensionless, frequency- and amplitude-independent periodic function. ISF describes how much phase shift results from applying a unit impulse at a node of interest at a given instance in oscillation cycle. For example, a small current impulse injected across an *LC* resonator around the zero crossing of oscillation waveform resulted in a notable phase shift whereas the same current impulse injected around the peak of the waveform resulted in a very small or no phase shift as illustrated in Fig. 4 of [37].

As mentioned earlier, the current-to-phase transfer function is linear, although it is time-varying. However, the resulting phase shift from a single tone injection produces two equal side bands around the carrier as shown in Fig. 9 of [37]. This process is governed by the classical phase modulation (PM) process [56] and this is the nonlinear part of the current analysis. After all, frequency translation is a property of a nonlinear system.

For noise currents $i_n(t)=I_n\cos[(n\omega_0+\omega_m)t]$, where n is a non-negative integer, the resulting sideband noise power with respect to the carrier is given as

$$P_{SBC}(\omega_m) = \left(\frac{I_n c_n}{4q_{max}\omega_m}\right)^2 \tag{2.18}$$

where c_n are the Fourier coefficients of the ISF and q_{max} is the maximum charge displacement at the node under test. The sum of P_{SBC} resulting from the frequency conversion of the white noise components ($n=0, 1, 2,\ldots$) forms the -20dB/decade region in the phase noise plot, and is given as

$$\mathcal{L}\{\omega_m\} = \frac{\Gamma^2_{rms}}{q^2_{max}} \frac{\overline{i^2_n}/\Delta f}{4\omega^2_m} \qquad (2.19)$$

where Γ_{rms} is the root mean square of the ISF. Whereas the low noise component ($n=0$) upconverts to form the -30dB/decade region, and is given as

$$\mathcal{L}\{\omega_m\} = \frac{c^2_0}{q^2_{max}} \frac{\overline{i^2_n}/\Delta f}{8\omega^2_m} \frac{\omega_{1/f}}{\omega_m} \qquad (2.20)$$

where $\omega_{1/f}$ is the flicker noise corner frequency of the noise source. Equating (2.19) and (2.20), and solving for ω_m results in the corner frequency between the -30dB/decade and -20dB/decade regions as

$$\omega_{1/f^3} = \omega_m = \omega_{1/f} \cdot \frac{c^2_0}{2\Gamma^2_{rms}} \approx \omega_{1/f} \cdot \left(\frac{c_0}{c_1}\right)^2 \qquad (2.21)$$

The approximation in (2.21) is valid for ISF dominated by its fundamental harmonic ($2\Gamma^2_{rms} \approx c^2_1$). In other words, it is when the thermal noise contribution is dominated by the thermal noise around the frequency of oscillation [37]. However, this assumption is not always valid as some noise sources like the tail current bias transistor in a differential LC tuned oscillator has the ISF fundamental harmonic at twice the oscillation frequency [38]. In any case, since $2\Gamma^2_{rms}$ is larger than c^2_n for all value of n, ω_{1/f^3} is always lower than $\omega_{1/f}$ [9], [37].

From above analysis, it is apparent that devices with relatively large flicker noise such as submicrometer CMOS FETs does not necessarily mean poor − 30dB/decade phase noise performance. This region of phase noise can be lowered by lowering c_0 or the DC value of the ISF. Low DC value of ISF is ensured by the waveform symmetry [9], [37], [38].

In Ref. [37], the Leeson's LTI model is claimed as a special case of the LTV model when the Fourier coefficients of ISF are all zero except $c_1=1$. By replacing q_{max} and $\overline{i_n^2}\,/\,\Delta f$ with CA_0 and $4kT/R$ respectively, the LTV model is reduced to

$$\mathcal{L}\{\omega_m\} = \frac{1}{2}\frac{kT}{A_0^2}\frac{1}{R(\omega_0 C)^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \tag{2.22}$$

However, (2.22) is factor of 2 smaller than (2.11) when $Q=R\omega_0 C$ is recognized. Ref. [37] argues that the discrepancy is coming from the fact that (2.22) is lacking the amplitude noise. But so is (2.11). The actual reason for the discrepancy comes from the fact that this special case of LTV model is still a time-varying model whereas (2.11) is a result of a time-invariant model. By making $c_n=0$ for all n except for $c_1=1$, folding of noise components from the DC and the harmonics other than the fundamental are disregarded, but the noise-to-phase transfer function is still time varying. It simply means the ISF is made purely sinusoidal. The fact that only the thermal noise around the carrier is causing the phase noise in this case is the same as the LTI case. However, since the current-to-phase conversion gain is not constant but follows a sinusoidal pattern, the resulting phase noise in the LTV case is half as much. This is because the root-mean-square of a pure sign wave is half the amplitude. Therefore, the special case

of the LTV model mentioned in [37] does not represent the Leeson's LTI model, because of the time-varying property of the LTV model.

Continuing with the LTV analysis, when the cyclostationary nature of noise sources is taken into account, the ISF is replaced with effective ISF, Γ_{eff}. It is basically a product of Γ and α, where α is a deterministic periodic function that describes the amplitude modulation of the current noise source [37].

Γ_{eff} is often significantly different from Γ for LC tuned oscillators because the current dissipation of active devices is minimized around the zero crossings and maximized around the peaks of oscillation waveform. This property of an LC tuned oscillator lowers the effective ISF and results in lower phase noise contribution from the active elements. One the other hand, the Γ_{eff} for ring oscillators is almost identical to Γ as the current is maximum around the zero crossings and minimum around the peaks of oscillation waveform. This is another reason why ring oscillators in general are inferior to LC tuned oscillators [9], [37].

For the completeness of the subject, although different to Hajimiri and Lee's approach, [40] is another good reference on spectrum folding of noise from the DC and the harmonics for LC tuned oscillators in bipolar technology.

2.4.2 Phase Noise Simulator

Phase noise analysis is one of the most challenging and crucial analyses of the modern RF integrated circuit (RFIC) designs. Although, there exists hand-calculatable

closed form equations for phase noise of oscillators of various types, their phase noise predictive power diminishes quickly as the nonlinearity in the circuit grows [9].

Closed form equations taking time varying nature and nonlinearity into account such as the LTV model still requires evaluation of the ISF for every noise source in the circuit. Ref. [37] proposed three different methods of calculating the ISF. The most accurate method is by directly measuring the impulse response of the circuit at various instances of the oscillation cycle. This method would require a large number of simulation iterations and the accuracy of the resulting ISF is based on the accuracies of the time domain simulator and the circuit model. Fortunately, much of this tedious and complex task of calculating phase noise is automated in modern RF circuit simulators.

Some commercial simulators namely, Advanced Design Systems (ADS) of Agilent Technologies, Eldo RF of Mentor Graphics and SpectreRF of Cadence Design Systems allow for the simulation of VCO phase noise. ADS and Eldo RF calculate phase noise based on the technique called harmonic balance, and SpectreRF does it by using periodic steady-state analysis.

Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits. This technique is able to calculate frequency-domain voltages and currents, or directly calculate the steady-state spectral content of voltages or currents in the circuit. When calculating oscillator phase noise, the simulator uses an iterative process to find a set of nonzero steady-state solutions to model the nonlinearity, and then the harmonic balance search algorithm sweeps the operating frequency to find the oscillation frequency. The flicker noise component is neglected in the device model and therefore must be added explicitly in the schematic level to include its effects [65].

The periodic steady-state analysis employed by SpectreRF is a time-domain analysis. SpectreRF linearizes the circuit around the steady-state waveform to perform the small-signal analysis. Because of the time-varying nature of oscillators, multiple transfer functions are used in the analysis. It is much like how the LTV model calculates the phase noise. The difference is that SpectreRF performs the phase noise analysis on all noise sources in the circuit simultaneously and uses a collection of many piecewise polynomials rather than just a few sinusoids [45]. Unlike ADS or Eldo RF, SpectreRF makes use of the flicker noise model included in the BSIM3v3 MOS models, eliminating the need to add flicker noise sources explicitly. SpectreRF was the only phase noise simulator accessible over the duration of this work.

2.4.3 Limitations of Simulator

Even the state-of-the-art simulators powered by advanced mathematics, theory and efficient handling of system resources are eventually limited by the accuracy of the models they use. Although BSIM3 MOSFET models are widely used, they are considered relatively primitive and the model parameters are quasi-empirical [33].

Advantage of the BSIM3 model is in its simplicity. With it, a simulator can perform a complete chip level simulation with reasonable time, hardware resources and accuracy. Other more sophisticated SPICE MOSFET models would have exponentially increased the number of parameters and this would limit number of circuit components in a simulation due to the computing hardware limitations. Even if the hardware limitations are overcome by the use of advanced computing techniques such as

multithreading or 64-bit processors, the simulation output may not agree with the physical measurement. Finally, modern CMOS processes exhibit process variations of at least ±20%, which limits the required accuracy of simulation in any event. This is not the case for analog or RF circuits where increased accuracy could well be used.

LC tuned VCOs are sensitive to the capacitance variation in the process. Because the fundamental frequency of oscillation is determined by the self-resonant frequency of the *LC* tuned circuit, given as

$$\omega_0 = \frac{1}{\sqrt{LC}} \qquad (2.23)$$

±20% variation in capacitance would result in approximately ±10% variation in ω_0. This is often a serious problem in RF systems as they usually need high accuracy in frequency. VCOs would have to be designed with a much larger tuning range than required by the system, solely to compensate for the process variations.

The flicker noise affects only a handful of selected circuit modules. For example, the close-in phase noise of a VCO and the output of a mixer are affected by the flicker noise. Other circuits, especially digital circuits are relatively insensitive to the flicker noise. Therefore the characterization of device flicker noise in CMOS process has been a relatively low priority.

The flicker noise mainly depends on the oxide-silicon interface condition. The oxide trap density at the interface is affected by the type of oxidation process and subsequent implant processes used [60]. The oxide trap density is not a well-controlled process parameter even with the state-of-the-art CMOS processes. Its value and tolerance are not as well specified nor characterized as other electrical parameters such as the threshold voltage or the transconductance [66].

The flicker noise model used in BSIM3 is given as

$$S_{i_d^2, 1/f} = \frac{KF \cdot I_d^{AF}}{f^{EF} C_{ox} W L_{eff}} \tag{2.24}$$

where, I_d is the drain current, KF is the flicker noise coefficient, AF is the flicker noise exponent, EF is the flicker noise frequency exponent, and L_{eff} is the effective length of the transistor gate.

As the transistor transconductance, $g_m = \sqrt{2 C_{ox} \mu W I_d / L_{eff}}$ in saturation, the flicker noise PSD given in (2.17) approximates to

$$S_{i_d^2, 1/f} \approx \frac{q^2 \mu N_{ot} I_d}{C_{ox} L_{eff}^2} \frac{1}{f} \tag{2.25}$$

By comparing (2.25) with (2.24), KF equals to $q^2 \mu N_{ot}$, assuming $AF=1$, and $EF=1$. Although the oxide trap density (N_{ot}) is assumed to be constant in simulations, it is found to be a function of the gate voltage [66]. In practice, not only N_{ot} or KF are poorly controlled, but their variations in MOSFET are not modeled in the simulation. Therefore, the amount of upconverted flicker noise shown in a phase noise simulation must be interpreted with care.

Another limitation of SPICE simulators is that none of these simulators take the electromagnetic effects into account. Magnetic field around the inductor structure may couple to other surrounding conductors and cause undesired variation in the inductance or increased thermal loss. This is a real effect and can be very serious for monolithic implementation of passive structures, especially inductors and transformers. Simulating electromagnetic effects would involve extraction of the three dimensional structure of the circuit and its surroundings. Even if the three dimensional structure is available, due

to intensive matrix multiplications associated with field solvers, analyzable circuit size would be limited to simple inductor or transformer structures.

A 2.5 dimensional field solver Momentum as a part of ADS from Agilent does a reasonably good job in simulating electromagnetic circuits of arbitrary shape. ASITIC (Analysis and Simulation of Inductors and Transformers in Integrated Circuits) is another 2.5 dimensional field solver in the public domain [64]. Although there are some non-critical bugs in the software, it runs quickly and relatively easy to use.

2.5 CONCLUSIONS

The pros and cons of the LTI and the LTV models of VCOs have been discussed in this chapter. The simple LTI model allows a quick and rough estimate of the phase noise in the −20dB/decade region for *LC* tuned oscillators. While the closed form equation of the LTI model is qualitatively correct in the −20dB/decade region, the phase noise factor *F* is left as an empirical fitting parameter between the LTI theory and the actual measurement. Furthermore, the −30dB/decade region of the phase noise closer to the carrier is not explained by the simple LTI model. However, owing to its qualitative validity in the −20dB/decade region, a normalized FOM equation can be developed based on the LTI closed form equation, and is widely used to compare VCOs with different parameters. The validity of the FOM is limited to the −20dB/decade region and the VCO tuning range is not considered in the FOM calculation.

The LTV model is able to describe the VCO phase noise more accurately. Also, the oscillator type is not limited to the *LC* tuned oscillators. Although the phase noise

estimation with the LTV model would require a series of iterative simulations, its result is both qualitatively and quantitatively correct. The accuracy of the LTV model is limited only by the accuracy of the device models used in the simulations.

Most popular commercial CAD tools are now shipped with some sort of phase noise estimation tools, and they all recognize a VCO as an LTV system. They provide valuable indications as to how the phase noise changes with respect to certain circuit parameters in the VCO. Therefore they prove themselves to be very useful in optimization processes. However, although they may be the best phase estimation tools available to designers today, the device models are often not accurate enough for accurate estimation of the absolute phase noise values. Therefore phase noise simulation results must be taken as indications only.

Chapter 3

DIFFERENTIAL *LC* TUNED OSCILLATORS

3.1 INTRODUCTION

LO signals in high performance RF systems are often required in differential or quadrature (I/Q) format, depending on the transceiver architectures employed. Quadrature signals are used for systems providing high image rejection ratio such as the Weaver architecture [33], or direct conversion or low-IF architectures involving the QAM scheme as in the high-speed 5GHz WLAN applications. In the digital data communication domain, a half-rate data clock recovery (DCR) architecture employs I/Q signals to operate at half the frequency of incoming data stream [16].

Although the single-ended signal is the minimum required for heterodyne architectures working with IF frequencies, differential signals are often preferred for finer frequency selectivity due to their superiorities over single-ended counterparts. Differential signals offer better environmental noise immunity owing to the common-mode rejection property of differential circuits. Also, differential signals have better spectral purity due to the better linearity and dynamic range associated with differential circuits [67].

A differential signal can be derived from a single-ended source through use of a balun (BALanced to UNbalanced) transformer. For example, a RF signal received through a monopole antenna is single-ended. This signal is fed to a passive balun and converted to a differential signal before further processing. However, an LO signal is a locally generated signal and the designer has freedom to generate it differentially, taking advantage of differential circuits and avoid the use of a balun.

In this chapter, popular differential *LC* tuned oscillator topologies in CMOS technology are studied in section 3.2. In section 3.3, the frequency tuning methods of *LC* tuned VCOs are investigated. Section 3.4 identifies noise sources and discusses their contribution towards the phase noise in differential *LC* tuned oscillators. Details on quadrature signal generation is omitted since quadrature oscillators are often derived from quadratic coupling of two differential oscillators, or through frequency dividers, or by use of polyphase filters [16], [27], [55], [68].

3.2 CROSS-COUPLED OSCILLATORS

A cross-coupled FET pair is one of the major building blocks of a differential *LC* tuned oscillator. A NMOS cross-coupled pair is shown in Fig. 3.1(a) and its PMOS counterpart is shown in Fig. 3.1(b).

The role of a cross-coupled pair is to provide negative resistance to the parallel *LC* circuit, which is to be connected across the two output terminals, v_{out+} and v_{out-}. For the NMOS cross-coupled pair, since v_{out+} and v_{out-} are opposite in phase, when v_{out+} rises, v_{out-} is lowered and this reduces current entering through v_{out+}, creating negative

resistor like impedance at v_{out+}. On the other hand, when v_{out+} is lowered, v_{out-} rises, and current flowing through the left branch is increased. This again shows negative resistor like impedance at v_{out+}. Negative impedance looking into v_{out-} node can be explained likewise.
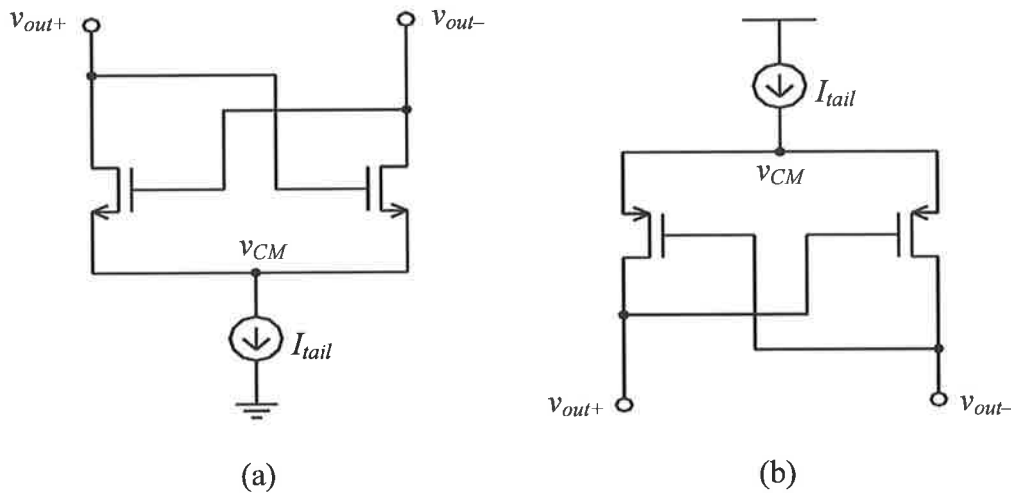
Fig. 3.1: (a) NMOS cross-coupled pair (b) PMOS cross-coupled pair.

As mentioned in the previous chapter, all practical VCOs contain one or more nonlinear active elements and they limit the oscillation amplitude. Ideally each transistor in a cross-coupled pair should provide constant negative resistance or conductance looking into its drain. The degree of nonlinearity depends on the amplitude of oscillation. For simplicity, only the NMOS cross-coupled pair is used as an example in the following analysis of the operation of a cross-coupled pair.

For now, let's assume that v_{CM} is well bypassed to AC ground so that the cross-coupled pair is biased at constant tail current (I_{tail}), however instantaneous current sunk by the transistor pair may deviate from it.

(a)

(b)

(c)
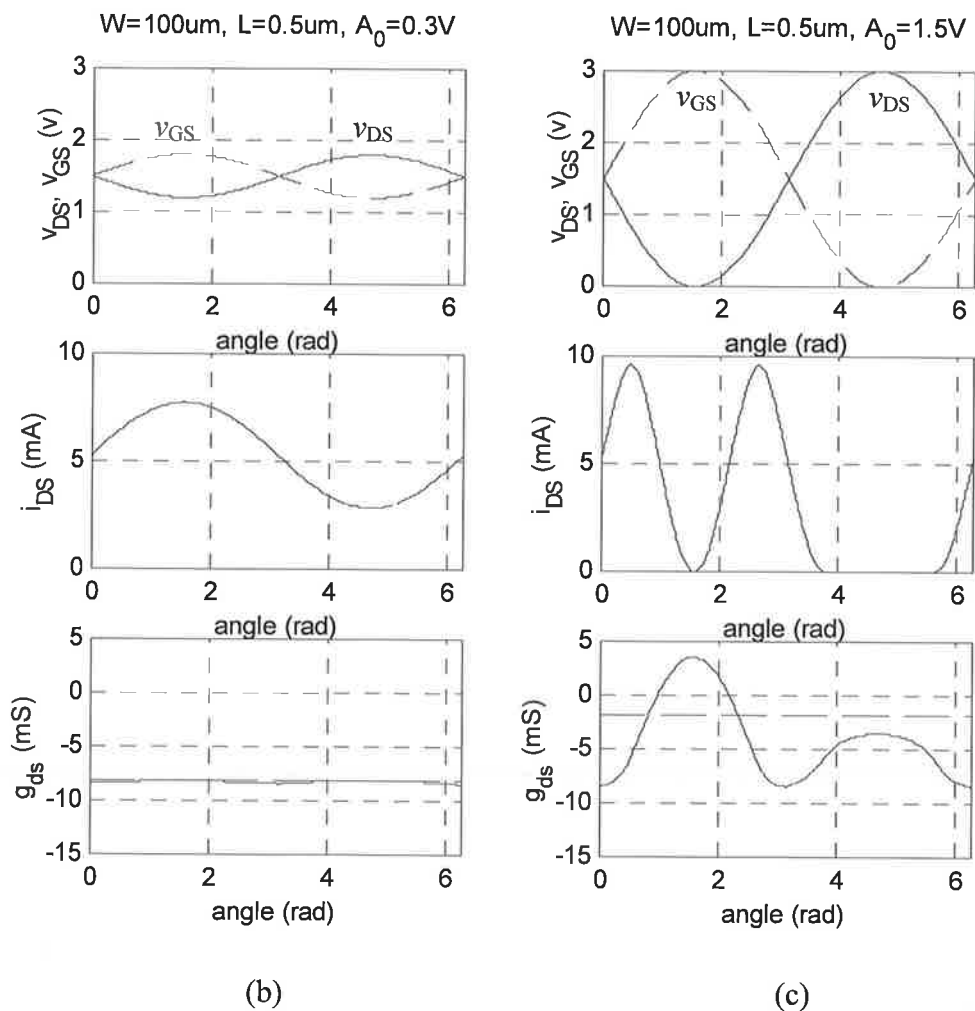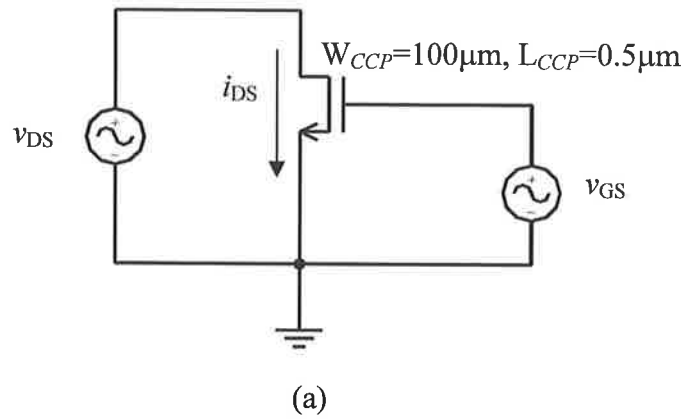
Fig. 3.2: (a) One of cross-coupled transistors set up for transient simulations, (b) small-signal transient simulation result, and (c) large-signal transient simulation result.

For a proper operation of the cross-coupled pair of Fig. 3.1(a), v_{out+} and v_{out-} are biased at a certain level above v_{CM} and this potential becomes the mean potential of the oscillator output waveform. The bias potential between v_{out} and v_{CM} is the same as the drain-source (V_{DS}) and the gate-source bias potentials (V_{GS}) of each transistor. For brevity, the bias potential of a cross-coupled pair is referred to as V_{CCP} hereafter.

V_{CCP} determines the bias current of the cross-coupled pair, as well as the upper limit on the single-ended oscillation amplitude (A_0). Although V_{CCP} is not a hard-limit, A_0 does not tend to grow beyond this limit, because as soon as v_{out} reaches V_{CCP}, one of the transistors is completely cut off and does not contribute towards the loss compensation of the passive *LC* circuit.

When A_0 is small, the signal is considered small-signal and the circuit is highly linearized about the DC bias point. A transistor representing one of the cross-coupled transistors shown in Fig. 3.2(a) is driven with sinusoidal signals v_{DS} and v_{GS} with amplitude of 0.3V each in simulation. The two input signals, the output drain current (i_{DS}), and the calculated small-signal drain-source conductance (g_{ds}) are plotted in Fig. 3.2(b). i_{DS} closely resembles near perfect sinusoid, indicating linear response to the input signals. g_{ds} is quite constant throughout the whole oscillation period, again indicating a linear relationship between the input voltage and the output current. The effective g_{ds}, $G_{ds.eff}$ is calculated to be around -8.2mS, which can cancel 122Ω of the equivalent parallel resistance of the tank at resonance (R_{tank}). $G_{ds.eff}$ is not a simple average of g_{ds} over time. Calculations of g_{ds} and $G_{ds.eff}$ are detailed in Appendix A.

When A_0 is large, the signal is considered large-signal and the circuit behavior is highly nonlinear. The circuit in Fig 3.2(a) is simulated again with larger input signals,

and the corresponding set of results is plotted in Fig. 3.2(c). i_{DS} and g_{ds} are highly distorted this time, indicating nonlinear relationship between the input voltages and the output current. Nevertheless, g_{ds} is still mostly negative over the period, and $G_{ds.eff}$ calculated in this case is around $-1.8mS$, which can manage to cancel R_{tank} of 550Ω.
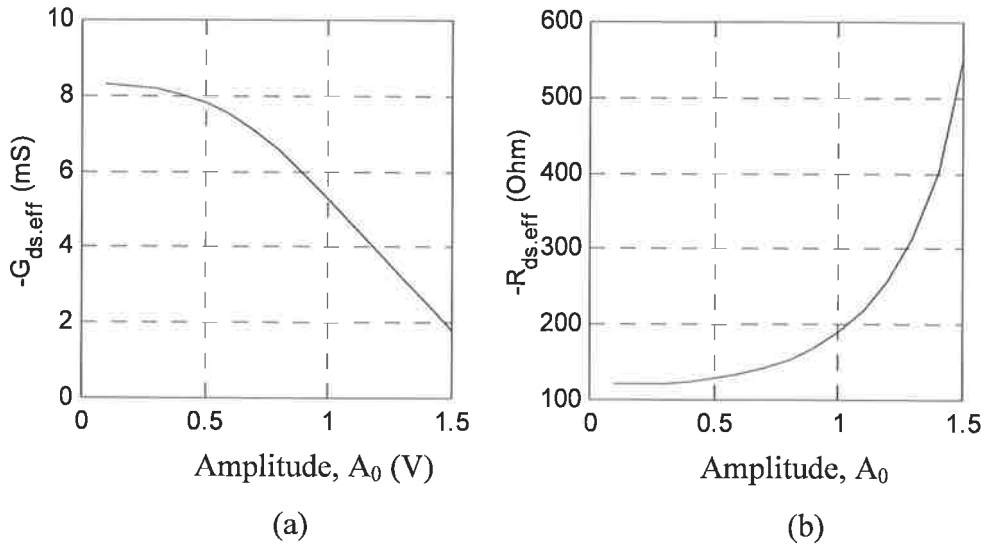
Fig. 3.3: (a) Effective negative drain-source conductance, $-G_{ds.eff}$ and (b) its inverse, $R_{ds.eff}$ are plotted against oscillation amplitude, A_0.

The variations in $-G_{ds.eff}$ and its inverse, $-R_{ds.eff}$ with respect to A_0 are simulated and plotted in Fig. 3.3. This figure provides an insight of how a cross-coupled oscillator maintains constant amplitude of oscillation for a given tank impedance.

Although a cross-coupled *LC* tuned oscillator contains inevitable nonlinear capacitance such as the varactors or the parasitic capacitors associated with the cross-coupled pair, R_{tank} is assumed to be constant with respect to A_0 for the sake of the ongoing analysis.

If R_{tank} is smaller than $-R_{ds.eff}$ for all A_0, it means there is no solution for A_0, and oscillation will not start. On the other hand, if R_{tank} is larger, oscillation will start and A_0

will increases until the magnitude of $-R_{\text{ds.eff}}$ reaches R_{tank}. In the event of small increase of A_0 due to perturbation, $-R_{\text{ds.eff}}$ is increased above R_{tank} and the cross-coupled pair cannot fully compensate for the losses in the tank. Therefore, A_0 will decay until $-R_{\text{ds.eff}}$ levels again with R_{tank}.

On the other hand, if the perturbation decreases A_0 by a small amount, $-R_{\text{ds.eff}}$ is decreased below R_{tank} and the loss compensating force is excessive this time. As a result, A_0 will increase until $-R_{\text{ds.eff}}$ reaches the tank resistance again. Therefore, it is evident from above that in a real *LC* tuned oscillator, the oscillation amplitude is maintained at a constant level as long as the equivalent tank resistance and V_{CCP} remain constant, even in the presence of small amplitude perturbations.

As an example, the result from Fig. 3.2 can be interpreted as follows; the NMOS cross-coupled pair with transistor width (W_{CCP}) of 100μm and length (L_{CCP}) of 0.5μm biased at V_{CCP}=1.5V would oscillate with amplitude of 0.3V when the parallel equivalent tank resistance of the tank at resonance is 122Ω. Also, for a resonator with R_{tank} of 550Ω, the tank is now less lossy, and therefore the cross-coupled pair is able to increase A_0 to 1.5V. The transistor model used in this example is the Peregrine Semiconductor's 0.5μm regular N-type MOSFET.

3.2.1 NMOS-Only Topology

A typical NMOS-only topology employing one cross-coupled NMOS transistor pair is shown in Fig. 3.4. The DC bias potential at the differential output v_{out+} and v_{out-} is V_{DD}. This is the mean potential of the output waveform for this topology. It is firmly

defined by V_{DD}. As mentioned earlier, the lower limit of the output potential is defined

by v_{CM}. Since v_{CM} can be lowered close to ground and assuming sinusoidal output

waveform, the upper limit of the single-ended oscillation amplitude (A_0) for this

topology is V_{DD}. The limit is reached when $V_{CCP} \rightarrow V_{DD}$ or V_{DS} of M3 approaches zero.
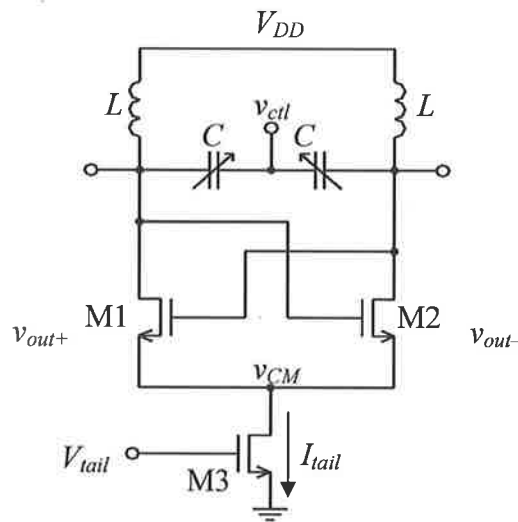
Fig. 3.4: Typical NMOS-only topology.

M3 is often referred to as a tail bias transistor. The tail bias voltage, V_{tail}

determines the tail bias current I_{tail}, which in turn determines V_{CCP} of the cross-coupled

pair.

In addition to the AC ground V_{DD}, the common-mode potentials of the circuit

v_{CM} and v_{ctl} are also regarded as AC grounds at the frequency of oscillation. However,

due to the nonlinearities in M1 and M2, v_{ctl} and v_{CM} may contain even order harmonics

of the oscillation if not properly bypassed to ground.

The capacitors in the tank are made variable in order to control the frequency of oscillation rather than making the inductors variable. Various frequency-tuning methods are studied in section 3.3.

Advantages of this topology are as follows.

1. Oscillation amplitude can be as high as the supply potential.

2. Mean potential of oscillation is locked to the AC ground V_{DD}, rather than left floating.

3. NMOS cross-coupled pair provides largest gain per transistor width.

4. Good supply rejection owing to the precisely controlled bias current source and its high output impedance.

High oscillation amplitude is always welcome in the context of low noise oscillator design. The fact that this topology can provide A_0 as large as V_{DD} can be very advantageous for circuits operating off a low supply source such as a 1.5V battery cell.

Any fluctuation in the DC bias potential of the oscillation waveform can cause a frequency modulation in the presence of a high gain varactor. Since the DC bias potential is set by V_{DD}, this VCO topology does not suffer from the aforementioned problem. More on this type of noise upconversion process is discussed in section 3.4.

The NMOS devices have larger transconductance (g_m) per unit gate width than the PMOS devices owing to the higher mobility of electrons over holes [69]. This allows for smaller sizes for the cross-coupled pair, and consequently, unwanted nonlinear parasitic gate capacitance and resistance are minimized.

The tail current bias transistor, M3 is in the common-source configuration and its output resistance is very high. This high output impedance ensures constant tail bias

current, I_{tail}, even in the presence of small fluctuations in V_{DD} or v_{CM}. Therefore the supply rejection ratio is relatively high.

Disadvantages or potential problem of this topology are as follows.

1. Oscillator phase noise is highly vulnerable to noise on V_{tail} due to high gain of the common-source configuration.

2. Flicker noise associated with NMOS devices degrades phase noise performance.

3. Potential device reliability problem as oscillator output exceeds V_{DD}.

M3 biased in the common-source configuration makes the bias current highly sensitive to V_{tail}. To alleviate this potential problem, an LP pass filter may be placed between the bias circuit defining V_{tail} and the gate of M3. Although, the pole of the LP filter must be positioned very close to DC for it to be effective. Monolithic implementation of the filter may take up a significant area of the VCO layout. Another approach would be to replace M3 with a PMOS device. That way, the current source is now in the source-follower configuration, and I_{tail} becomes less sensitive to its gate potential. However, side effects to this approach are increased lower limit on v_{CM} bias potential, which limits maximum A_0, and increased sensitivity of I_{tail} to v_{CM}, which results in a degraded supply rejection ratio.

Although the NMOS devices are faster and have higher g_m density compared to the PMOS devoces, they are noisier as well. The flicker noise of NMOS devices is often of the order of 10 times more than that of PMOS devices with the same geometry [58], [55]. M3 is often pointed as the major source of the flicker noise in this topology [9], [24], [38], [43], [44], [53], [70]. The circuit shown in Fig. 3.5 is a variant of the circuit

in Fig. 3.4, which alleviates potential problems associated with the excessive tail

transistor flicker noise.
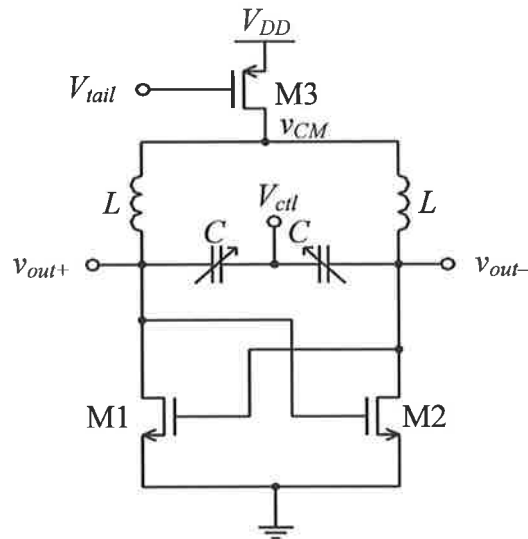
Fig. 3.5: Top biased NMOS-only topology.

With the top biasing PMOS transistor shown in Fig. 3.5, the flicker noise

contribution from the bias circuit is reduced for processes that offer lower flicker noise

PMOS devices. One minor drawback of this circuit would be the floating output bias

potential. Although v_{CM} can be stabilized by bypassing it to ground at high frequencies,

the flicker noise of M1, M2 or M3 can shift the bias level up or down, and result in

close-in phase noise. This noise upconversion process is also discussed in section 3.4.

Although large A_0 is desired for low noise operation, output voltage significantly

exceeding V_{DD} raises serious reliability concerns. The long-term reliability of devices

such as the transistors or the Metal-Insulator-Metal (MIM) capacitor degrades rapidly as

the operating voltage exceeds the maximum allowed. This is because their operations

depend on the quality and the integrity of the thin oxide layers they contain, which are

easily damaged by high electric fields. Therefore, the high oscillation amplitude of this topology may cause a reliability problem.

This problem can be addressed by operating the circuit at reduced V_{DD}, or by ensuring A_0+V_{CCP} does not exceed the maximum allowable supply potential. The motive for reducing V_{DD} may well come naturally due to the supply voltage limit of the application.

Understanding the oscillation amplitude dependence on other circuit parameters such as I_{tail}, V_{DD}, R_{tank} or the bias condition is important in the design of reliable circuits, and the optimization of their performance. It should be emphasized that knowing how to maximize oscillation signal power for a given power budget maximizes the signal-to-noise ratio (SNR) and minimizes the phase noise.

Despite its importance, studies on oscillation amplitude of a cross-coupled *LC* tuned oscillator are still primitive. Although the circuit simulators provide accurate simulation of oscillation amplitude, optimization can only be performed by designers who understand how the oscillation amplitude is determined.

In Ref. [71], the oscillation amplitude for the NMOS-only topology is approximated as

$$A_0 = \frac{2}{\pi} I_{tail} R_{tank}$$
(3.1)

This equation assumes that the cross-coupled pair has enormous gain at the DC bias state and that the cross-coupled transistors completely switch for small difference in the differential output, such that the drain current becomes square wave that swings between I_{tail} and 0A. At high frequencies of oscillation, the harmonics of the square wave current are suppressed due to insufficient current gain, and the current wave edges

are blunted. Under such condition, the drain current approaches sine wave with maxima

at I_{tail} and minima at zero, and (3.1) is reduced to (3.2) [38].

$$A_0 = \frac{1}{2} I_{tail} R_{tank} \tag{3.2}$$

However, even when a cross-coupled pair with a very high transconductance is

used (or equivalently, very high Q tank is used), the drain current cannot become a

square wave. For the oscillator in Fig. 3.4, when v_{out+} is at its maximum, that is

$v_{out+}=V_{DD}+V_{CCP}$, v_{out-} is at its minimum, that is $v_{out-}=V_{DD}-V_{CCP}$. Under this condition,

current through M1 is zero because its v_{GS} is zero, and the current through M2 is also

zero because its v_{DS} is zero. The i_{DS} plot in Fig. 3.2(c) clearly demonstrates this behavior.

Going back to the circuit of Fig. 3.4, when the current sunk by the cross-coupled pair

approaches zero, M3 starts to cut off and its drain potential (v_{CM}) approaches ground

unless a bypass capacitor to AC ground is placed at this common-mode node. Since the

tail current approaches zero for every peak of the output voltage, the frequency of v_{CM}

approaching ground is twice the frequency of oscillation. This voltage variation at the

common-mode node is observed in simulations and the literature [38], [43], [44], [53].

Some researchers encourage the fluctuation of v_{CM} [43], [44], [52]-[54], while some

discourage it [9], [37], [38]. Issues relating to v_{CM} bypassing are discussed in Chapter 4.

If the drain current of M1 or M2 were to be square wave or sine wave with

amplitude of half I_{tail}, Current through M3 and v_{CM} would have been constant. To show

the invalidity of (3.1) and (3.2), an example is provided; when the transistor of Fig.

3.2(a) is used for the cross-coupled pair of Fig. 3.4 with V_{CCP} of 1.5V and R_{tank} of 122Ω,

I_{tail} equals to twice the average bias current through each of M1 or M2. This is around

10.6mA. According to (3.1), A_0 should be 0.82V. (3.2) suggests A_0 of 0.65V. However,

simulated A_0 under this bias condition was only 0.3V. Therefore, according to this derivation, generally accepted oscillation amplitude expressions (3.1) and (3.2) should not be depended upon to predict A_0.

Due to the nonlinearity in transistor drain current, A_0 can only be estimated through a series of transient simulations of drain current and effective conductance calculations as demonstrated earlier with the circuit in Fig. 3.2(a). To gain a further insight on how A_0 varies with respect to other circuit parameters for the VCO in Fig. 3.4, the following plot was generated from drain current simulation of the transistor in Fig. 3.2(a).
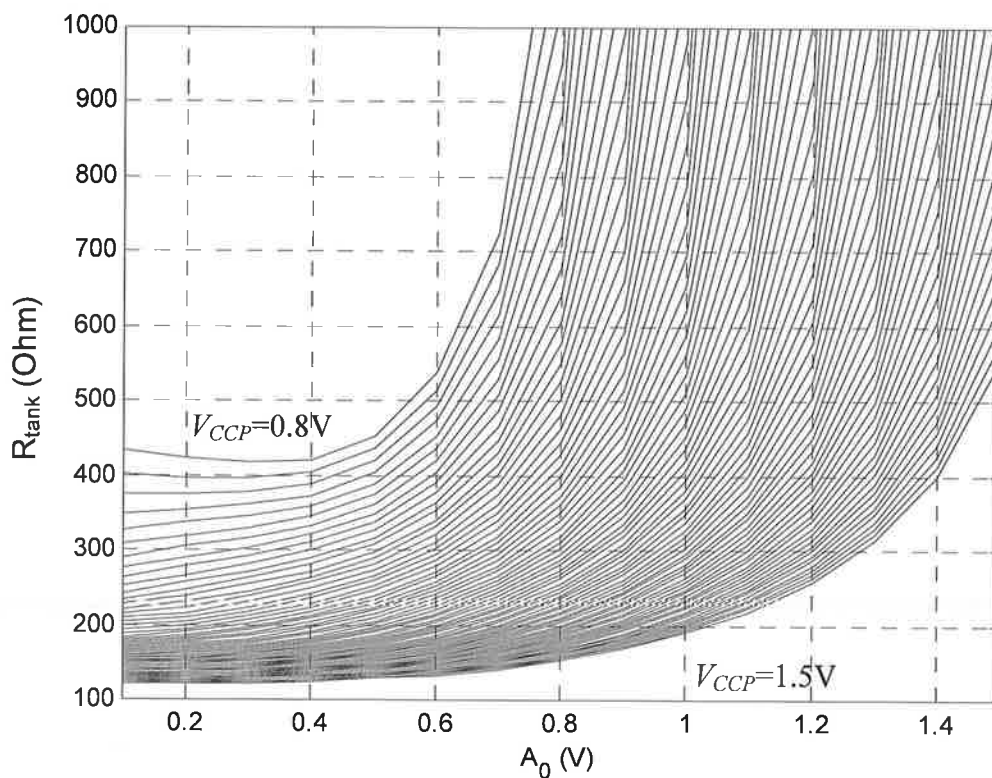
Fig. 3.6: R_{tank} versus A_0, while sweeping V_{CCP} from 0.8V to 1.5V in 10mV steps.

Fig. 3.6 shows R_{tank} versus A_0 curves for a range of V_{CCP} values. An important observation made from this plot is that increasing V_{CCP} increases oscillation amplitude for a constant R_{tank}, or for a given tank.

A series of plots in Fig.3.7 are derived from the curves in Fig. 3.6. The wrinkles seen on curves are due to interpolation errors in calculation. Fig. 3.7(a) shows the oscillation amplitude variation with respect to the DC bias current (I_{DC}) of the cross-coupled pair for various R_{tank}. R_{tank} is swept from 150Ω to 800Ω in 50Ω intervals. I_{DC} is the sum of current sunk by the cross-coupled transistors when their drains and gates are at their DC bias potential. The next plot, Fig. 3.7(b) is similar to Fig. 3.7(a) but the current is the average current over a complete oscillation cycle. This current, I_{tail} is what the circuit actually draws from the supply over time and differs from I_{DC} because of the inevitable nonlinearity in drain current waveform. Fig. 3.7(c) is another oscillation amplitude plot, but this time it is plotted against the cross-coupled pair bias potential, V_{CCP}.

It should be noted from Fig. 3.7 that none of the plots resembles the usual amplitude versus bias current plots often found in the literature. Fig. 4 of [38] and Fig. 4 of [72] are both classical examples of A_0 versus I_{tail} plots found in the literature. In these plots, the A_0 versus I_{tail} curves are divided into two sections. The first is named current-limited region, where the oscillation amplitude increases proportionally with the bias current. The second region is named voltage-limited region, where the oscillation amplitude is limited by the supply voltage and does not increase with the bias current.
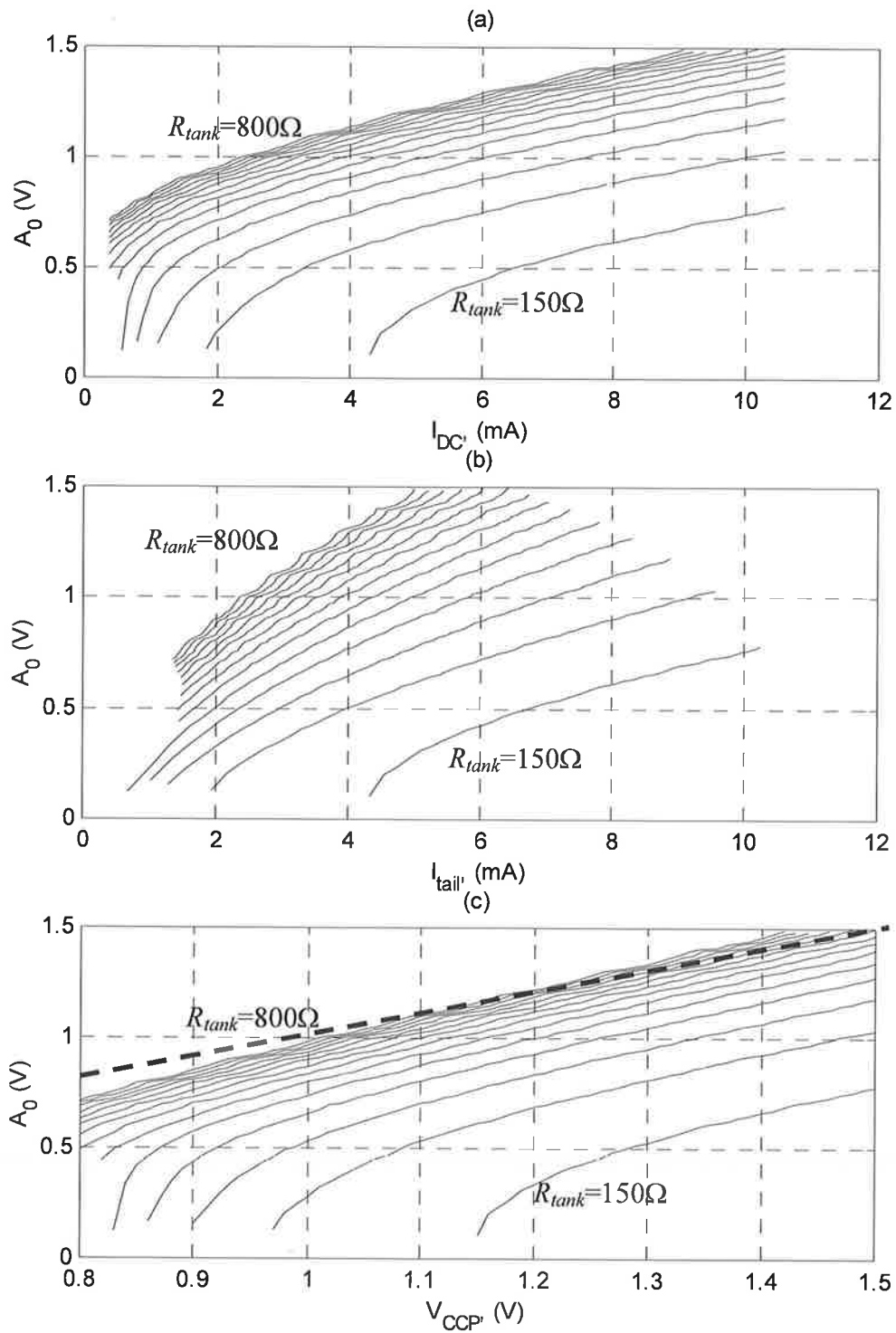
Fig. 3.7: (a) Amplitude versus DC bias current, (b) amplitude versus average bias current, and (b) amplitude versus cross-couples pair bias potential, while sweeping R_{tank} from 150Ω to 800Ω in 50Ω intervals.

The optimal A_0 is often based on the value of A_0 at the junction between the two regions where A_0 begins to saturate due to the supply voltage limit. This is illustrated in Fig. 3.8. Although proven to be invalid, (3.1) or (3.2) were thought to be governing the A_0 versus I_{tail} relationship within the current-limited region [9], [38], [43], [52], [53], [72].

From comparison between Fig. 3.7(b) and Fig. 3.8, it is observed that the curves in Fig. 3.7(b) representing different tank impedances do not have the plateau like the curve in Fig. 3.8.
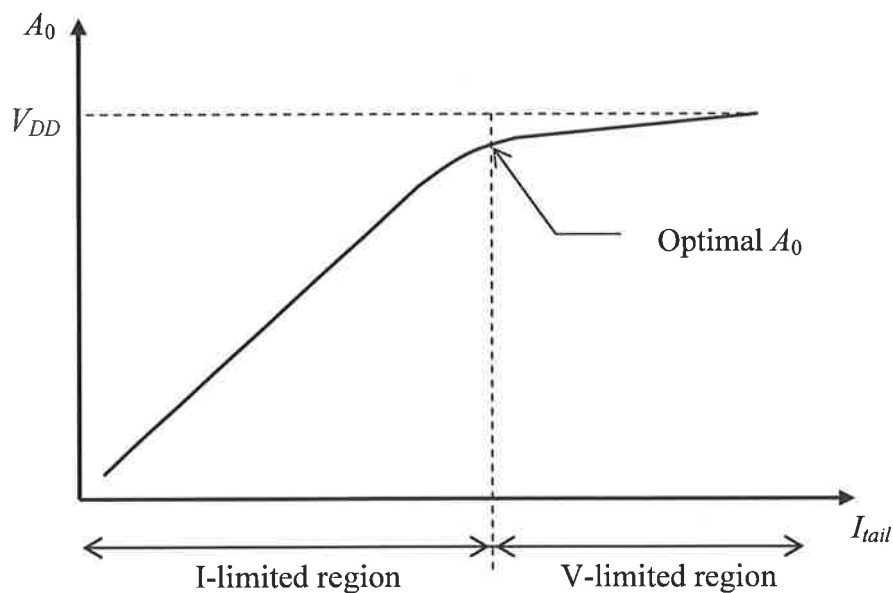
Fig. 3.8: Classical oscillation amplitude variation with respect to tail bias current.

I_{tail} increases with V_{CCP}. The upper ends of the curves in Fig. 3.7(b) correspond to V_{CCP} of 1.5V. The curves with R_{tank} between 500Ω and 800Ω reached the amplitude limit set by the supply voltage, assuming 1.5V is the supply voltage. Other lower curves do not reach V_{DD}. The curves cannot be continued any further, because then the V_{CCP}

would have to exceed V_{DD}. Therefore, a true A_0 versus I_{tail} curves actually do not have the plateau region, referred to as the voltage-limited region in the literature.

The plateau region found in the literature may have resulted from reading the reference bias current rather than the actual bias current through the cross-coupled pair.

Fig. 3.9 shows a typical tail current bias circuit for a cross-coupled oscillator like the NMOS-only VCO in Fig. 3.4.
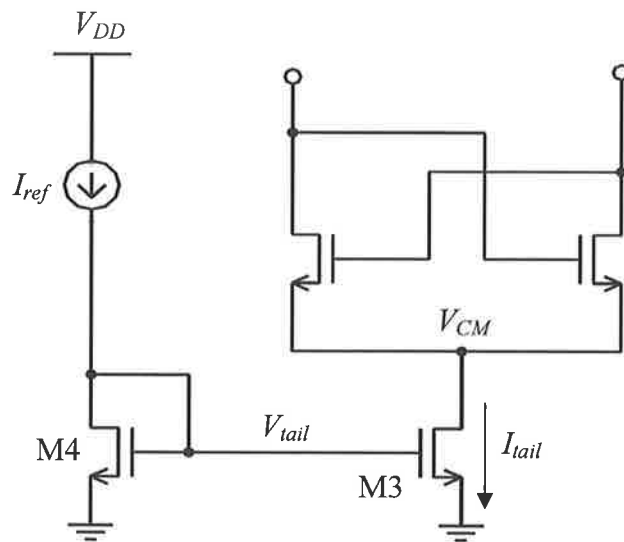
Fig. 3.9: Simple tail current bias scheme for a cross-coupled pair.

Although I_{ref} is supposed to mirror its current to I_{tail} with a multiplication factor equal to the gate width ratio between M3 and M4, due to the channel length modulation effect of MOSFETs, I_{ref} and I_{tail} are different from each other when V_{tail} and V_{CM} are different. A_0 versus I_{tail} and A_0 versus I_{ref} are simulated with the circuit in Fig. 3.4 biased by the circuit in Fig. 3.9 with V_{DD}=1.5V, while varying R_{tank} from 150Ω to 750Ω in 150Ω intervals. Width and length of M3 and M4 are sized as W=2000μm and L=0.5μm respectively. The results are plotted in Fig. 3.10.

The dashed curves representing A_0 versus I_{ref} are quite similar to the curve found in Fig. 4 of [38] or Fig. 4 of [72]. The plateau regions are also observed. On the other hand, the solid curves representing A_0 versus I_{tail} do not show any plateau region. The curves cannot be extended further into higher oscillation amplitudes, because the drain potential of M3 is approaching ground, and I_{tail} cannot be increased any further by increasing V_{tail}.
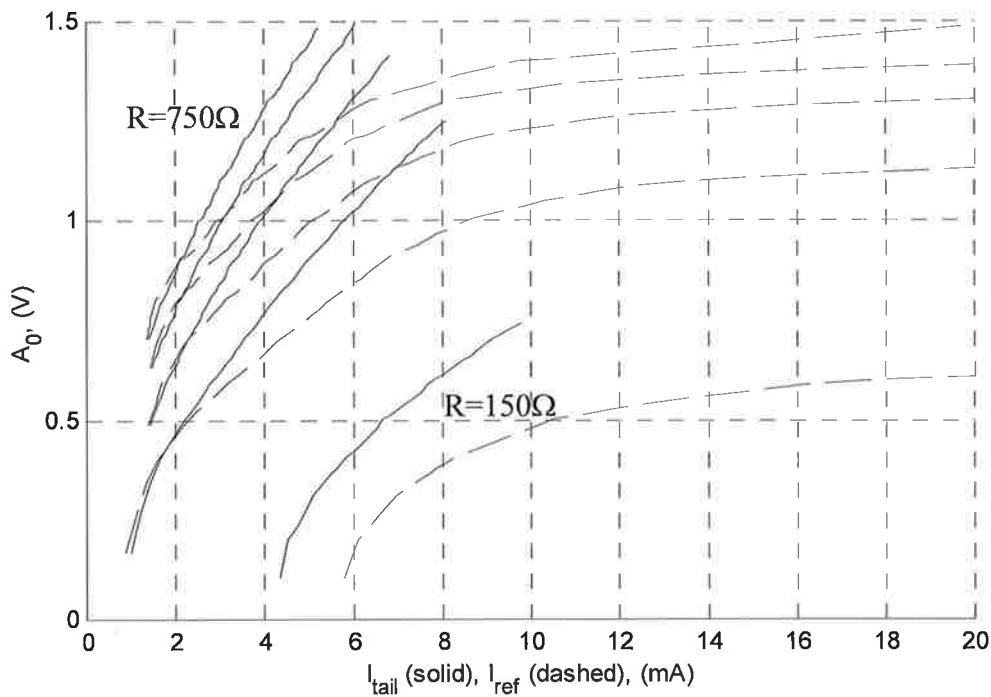
Fig. 3.10: A_0 versus I_{tail} (solid line) and A_0 versus I_{ref} (dashed line), while varying R_{tank} from 150Ω to 750Ω in 150Ω intervals.

V_{DD} is the ultimate upper limit of A_0 for the current VCO topology, because V_{CCP} can only grow up to V_{DD} and A_0 is limited by V_{CCP}. Although A_0 increases with V_{CCP}, for a given R_{tank}, A_0 maintains a constant level below V_{CCP}. The dashed line in Fig. 3.7(c) is the upper limit of A_0 set by V_{CCP} and the curves run more or less parallel to the dashed

line for A_0>0.5V. Curves near the dashed line can approach V_{DD} along with V_{CCP}, but curves located noticeably below the dashed line have no way of reaching V_{DD} even for V_{CCP} approaching V_{DD}. Therefore, the maximum A_0 achievable for a given tank is determined by R_{tank} and the maximum I_{tail} sinkable by the cross-coupled pair, rather than V_{DD}. Although the absolute upper limit of A_0 is still V_{DD}.

With regard to the current-limited, and the voltage-limited regions from the literature, a VCO with any constant R_{tank} will operate in the current-limited region as long as the cross-coupled pair has a sufficient gain to compensate for the loss in the tank. However, no VCO with a constant R_{tank} can enter the voltage-limited region. In other words, the voltage-limited region, where A_0 becomes constant with respect to I_{tail} does not exist. Also, only the VCO with a sufficiently high R_{tank}, or sufficiently wide cross-coupled transistors can have its amplitude reaching the ultimate upper limit, V_{DD}. All of which is simply because I_{tail} cannot be increased indefinitely for a given V_{DD}, R_{tank}, and cross-coupled pair.

To show the results obtained thus far are not process specific, plots in Fig. 3.7 are reproduced with NMOS transistors from the TSMC 0.18μm bulk process and shown in Fig. 3.11. The width and length of each transistor in the cross-coupled pair are W$_{CCP}$=100μm, and L$_{CCP}$=0.18μm respectively, and V_{DD} is set to 0.9V in this case.
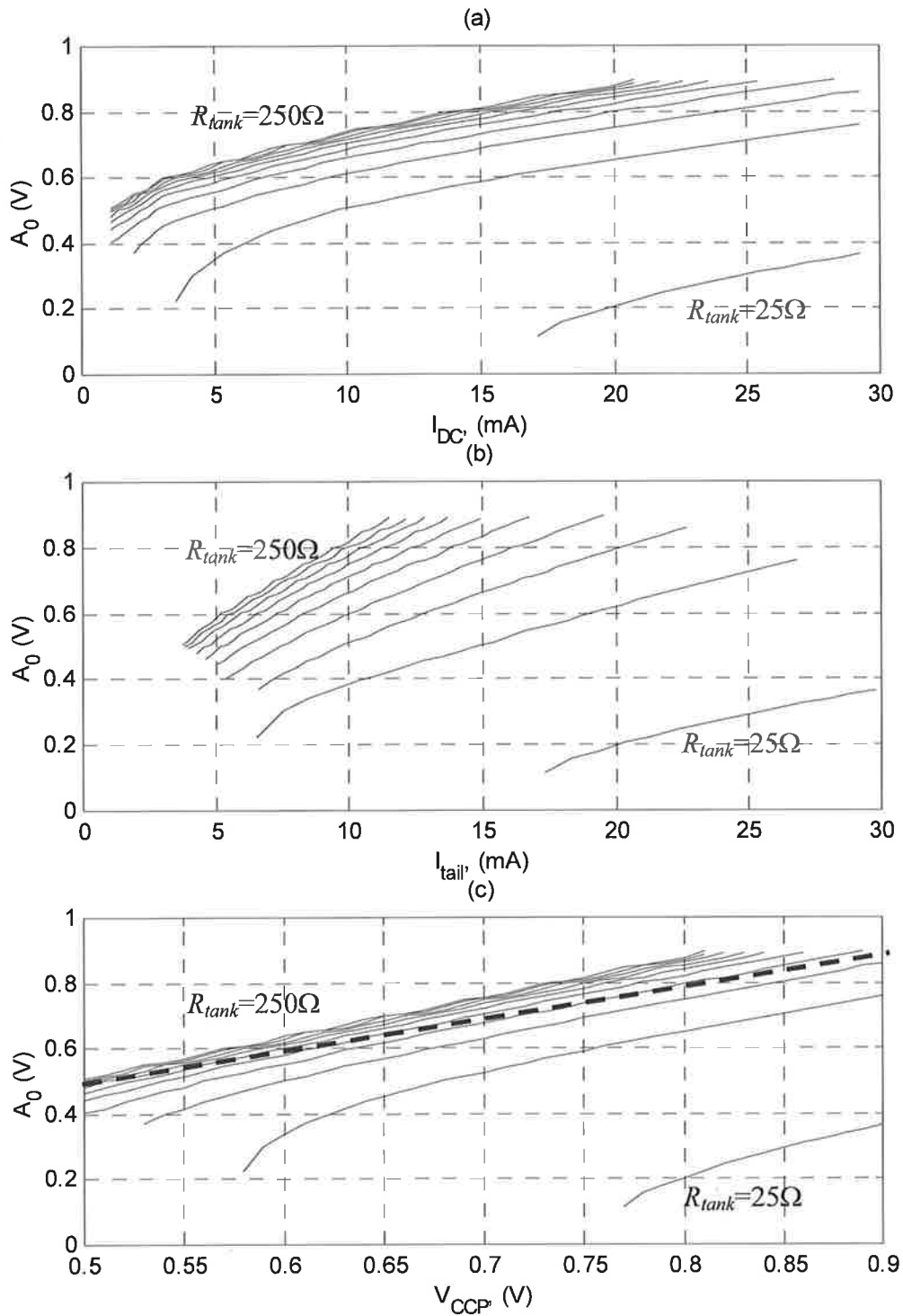
Fig. 3.11: (a) Amplitude versus DC bias current, (b) amplitude versus average bias current, and (b) amplitude versus cross-coupled pair bias potential, while sweeping R_{tank} from 25Ω to 250Ω in 25Ω intervals.

Note that no curves show any sign of the voltage-limited region as expected. Also, curves in Fig. 3.11(c) run parallel to the line, $V_{CCP}=A_0$, shown as the dashed line, indicating approximately constant value of $V_{CCP}-A_0$ for a given R_{tank} over all possible values of I_{tail}.

3.2.2 Other Cross-Coupled Topologies

The PMOS-only topology is an inverted version of the NMOS-only topology. All transistors are replaced with PMOS transistors and their biasing is also inverted, such that the output oscillates about the ground potential rather than V_{DD}. Its schematic is shown in Fig. 3.12.
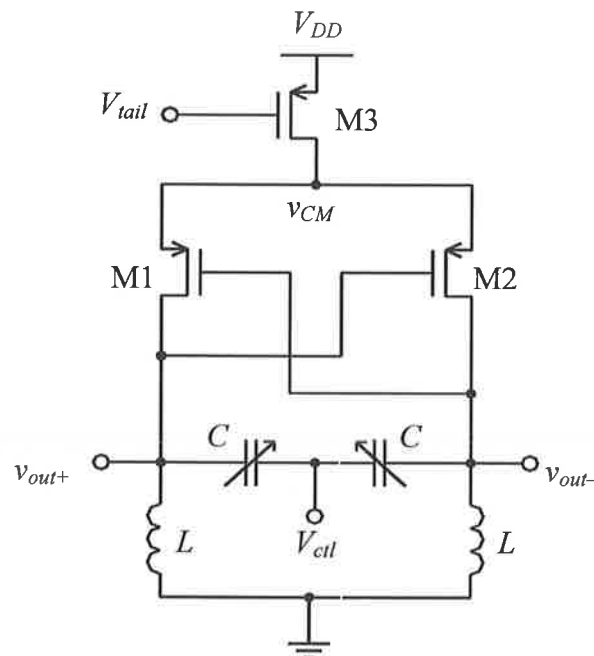
Fig. 3.12: PMOS-only topology.

Properties of the PMOS-only topology are almost identical to that of NMOS-only topology. The only differences are the different DC bias potential of the output signal, reduced current density per unit width of transistors, and reduced flicker noise for a given bias current.

Since the output is oscillating about the ground potential, if the buffer circuit is built with high gain NMOS transistors, a DC level shifter would be required to interface the VCO to the buffer. This is not a complex task, but it involves little more than direct coupling that could be used with the NMOS-only topology.

A major advantage of this topology is reduced flicker noise contribution in the output phase noise. The buried channel PMOS devices intrinsically have lower flicker noise than their NMOS counterparts [73]. Although this may not be true for some SOI PMOS devices as will be seen in Chapter 5.

A disadvantage would be increased transistor width for M1 and M2. PMOS devices have less drain current density for a given gate size and bias condition, compared to the NMOS devices. Therefore, in order to achieve the equivalent transconductance, the gate width needs to be sized two to three times larger than the NMOS devices.

Increase in gate area for the bias transistor, M3 is encouraged, because the flicker noise is inversely proportional to the transistor gate area, and larger gate area for M3 does not have any negative effect on the oscillator performance.

However, it is the increased size of M1 and M2 that may degrade the oscillator performance due to the increased nonlinear, low-Q parasitic capacitors associated with M1 and M2. The channels of cross-coupled transistors are constantly cycled between inversion and depletion. That makes their parasitic gate capacitance nonlinear. Also, Q

of the parasitic capacitor varies as the channel conductance varies. It is often poor compared to that of a MIM capacitor.

The total capacitance in a tank, C is formed by a combination of the parasitic gate capacitor, fixed MIM capacitor, varactor, and other metal routing parasitic capacitors. Since the fixed MIM capacitor is usually the highest Q capacitor in a given process, its contribution in C must be maximized in order to maximize the overall capacitor Q.

In the PMOS-only topology, the sizes of parasitic gate capacitors of M1 and M2 are increased proportionally with the increased gate width. As a consequence, the MIM capacitor size is reduced and the overall capacitor Q is reduced. Furthermore, because the contribution of the nonlinear capacitor in the tank has increased, the linearity of the total C is also degraded, resulting in distortion in the output waveform.

If the frequency of oscillation is relatively low and the size of tank C is very large that the contribution of the parasitic gate capacitors to the overall tank C is small, the increase of the parasitic gate capacitances would not be as detrimental. The oscillator would only benefit from the reduced flicker noise.

However, for the 5GHz or higher operation with a modern CMOS process, the added gate parasitic capacitances from using PMOS devices are often significant. Therefore, the use of PMOS devices is less frequent than the NMOS devices, at least with current CMOS process technologies.

Another cross-coupled topology frequently used in CMOS is the complementary topology. Fig. 3.13 shows the schematic diagram of this VCO topology.

This topology utilizes an NMOS cross-coupled pair and a PMOS cross-coupled pair in a complementary fashion. The result is almost doubled overall transconductance

per unit bias current due to current reuse by the complementary cross-coupled pairs. However, this topology does not provide doubled power efficiency, because the supply voltage must be doubled at the same time.
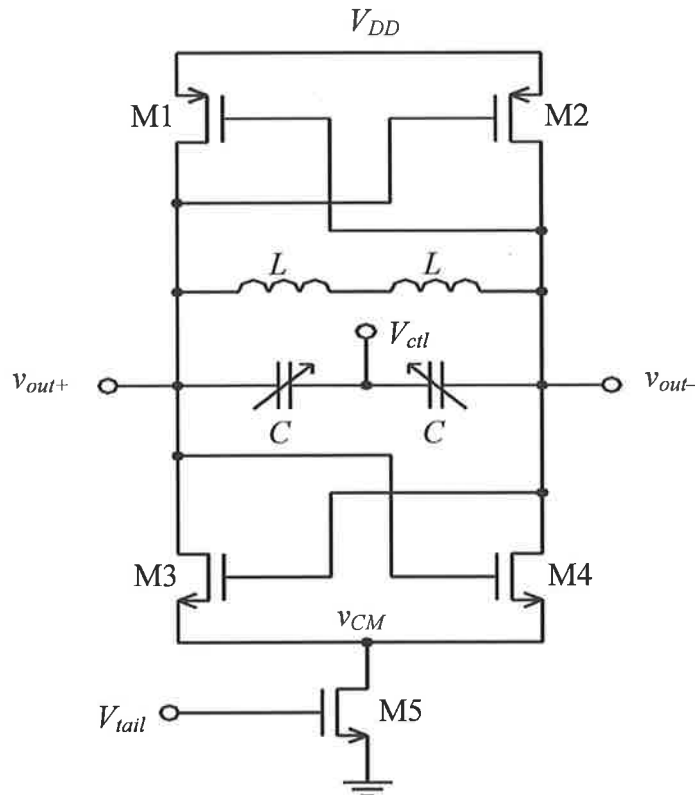
Fig. 3.13: Complementary CMOS VCO topology.

The oscillator output swing is confined between V_{DD} and ground, eliminating any potential reliability issues relating to excessive output swing as in NMOS-only or PMOS-only topologies. The maximum A_0 for this topology is half V_{DD}, and the average potential of the output is approximately determined by the DC bias point of the drains of M1, M2, M3, and M4. It is approximate, because the DC bias potential varies slightly from the mean potential of the output due to the transistor nonlinearity.

In order to maximize A_0, the mean potential of oscillation waveform must be set near half V_{DD}. Unfortunately, this is difficult to guarantee in practice, because the process spread in the transistor transconductance in a CMOS process is typically ±20%. Since the mean potential of oscillator output relies on the 1:1 matching between g_m of the NMOS devices and g_m of the PMOS devices, it is difficult to predict the mean potential of oscillation prior to fabrication. This makes oscillation amplitude and its mean potential harder to control. Also this may severely impact the tuning characteristic of the oscillator, which depends on the amplitude and the mean potential of the oscillation as will be discussed in section 3.3.1.

Despite its disadvantages, the complementary topology is favored over the NMOS-only topology by many, because this topology is believed to produce more symmetric output waveforms due to the complementary action of the cross-coupled pairs and is more power efficient [9], [20], [24], [37], [38], [50], [51], [72].

Indeed, the symmetry in output waveform is welcome for low noise operation [9], [38], [50]. However, the complementary topology does not guarantee symmetric waveform. Because the transconductance matching between the two complementary cross-coupled pairs is difficult as mentioned earlier and it is out of designer's control in practice due to the wide process spread.

Also, for a given tail bias current, the complementary topology provides twice the oscillation amplitude because there are two cross-coupled pairs instead of just one as in the NMOS-only topology. However, the fact that the complementary topology requires twice the supply voltage to achieve the twice the oscillation amplitude has been overlooked. Therefore, there is nothing superior about the complementary topology in terms of the power efficiency.

Hajimiri and Lee have made a phase noise performance comparison between the two topologies in Fig. 14 of [38]. The figure shows that the phase noise of the NMOS-only topology stays above that of the complementary one for all tail current and supply voltage. However, this is not a fair comparison between the two topologies because the two topologies require different supply conditions for the optimal performance.

To show the complementary topology is not superior to the NMOS-only topology, Fig. 13 and Fig. 14 of [38] are carefully observed as an example. From Fig. 13 of [38], the complementary VCO produced phase noise slightly over -123dBc/Hz at 600kHz offset, while drawing 8mA from a 2V supply. Fig. 14 of [38] shows that the NMOS-only VCO produced phase noise slightly under -123dBc/Hz at 600kHz offset, while consuming 16mA from a 1V supply. Therefore, the NMOS-only VCO achieved almost identical phase noise performance if not better, while consuming the same amount of DC power from a reduced supply voltage.

Some VCOs reported in the literature do not have the tail bias current transistor [20], [24], [55]. All of the VCO topologies investigated so far can operate without the tail transistor. Benefits of omitting the tail transistor would be increased headroom for A_0, and elimination of the flicker noise contribution from the tail bias transistor. Although the tail transistor is often pointed as the major contributor of the upconverted flicker noise [20], [24], [38], [43], [44], [53], [54], [55], [70], its contribution can be lowered below that from the cross-coupled pair transistors. This is demonstrated in Chapter 5.

The major role of the tail bias transistor is to provide a precise control over the bias current through the tank and the cross-coupled pair. Some assert that the tail bias transistor also provides a high impedance path for the cross-coupled transistors when

they enter the linear region, which prevents the transistors from loading the tank [43], [44], [53].

Without the tail transistor, A_0 becomes dependent on V_{DD}, because V_{CCP} is now same as V_{DD} for the NMOS- or the PMOS-only topologies, and approximately half V_{DD} for the complementary topology. Therefore, A_0 becomes highly sensitive to the supply perturbation, and the supply rejection ratio degrades severely. Also, a strong oscillator signal is directly coupled to V_{DD}, because the current drawn by the VCO is often irregular. Ref. [24] and [39] suggest using a voltage regulator to overcome the problem. However, in order to gain a control over A_0, the voltage regulator output must be variable. This adds complexity to the system and the output noise of the voltage regulator is passed on to the VCO. This regulator noise would upconverted to the frequency of oscillation. For example, if the voltage regulator were a switched capacitor type, its switching noise will create undesired spurs on the oscillator output spectrum.

3.3 FREQUENCY TUNING METHODS

The frequency of oscillation of an *LC* tuned oscillator is given as (2.23). In order to change f_0 or ω_0, either L or C or both must be changed. The inductance of a monolithic passive inductor is determined by the physical geometry of the metal trace that forms the inductor. Therefore, the inductance is set to a constant value at the design stage and cannot be changed once the chip is fabricated. An exception to this would be Micro-Electro-Mechanical Systems (MEMS), where inductor geometry may be varied

by electro-mechanical means at chip level. However, monolithic implementation of such devices has not been reported to date.

Instead, the capacitance in the tank, C is varied to gain control over f_0. A variable capacitor commonly referred to as varactor or sometimes-called varicap can be implemented in a standard CMOS process without introducing any additional processing steps.

While varactors can provide continuous variation in C, a switched capacitor technique allows variation in C in discrete steps.

3.3.1 Varactors

Traditionally a varactor is constructed by the p^+-n junction of a diode. A reverse bias diode forms a junction capacitor between the p^+ and n regions. The junction capacitance is inversely proportional to the reverse bias voltage applied. This junction capacitance is maintained just until the junction becomes forward biased. When the junction becomes forward biased, DC current starts to flow across the junction. Fig. 3.14 shows an example of a cross section view of a p^+-n junction diode and its symbol. When used in a cross-coupled oscillator, connections are made as shown in Fig. 3.15.
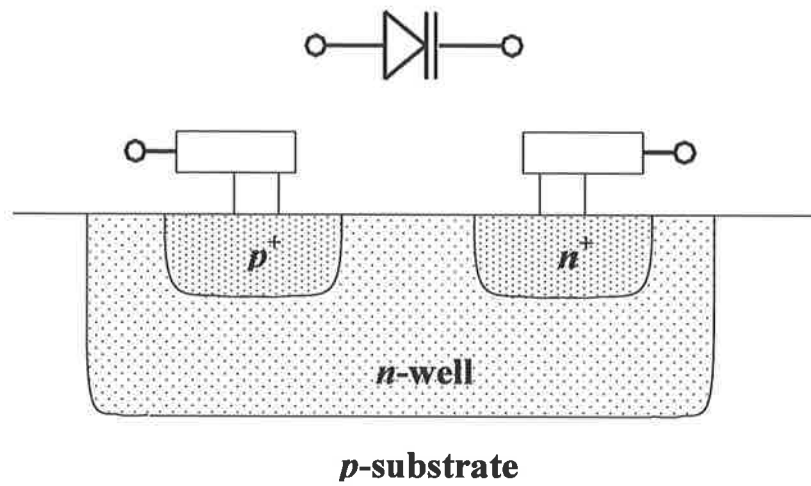
Fig. 3.14: p^+-n junction diode symbol and cross-section side view.
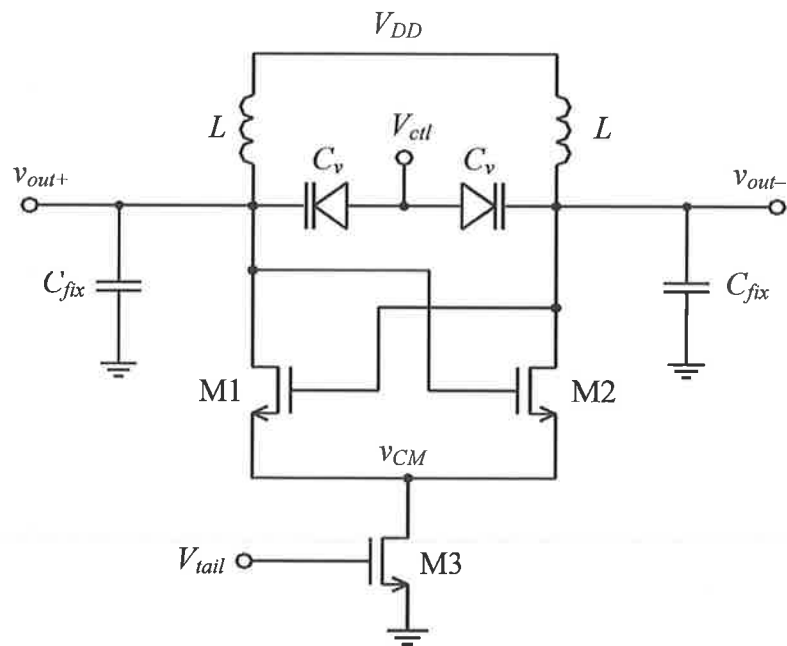
Fig. 3.15: A cross-coupled NMOS-only VCO utilizing a pair of p^+-n junction diodes for a continuous frequency tuning.

While C_v provides a varying capacitance, C_{fix} provides a constant capacitance. The sum of both capacitances forms the overall tank capacitance, C. Increasing C_v contribution to C increases the VCO tuning range.

Since the junction width is proportional to the reverse bias voltage, V_{np}, the junction capacitance is inversely proportional to the junction width. This is illustrated in Fig. 3.16.
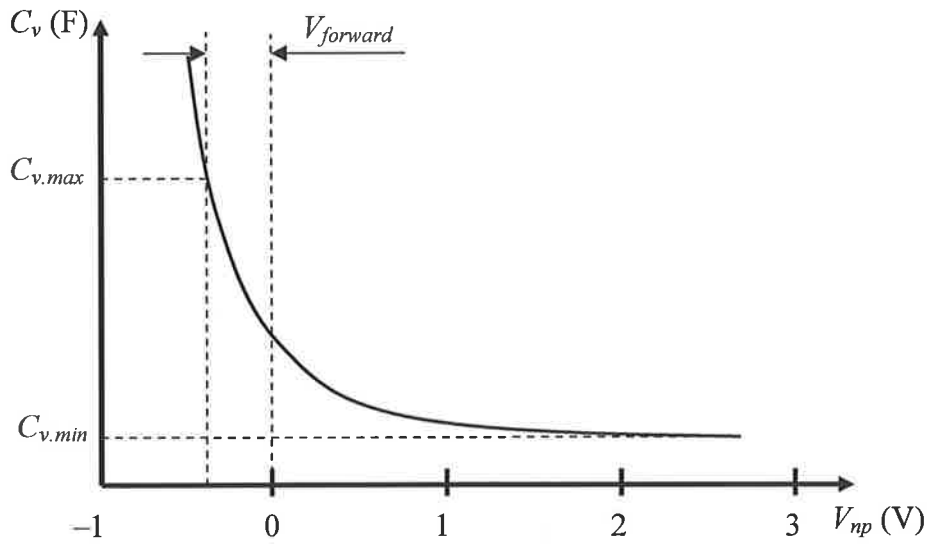
Fig. 3.16: Reverse biased diode junction capacitance variation.

Let $C_{v.max}$ and $C_{v.min}$ be the maximum and minimum varactor capacitances respectively. The ratio between the two (ξ) is one of the important parameters of a varactor, along with the minimum varactor Q, which is defined by $(R_s C_{v.max})^{-1}$, where R_s is the series equivalent resistance when $C_v = C_{v.max}$.

$$\xi = \frac{C_{v.max}}{C_{v.min}} \tag{3.3}$$

A varactor with a larger ξ can yield a larger frequency tuning range. The minimum Q of a diode varactor depends on the amount of forward bias current. As V_{np} decreases beyond 0V, the forward bias current begins to flow and that degrades the varactor Q rapidly. A typical diode varactor having ξ of around 1.5 to 1.8 has minimum Q in the order of 100 at 1GHz [74]. This is considered high quality in CMOS.

A drawback of p^{+}-n junction diode varactor is the limited dynamic range of the frequency control input, V_{ctl}. For the NMOS-only topology, the lowest output potential is V_{DD}–A_0. The upper limit of V_{ctl} is set by $(V_{DD}$–$A_0)$+$V_{forward}$, where $V_{forward}$ is the forward bias potential of the diode that causes the detrimental DC current across the junction. Typical $V_{forward}$ is only around a few hundreds of millivolts. Therefore, the oscillator suffers from the undesired tradeoff between A_0 and the dynamic range of V_{ctl} [67].
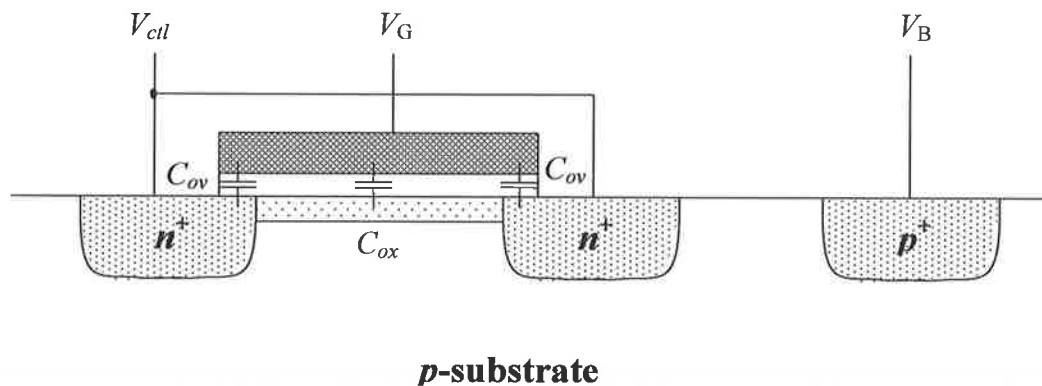
Fig. 3.17: Inversion mode NMOS varactor.

The situation has improved since the introduction of the MOS varactors. A MOS varactor makes use of the change in the gate capacitance of a MOSFET as the transistor channel changes from depletion to inversion or from depletion to accumulation,

depending on the type of MOSFET and configuration used. A cross sectional view of an NMOS transistor used as an inversion mode varactor in a bulk silicon process is shown in Fig. 3.17.

The source and drain of the NMOS transistor are tied together to form a control node, and the gate is to be connected to the oscillator output node. The back gate node or the body of the transistor is connected to the lowest DC potential in the circuit, usually the ground. An example of inversion mode NMOS varactor used in an NMOS-only VCO is shown in Fig. 3.18.
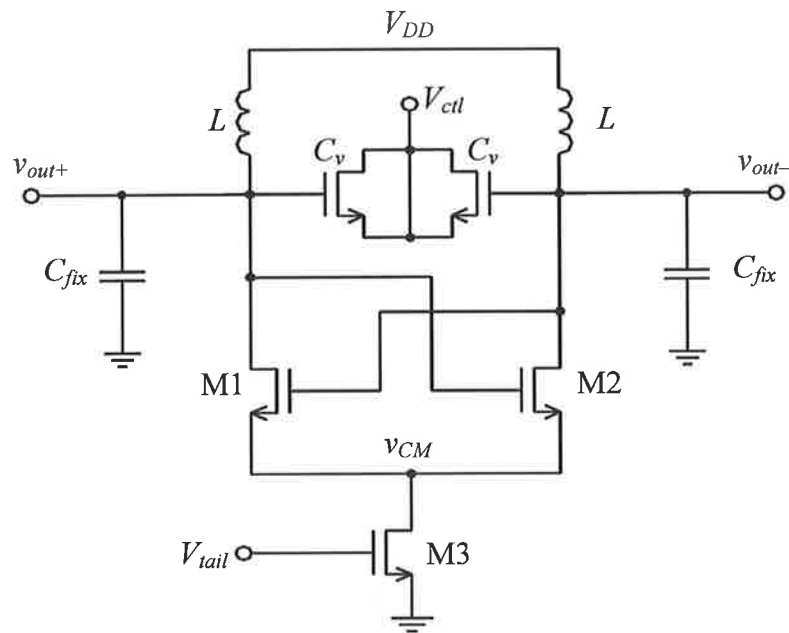
Fig. 3.18: A cross-coupled NMOS-only VCO utilizing a pair of inversion mode NMOS varactors for frequency tuning.

When $V_G - V_{ctl}$ exceeds the transistor's threshold voltage (V_{TH}), a conductive channel is formed under the gate oxide. This channel forms the bottom plate of the gate oxide capacitor (C_{ox}), and connects to V_{ctl}. The maximum capacitance ($C_{v,max}$) is reached during the channel inversion, with its magnitude being equal to $2C_{ov} + C_{ox}$, where C_{ov} is

the overlap capacitance. On the other hand, when $V_G - V_{ctl}$ is below V_{TH}, the channel disappears, and the bottom plate of C_{ox} also disappears. This is when the minimum capacitance ($C_{v.\min}$) occurs. Its value equals to $2C_{ov}$.

When V_G is lowered below V_B, the accumulation channel starts to form under the gate oxide. An accumulation channel is formed under this configuration. It connects the bottom plate of C_{ox} to the back gate node, through the highly resistive p-substrate. Therefore, the magnitude of the gate capacitance reaches $C_{v.\max}$ again. However, the Q is severely degraded in this case. Because the back gate is connected to ground and as long as V_G stays above ground, the accumulation channel does not form under the gate oxide.

Typical ξ for a MOS varactor is around 2 or thereabout [74]. The ratio is affected by the MOS varactor geometry. As the process feature size shrinks, the size of parasitic C_{ov} is reduced and C_{ox} per unit gate area is increased thanks to the reduced gate oxide thickness. With a state-of-the-art modern SOI CMOS process, maximum ξ reported is as high as 5, while maintaining minimum Q of 100 at 1GHz [20].

Q of a MOS varactor in the depletion region is determined by the sum of resistance from the gate polysilicon and highly doped source/drain active regions, and C_{ov}. Since C_{ov} is relatively small and the sum of series resistances can be lowered by layout techniques, the varactor Q in depletion region can be made as high as 100 or more at 1GHz [20], [74], [75].

However, when the MOS varactor enters inversion region, the total gate capacitance increases by a factor of 2 or more, and the sum of series resistances is increased as the channel resistance starts to contribute to the total series resistance. Therefore, the Q is lowered in the inversion region. Since the channel resistance and C_{ox}

are both functions of the MOS varactor geometry and the layout pattern, both quantities

can be lowered to increase the minimum varactor Q. However, a side effect is a

somewhat reduced ξ.
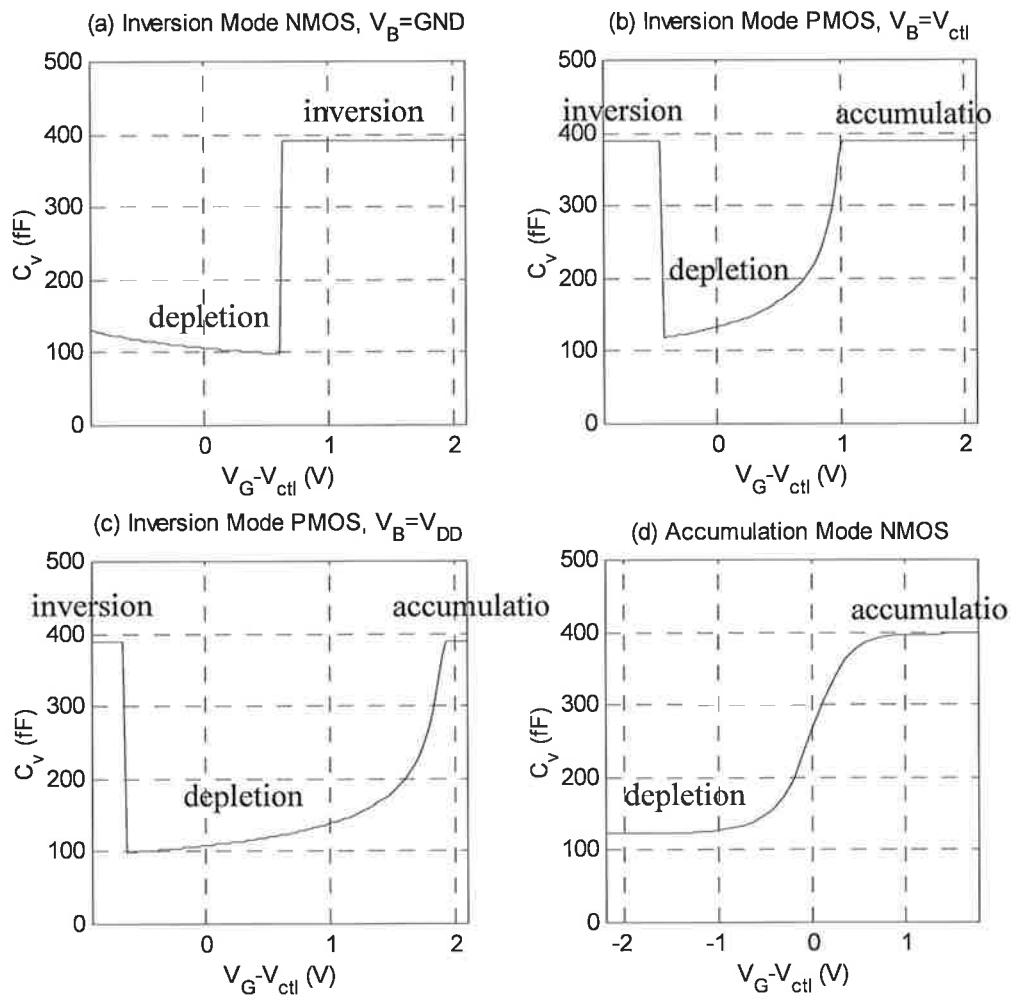
Fig. 3.19: MOS varactor tuning characteristics: (a) inversion mode NMOS varactor, (b) inversion mode PMOS varactor with $V_B=V_{ctl}$, (c) inversion mode PMOS varactor with $V_B=V_{DD}$, and (d) accumulation mode NMOS varactor.

A simulation plot of an inversion mode NMOS varactor gate capacitance with

respect to the bias voltage $(V_G–V_{ctl})$ is shown in Fig. 3.19(a). 18 parallel NMOS devices,

each having W=2μm and L=0.9μm are used in the simulation. V_{ctl} is set to 0.9V and V_G

is varied from 0V to 3V. Lowering V_{ctl} would shift the abrupt transient point between the depletion and the inversion regions to left, and increasing V_{ctl} would shift it to right.

Q values simulated with a standard BSIM3v3 MOSFET model is highly overestimated because the channel resistance and parasitic resistances associated with the source/drain are underestimated in the simulation, because the drain current of the device is zero [76]. Therefore, the MOS varactor Q simulation results are not provided.

A PMOS device implemented in an n-well can also serve as a varactor. A cross sectional view of an inversion mode PMOS varactor is shown in Fig. 3.20. The well contact or the transistor back gate node (V_B) could either be connected to the source/drain potential, V_{ctl}, or to the highest DC potential, V_{DD}. Since operation in the accumulation region for an inversion mode MOS varactor is undesired due to poor Q, V_B is preferred to be connected to V_{DD}. This increases the depletion mode bias range, as can be see from comparing Fig. 3.19(b) to Fig. 3.19(c).
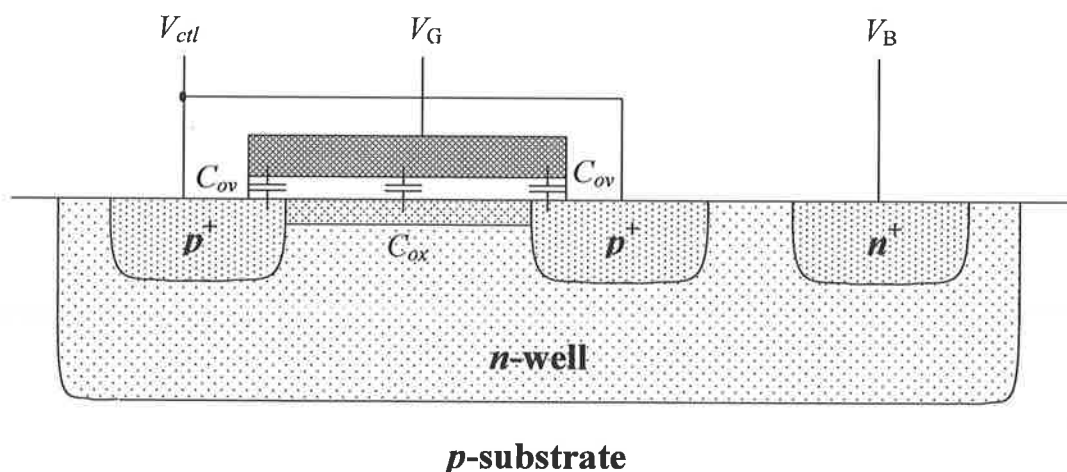
Fig. 3.20: Inversion mode PMOS varactor.

There is yet another type of varactor recently made available by the foundries of the modern bulk CMOS processes. This is an accumulation mode MOS varactor made from an NMOS device in an n-well as shown in Fig. 3.21. This varactor does not have a separate well contact diffusion area, because the source/drain active area can define the well potential. The device is specifically designed to serve as a varactor, rather than as a transistor. Therefore, the device model provided takes the accumulation channel resistance and other secondary effects into account, hence the simulation result shown in Fig. 3.19(d) closely models the actual device as a varactor. It has been reported in [75] that the accumulation mode NMOS varactor outperforms other varactors in terms of lower loss and better oscillator phase noise.
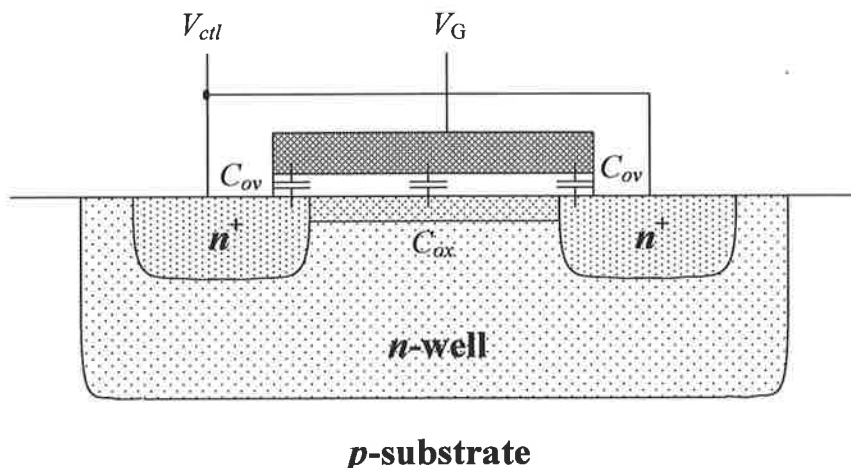
Fig. 3.21: Accumulation mode NMOS varactor.

MOS varactors in SOI processes are similar to the ones from the bulk processes, except they do not have the back gate connections that determine the bulk or the well potentials because their substrate is an insulator. Cross sectional views of NMOS and PMOS transistors configured to work as varactors in a SOI process are shown in Fig.

3.22. Simulation results of the gate capacitances for inversion mode NMOS and PMOS varactors are plotted in Fig. 3.23(a) and Fig. 3.23(b) respectively. The transistor models used are from Peregrine Semiconductor's 0.5µm SOS process. The gate geometry used is W=20×0.5µm, and *L*=6µm for both devices.

Insulator Substrate

(a)

Insulator Substrate

(b)
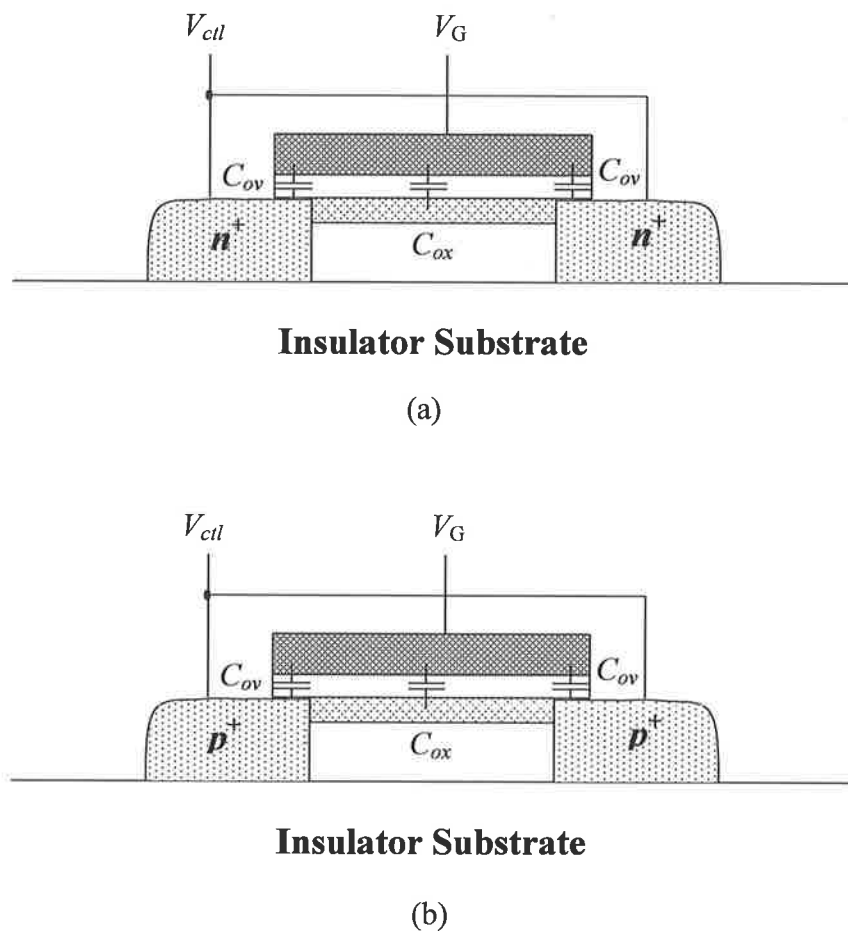
Fig. 3.22: SOI (a) NMOS transistor and (b) PMOS transistor whose source and drain are connected together to work as varactors.

Since SOI devices do not have the bulk connections, there is no source for the minority carriers to accumulate under the gate oxide. Therefore, inversion mode varactors in SOI processes do not have the accumulation region for all bias conditions.

This helps to maximize ξ, and prevents the degradation in Q due to the minority carrier accumulation.

Various MOS varactor variants are reported in the literature. The gated MOS varactor reported in [78] combines the characteristics of p^+-n junction diode and MOS varactor to increase the overall ξ by about 53%. However, this three terminal varactor suffers from poor Q.
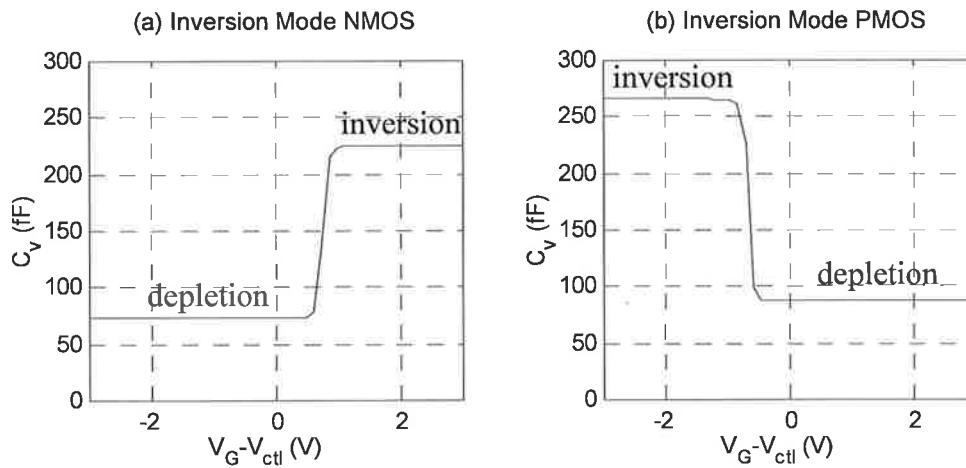
Fig. 3.23: Varactor capacitance variation in a SOI process: (a) inversion mode NMOS varactor, and (b) inversion mode PMOS varactor.

In an attempt to increase ξ by reducing the gate overlap capacitances of a MOS varactor, the use of shallow trench isolation (STI) technique has been suggested in ref. [18] and [23]. The STI provides an oxide spacer between the edge of gate and source/drain active areas to reduce C_{ov}. The result is somewhat increased ξ. However the penalty paid is severely degraded Q due to the increased series resistance, because the STI spacers are blocking the shortest path between the channel and source/drain active areas.

3.3.2 Continuous Tuning

When inversion mode MOS varactors are used in a VCO, their gate potential changes along with the oscillator output. This causes the varactors to switch between the depletion and the inversion regions. The varactor control voltage sets the amount of time they spend in each of the regions. The effective capacitance of the varactors over an oscillation period is not the same as the time averaged capacitance over one period. Instead, a detailed calculation of the effective MOS varactor capacitance, taking into account the voltage and current requirements by the tank is given in [79] as below.

$$C_{v.eff} = \frac{1}{2}\left(C_{v.max} + C_{v.min}\right) + \frac{1}{\pi}\left(C_{v.min} - C_{v.max}\right) \cdot \left(\sin^{-1}\frac{V_{eff}}{A_0} + \left(\frac{V_{eff}}{A_0}\right)\sqrt{1 - \left(\frac{V_{eff}}{A_0}\right)^2}\right) \tag{3.4}$$

where V_{eff} is $V_G - V_{ctl} - V_{TH}$. This expression allows one to calculate the VCO constant, K_V [79] as

$$K_V = \frac{\partial \omega_0}{\partial V_{ctl}} \cong \frac{1}{2}\frac{\omega_0}{C_{eff}}\frac{\partial C_{eff}}{\partial V_{eff}} \tag{3.5}$$

Ideally, the frequency-tuning curve of a VCO should be monotonic and K_V is constant within the tuning range. This is most closely achieved by using varactors whose capacitance varies linearly with respect to the control voltage. From (3.4) it is evident that $C_{v.eff}$ is a function of A_0 and V_{ctl}. Fig. 3.24 shows how $C_{v.eff}$ changes with different A_0 for three different MOS varactors in a bulk process. Larger A_0 averages out the curves. For the inversion mode PMOS varactor with $V_B = V_{ctl}$, the local minimum is raised as A_0 is increased due to the averaging effect, resulting in reduced ξ as expected.
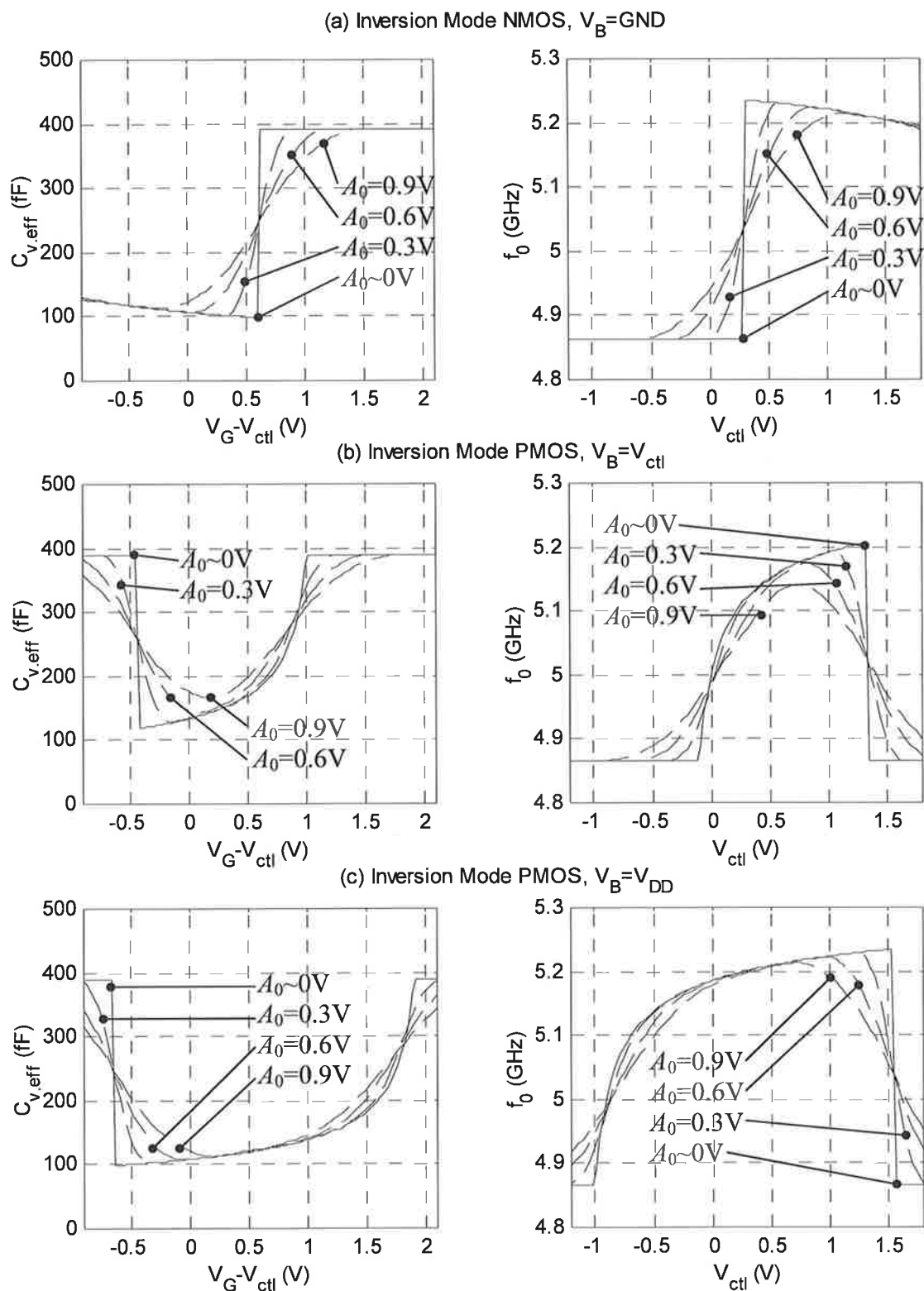
Fig. 3.24: $C_{v.eff}$ curves and VCO frequency-tuning curves at different oscillation amplitudes: (a) inversion mode NMOS, (b) inversion mode PMOS with $V_B = V_{ctl}$, and (c) inversion mode PMOS with $V_B = V_{DD}$.

Also shown in the same figure are the VCO frequency-tuning curves at different values of A_0. The circuit shown in Fig. 3.18 is used to generate the plots in Fig. 3.24. The DC bias potential of the output waveform is set at 1V, C_{fix}=1.75fF, and L=0.5nH. Note that the varactor capacitance variation directly affects the frequency-tuning characteristic of the VCO. The inversion mode NMOS varactor shows the most linear $C_{v.eff}$ and frequency-tuning curves out of the three varactors investigated. This is because the VCO input and output voltages are well outside the range to form an accumulation channel for this varactor. Similar results are reported in [80].

(a) SOI Inversion Mode NMOS Varactor Capacitance

(b) VCO Frequency-Tuning Characteristic
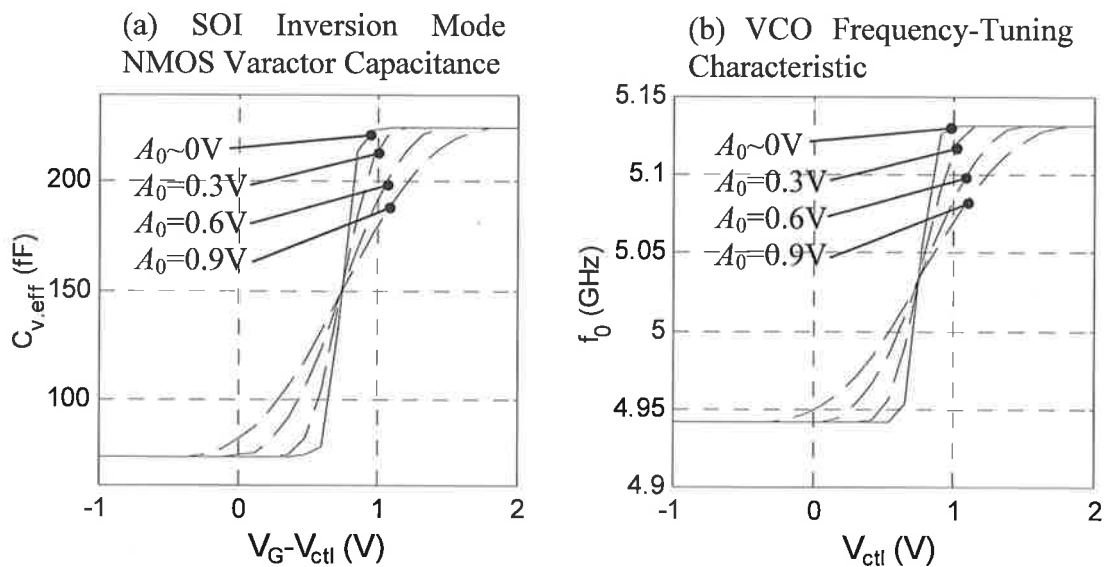
Fig. 3.25: (a) $C_{v.eff}$ curves and (b) VCO frequency-tuning curves at different oscillation amplitudes, using inversion mode NMOS varactors from a SOI process.

The inversion mode MOS varactors in a SOI process do not have the accumulation region, therefore, the varactors provide highly linear $C_{v.eff}$ curves. The frequency-tuning curves of a VCO using these varactors are also highly linear. This is demonstrated in simulation and the results are shown in Fig. 3.25. The $C_{v.eff}$ versus bias

potential curves for different values of A_0, and the corresponding VCO frequency-tuning curves are plotted in Fig. 3.25. The DC bias potential of the oscillator output is set at 1.5V, and C_{fix}=1.85fF and L=0.5nH as before.

The VCO constant, or the VCO gain, K_V is obtained by differentiating the frequency-tuning curve with respect to the control voltage as in (3.5). Since varactors with perfectly linearly varying capacitance do not exist, K_V in practice is not constant over the full tuning range. K_V is one of the loop gain parameters that define the forward loop gain of a PLL. Therefore, its value should be maintained within an acceptable range, so that the loop can function within its specification.

Some applications however, may require a very wide tuning range, while demanding a moderate K_V. A crude approximation of K_V for a VCO with relatively linearly varying varactor capacitance can be written as (3.6).

$$K_V \approx \frac{f_{0.\max} - f_{0.\max}}{V_{ctl.\max} - V_{ctl.\min}} \qquad (3.6)$$

Unnecessarily high K_V is potentially detrimental to the VCO phase noise performance. Any noise present at the control node or at the DC bias potential of the output waveform or in the oscillation amplitude can cause frequency modulation, and appear as phase noise. More on this is discussed in section 3.4.

3.3.3 Discrete Tuning

While continuous tuning of a VCO is an essential feature for it to work in a PLL, the VCO may suffer from limited tuning range due to low K_V requirement by the loop

or the phase noise performance requirement by the host system. Also, the typically wide process spread of CMOS processes makes the frequency tuning range requirement even more stringent.

Various discrete frequency tuning methods have been developed over the years to address the limited tuning range problem associated with continuous tuning by varactors. Switched VCOs, switched inductors, and switched capacitors have been investigated in [57]. All three switching methods have yielded similarly wide tuning range with low K_V. However, switching of the inductors or the VCOs with different center frequencies require excessive amount of chip area. On the other hand, the switched capacitor bank only takes a fraction of the chip area consumed by a typical on-chip inductor.
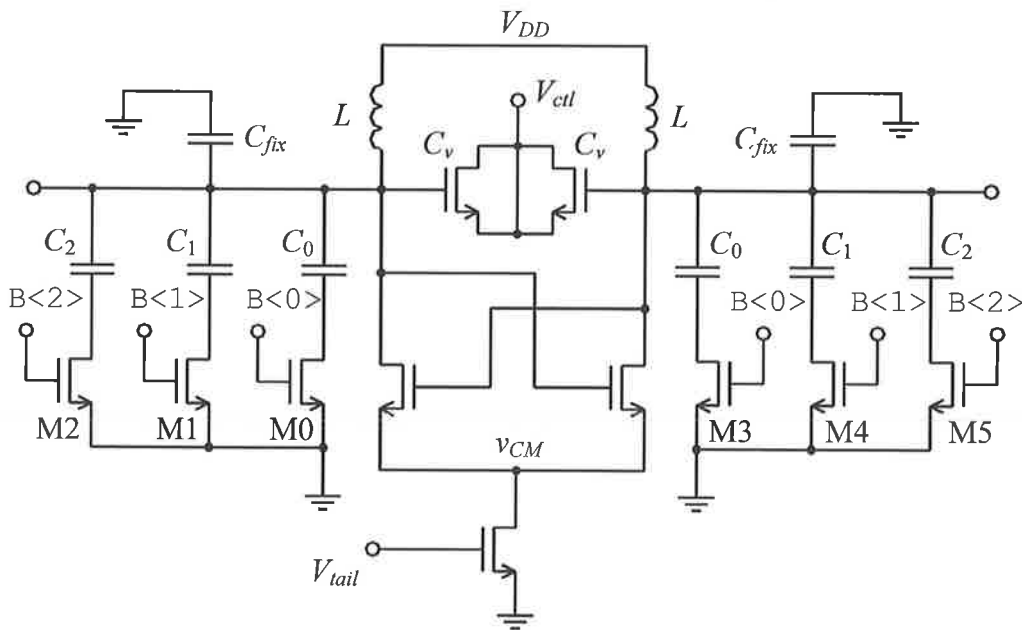
Fig. 3.26: NMOS-only VCO with 3-bit binary weighted switched capacitors for discrete and wider frequency tuning.

A binary weighted switched capacitor bank connected across the tank can boost the VCO tuning range without affecting K_V directly. An example of a schematic diagram featuring an NMOS-only VCO utilizing 3-bit switched capacitor bank for wider frequency tuning range is shown in Fig. 3.26.

The capacitors are binary weighted such that $C_1=2C_0$ and $C_2=4C_0$. Transistor M0 to M5 serve as switches between the binary weighted capacitors and ground. Widths of the switch transistors are also binary weighted, proportional to the size of capacitors they are connected to. B<2>, B<1> and B<0> are digital control signals to the switched capacitor bank.

$C_{v.max}-C_{v.min}$, or ΔC_v should be at least equal to or larger than C_0 to continuously cover the full frequency range. The minimum oscillation frequency, $f_{0.min}$ is achieved when all capacitors are switched in by setting B<2:0>=[1,1,1], and $C_v=C_{v.max}$.

$$f_{0.min} = \frac{1}{2\pi\sqrt{L(7C_0 + C_{v.max} + C_{fix})}} \qquad (3.7)$$

The maximum oscillation frequency, $f_{0.min}$ is reached when all capacitors are switched out by setting B<2:0>=[0,0,0], and $C_v=C_{v.min}$.

$$f_{0.max} = \frac{1}{2\pi\sqrt{L(C_{v.min} + C_{fix})}} \qquad (3.8)$$

The 3-bit binary control input results in $2^3=8$ different discrete output frequencies and each frequency gap is continuously covered by the varactor. The circuit in Fig. 3.27 is simulated with $C_0=100fF$, $C_{fix}=1.15pF$ and $L=0.5nH$. Other circuit parameters, including the varactor size are same as the ones used for the simulation of the circuit in Fig. 3.25. The output frequency simulation result is plotted in Fig. 3.27.

The frequency tuning range was just under 200MHz for the circuit in Fig. 3.25. With the switched capacitor bank, the range is increased to almost 500MHz.
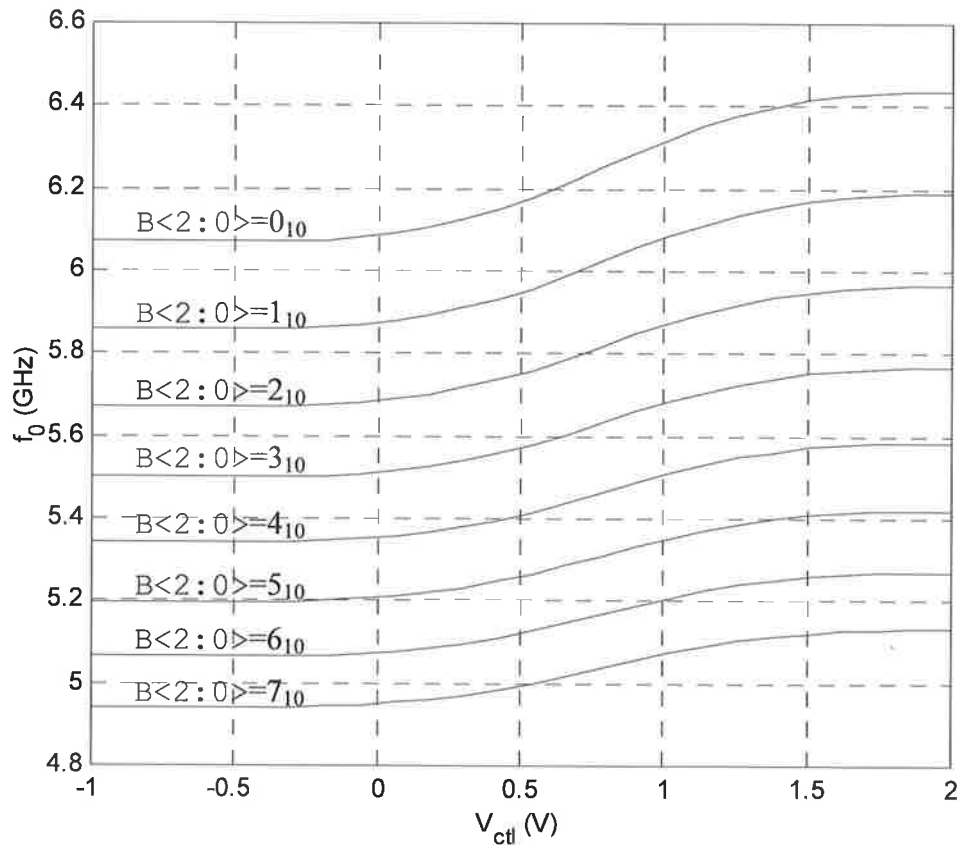
Fig. 3.27: Frequency tuning curves of a VCO with 3-bit switched capacitor bank.

It should be noted that the gap between the curves becomes larger as the tank capacitance is reduced in constant steps. Also, the continuous tuning range covered by the varactor is increased at higher frequencies. This is because the VCO output frequency follows the inverse square root relationship with respect to the total tank capacitance. In other words, when C is large, a small change in C results in a small change in f_0, but when C is small, the same small change in C results in a larger change in f_0. Since the frequency tuning range covered by the varactor varies depending on the

size of the total C, the switched capacitor indirectly affects K_V such that K_V increases slightly with f_0. This effect becomes more pronounced as the variable portion of C is increased.

A VCO utilizing this type of tuning scheme may require an analog-to-digital converter to convert the charge pump output signal to a digital signal and use it to coarsely stir the VCO to bring it to a locking range of the PLL, then switch to the varactor control input to acquire the final frequency lock.

Since the switched capacitor bank covers the bulk of the frequency tuning range, K_V can be chosen freely to satisfy the loop gain and the noise requirements.

Varactors available in SOI processes allow implementation of the switched capacitor bank with varactors. A distinct property of SOI inversion mode MOS varactors identified in section 3.3.1 is that they do not have the accumulation region. Therefore, their capacitance varies quite linearly with respect to the control voltage. Also, beyond each ends of the variable capacitance range, the varactor capacitance remains constant with respect to the control voltage, as can be seen from Fig. 3.25. Therefore, the digital control signal can make use of the two flat regions in the varactor capacitance curve, and switch the varactors between $C_{v,\min}$ and $C_{v,\max}$. An example circuit diagram is shown in Fig. 3.28.

Again, B<2:0> is the 3-bit digital control input. C_0, C_1, and C_2 are binary weighted varactors. Although they are varactors, their control input is in binary form. Therefore, they are switched between the fully depleted region and the fully inverted region, providing discrete capacitance variation just like the switched capacitor bank in the previous example.

In bulk silicon processes, the inversion mode NMOS varactors may be used for this type of frequency tuning scheme. However, the varactor capacitance in the depletion region is not as constant with respect to the control voltage compared to that of the SOI MOS varactors. Therefore, the output frequency becomes sensitive to any noise present in the digital control input, especially low frequency noise components.
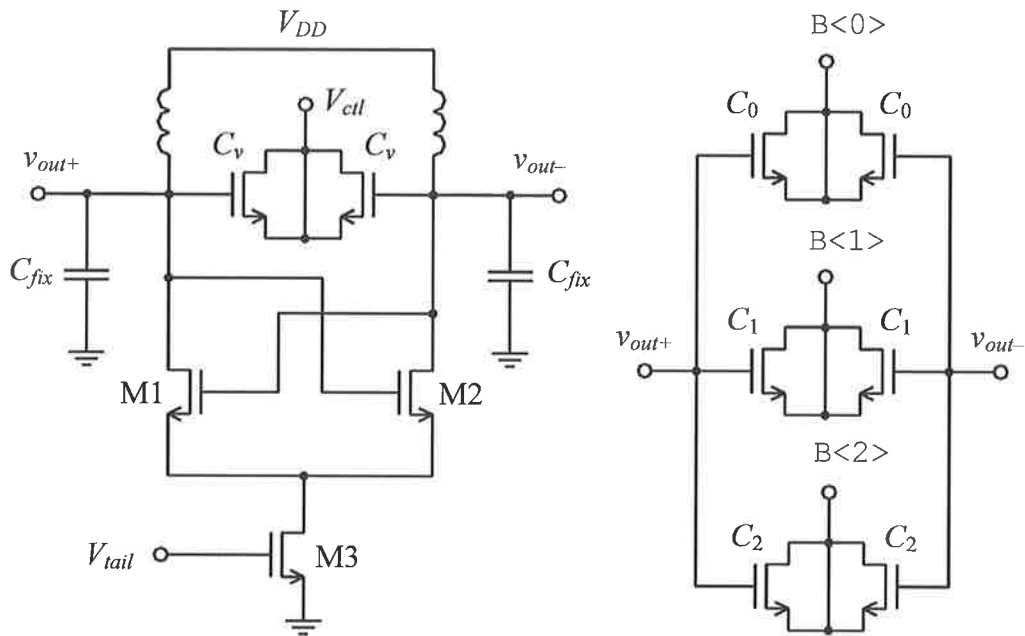
Fig. 3.28: 3-bit switched capacitor bank implemented with SOI MOS varactors.

3.4 PHASE NOISE SOURCES

All noise sources connected to the VCO are potentially harmful to the phase noise performance. Noise sources can be either internal to the VCO or external to it.

Internal noise sources include the thermal noise from the passive *LC* tuned circuit, and the transistor channel noise from the differential pair transistors and the tail

current bias transistor. The channel noise associated with active transistors contains both the thermally induced white noise and the flicker noise caused by either the carrier number fluctuation or the carrier mobility fluctuation [31].

Noise external to the VCO may enter through the supply and ground rails, the frequency control input, the bias current reference or the substrate shared with other noisy circuits in the case of bulk silicon processes.

This section identifies noise sources affecting the VCO phase noise and discusses various frequency conversion paths they take to appear at the frequency of oscillation. Fig. 3.29 summaries the noise sources and processes affecting the oscillator phase noise.
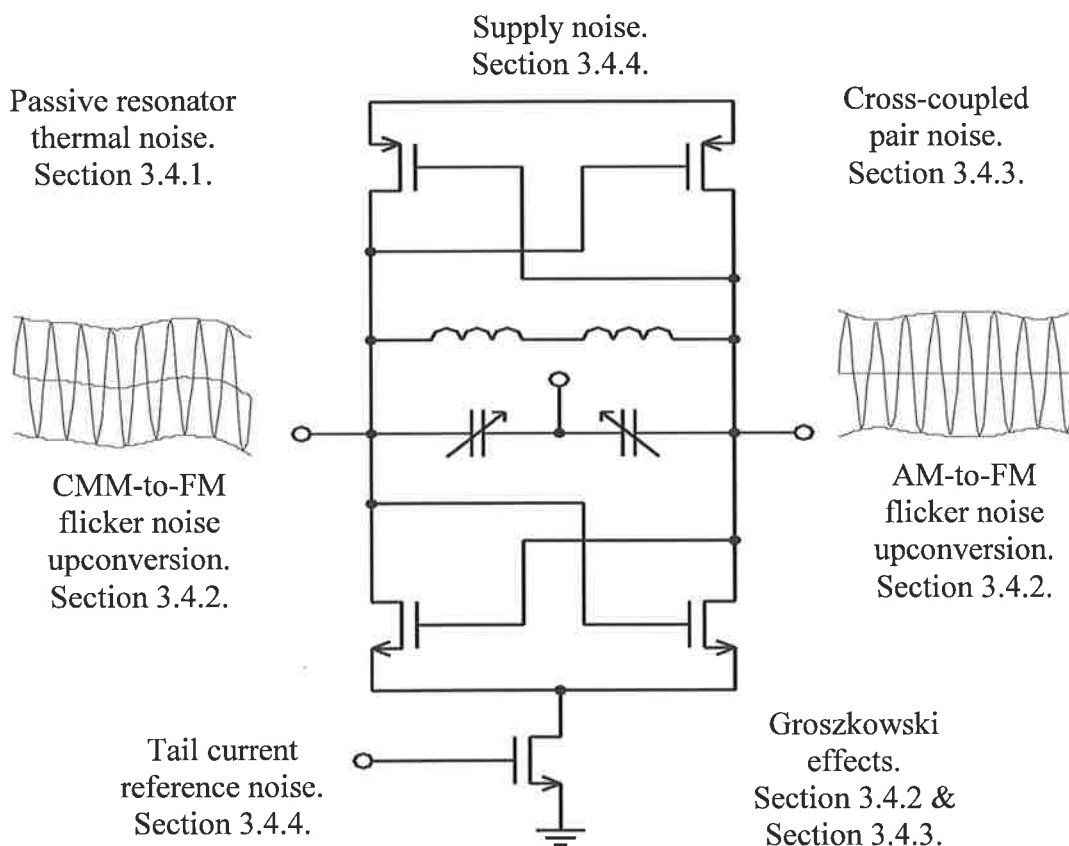
Fig. 3.29: Noise sources and processes affecting the oscillator phase noise.

3.4.1 Passive Resonator Noise

A practical *LC* tuned circuit of a VCO is more than just a simple parallel connection of *L* and *C*. As described in the previous section, the capacitance consists of a fixed part and variable parts.
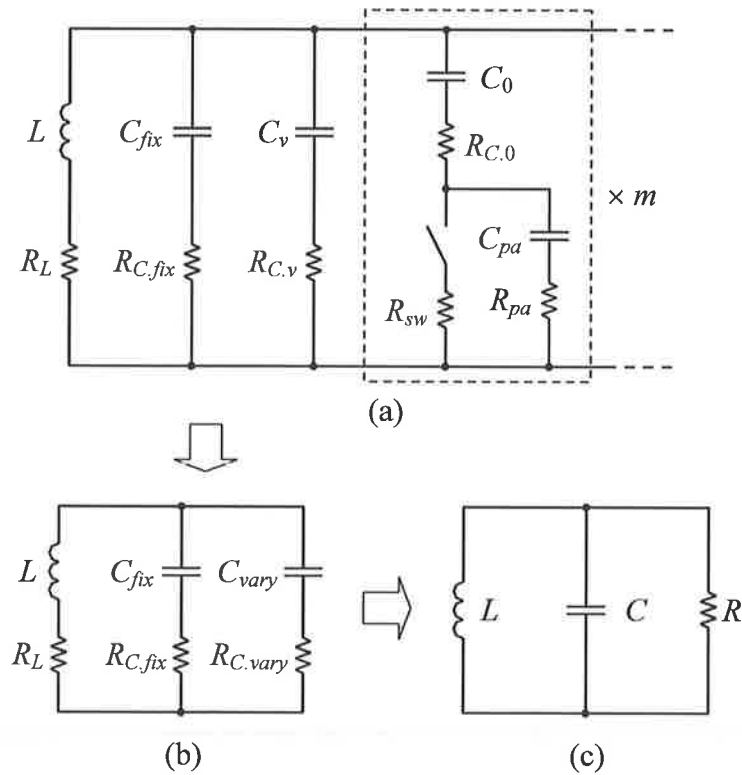
Fig. 3.30: Equivalent circuits of a passive *LC* resonator with an *m*-bit switched capacitor bank.

The equivalent circuit of the tank in Fig. 3.26 can be drawn as in Fig. 3.30(a). R_L and $R_{C.fix}$ are the series resistances of L and C_{fix} respectively. C_v and $R_{C.v}$ are the varactor

capacitance and its series resistance respectively, which vary in the same direction across the frequency tuning range. This is an unfortunate property of a varactor that results in a large difference between the maximum and the minimum values of Q. R_{sw} is the on-resistance of the switch. C_{pa} and R_{pa} are the parasitic capacitance and its series resistance at the drain of the switch transistor respectively. C_0 is a constant capacitor like C_{fix}, and $R_{C.0}$ is its associated series resistance. A switched capacitor bank can be constructed by replicating the least significant switched capacitor block shown in the dashed box $2^m - 1$ times, where m corresponds to the number of digital control bits.

Fig. 3.30(b) is a simplified equivalent circuit that sums all variable capacitors together and represents it as C_{vary}. $R_{C.vary}$ is its equivalent series resistance associated with C_{vary}. Therefore, C_{vary} and $R_{C.vary}$ are functions of the varactor bias condition and the input of the switched capacitor bank. This equivalent circuit can be further simplified to its simplest form as shown in Fig. 3.30(c), where C is the parallel combination of C_{fix} and C_{vary}, and R is the parallel combination of all series resistors, namely R_L, $R_{C.fix}$ and $R_{C.vary}$.

R in Fig. 3.30(c) is also referred to as R_{tank}. It is a useful quantity that allows one to determine the required size of the cross-coupled transistors and the bias current to achieve the desired oscillation amplitude. Also, the oscillation signal power is calculated based on this resistor value and the oscillation amplitude.

White noise in the tank is shaped by the band-pass property of the tank and only a half of it appears as phase noise with −20dB/decade slope when plotted against the offset frequency, f_m as described in Chapter 2. This region is referred to as the − 20dB/decade region of the spectral phase noise plot

3.4.2 Tail Transistor Noise

Transistors used to implement the cross-coupled pair and the tail bias current source have noise associated with their nonzero DC biased conducting channels. The shape of the noise spectrum is a combination of the pink noise near DC and the white noise at other frequencies.

The −30dB/decade slope region of the oscillator output phase noise spectrum is located closer to the carrier frequency as shown in Fig. 2.2. This region is referred to as the −30dB/decade region of the phase noise plot. The flicker noise emerging from all active MOSFET devices with nonzero DC bias current in the circuit contributes towards the phase noise in the −30dB/decade region.

The tail transistor is often pointed to as the dominant contributor of the flicker noise [58], [43], [54], [70]. There are a number of ways in which the near in DC flicker noise of the tail transistor makes its way to the frequency of oscillation.

One way is by amplitude modulating (AM) the output waveform by modulating the gain of the cross-coupled pair with the flicker noise from the tail transistor. AM by definition should only change the amplitude of oscillation, not the phase nor the frequency. However, the effective capacitance of a high gain varactor is a function of oscillation amplitude. Therefore, noisy A_0 results in noisy $C_{v.eff}$, and since f_0 is a function of the total capacitance in the tank, frequency modulation (FM) occurs. This AM-to-FM conversion process is also detailed in [24].

Another way is by modulating the common-mode (CM) or the mean potential of the output waveform with the flicker noise from the tail transistor. This is referred to as

the CMM-to-FM conversion process in [24]. However, this type of flicker noise upconversion process is only relevant to the complementary VCO topology, where the DC bias potential of the output is not firmly defined by any of the AC grounds but defined by the balance between the PMOS and the NMOS cross-coupled pairs. V_{CCP} of a cross-coupled pair is a function of its bias current. Its rate of change with respect to their bias current is not necessarily the same for NMOS and PMOS devices. Even if they were made equal in design stage, process spread could easily offset the balance in practice. Modulation of the mean output potential has the effect of modulating the V_{eff} of (3.4). As a result, $C_{v.eff}$ is modulated, and so is f_0.

Fortunately, other cross-coupled VCO topologies such the NMOS-only topology do not suffer from this particular type of flicker noise upconversion process, because the DC bias potential of the output is firmly defined by the AC ground such as V_{DD}.

Although [24] states that the two flicker noise upconversion processes discussed above only take place in the presence of a strong varactor gain, even a VCO with zero varactor gain is affected by one or both of the upconversion processes. This is because the parasitic gate capacitances of the cross-coupled transistors also form a part of the tank capacitance, and their values are affected by the variations in the oscillation amplitude (AM-to-FM) and/or its mean bias potential (CMM-to-FM). This is similar to how the varactor capacitance is affected by the variations in the oscillation amplitude and/or its mean bias potential [70]. Again, unlike the complementary topology, the NMOS-only VCO is only affected by the AM-to-FM upconversion process only.

In 1934, Groszkowski claimed that a small deviation in an *LC* tuned oscillator's output frequency from its self-resonant frequency is attributed to the mismatch between the stored energy in L and C due to the output waveform distortion or change in the

harmonic content [83]. Ref. [43] claimed that the flicker noise from the tail transistor distorts the gain of the cross-coupled pair, and this in turn distorts the output waveform or changes the harmonic contents of the output. Through the Groszkowski effect, the output frequency deviates from the self-resonant frequency of the tank in the presence of the harmonics. As a result, the frequency modulation by the flicker noise occurs again [43].

While the low frequency flicker noise of the tail transistor contributes towards the -30dB/decade region of the phase noise, high frequency noise at $2\omega_0$ from the tail transistor can downconvert to the frequency of oscillation and also contribute towards the -30dB/decade region of the phase noise [9], [38], [43]. Hajimiri and Lee explain this noise downconversion phenomena based on the observation of the ISF of the tail transistor's drain potential being at twice the oscillation frequency [9], [38], while Rael and Abidi explain it by recognizing the VCO as a single balanced mixer that downconverts noise from $2f_0 \pm f_m$ to $f_0 \pm f_m$ [43].

Both arguments are correct. The ISF associated with the tail transistor has the fundamental frequency at $2f_0$, because the potential at the drain of the tail transistor varies at twice the oscillation frequency [38]. This supports the argument that the tail current white noise around the even harmonics of the output oscillation downconverts to f_0 and appear as phase noise.

From the other viewpoint, a noise component at $2f_0 + f_m$ would downconvert to $f_0 + f_m$ by mixing with f_0 in the oscillator. In the presence of the amplitude limiting effect of a real oscillator, a single tone injected near the carrier ($f_0 + f_m$) is transformed into a phase noise component. This transformation process is well illustrated in [42]. Fig. 3.31 recaptures their illustration.
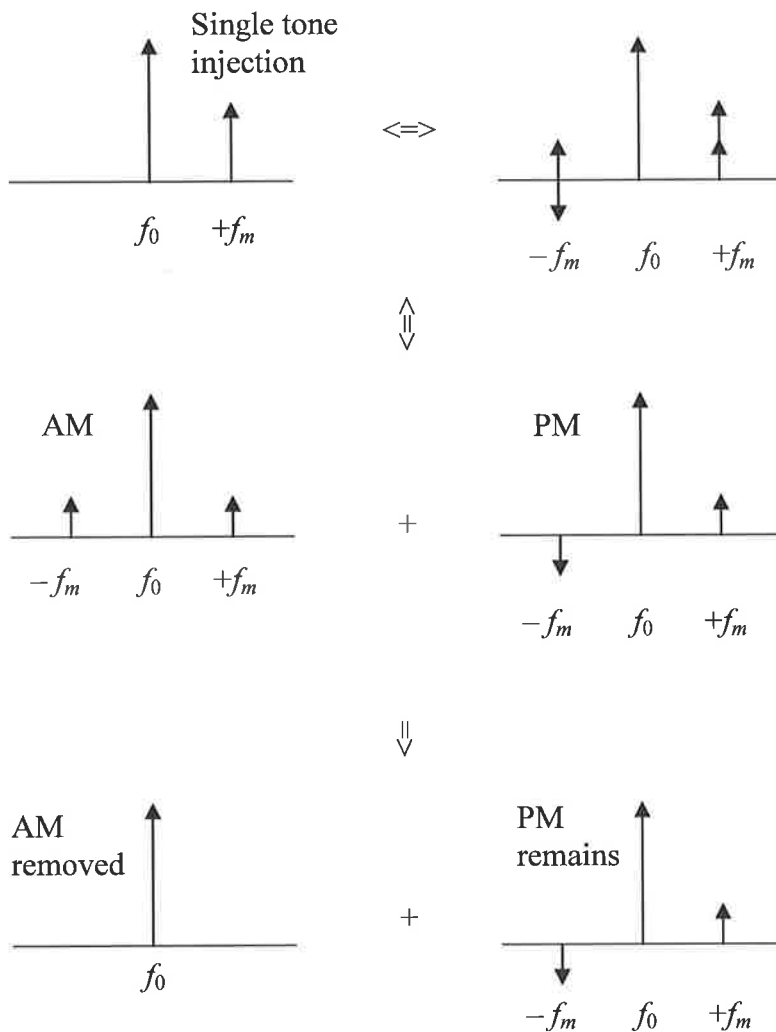
Fig. 3.31: Single tone injected near the carrier transforms to phase noise due to amplitude limiting property of a real VCO.

3.4.3 Cross-Coupled Pair Noise

The cross-coupled transistors also have the low frequency flicker noise as well as the white noise. Ref. [58] states that the flicker noise is a correlated noise and only exists in a system with memory. The switching action of the cross-coupled pair should

remove all memory, and consequently the flicker noise. Unfortunately, complete removal of the flicker noise is not observed in practice, even without the presence of the tail transistor. It is reported that switching transistors exhibit lower flicker noise than transistors biased at a constant DC drain current [82]. Therefore, some reduction in the flicker noise is expected due to the switching action of the cross-coupled pair, rather than a complete removal.

The flicker noise in each of the cross-coupled pair transistors is correlated to each other, because the drain current conduction timing depends on opposite transistor's instantaneous gate and drain potentials. However, since each transistor's gate oxide trap density is independent of each other, the correlation is only partial. Therefore, there will be imbalance between the current sunk by the two transistors due to their flicker noise.

This imbalance in current implies different gain provided by each transistor. It results in an amplitude mismatch between v_{out+} and v_{out-}. As explained in the previous section, the change in oscillation amplitude changes the oscillation frequency due to the variation in the total C in the tank.

A cross-coupled *LC* tuned oscillator can be viewed as two single-ended *LC* tuned oscillators coupled to each other with a 180 degrees phase offset. In the event of gain mismatch between the two sides due to the flicker noise from the cross-coupled pair, the two single-ended sides of a VCO will pull each other in frequency and settle at a frequency between the two different frequencies of oscillation. This frequency averaging effect helps to reduce the flicker noise contribution by the cross-coupled pair. This is considered as another advantage of the differential circuit.

Rael and Abidi claimed in [43] that the flicker noise from the cross-coupled pair modulates the duty cycle of the commutating current waveform. This in turn modulates

the negative impedance looking into the drains of the cross-coupled transistors. The sum of the parasitic capacitances present at the common-source node of the cross-coupled pair is seen as a negative capacitance modulated by the flicker noise. Another Groszkowski's equation is provided in [43] to describe the frequency modulation caused by this modulating negative capacitance seen through the drains of the cross-coupled transistors. This is their basis for arguing that the use of tail bypass capacitor should be avoided.

However, it contradicts the claims made by Hajimiri and Lee in [9] and [38], where they claimed the use of a tail bypass capacitor improves the waveform symmetry and thereby reduces the flicker noise upconversion from the tail transistor. That is because the DC value of the ISF that is responsible for the upconversion of the flicker noise approaches zero as the waveform symmetry improves.

Going back to the arguments made by Rael and Abidi, they claimed that the flicker noise originating from the cross-coupled pair does not directly upconvert to f_0, but directly upconverts to $2f_0$. Because the cross-coupled pair samples the low-frequency noise in the drain current at a sampling rate of $2f_0$, and therefore, the sampled noise current impulses have a fundamental frequency at $2f_0$ [43]. Instead, they explain the upconversion of the flicker noise to f_0 by the Groszkowski effect mentioned above.

However, it is observed in this research work that the direct upconversion of the flicker noise from the cross-coupled pair does in fact exist. As mentioned earlier, the flicker noise originating from each of the cross-coupled transistor is partially correlated to each other. The correlated components of the flicker noise from the cross-coupled transistors are in phase of each other, and show the similar effects as the flicker noise originating from the tail transistor, namely the AM-to-FM and the CMM-to-FM

upconversion processes. This is experimentally demonstrated in Chapter 5 that the flicker noise from the cross-coupled pair is upconverted to f_0, in the absence of the Groszkowski effect.

Lastly, the white noise components of the cross-coupled pair near the positive integer multiples of f_0 are downconverted or folded in frequency to f_0, according to [9]. Contributions from the higher order harmonics are rapidly diminishing as the downconversion gain diminishes rapidly with the increasing harmonic number. Therefore, only the first few harmonics are considered to be important in practice. The ISF associated with the cross-coupled transistors have the fundamental frequency at f_0. Therefore, any noise injected close to the harmonics of f_0 downconverts and appears as phase noise.

3.4.4 External Noise Sources

The noise sources and the frequency conversion processes of noise considered thus far are all internal to the VCO. External noise includes any noise injected from outside of the VCO.

The noise in the tail bias current is usually more than the contribution from a single tail transistor, because the diode-connected transistor that mirrors its drain current to the tail transistor is not noiseless [24].

For a low-noise operation, the diode-connected transistor is given the same gate width as the tail transistor and sinks the same amount of current. The current sunk by the diode-connected transistor does nothing more than simply defining the DC bias gate

potential for the tail transistor. This bias current can be quite wasteful for VCOs drawing tens of milliamps. A simple way of reducing this current wastage would be to narrow down the width of the diode-connected transistor and use the current multiplication property of the current mirror.

While this technique may reduce the power consumption of the diode-connected transistor, the VCO may suffer from increased tail current noise. Because the current mirror multiplies the noise current in the diode-connected transistor along with its bias current. Furthermore, since the flicker noise is inversely proportional to the gate area of the transistor, the narrower diode-connected transistor exhibits a larger flicker noise to drain current ratio than that of the tail transistor.

In a highly integrated circuit environment, the VCO may share the voltage source with other circuit modules in the system. Any real voltage source has some finite output impedance. Also, the current drawn by the other circuit modules sharing the same voltage source are not necessarily constant at all times. Therefore, the supply voltage rail is bound to fluctuate.

The fluctuation in V_{DD} may be a mixture of deterministic signals and random signals. As far as the operation of the VCO is concerned any frequency components other than the oscillation frequency are considered as noise.

Noisy V_{DD} can directly modulate the DC bias potential of the output waveform of the NMOS-only topology with NMOS tail biasing. The CMM-to-FM upconversion process discussed in section 3.4.2 upconverts low frequency noise fed through V_{DD} to phase noise. Other topologies such as the complementary topology with a tail bias transistor are slightly less affected by the supply noise.

Also, noisy V_{DD} may modulate the bias current of the VCO through channel length modulation of the tail transistor. If I_{tail} is modulated by the supply noise, AM-to-FM upconversion of the supply noise would take place. Therefore it is essential to maintain the tail bias transistor in saturation region at all times to keep its output impedance high.

To further improve the supply rejection, transistor gate length larger than the minimum should be considered for the tail transistor. It has added benefit of increased gate area that results in lower flicker noise. The price paid is a slightly increased chip area consumed by the tail transistor, which is often negligible.

It should be noted that only the low frequency noise upconverted through the two upconversion processes appear as close-in phase noise. Since an on-chip capacitor cannot be made large enough to filter out near DC noise components in the supply rail, use of internal bypass capacitors does not help to clean up the low frequency noise.

Any noise present at the frequency control input of the VCO is another example of externally fed noise. Ideally, the VCO control input should be at near DC or has frequency components less than the loop filter's bandwidth when used in a PLL. Unfortunately, the switching noise of the charge pump and the phase/frequency detector are not completely filtered out by the loop filter. The switching noise is concentrated at the reference frequency. Therefore a typical spectral plot of a PLL output contains spurs on both sides of the carrier frequency with offset frequencies equal to the reference frequency [1], [47].

Lastly, in a bulk silicon process where the substrate is conductive, substrate noise originating from other circuits on the same substrate can couple to the VCO. Although coupled noise would be common-mode to the VCO, the presences of

nonlinear devices such as the varactors make it possible for the coupled noise to frequency modulate the output.

3.5 CONCLUSIONS

Some of the popular cross-coupled *LC* tuned VCO topologies used in CMOS processes are studied in this chapter. All VCO topologies presented here have their own pros and cons. No one topology is considered to be superior over all other topologies. The choice between the complementary topology and the NMOS-only topology should be made based on the given supply condition.

Important findings from section 3.2 are summarized as follows.

- The linear relationships of oscillation amplitude frequently reported in recent literature such as (3.1) and (3.2), or their equivalents for the complementary topology are largely in error. Therefore, they should not be used to estimate oscillation amplitude.

- The VCO bias region called the 'voltage-limited region' of a cross-coupled *LC* tuned VCO frequently reported in the literature does not exist.

- For a given R_{tank}, A_0 stays at a constant level below V_{CCP} for a wide range of values of I_{tail}.

- The complementary topology does not provide twice the power efficiency over the NMOS-only topology, contradicting claims by some in the literature.

- The complementary topology does not have topological advantage over the NMOS-only topology in terms of phase noise performance.

Section 3.3 investigated various frequency tuning methods available in CMOS. In a modern CMOS process, continuous frequency tuning is easily implemented by a number of MOS varactors. The type of MOS varactor to use is decided based on the dynamic range of the oscillator output waveform and the dynamic range of the frequency control signal.

The maximum to minimum capacitance ratio trades against the quality factor of the varactor.

When the continuous tuning range offered by MOS varactors is not sufficient to cover the full frequency range required by the application, a discrete frequency tuning scheme may be added to extend the tuning range without affecting the VCO constant, K_V. However, one should be prepared for some degradation in the loaded Q of the tank, as Q of the switched capacitor bank is less than the fixed capacitor Q.

Section 3.4 identified various noise sources both internal and external to a VCO. Noise components at frequencies other than the fundamental frequency of oscillation can be folded in frequency domain and accumulate around the frequency of oscillation. Hence, the phase noise is a combination of all folded noise components from the near DC flicker noise and the white noise around the harmonics of the frequency of oscillation.

Understanding what contribute to the phase noise, and how, makes it possible for one to develop a systematic way of designing high performance VCOs. The following chapter concentrates on the development of the design methodology of high performance VCOs based on the findings of this chapter.

Chapter 4

OPTIMIZATION TECHNIQUES

4.1 INTRODUCTION

The sources of oscillator phase noise can be both internal and external to the oscillator, as discussed in the previous chapter. While contributions from the external noise sources may be reduced by appropriate filtering or isolation techniques, the internally generated noise sources cannot be isolated from the oscillator circuit. Therefore, every effort shall be made to reduce the internally generated noises, and their frequency translation into the oscillation frequency.

In this chapter, optimization techniques for the individual building blocks of a cross-coupled LC tuned VCO are developed. Section 4.2 discusses various inductors available in CMOS processes. A new geometric optimization technique is developed for the monolithic planar spiral inductors in section 4.3. Section 4.4 develops a new optimization technique for an LC tuned oscillator by exploring the impact of the ratio between L and C on phase the noise performance and the power consumption. Section 4.5 describes optimization of the transistor gate geometries of the cross-coupled pair

and the tail transistor. Section 4.6 discusses a couple of other optimization measures to ensure low-noise and low-power operation of a VCO.

4.2 MONOLITHIC INDUCTORS

All the passive electrical components, namely resistors, capacitors and inductors are made monolithically in modern CMOS processes. Of those, the inductor is considered as the most non-ideal and difficult-to-model component.

A number of different types of inductor are compatible with the modern CMOS processes. Monolithic active inductor, discrete external inductor, bond-wire inductor, MEMS inductor, and monolithic planar spiral inductor are among the ones proven to be compatible. Although, technically possible to implement, not all of these inductors are suitable for low cost mass production.

Investigation of discrete external inductors is excluded in this study, because they do not form an integral part of a packaged CMOS chip. Besides, the size of parasitic inductance associated with bond-wires, and the wire leads of a packaged chip, is often the same order of magnitude as the inductance required for 5GHz or higher operation. These values are difficult to control over wide process variation.

Properties of inductors, other than the discrete external inductor mentioned above, are investigated in this section. As the planar spiral inductors are considered as the most cost effective way to realize passive inductance on chip, their optimization is investigated in detail.

4.2.1 Active Inductors

Transistors are the most abundant, and readily available devices in a CMOS process. An active inductor is constructed mostly with active transistors and a small number of resistors and capacitors. The idea behind the active inductor is that they use active transistors to transform the impedance of a capacitor to an inductive impedance [81].

A typical active inductor exhibits very large Q over a wide range of frequencies. Ref. [109] reported a VCO employing an active inductor with Q over 100 in the vicinity of 1.7GHz, over 18% tuning range. Within the tuning range, the peak inductor Q measured over 3400. The tunability of an active inductor is provided by the varying capacitance of a varactor [77].

It has been reported that active inductors can provide unmatched parameter flexibility by allowing for independent control over L and Q as desired [77].

According to the linear approximation of the oscillator phase noise in (2.12), the phase noise should improve dramatically with a large value of Q. Unfortunately, none of the high performance VCOs reported to date feature active inductors in their resonator. The VCO phase noise reported in [109] was around −100dBc/Hz at 1MHz offset while drawing 45mA from a 9V supply by the active inductor alone. Even the ring oscillator reported one year earlier outperformed the phase noise by 9dB, while consuming far less power [29].

Excessive noise from the active devices used in the active inductor is the problem [35], [109]. It can be viewed as the oscillator noise factor, F in (2.12) is growing faster than the square of Q [9]. Besides, Q in (2.12) is the loaded Q of the LC tuned circuit, not the quality factor of the inductor alone. (4.1) shows how the loaded Q of a tank, Q_{tank} is determined.

$$\frac{1}{Q_{tank}} = \frac{1}{Q_L} + \frac{1}{Q_C} \tag{4.1}$$

where Q_L and Q_C are the quality factors of the inductor and the capacitor respectively. Although Q_C in a modern CMOS process is quite high, often it is below 100 when wide frequency tuning schemes operating at multigigahertz frequencies are used. Therefore, the exceptionally high Q_L of an active inductor is masked out by Q_C, and does not contribute towards a dramatic improvement in the phase noise.

The fact that the inductance of an active inductor can be tuned is advantageous in a VCO design. However, since their inductance is based on the impedance of a capacitor, the wide process spread of capacitance in a CMOS process makes it difficult to control the inductance.

Traditionally, active inductors are used for the implementation of monolithic active filters, where the high frequency selectivity is the utmost importance [109]. Nevertheless, use of active inductors in oscillators should be limited to systems where the phase noise requirement is relaxed, such as the clock and data recovery circuit reported in [8].

4.2.2 Bond-Wire Inductors

Conventional packaging of a chip involves bonding wires between the pads on the chip and the pin frame on the package. The wires that make connections from the pads to the pin frame are called bond-wires.

Typical bond-wire inductance ranges from 1nH to 10nH [73], [85]. Every millimeter of bond-wire approximately equates to 1nH of inductance [72].

The series resistance of a bond-wire inductor is so low that its Q has been reported as high as 80 at 1.9GHz [86]. Unlike the active inductors, the bond-wires are passive, which means the improvement obtained in the loaded Q of the tank is directly passed on to the improvement of phase noise without affecting the phase noise factor, F in (2.12). Indeed, a CMOS VCO employing bond-wires as its inductors has unmatched phase noise performance [87]. In 1995, a CMOS VCO using bond-wire inductors featuring FOM of −180.3dBc was reported [88]. CMOS VCOs featuring such a high FOM without bond-wire inductors were only reported about four year later [44].

Since bond-wires have relatively constant diameter, the length is the only means of controlling its inductance. Unfortunately, the bond-wiring process is not a well-controlled process that the length of the bond-wire suffers from a wide process spread. Typical spread of bond-wire inductance is around ±20% [85]. Together with ±20% process spread of capacitors in a CMOS process, it becomes extremely difficult to meet the frequency tuning range requirements. This is because the varactors or the switched capacitor bank would now have to provide ±40% variation in C just to cover the process spreads.

Attempts were made to reduce the process spread of a bond-wire inductor by adding a relatively constant on-chip planar spiral inductor in series [73], [85]. The typical process spread of an on-chip spiral inductor is around ±5% [85]. However, as the process variation of the composite inductor is reduced, the overall Q is also reduced.

A wider frequency tuning range is needed to account for the wide process spread of bond-wire inductors. That degrades the quality of the capacitance in the tank as discussed in the previous chapter. Therefore, in practice, the improvement in phase noise by using bond-wire inductors is not as high as those reported in the literature, while the design complexity is increased.

Nevertheless, the applications where high performance is desired and the yield is not considered important, bond-wire inductors can deliver the performance.

4.2.3 Planar Spiral Inductors

In a large-scale integration (LSI), the most commonly found type of monolithic passive inductor is the planar spiral inductor. It is readily available to any LSI process featuring metal interconnect layers, without any process modification.

The typical back-end process only offers a handful of stacked metal layers with relatively small vertical separations between the layers and so the inductor is planar. Typical vertical separation between two adjacent layers is usually of the order of 1μm or less, whereas the lateral dimension of a typical spiral inductor structure easily exceeds 100μm or more.

(a)

(b)
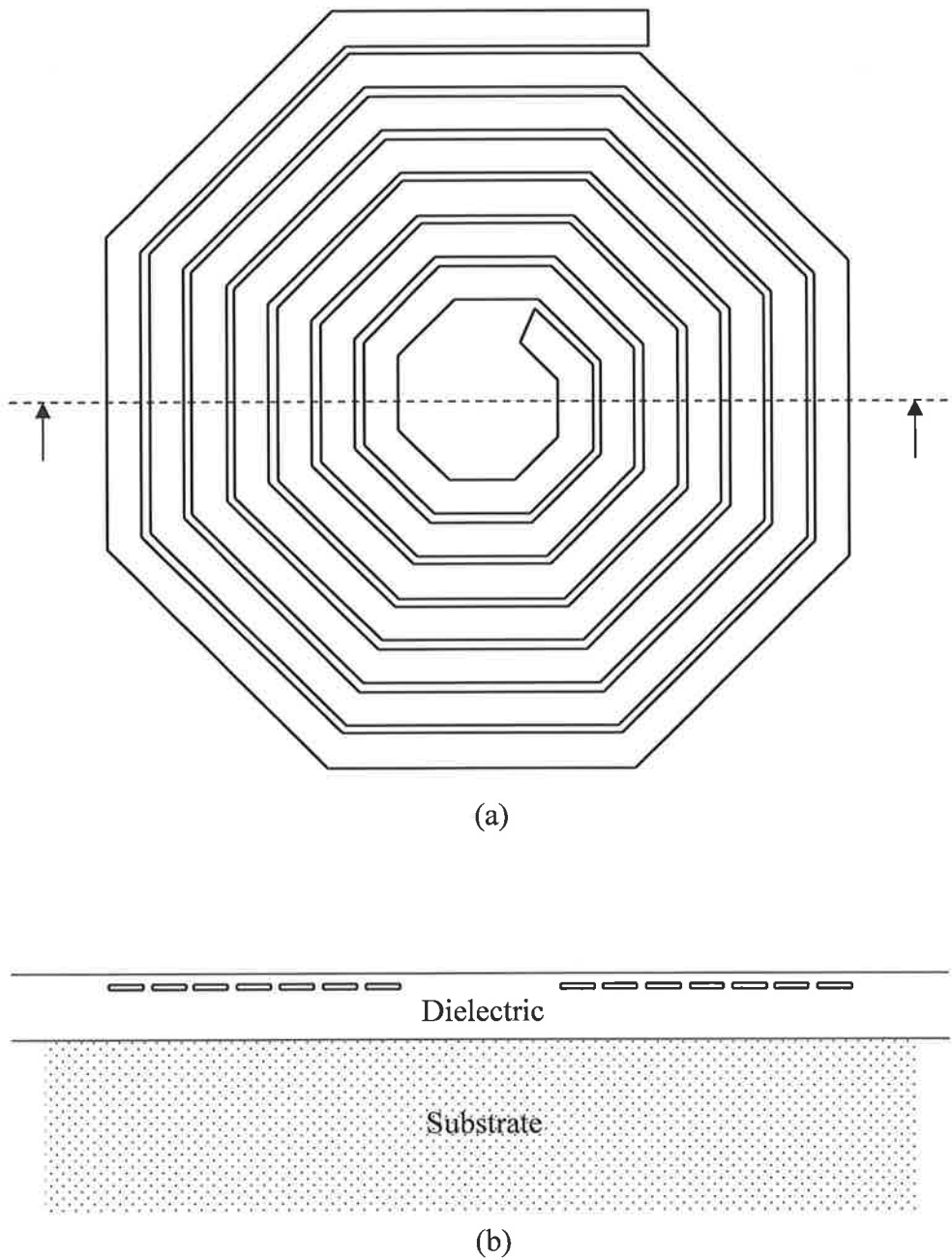
Fig. 4.1: (a) Top view, and (b) cross-sectional side view of an octagonal planar spiral inductor.

In order to gain a sufficient inductance, multiple current loops are created by spiraling inwards, rather than stacking up vertically as in a solenoid. Although there

might exist say, six layers of metal in the TSMC 0.18μm bulk CMOS process, creating an inductor by staking up multiple layers of current loops on top of one another is avoided. The reason for this is that the parasitic capacitance between each layer, vertically separated by a thin film of dielectric, severely limits the maximum operating frequency of the inductor.

The width of the loops or turns is usually made much larger than the thickness of the metal layer in order to reduce the ohmic loss in the conductor. The parasitic capacitance resulting from small lateral separation of spiral turns typically in the order of few micrometers is considered not as detrimental as the parasitic capacitance resulting from the vertically stacked turns. This is because the thickness of the conductor is much lower than the typical width. An example layout view of an octagonal spiral inductor is shown in Fig. 4.1.

The lateral geometric process spread of metal layers is relatively well controlled to within 5% variation in a typical CMOS process. Therefore, spiral inductors make an excellent candidate for passive monolithic inductors.

4.2.4 MEMS Inductors

MEMS inductors are probably the second best CMOS compatible on-chip inductors, after the bond-wire inductors in terms of the quality factor. They have been devised to reduce or eliminate the substrate effects of planar spiral inductors in bulk processes.

Implementation of these inductors involves a micromachining post process, which is a nonstandard CMOS processing step. Front side bulk micromachining post process involves etching away of the substrate from the top of the wafer, thereby introducing a large air gap between the spiral and the substrate [89], [90], [91]. Although the substrate under the spiral is not completely removed and the magnetic coupling to the substrate still exists, improvement in Q reported is from 5 to 20, before and after the post process. Also, the frequency where the maximum Q occurs is shifted from 3GHz to 7GHz [91]. The improvement is mainly due to the reduced parasitic capacitance to the substrate and increased self-resonant frequency (f_{self}).

When electroless copper plating was used in [92] in addition to front side etching, the resulting maximum Q was as high as 30.

A completely new layer of thick spiral inductor structures suspended in air by using a custom surface micromachining technique was reported in [93]. A Q of over 25 was achieved in the 1~4GHz range.

Back side bulk micromachining technique involves etching of the substrate from the back of the wafer [94], [95]. This method completely removes the substrate under the spiral. The resulting spiral inductors have the similar properties as those found in SOI processes. Using this technique, f_{self} was increased from 7GHz to over 10GHz, and the maximum Q was increased from 3.5 to 20 [95].

Another interesting MEMS inductor example is reported in [96], where three-dimensional self-assembling out-of-plain coils are implemented. An inductor Q of 85 was measured at 1GHz.

Despite the performance boost of monolithic inductors using these various MEMS technologies, there are reliability concerns such as packaging yield, and long-

term mechanical stability. Furthermore, since none of these MEMS processes is supported in the mainstream CMOS industry, low-cost integration of MEMS inductors becomes difficult to achieve in practice [97]. Therefore MEMS inductors are not widely accepted as a standard in RF CMOS processes.

4.3 SPIRAL INDUCTOR OPTIMIZATION

Although a monolithic spiral inductor is not the highest quality inductor available in a CMOS process, it certainly is the cheapest and most accurate one to implement.

The often-poor Q of a spiral inductor is the only major downside to it. The quality of a spiral inductor is mostly determined by its physical shape and size. By optimizing the shape and size, we obtain the highest quality spiral inductors achievable in a given process can be implemented.

4.3.1 Simple Inductor Expressions

Traditionally, an inductance is obtained by forming one or more current loops enclosing a given area or space. A coil wound around an air core or a ferrite material is a good example of a simple inductor that yields high inductance to volume ratio, because the magnetic flux generated by the current loops is concentrated in the core of the loops. A well-known inductance equation for an air-cored solenoid is given as (4.2) [98].

$$L = \frac{\pi \mu_0 N^2 r^2}{l_{sol}} \qquad (4.2)$$

where μ_0 is the magnetic permeability of free space, N is the number of current loops, r is the radius of the current loops, and l_{sol} is the length of the solenoid, or the height of the current loop stack.

Although a spiral inductor has somewhat different geometric properties to a solenoid, the physics is the same. The inductance of a spiral inductor is approximately proportional to the square of the number of turns and the square of the mean radius of the spiral.

Simple inductance formulas for discrete spiral inductors have been first proposed by Wheeler, in 1928 [99]. Later, they have been modified to improve accuracy in the integrated environment.

In Ref. [100], a modified Wheeler expression is provided for square, hexagonal, and octagonal inductors. The inductance expression is accurate to within 3% error when compared to results from 2.5-D field solver simulations, and within 5% error when compared to measured results. The modified Wheeler expression is given in the following equation [100],

$$L = K_1 \mu_0 \frac{n^2 D_{avg}}{1 + K_2 \rho} \qquad (4.3)$$

where n is number of turns, μ_0 is the magnetic permeability of free space, ρ is the fill ratio defined as $(D_{out}-D_{in})/(D_{out}+D_{in})$, where D_{out} and D_{in} are the outer and inner diameters of the spiral respectively, D_{ave} is the average diameter, and the coefficients K_1 and K_2 are given in table 4.1.

Scalable closed-form expressions for square and octagonal inductors have been proposed in [101]. Accuracy of these expressions is quite similar to that of modified Wheeler's expressions and has the added advantage of geometric scalability.

Table 4.1: Coefficients for modified Wheeler Expression.

Layout	K_1	K_2
Square	2.34	2.75
Hexagonal	2.33	3.82
Octagonal	2.25	3.55

Although these inductance expressions of various spirals are simple and easy to use, their accuracy falls as the frequency of operation increases. The high frequency effects of monolithic spiral inductors are discussed in the following section.

4.3.2 High Frequency Inductors

The high frequency effects affecting the quality of monolithic spiral inductors include the skin effect, the proximity effect, and the substrate effects such as capacitive coupling, and magnetic coupling.

Skin effect is a tendency for RF current to flow mostly near the outer surface of a solid conductor. Skin depth (δ) is a depth into a conductor, where the magnitude of current density becomes e^{-1} of the current density at the surface of the conductor [102]. The skin depth is given as (4.4).

$$\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}} \qquad\qquad (4.4)$$

where ω is the angular frequency of the current, μ and σ are the permeability and the conductivity of the conductor respectively.

The magnetic field generated by nearby turns in a spiral generates eddy currents in the conductor. This is referred to as the proximity effect [87], [103]. The proximity effect has a more profound effect on the current distribution across the conductor width than the skin effect [103].

The eddy current generated on a conductor opposes the magnetic field that generated the eddy current. As a result, the current across the conductor width is pushed to one side. In an extreme case, where the magnetic field is very strong near the center of the spiral for example, negative current is observed on the outer edge of the conductor [87]. The consequence of the high frequency effects like the skin effect, or the proximity effect, is that they effectively increase the equivalent series resistance of the inductor.

Fig. 4.2 illustrates the effect of eddy current on the current distribution of a square spiral inductor. Without the proximity effect, the current distribution across the conductor width at high frequency should be like the current density (J) shown in Fig. 4.2(a), where the current density is higher around the edges. That is due to the skin effect alone.

In the presence of the proximity effect, eddy current is formed where there is a change in magnetic field. Towards the center of the spiral, the magnetic field is intensified, hence the eddy current generated is stronger than the ones generated in the outer turns [87]. Near the outermost turn, the magnetic field is much weaker and has

opposite direction to the magnetic field near the center. Therefore, the eddy current generated is opposite in direction and much weaker. Fig. 4.2(b) shows how the current density changes across the turns. Note that the innermost turn has higher current density on the inner edge of the turn, while the outermost turn has higher current density near the outer edge of the turn.

(a)   (b)
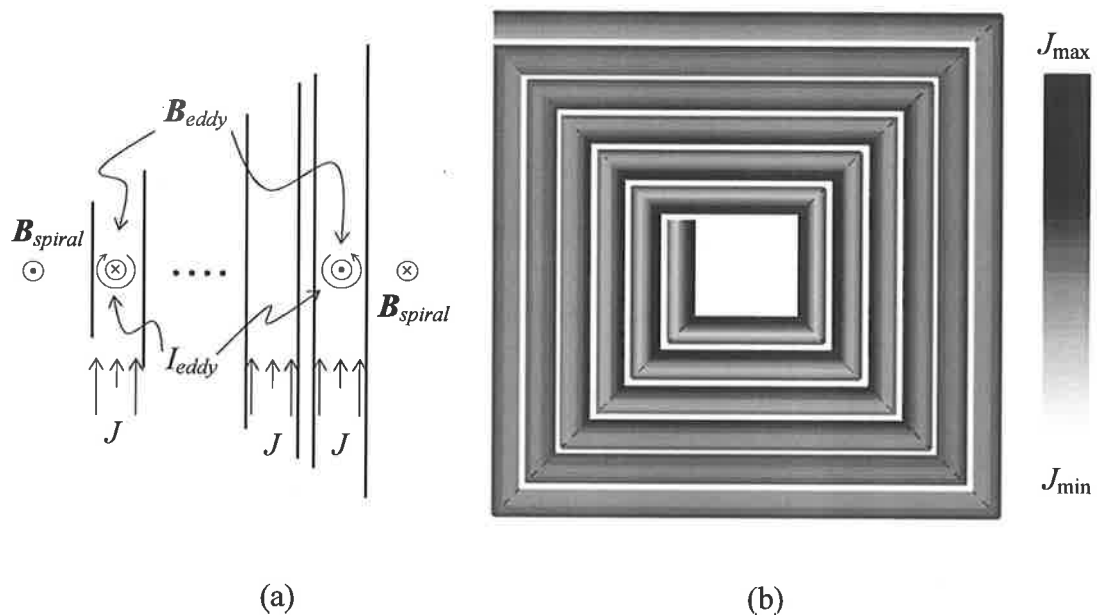
Fig. 4.2: (a) Eddy current generation, and (b) resulting current density plot generated by ASITIC.

The current crowding as a result of eddy current increases the effective series resistance of the conductor. Turns near the center of the spiral are mostly affected by the current crowding. Simulations show higher resistance is observed from the inner turns rather then the outer turns at high frequencies, despite the fact the inner turns have shorter conductor length [87].

An inductor layout optimization technique has been proposed in [95], where the width of the conductor is progressively made narrower towards the center of the spiral.

The idea is to reduce the eddy current generation near the center of the spiral by making the conductor width narrower towards the center. However, improvement in Q was not convincingly high, because the narrower conductor increased the series resistance of the inductor at the same time.

On the other hand, the hollow spiral inductors proposed in [87] are more effective in reducing the proximity effect. The innermost turns of a spiral constitute a relatively small part of the overall inductance, while making a significant contribution towards the overall series resistance. Therefore the innermost turns are better to be left out of the spiral. A small loss of inductance can be compensated by slightly enlarging the spiral diameter. ASITIC simulations show that at 5GHz, two square inductors shown in Fig. 4.3 have the same inductance of 3.2nH, while the series resistance is 13% lower with the hollow inductor on the right hand side.

(a)   (b)
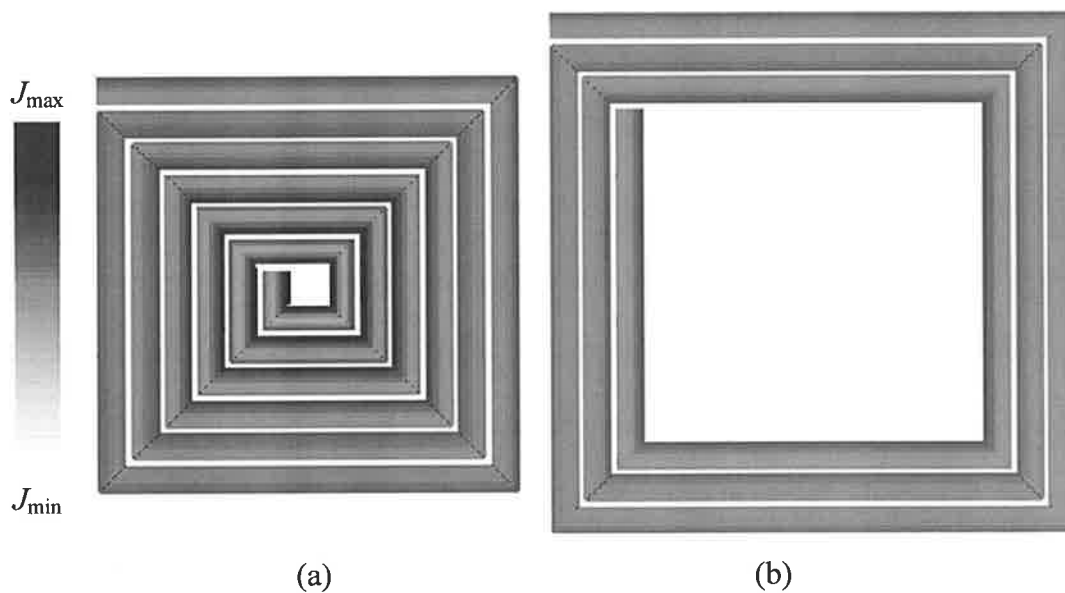
Fig. 4.3: Current crowding reduction by hollow spiral geometry.

The vertical separation of a typical spiral inductor from the substrate is very small compared to the diameter of the spiral. Therefore, almost half the magnetic flux path around the spiral is made though the substrate. In an SOI process, where the substrate is insulating, this is not a problem, because there is no free charge in the substrate to interfere with the changing magnetic field. However, with a conductive bulk substrate, it can cause a number of problems for the spiral inductor.

The changing magnetic field of a spiral inductor generates eddy current in the conductive substrate. This causes thermal dissipation in the substrate. The thermal loss in the substrate effectively increases the equivalent series resistance of the inductor.

In addition, the induced eddy current in the substrate generates a magnetic field of its own, which opposes the magnetic field that originally created it. The consequence is a weakened net magnetic field. That implies reduced stored energy, or reduced inductance.

Another side effect associated with a low resistive substrate is that the parasitic capacitors between a spiral and the substrate strongly couple the inductor to the substrate. Therefore noise, or undesired signals, may couple to or be coupled from the substrate and interfere with the circuit employing the inductor or circuits nearby.

In addition, the parasitic capacitors are bound to resonate with the inductor at a certain high frequency, where the inductance and the quality factor of the inductor structure effectively become zero. This frequency is referred to as a self-resonant frequency, or f_{self}.

Fortunately, modern bulk CMOS processes allowing for mixed-mode operations have much higher substrate resistivity than that of the purely logic processes. The typical substrate resistivity of a mixed-mode process is as high as few tens of Ωcm,

whereas the typical substrate resistivity of a digital epitaxial processes is in the order of few tens of mΩcm.

Nevertheless, even with high resistivity substrates, the substrate effects discussed above are only weakened but are still present. Consequently, one must be aware of these effects in order to optimize the performance of monolithic spiral inductors.
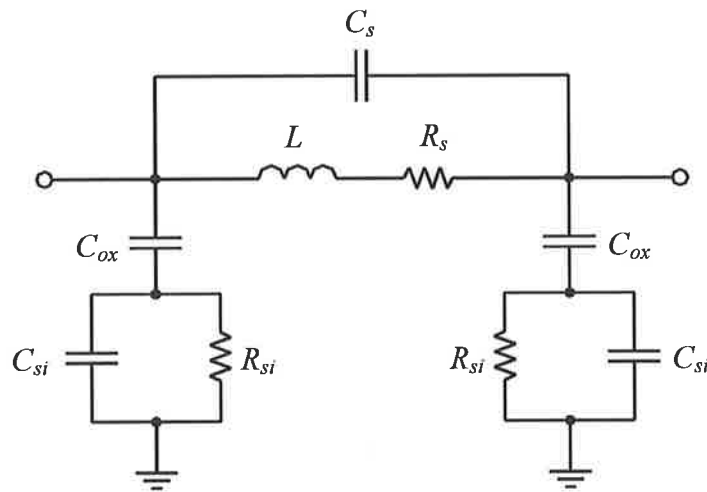
Fig. 4.4: Physical Π model of a spiral inductor on a lossy substrate.

Fig. 4.4 shows a physical Π model commonly used to represent a spiral inductor on a lossy substrate [97], [103], [104]. At high frequencies, the series inductance of the spiral (L) decreases slightly due to the induced eddy currents on the conductor and the substrate.

Also, at high frequencies, the skin effect, the proximity effect, and the thermal dissipation in the substrate increase the series resistance of the inductor (R_s) from its DC value.

C_s is a shunt capacitance between the two output terminals, mainly originating from the capacitance at the crossovers between the spiral and the under path connection accessing the inner terminal of a multi turn spiral. For a single turn inductor, this capacitance can be negligible because there is no need for an under path.

C_{ox} is the parasitic oxide capacitance between the spiral and the substrate. And the silicon substrate capacitance and resistance are modeled by C_{si} and R_{si} respectively.

In Ref. [97] C_{ox}, C_{si} and R_{si} are replaced with a parallel combination of C_p and R_p for simplicity as shown in Fig. 4.5. Measurements reported in [97] show that C_p and R_p decrease with increasing operating frequency. At low frequencies, the electric field from the spiral terminates at the substrate surface but, as frequency increases, the electric field starts to penetrate into the substrate and terminates inside the substrate, resulting in decreased series combination of C_{ox} and C_{si}. Also, the decrease in R_p signifies increased energy dissipation in the substrate due to electric field penetration into the lossy substrate.
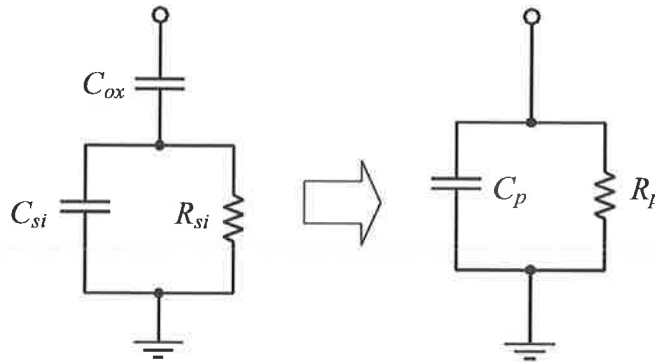
Fig. 4.5: C_{ox}, C_{si} and R_{si} replaced with a parallel combination of C_p and R_p for simplicity.

The quality factor of a spiral inductor is given as (4.5) based on the circuit components shown in the Π mode [97]. It represents Q_L as a product of three terms.

The first term is a common definition of a lossy inductor Q in the presence of series inductance and resistance alone, the second term accounts for ohmic loss in the substrate due to capacitive coupling, and the last term is responsible for the rapid drop in Q_L as the operating frequency approaches f_{self} [97].

$$Q_L = \frac{\omega L}{R_s} \cdot \frac{R_p}{R_p + R_s\left[\left(\omega L / R_s\right)^2 + 1\right]} \cdot \left[1 - \frac{R_s^2\left(C_s + C_p\right)}{L} - \omega^2 L\left(C_s + C_p\right)\right] \quad (4.5)$$

A patterned ground shield (PGS) constructed underneath a spiral with polysilicon layer [97] or the n^+ buried n-well layer [105] is shown to reduce the degradation of Q_L due to the second term in (4.5). The idea is to provide a low resistive path to ground at the substrate surface, and effectively shield out the substrate from the electric field generated by the spiral. By making R_{si} small, R_p is enlarged, and the second term in (4.5) approaches unity.

A side effect to this is that C_p now stays high across frequency, causing shift of f_{self} to a lower value. In addition, the PGS may effectively shield out the electric field, but it is ineffective in shielding out the magnetic field. Therefore the magnetic coupling to the substrate still exists. This is a more significant problem with the low resistive digital substrates than the high resistive mixed-mode substrates.

Researchers have developed analytical expressions for broadband spiral inductors in an attempt to speed up the characterization and optimization of spiral inductors [97], [103], [104]. The physical model reported in [97] and [104] accounts for the skin effect and the substrate loss due to the capacitive coupling, but lacks the proximity effect on the conductor and the eddy current effect in the substrate.

A double Π model proposed in [103] fully accounts for the skin effect, the proximity effect, and the substrate effects including the capacitive coupling as well as

the magnetic coupling. However, the set of analytical equations presented are cumbersome to solve. Therefore, optimization based on these equations would be difficult.

Above discussion suggests that predicting inductor performance analytically in RF frequencies is a very complex task. The problem is better handled with a full three-dimensional (3-D) field solver that takes into account as many high frequency effects as possible for good accuracy. Unfortunately, a typical 3-D field solver often requires a large amount of computing resources and simulation time. On the other hand, a 2.5-D field solver using a set of approximations that are applicable to planar spiral inductors such as Sonnet or ASITIC run faster than 3-D field solvers and only require a reasonable amount of computing resources.

4.3.3 Geometric Inductor Optimization

In this geometric inductor optimization process, the field solver ASITIC has been used extensively as a part of the optimization process. A field solver is more accurate than any of the analytical expressions reported to date. A modern microprocessor clocked at a low gigahertz frequency commonly available these days allows a typical inductor problem to be solved within few tens of seconds, making this optimization process feasible.

A flowchart shown in Fig. 4.6 outlines the inductor optimization process developed in this work. The optimization process is designed to produce the most

optimal spiral inductor structure for a given inductance and a given chip area allocated for the inductor.
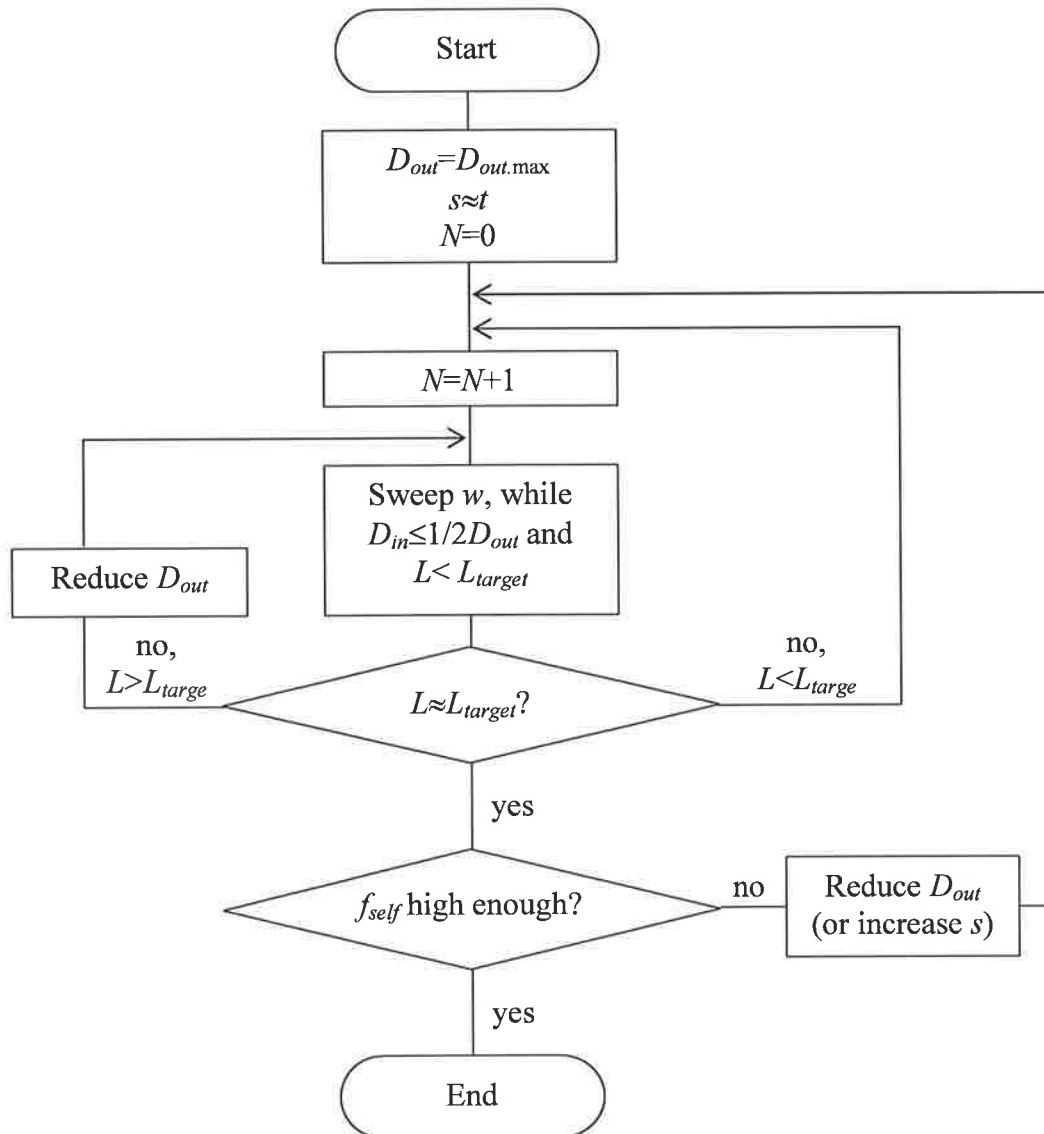
Fig. 4.6: Spiral inductor optimization flowchart.

The optimization process begins with a target inductance (L_{target}), and the maximum area allocated for the inductor. (4.3) implies that L is proportional to N^2 (or n^2) and D_{out} ($\sim D_{avg}$). Therefore,

$$L \propto N^2 D_{out} \tag{4.6}$$

R_s is proportional to the total conductor length (l), and inversely proportional to its width (w). Since l is approximately proportional to the product of the number of turns, N and D_{out}.

$$R_s \propto \frac{N D_{out}}{w} \tag{4.7}$$

Assuming the same fill ratio, N is proportional to D_{out}/w. Therefore,

$$R_s \propto N^2 \tag{4.8}$$

In the absence of a lossy substrate, Q_L is equal to the first term in (4.5). Therefore, (4.6) and (4.8) results in (4.9).

$$Q_L \propto D_{out} \tag{4.9}$$

However, it does not mean that N/w can be chosen freely. Smaller N is preferred to take advantage of the hollow spiral inductor effect. The hollow inductor effect is not taken into account in (4.5), because (4.5) lacks the proximity effect. Therefore, for a given maximum D_{out}, N/w should be kept as low as possible, yet large enough to provide the required inductance. In the flowchart shown in Fig. 4.6, the hollow inductor geometry is ensured by limiting the inner diameter, D_{in} to be no less than half D_{out}.

The upper limit on D_{out} is either set by the chip area available for the spiral or the parasitic capacitance C_p between the spiral and ground. If the spiral is made too large, C_p is also enlarged and f_{self} is lowered. Therefore, if a spiral is suffering from a low f_{self} due to a large C_p, then D_{out} should be lowered to reduce C_p. This adjustment process is also included in the flowchart.

The size of separation between spiral turns (s) is initially given the value of the conductor thickness (t). Low s is preferred to maximize w for given N, D_{out} and D_{in}.

However, if s is made too small, C_s increases, and f_{self} is lowered. Simulations show that $s \approx t$ is sufficiently large enough for low C_s and small enough to allow for large w. If a low f_{self} is primarily caused by a large C_s, then s should be increased rather than reducing D_{out}, when correcting for the low f_{self} problem in the flowchart.

In a mixed-mode process, the top metal layer is usually made thicker than lower metal layers to allow for low-loss spiral inductor construction. In the TSMC 0.18μm mixed-mode process, the sixth, or the top metal layer is 2μm thick, while the other lower metal layers are only 0.53μm thick [106]. In the Peregrine SOS 0.5μm FC process, the top metal layer is 3μm thick, while the lower metals layers are around 1μm thick or less [107]. Also, using the top metal layer rather than any of the lower layers in a bulk process has the added advantage of reducing C_p as it provides the maximum separation from the substrate.

Multi-layer spirals are sometimes used in an attempt to lower their series resistance and improve Q [108]. However, there are issues relating to the multi-layer spirals, which have not been given due consideration in the literature. Their series DC resistance drops with the multi-layer structures, but it may not stay beneficial at RF frequencies because of the skin effect. Also, in a bulk process, the parasitic capacitance between the multi-layer spiral and the substrate is higher due to the utilization of lower metal layers. That causes a drop in f_{self}. The high frequency effects associated with the multi-layer spirals are studied in the next chapter with experimental results from a test chip.

Lastly, the shape of a spiral does not have a strong influence on the inductance to DC resistance ratio of the spiral. Because the commonly used spiral inductor shapes

such as square, octagon, and circle have the same area to perimeter ratio of $r/2$ as illustrated in Fig. 4.7 and summarized in Table 4.2.
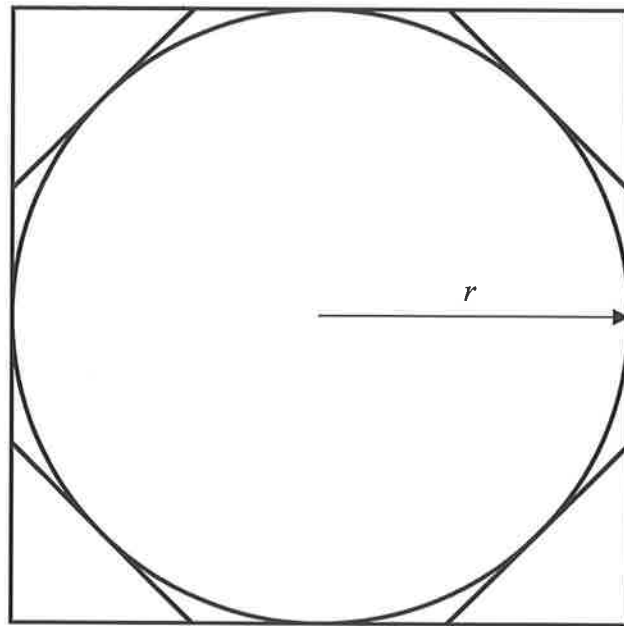
Fig. 4.7: Square, octagonal, and circular shapes have the same area to perimeter ratio.

Table 4.2: Geometric properties of three common spiral inductor shapes.

	Square	Octagonal	Circular
Area	$4r^2$	$8\tan(\pi/8)\,r^2$	πr^2
Perimeter	$8r$	$16\tan(\pi/8)\,r$	$2\pi r$
Area/Perimeter	$r/2$	$r/2$	$r/2$

According to Table 4.2, the square inductor is the most area efficient inductor in terms of inductance per unit area, as inductance is proportional to the area enclosed.

However, the abrupt changes or discontinuities in current flow at every corner of the spiral can cause significant amount of radiation loss at high frequencies [102]. This implies loss of energy and lower Q.

A common rule of thumb in microstrip line design is that the radius of curvature greater than $3w$ gives a corner that is hard to distinguish from a normal straight section of the line. The octagonal shape makes a good compromise between the area efficiency and the radiation loss. Also, an octagonal spiral inductor is much quicker to simulate than a circular spiral inductor consisting of many pieces of straight sections that form the circular spiral.

4.4 *L/C* RATIO OPTIMIZATION

The angular frequency of oscillation of an LC tuned circuit is determined by the inverse of the square root of the product of L and C as in (2.23). As long as the product of L and C stays constant, the frequency of oscillation, f_0 does not vary. Although the ratio between L and C does not affect f_0, the oscillator phase noise and the power consumption are strongly linked to the L/C ratio.

The significance of the L/C ratio has not been given the treatment it deserves in the literature. Of those who have made remarks on the L/C ratio, some prefer it to be high [35], [50], [55], while some prefer it to be low [51], [52], for the same purpose of low-noise operation.

The authors of [50] and [55] claim that increasing the L/C ratio results in a higher Q_{tank}, because they believe Q_L increases with L. Their claim is based on an

assumption that the inductance of a spiral increases faster than its series resistance as the inductance is increased. However, there is no clear evidence, nor report on the increase of Q_L with respect to L. Ref. [52] claimed that Q_L stays relatively constant for a wide range of L, but no evidence was provided to back their claim.

In Ref. [35], Craninckx and Steyaert have stated in their conclusion that the phase noise is completely determined by the parasitic series resistances in the loop. Enlarging the capacitance has no influence on the phase noise but increases the power consumption quadratically with capacitance. Therefore, inductors should be made as large as possible with minimum series resistance. Their statement is true in the sense that smaller series resistances on the inductor and the capacitor result in lower phase noise. Their version of the LTI phase noise expression (4.10) is similar to (2.12) derived in section 2.3.1.

$$\mathcal{L}\{\omega_m\} = \frac{2kTR_{series}(1+\gamma)}{A_0^2}\left(\frac{\omega_0}{\omega_m}\right)^2 \qquad (4.10)$$

where R_{series} is the sum of series resistances associated with the inductor and the capacitor in the tank.

There are two minor differences between (4.10) and (2.12). One is that their expression uses the sum of the parasitic series resistances, rather than the parallel equivalent resistance, hence the disappearance of Q in (4.10). The other is that (4.10) assumes the worst-case noise by including the amplitude noise in the expression. Hence (4.10) is a factor of 2 larger than (2.12). Nevertheless, both expressions are equivalent to each other.

This work has found, contrary to the claim made by Craninckx and Steyaert in [35], that enlarging the capacitance has a strong influence on the series resistance of the

inductor and the capacitor. This in turn has an influence on the phase noise according to their own phase noise equation (4.10).

The following example shows how the increase in the tank capacitance affects the phase noise. The capacitor Q (Q_C) is quite constant with respect to the size of the capacitance since larger capacitance simply means another capacitor of the same type is added in parallel. This does not change the quality of the capacitor. If the tank capacitance is doubled, its parasitic series resistance is halved since Q_C stays constant. In order to keep the same f_0, L needs to be halved. Assuming Q_L stays constant with respect to L, its series resistance is also halved. Therefore, doubling of the capacitance results in halving of the sum of series resistances associated with L and C (R_{series}) in the tank. According to (4.10), the phase noise should be halved as a result.

Nevertheless, if the price paid for the reduction in phase noise by half is quadratically increased power consumption, as claimed in [35], the improvement in phase noise is considered too pricey.

Fortunately, the power consumption increases linearly with C in practice. The following example shows how the power consumption varies with the size of C. The variation of the phase noise with respect to C is also shown for this example.

Assume two identical VCOs under identical bias conditions. If the two VCOs are connected in parallel, such that every pair of nodes with the same potential are electrically connected together, the resulting tank capacitance is doubled, and the inductance is halved, while maintaining the same frequency of oscillation. The new L/C ratio of the resulting VCO is a factor of 4 times smaller than that of each individual VCO. The transistors in the two VCO are connected in parallel, so the current consumed by the resulting VCO is twice the current consumed by each individual VCO.

However, the amplitude of oscillation is unaffected. Noise current sources in the two VCOs are also connected in parallel. Since they are uncorrelated noise sources, the resulting noise current power spectral density is halved. Therefore, the resulting phase noise is also halved. The results of this example can be summarized by the following set of expressions. These expressions assume a constant amplitude of oscillation, constant Q_C, constant Q_L, and constant frequency of oscillation.

$$C \propto \text{Power Consumption} \tag{4.11}$$

$$C \propto (\text{Phase Noise})^{-1} \tag{4.12}$$

$$L \propto (\text{Power Consumption})^{-1} \tag{4.13}$$

$$L \propto \text{Phase Noise} \tag{4.14}$$

$$L/C \propto (\text{Power Consumption})^{-2} \tag{4.15}$$

$$L/C \propto (\text{Phase Noise})^{2} \tag{4.16}$$

$$\text{Power Consumption} \propto (\text{Phase Noise})^{-1} \tag{4.17}$$

A VCO with a high L/C ratio may give a deceptive view of high performance, where large oscillation amplitude can be achieved with small power consumption. However, as stated in [51], for a given tank energy, a larger tank amplitude obtained by increasing the inductance does not result in a better noise performance. This is because the oscillator has a similar response to both the tank energy and the thermal noise energy. In other words, with a larger inductance, the amplitude of oscillation becomes larger for a given power consumption. However, at the same time, the oscillator noise power is also magnified by the same amount. Therefore, no improvement in phase noise is achieved, even though the amplitude of oscillation is increased.

From (4.11) to (4.17) the following observations are made. The phase noise of an LC tuned oscillator trades linearly with the power consumption through the L/C ratio scaling. Higher L/C ratio implies lower power and higher phase noise, while lower L/C ratio implies the opposite. As a result, the FOM based on (2.15) stays constant with respect to the L/C ratio scaling. All of which is based on the assumption that Q_{tank}, f_0 and A_0 stay constant before and after the L/C ratio scaling.

However, in practice, the assumption of constant Q_{tank} may not always hold true. As mentioned previously, Q_C can be regarded as a constant quantity regardless of the size of C, because the size of C can be varied by taking or adding the same type of capacitor in parallel. Inductors on the other hand are different, especially in integrated environments. In an integrated environment, every inductor with different inductance or area budget has a unique geometry. This implies different Q_L for every inductor with different inductance or area budget. According to (4.1), Q_{tank} is a function of Q_L and Q_C. When an oscillator is scaled by the L/C ratio, Q_C should stay constant, but Q_L may show some change due to the geometric change of the spiral inductor. This would result in some change in Q_{tank} in practice.

(4.9) suggests Q_L improves with D_{out}. Also, as mentioned earlier, a lower N/w ratio is preferred to take advantage of the hollow inductor effect. Based on these observations, it can be said that the highest Q_L should come from an inductor employing the largest D_{out}, and smallest N. Once D_{out} is fixed to its largest allowable value either limited by the area budget or low f_{self}, the lower limit on N is determined by the amount of inductance required. If the required inductance is reduced, N is also reduced. This helps to take advantage of the hollow inductor effect and improve Q_L. Therefore it can be said that lower inductance is preferred to achieve higher Q_L. This leads to the

conclusion of this section that a VCO with a lower L/C ratio should exhibit higher Q_L or Q_{tank} and, hence better FOM and phase noise. This new finding is experimentally verified in Chapter 5 and 6.

4.5 TRANSISTOR SIZE OPTIMIZATION

For a given tank impedance, the size of cross-coupled transistors plays a major role in determining the power consumption, and the phase noise. Because the average DC power consumption and the transistor noise current are determined by the cross-coupled pair bias voltage (V_{CCP}), the output waveform, and the width of the cross-coupled transistors. In addition, the phase noise is strongly affected by the oscillation amplitude and the sum of all noise contributions from the tank and the transistors. Therefore, all transistors must be sized carefully to minimize the phase noise, and improve the FOM for a given tank and power budget.

4.5.1 Tail Transistor Size

The tail current bias transistor affects the VCO phase noise performance mostly in the −30dB/decade region due the flicker noise in the tail transistor. Also, it creates a small voltage overhead to maintain its high output impedance by remaining in the saturation region.

The flicker noise expression, (2.17) implies that the flicker noise of the tail transistor can be lowered by enlarging the transistor gate area. Enlarging the gate area

by increasing the gate width also lowers the minimum drain-source saturation voltage ($V_{DS.sat}$) of the transistor, thereby minimizing the voltage overhead. Hence, the tail transistor must be made as wide as possible for low noise operation and maximum oscillator output dynamic range.

4.5.2 Cross-Coupled Oscillator Noise Analysis

Unlike the tail bias transistor, the cross-coupled pair optimization is not as straight forward. Therefore, a detailed analysis of the correlation between the cross-coupled pair size and the phase noise performance must be made.

Plots in Fig. 3.11 (or Fig. 3.7) can be viewed as bias spaces of a VCO. The plots show the oscillation amplitude (A_0) under all possible bias currents, bias voltages, and tank resistances for a given size of the cross-coupled transistors. Corresponding phase noise space or FOM space may be derived based on these bias spaces as will be shown in this section. Any change in the size of the cross-coupled pair will modify the bias spaces. This in turn influences the corresponding phase noise space or FOM space. Therefore the optimization of the size of the cross-coupled transistors involves observation of the variation in the phase noise space and/or the FOM space with respect to the cross-coupled pair size variation.

In order to calculate the phase noise, and the FOM based on the simple LTI phase noise expression, one needs to first estimate the noise current in the cross-coupled transistors. In addition to that, the oscillator output power, average power consumption, R_{tank}, noise associated with R_{tank} and Q_{tank} are also needed.

The drain current noise power spectral density of a transistor is given as

$$\overline{i_n^2} = 4kT\gamma g_{ds0} \qquad (4.18)$$

where g_{ds0} is the drain to source conductance, when $V_{DS}=0V$. For a long channel device (or equivalently a low V_{DS} device), g_{ds0} can be replaced with g_m [67]. However, the cross-coupled transistors in a VCO are often biased with a large V_{DS}. Therefore, the long channel approximation cannot be applied due to the channel length modulation effect. Furthermore, the value of the long channel transistor noise factor (γ) of 2/3 is not appropriate to use with (4.18). Instead, g_{ds0} at different V_{GS} is obtained from a series of simulations, and γ under various channel length and bias conditions is obtained from measured values published in [63]. It is noted that for 0.18μm devices, $\gamma \approx 1.1$, and for 0.5μm devices, $\gamma \approx 0.8$ over wide ranges of V_{GS} and V_{DS}.

The LTI phase noise expression given in (2.12) assumes constant noise current power. However the cross-coupled transistor noise current varies along with the voltages applied at the gate and the drain. In order to improve the accuracy of the phase noise expression, the cyclostationary nature of the transistor noise current is taken into account.

The LTI phase noise expression is basically given as

$$\mathcal{L}\{\omega_m\} = \left(\frac{1}{2}\right)\frac{(\text{passive tank noise power} + \text{FET noise power})}{\text{oscillator noise power}}\left(\frac{\omega_0}{2Q\omega_m}\right)^2 \qquad (4.19)$$

where the first term assumes the amplitude noise suppression, and the last term is responsible for noise shaping by the tank close to f_0. For a cross-coupled NMOS-only topology, (4.19) can be rewritten as

$$\mathcal{L}\{\omega_m\} = \left(\frac{1}{2}\right)\frac{\left(4kT/R_{tank} + f_0 \int_0^{f_0^{-1}} \overline{i_n^2}(\tau)d\tau\right)}{A_0^2/2R_{tank}^2}\left(\frac{\omega_0}{2Q_{tank}\omega_m}\right)^2 \qquad (4.20)$$

where the integral represents the time-averaged noise power spectral density of the FET over a single oscillation cycle. This is to take into account the cyclostationary nature of the transistor noise current.

The above expression is the appropriate phase noise expression for the NMOS-only topology. Example plots of the phase noise space and the FOM space are plotted in Fig. 4.8(b) and (c) respectively. The phase noise space and the FOM space also make use of the bias space plot in Fig. 4.8(a) to acquire A_0, R_{tank} and the DC power consumption needed for their calculations. A Q_{tank} value of 7 is assumed, and the phase noise is calculated for 1MHz offset.

Fig. 4.8(a) is generated using the same devices used to generate Fig. 3.11(a). The transistors used for the cross-coupled pair are two NMOS devices of the TMSC 0.18μm bulk CMOS process with their gate width and length being W_{CCP}=100μm and L_{CCP}=0.18μm respectively. The difference is that Fig. 4.8(a) uses a different set of R_{tank} values. This time, R_{tank} is varied logarithmically from 25Ω to 250Ω over 10 steps.

The DC power consumption required by the FOM space calculation is evaluated as a product of I_{tail} and V_{DD}, where V_{DD} is defined as a sum of V_{CCP} and 0.2V. The addition of 0.2V is to account for the $V_{DS,sat}$ overhead of the tail bias transistor.

In practice, a constant V_{DD} is used for all bias conditions, and the V_{DS} drop across the tail bias transistor would be larger than $V_{DS,sat}$ for most bias conditions. However, using a constant and large value of V_{DD} would result in poorer FOM for low V_{CCP} bias conditions, solely due to the larger DC drop across the tail bias transistor.

Therefore, in order to be fair for all bias conditions, a fixed DC drop of 0.2V across the tail transistor is assumed in the FOM calculations.

Looking at Fig. 4.8(b), as one would expect, the phase noise curves show monotonic improvements with respect to A_0 for all R_{tank}. Also, a lower bound in the phase noise space is observed. The lower bound is lowered as V_{CCP} (or equivalently the power consumption) is increased.

On the other hand, the FOM curves shown in Fig. 4.8(c) show local minima with respect to V_{CCP}. The V_{CCP} range is not wide enough to view the minima for all curves, but they are observed for the curves representing R_{tank} values of 31.5Ω, 39.6Ω, 49.9Ω and 62.8Ω. For a VCO with a relatively high R_{tank}, the best FOM (or the minimum) is observed near the lower end of V_{CCP}, while the opposite is observed for a VCO with a relatively low R_{tank}. Also, unlike the lower bound of the phase noise space, the lower bound for the FOM space is increasing with respect to V_{CCP}.

The existence of significant variations in the FOM curves with respect to V_{CCP} means the power consumption and the phase noise do not trade equally across the V_{CCP} variation. This is in contrary to the VCO scaling by the L/C ratio discussed in the previous section, where the FOM is constant with respect to the L/C ratio variation. It should be noted that they are two different ways of trading power consumption for lower phase noise.
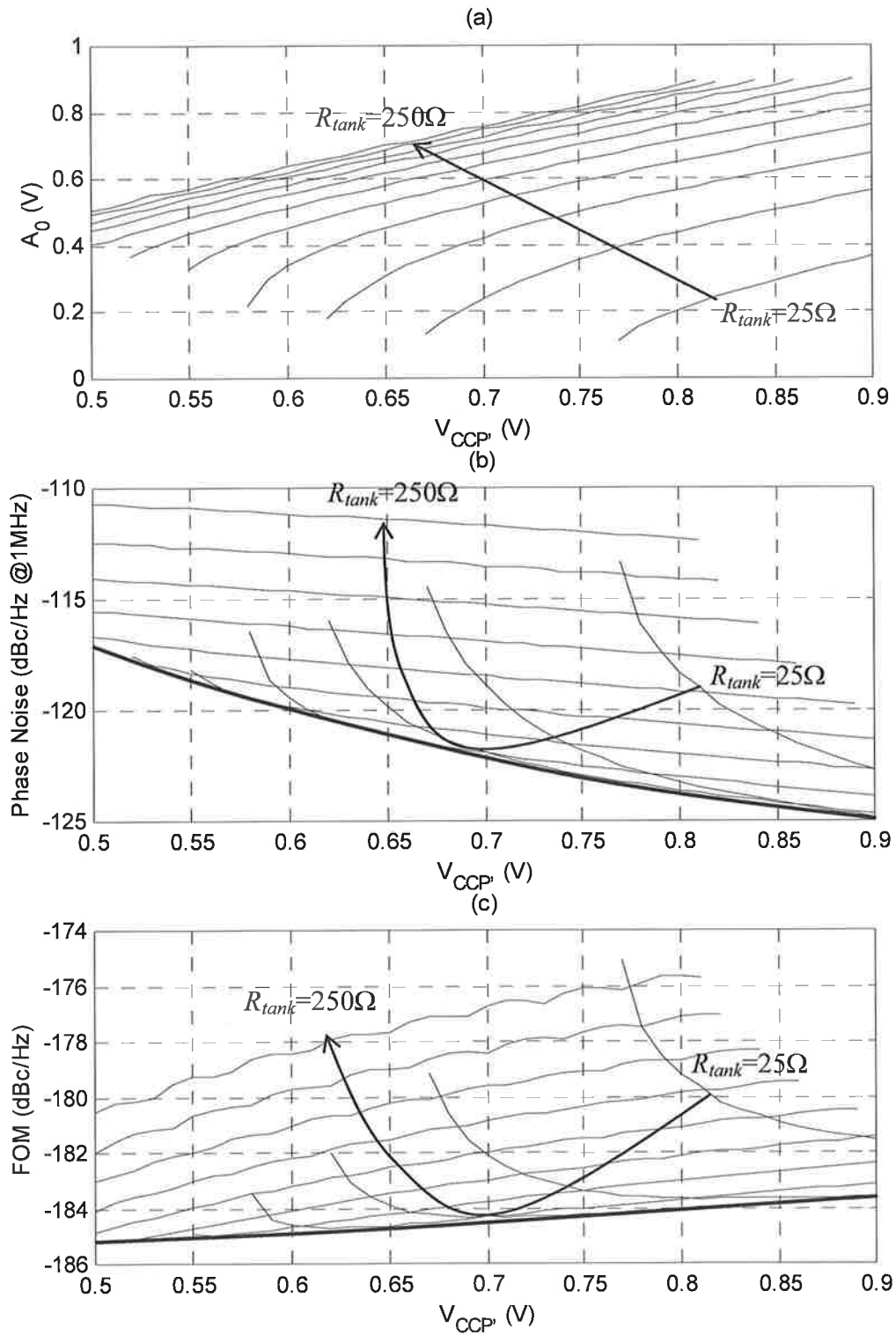
Fig. 4.8: (a) bias space, (b) phase noise space, and (c) FOM space for logarithmic sweep of R_{tank} from 25Ω to 250Ω over 11 steps, while W_{CCP} is held constant at $100\mu m$.
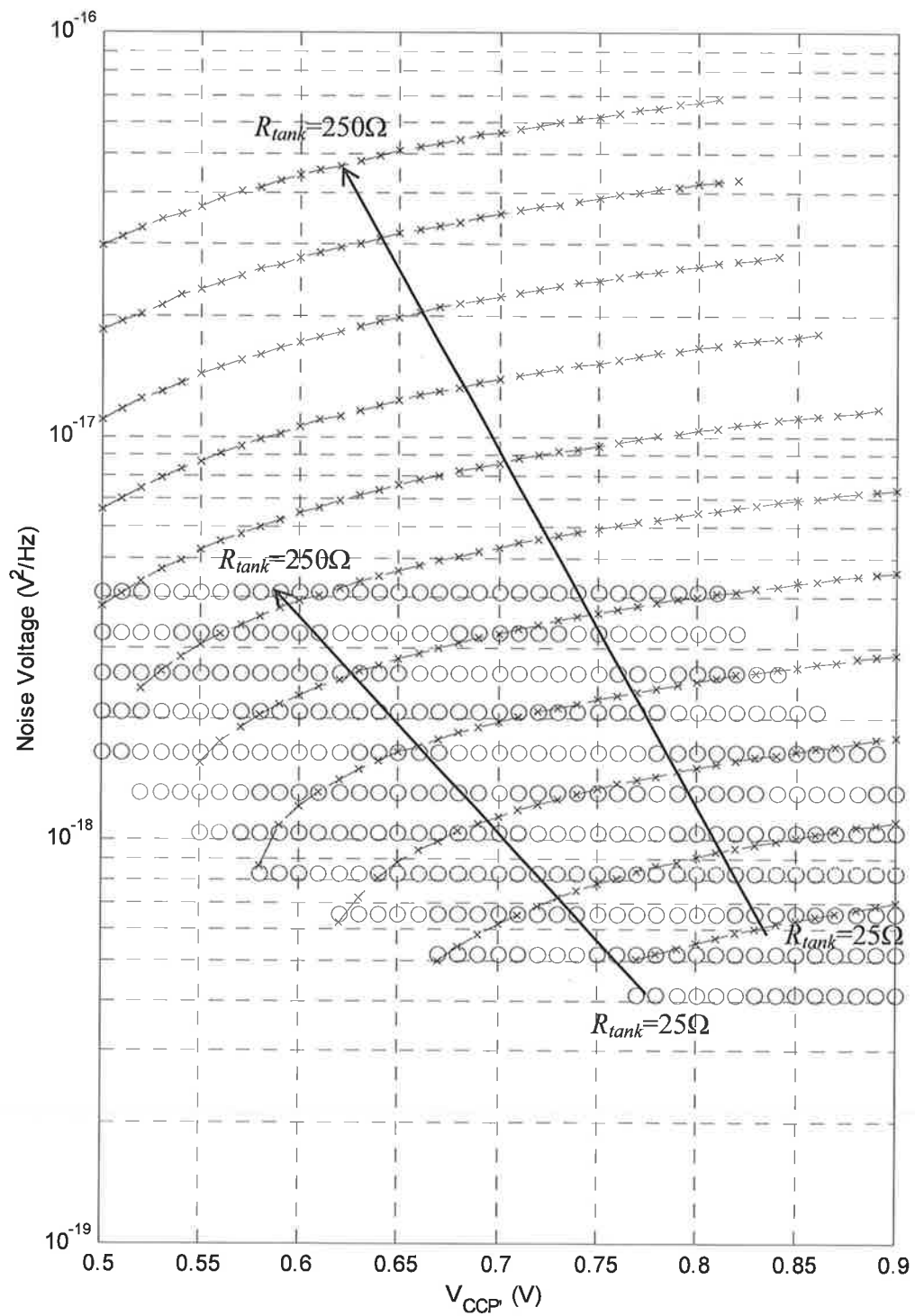
Fig. 4.9: Noise contributions from passive tank (o) and active cross-coupled transistors (×) at different sizes of R_{tank}.

Fig. 4.9 shows the noise contributions from the passive tank and the active transistors of the cross-coupled pair. The noise voltage originating from the passive tank is constant with respect to V_{CCP} for a given R_{tank}. On the other hand, the noise voltage of the transistors grows with V_{CCP}. This is because as V_{CCP} is increased, the bias current increases, and that causes an increase in g_{ds0} of (4.18).

The monotonic improvement in the phase noise and the local minima observed in the FOM curves in Fig. 4.8(b) and (c) respectively can be explained as follows. The rate of increase of the sum of the two noise powers shown in Fig. 4.9 is slower than the rate of increase of A_0^2 for any given R_{tank}. As a result, the phase noise and the FOM improve rapidly with increasing A_0 for low values of A_0. However, as A_0 is increased further, the rate of increase of A_0^2 slows down due to the nonlinearity buildup in the drain currents of the cross-coupled transistors. The rate of increase of the total noise power is still slower than that of A_0^2 and the phase noise continues to benefit from the increased oscillation amplitude at somewhat reduced rate. This explains the continual but somewhat reduced rate of improvement in the phase noise with respect to V_{CCP}. However, the efficiency of the DC power to A_0^2 conversion process of the VCO is not as efficient as it used to be at low values of A_0. And this is why the local minima are observed in the FOM curves.

Although the width of the cross-coupled transistors, W_{CCP} was kept constant while generating the curves in Fig. 4.8(a), the same set of curves can be used to represent the bias space of a VCO with different W_{CCP} and R_{tank}. Because W_{CCP} scales linearly with the inverse of R_{tank} while leaving A_0 and V_{CCP} unaffected. In other words,

as long as the ratio between W_{CCP} and R_{tank} stays constant for each of the curves, the curves can be reused to represent the bias space of a VCO with different W_{CCP}. For example, doubling W_{CCP} would result in the same set of curves in the bias space except that each curve now represents half the original tank resistances. It is like connecting two identical VCOs in parallel. That does not affect A_0 or V_{CCP} while doubling W_{CCP} and halving R_{tank}.

Connecting two identical VCOs in parallel has the effect of reducing the L/C ratio by a factor of 4 as discussed in section 4.4, just as it reduces the R_{tank}/W_{CCP} ratio by a factor of 4. Therefore, scaling a VCO by an L/C ratio change is equivalent to scaling it by a R_{tank}/W_{CCP} ratio change by the same factor. In other words, throughout an L/C ratio scaling of a VCO, the following relation is maintained.

$$\frac{L}{C} \propto \frac{R_{tank}}{W_{CCP}} \tag{4.21}$$

Therefore, the L/C ratio scaling and the W_{CCP}/R_{tank} ratio scaling are used interchangeably hereafter.

Since the FOM is unaffected by an L/C ratio scaling, the FOM operating space should stay unaffected by a W_{CCP}/R_{tank} ratio scaling either. This is demonstrated in Fig. 4.10. Each of the curves in Fig. 4.8(a) is W_{CCP}/R_{tank} ratio scaled such that each curve now represents a constant R_{tank} of 25Ω, but different W_{CCP}. These new curves are plotted in Fig. 4.10(a). Based on the curves of Fig. 4.10(a), the FOM space is plotted in Fig. 4.10(b). Note that the new FOM curves are also identical to that of Fig. 4.8(c).

Scaling a VCO by a change in the L/C ratio (or equivalently the W_{CCP}/R_{tank} ratio) is ineffective in improving the FOM. The only way to improve the lower bound of

the FOM space is by improving the phase noise without consuming more power. This can only be achieved by improving Q_{tank} in a given process technology.

(a)

(b)
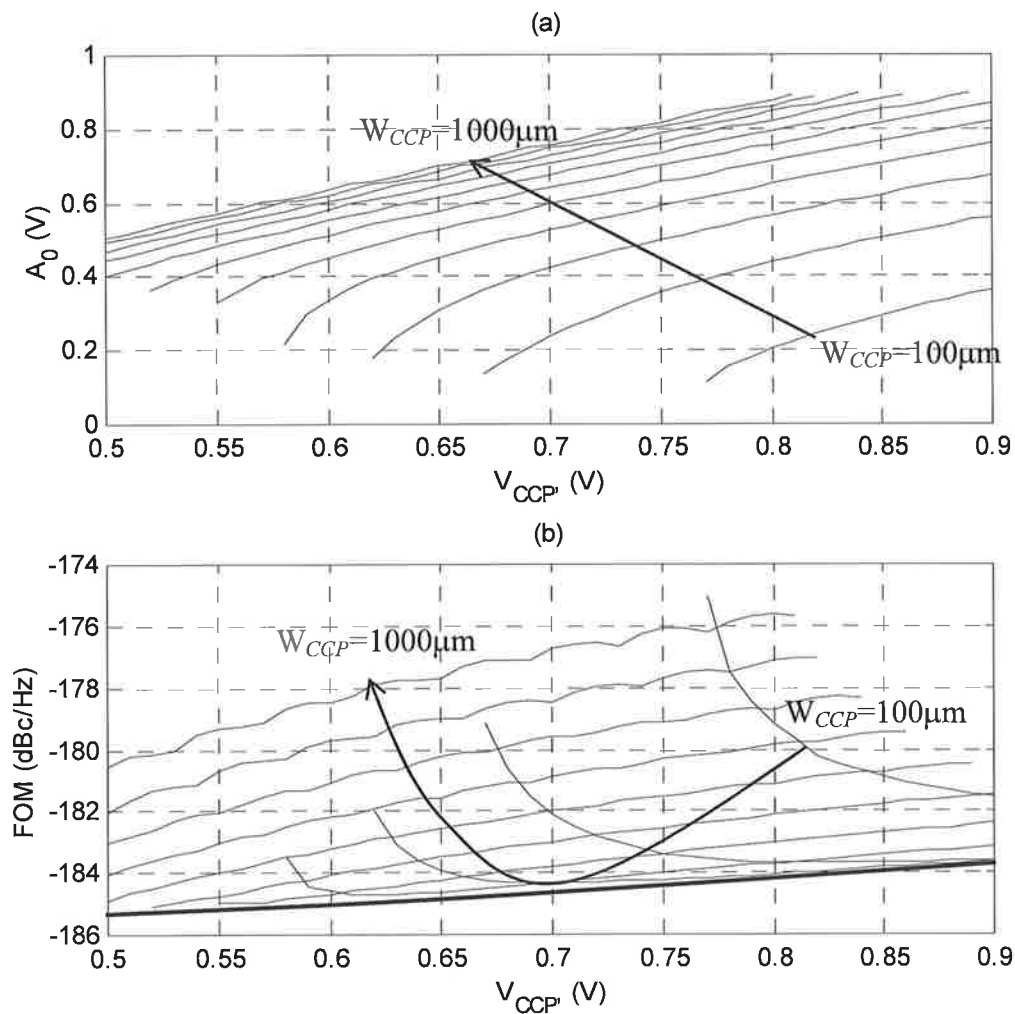
Fig. 4.10: VCO (a) bias space and (b) FOM space for R_{tank}=25Ω and Q_{tank}=7, while logarithmically sweeping W_{CCP} from 100μm to 1000μm over 11 steps.

The phase noise space on the other hand is affected by the W_{CCP}/R_{tank} ratio scaling. Because (2.12) implies that phase noise is proportional to R_{tank} for given A_0 and Q_{tank}. Fig. 4.11 shows two phase noise spaces for two different values of R_{tank}. One at 25Ω and the other at 250Ω. Reducing R_{tank} from 250Ω to 25Ω yielded 10 times or 10dB

improvement in the phase noise, while the transistor width is scaled 10 times wider. This translates to 10 times the more tail bias current or power consumption.

An important observation made from Fig. 4.11 is that there exists an optimal transistor width that yields the minimum phase noise for given V_{CCP}, and tank. A similar observation can be made from the FOM space plot in Fig. 4.10(b) as well. Fig. 4.12 is produced based on Fig. 4.10 and Fig. 4.11. It shows how A_0, the phase noise, and the FOM vary with respect to W_{CCP} for a constant R_{tank} value of 25Ω and various V_{CCP} bias voltages.
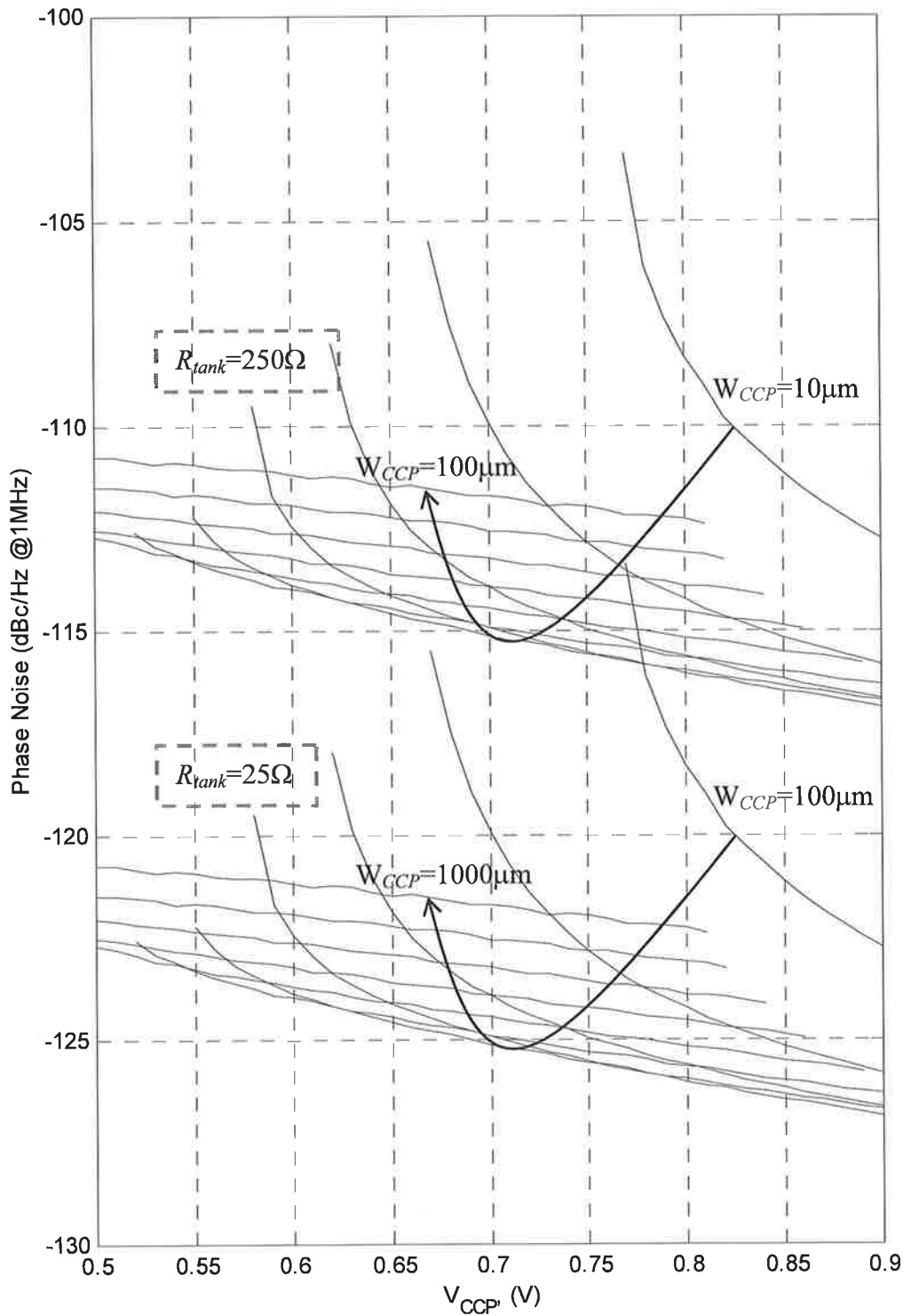
Fig. 4.11: Two phase noise spaces for two constant R_{tank} values of 250Ω and 25Ω, while logarithmically sweeping W_{CCP} from 10μm to 100μm and 100μm to 1000μm respectively.

(a)

(b)

(c)
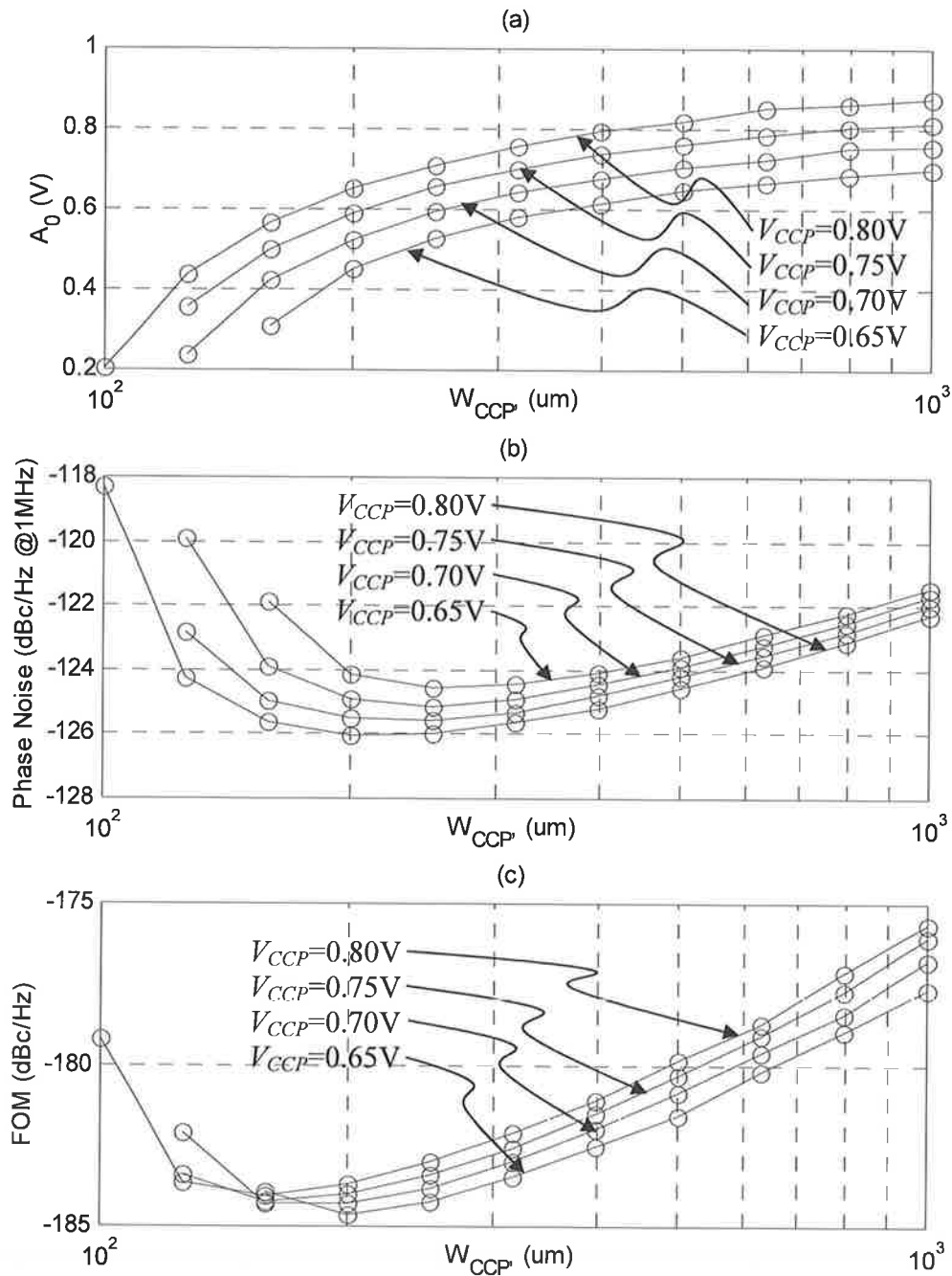
Fig. 4.12: (a) A_0, (b) phase noise, and (c) FOM variation with respect to W_{CCP} for a given tank and under 4 different V_{CCP} bias voltages.

Looking as Fig. 4.12(a), as one would expect, A_0 increases monotonically with increasing W_{CCP}. Because wider W_{CCP} for a constant V_{CCP} means more bias current and more gain provided by the cross-coupled pair.

From Fig. 4.12(b), it is observed that the phase noise improves rapidly with W_{CCP} at low values of W_{CCP}. This is mostly due to the rapid increase of A_0 with respect to W_{CCP}, due to the good linearity in the gain provided by the cross-coupled pair for low values of A_0. The phase noise ceases to improve at some larger value of W_{CCP} (or A_0) before degrading gradually as W_{CCP} is increased further. This is because A_0 is bound by a fixed value of V_{CCP} such that A_0 increases rapidly at first, and then becomes gradually limited by V_{CCP}, while W_{CCP} is continually increasing. On the other hand, throughout the entire range of W_{CCP}, the transistor noise current increases almost proportionally with W_{CCP}. Therefore, above a certain value of W_{CCP}, the rate of increase of the transistor noise power overtakes the rate of increase of the oscillator signal power, and the phase noise starts to degrade.

The FOM curves in Fig. 4.12(c) undergo a similar process and experience minima at certain values of W_{CCP}.

4.5.3 Cross-Coupled Pair Optimization

For a given process technology, there are limits on realizable Q_L, and Q_C. This implies there is a hard limit on best achievable FOM for a given process. On the other hand, the limit on the phase noise is soft. It is either set by the amount of power prepared to consume or the practical lower limit on the L/C ratio that can be implemented.
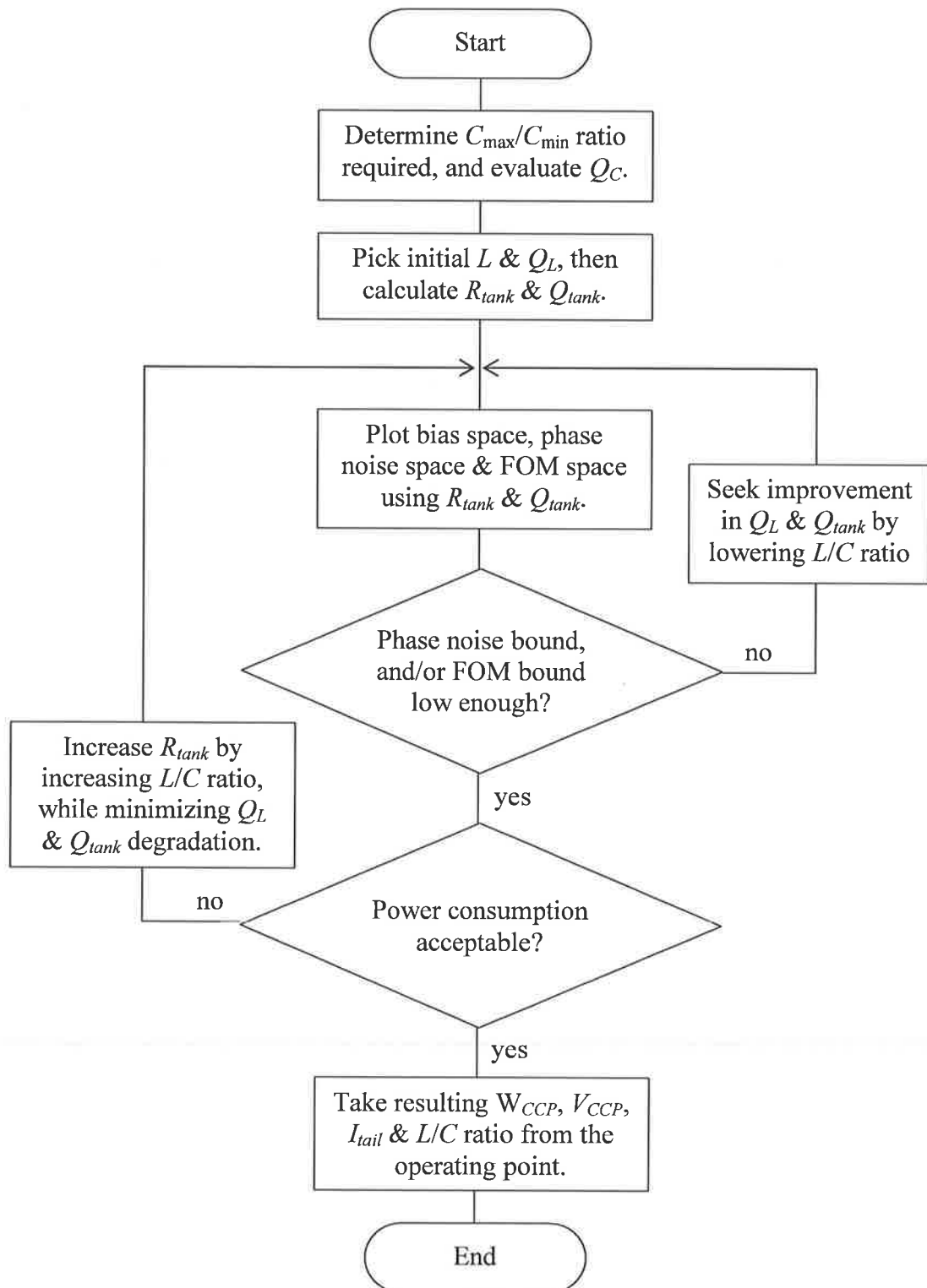
Fig. 4.13: High performance VCO optimization flowchart.

Now a sufficient understanding on the noise performance of a cross-coupled *LC* tuned oscillator is gained that it has become possible to draw a flowchart that provides a guideline in designing a high performance VCO. The VCO optimization flowchart shown in Fig. 4.13 helps to design a VCO operating near the limits imposed either by the process technology or the power budget.

The flowchart starts by determining the required C_{max}/C_{min} ratio. This ratio is determined based on the frequency-tuning requirement of the target application and the process spread in capacitance. Only the ratio is required at this stage to calculate Q_C, since Q_C is independent of the absolute value of the capacitance.

Then initial values of realizable L and Q_L are found from inductor simulations. Once L is determined, the absolute value of C is also determined. The phase noise space and the FOM space similar to the ones shown in Fig. 4.10 and Fig. 4.11 respectively are plotted based on R_{tank} and Q_{tank} evaluated from Q_L, Q_C. L and C. Depending on the requirement by the target application, the desired operating point is sought either from the phase noise space or the FOM space. Most often, the phase noise space should be the important one at which to look.

If the desired operating point is located below the lower bound of the space under interest, then the lower bound of the corresponding space can be lowered by downscaling the *L/C* ratio. While the lower bound for the phase noise space is lowered by the square root of the change in the *L/C* ratio, the lower bound for the FOM space can only be lowered by improving Q_{tank}. Since, lower *L/C* ratio helps to achieve higher Q_L, lowering the *L/C* ratio helps to lower the lower bound of the phase noise space as well as the lower bound of the FOM space.

If the desired operating point is found within the space under interest, the bias current required to operate at the chosen operating point is examined to see if the power consumption is acceptable. If it is, then W_{CCP}, the tank configuration, and the transistor bias condition are used to complete the optimization process. However, if the power consumption is too high, then this may be traded for a somewhat increased L/C ratio. Note that doing so will raise the lower bound of the phase noise space and possibly that of the FOM space as well. Sometimes a tradeoff between the phase noise performance and the power consumption is required.

As mentioned earlier in this section, there is a soft limit on the achievable phase noise for a given process. The lower bound of a phase noise space shows a negative slope as can be seen from Fig. 4.11. This implies the phase noise can be improved by extending the upper limit of the V_{CCP} until the peak-to-peak oscillator swing reaches the oxide breakdown voltage of the transistors. Under such an extreme bias condition, the long-term device reliability or the hot-electron degradation become the practical design limits [110].

In addition, improving the phase noise performance by scaling down the L/C ratio will eventually be limited by the parasitic inductances associated with the metal routings. At a low extreme of the L/C ratio, one would need to ensure that either the parasitic inductances associated with metal routings stay well controlled to form a part of the inductance in the tank, or L stays significantly larger than any of the parasitic inductances in the tank.

4.6 OTHER OPTIMIZATION MEASURES

The VCO optimization techniques investigated thus far have concentrated on the minimization of the internally generated noise, while maximizing the oscillator signal power. This section of the chapter discusses a couple of VCO optimization techniques that can help to reduce some of internally generated noises as well as externally fed noises.

4.6.1 Bypass Capacitors

Placing a bypass capacitor to stabilize a voltage fluctuation on a circuit node is a standard technique commonly found in many circuit designs.

A cross-coupled LC tuned VCO has a number of nodes that require a good AC grounding to improve the phase noise performance. For example, the cross-coupled NMOS-only VCO shown in Fig. 3.18 has nodes, namely V_{DD}, v_{CM}, V_{ctl}, V_{tail}, and the bottom plates of two C_{fix} requiring good AC grounding.

Every node in the tank should share the same AC ground where possible. This is to ensure high Q_{tank} while leaving no path for the external noise to feed through.

Usually, the two common AC grounds found in a circuit are V_{DD} and ground. However, due to the finite output impedance of a voltage source, V_{DD} may not always stay constant with respect to ground. Therefore, one must make a choice between the two for the common ground of the tank.

For the NMOS-only VCO shown in Fig. 3.18, the inductors are connected to V_{DD} due to their DC biasing requirement. Therefore, one is forced to make all other nodes in the tank to use V_{DD} as their common ground if possible.

The two bottom plates of C_{fix} can either be terminated at ground as shown, or at V_{DD}. Therefore, it is preferred to terminate the bottom plates of the two C_{fix} capacitors to V_{DD} rather than ground.

The two varactors form a part of the tank capacitance. The input control potential, V_{ctl} can be capacitively coupled to V_{DD} to stabilize V_{ctl}. The size of the coupling capacitor must not be significantly large so as to interfere with the operation of the loop filter of a PLL, while providing a good AC grounding at high frequencies.

The tail bias current is determined by V_{tail} with respect to ground. Therefore, for a constant and low-noise biasing of I_{tail}, V_{tail} is best to be AC grounded to ground.

The AC grounding of v_{CM} has been debated for quite some time. Those who encourage the use of a bypass capacitor at v_{CM} claim that it helps to improve the output waveform symmetry [9], [38], [51], [58]. This is critical in lowering the upconversion of the flicker noise originating from the tail bias transistor.

On the other hand, those who oppose the AC grounding of v_{CM} claim that high output impedance of the tail current source, especially at $2f_0$ improves the linearity in the drain currents of the cross-coupled transistors [43], [44], [52]-[54]. Therefore, a parallel LC filter placed between the common-mode node of the cross-coupled pair and the drain of the tail transistor makes the frequency of oscillation less sensitive to the flicker noise from the cross-coupled pair and the tail bias transistor. This filtering technique, suggested in [44], is designed to reduce the two Groszkowski effects discussed in section 3.4.2 and section 3.4.3.

In this work however, no notable improvement in phase noise was observed in measurements with the filtering technique suggested in [44]. Therefore, a decision was made to AC ground v_{CM} to V_{DD}.

However, one cannot conclude that the filtering technique suggested in [44] is without merit, but the filtering technique requires pinpoint accuracy with the parallel LC filter tuned at $2f_0$ for it to work properly [54], and the required accuracy can not be ensured in this work due to the process variation on the test chips fabricated. Therefore, the effectiveness of the filtering technique remains inconclusive as a result of this work.

Lastly, it should be noted that all practical internal bypass capacitors are typically of the order of few tens of picofarads, at most, due to the large chip area they could consume. This means they are not effective in filtering out low frequency noise such as the flicker noise.

4.6.2 Low-Power, Low-Noise Current Biasing

The oscillator power consumption is usually calculated as a product of the bias current through the oscillator core and the supply potential. However, a practical VCO usually requires more than just the tail bias current to operate. For example, the buffer amplifier stage interfacing the VCO output to other circuit modules is highly recommended to reduce the loading on the oscillator tank and keep Q_{tank} as high as possible.

Another significant source of power consumption other than the VCO buffer is the tail current bias voltage generator circuit similar to the one shown in Fig. 3.9. The

diode-connected transistor sinks the same amount of current as the VCO tail bias current to avoid flicker noise multiplication in the tail current by some large factor.

For low noise operation of a VCO, a large tail bias current is often required. Use of the 1:1 transistor width ratio between the diode-connected transistor and the tail transistor doubles the current consumption. Therefore only a half of the current budget allocated for a VCO module can be used in the VCO core, which is considered quite inefficient use of the allocated power budget.

As mentioned in section 3.4.4, a narrower transistor width may be used for the diode-connected transistor to conserve current. However, the side effect to this is increased flicker noise on the tail bias current at least by the current mirroring ratio between the two transistors.

In this work, a passive low-pass filtering technique is proposed to deal with this problem. A RC low-pass filter placed between the diode-connected transistor and the tail transistor as shown in Fig. 4.14 can reduce the excessive flicker noise generated by M_{ref}. The cutoff frequency of the filter must be at least lower than the loop bandwidth of the PLL to be most effective, because the noise components outside of the loop bandwidth are not attenuated by the loop.

This loop bandwidth can be very low in frequency, even lower than the flicker noise corner frequency of M_{ref}. This makes it difficult to implement the resistor and capacitor that from the RC filter. Because the size of the resistor would have to be of the order of megaohms and the size of the capacitor in the order of hundreds of picofarads.

Fortunately, modern CMOS processes offer MOS capacitors with very large gate capacitance density owing to their thin gate oxide thickness. In addition, very high resistances can be achieved using devices such as non-silicided polysilicon resistors or

lightly doped n^+ resistors. Therefore, with a modern deep submicrometer CMOS process, it is quite practical to implement an RC filter with a very low cutoff frequency without paying severe area penalty.

A VCO employing a tail bias RC filter can use almost all of its allocated current in the VCO core and maximize the phase noise performance. Examples of such a filter are demonstrated in the subsequent two chapters.
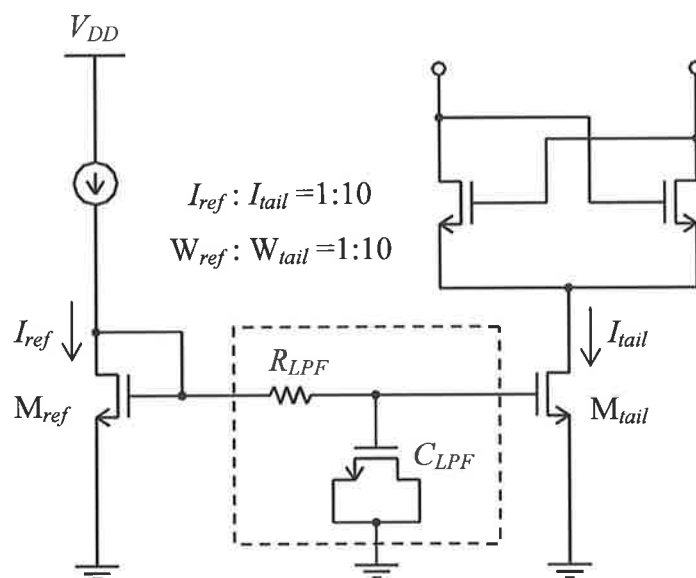
Fig. 4.14: Use of a RC low-pass filter to attenuate noise from reference current generator.

4.7 CONCLUSIONS

A number of possible monolithic implementations of inductors have been investigated in this chapter. Of these, the monolithic planar spiral inductors have been identified as the most cost-effective way to realize on-chip passive inductances.

However, due to their inherently poor Q performance, a geometric optimization technique has been developed for spiral inductors in CMOS processes to optimize Q_L. In general, a spiral inductor with large D_{out}, w, and small N results in optimal Q performance. In this case, lower inductance results in higher Q_L for a given area or fixed D_{out}.

The effects of different L/C ratio on the VCO performance have been investigated in detail. Low L/C ratio is preferred for low-noise operation, while high L/C ratio is preferred for low-power operation. This arises from the property that, for a given Q_{tank}, the phase noise changes proportionally with the square root of the change in L/C ratio, and the power consumption changes inversely with the square root of the change in L/C ratio.

Unlike the phase noise, as long as Q_{tank} stays constant, the FOM is not affected by the change in L/C ratio. Fortunately, one of the properties of a spiral inductor identified in this work is that Q_L can be made higher for a lower value of inductance. Therefore, the FOM and the phase noise can both be improved by lowering the L/C ratio.

The gate width of the cross-coupled transistors is identified as another significant design parameter affecting the VCO performance. An optimization technique has been developed to find the optimal transistor width for a given tank.

Together with the inductor optimization technique, the high performance VCO optimization technique developed in this chapter can deliver the best achievable VCO performance for given area, and power budget.

Lastly, proper usages of bypass capacitors on a cross-coupled NMOS-only VCO have been discussed, and a low-noise, low-power VCO biasing technique involving on-chip filtering of noise from the current reference source has been proposed.

Chapter 5

HIGH PERFORMANCE SOI CMOS VCOS

5.1 INTRODUCTION

This chapter presents a series of VCOs designed for 5GHz and 17GHz operation. A SOI CMOS process was the technology used to implement these VCOs. Section 5.2 briefly describes the features of this process technology.

There were three fabrication runs using the SOI process. The first test chip consists of four 5GHz VCOs and four 17GHz VCOs. These are presented in section 5.3 and 5.4 respectively.

The second test chip consists of six 5GHz VCOs. Unfortunately, all VCOs from the second test chip failed to oscillate. The designs were revised and implemented again on the third test chip. These VCOs were designed for low-noise operation, and presented in section 5.5.

The VCOs from the first test chip are the first set of VCOs produced in the course of this work. They are highly experimental and do not exactly conform to the low-noise optimization methodology developed later in the research. Nonetheless,

understandings acquired from these experimental VCOs have led to the designs of high performance VCOs.

5.2 0.5μm SOS CMOS PROCESS

The Peregrine Semiconductor's 0.5μm SOS CMOS process was used to implement the VCOs presented in this chapter. This process technology provides an alternative to a standard bulk CMOS process for high-density radio front-end electronics owing to its inherent radiation tolerance and lossless insulating substrate.

The biggest advantage of a SOI process over a bulk process is probably the lossless insulating substrate. It provides very high electrical isolation between devices. Also, it eliminates all the parasitic capacitors normally associated with the substrate. Furthermore, the lossless substrate is an ideal environment for the monolithic planar spiral inductors. Spiral inductors implemented on an insulating substrate have the same set of advantages as the bulk micromachined inductors without the attendant mechanical instability and the low packaging yield concerns.

One down side of the SOS process when used for high performance VCO implementation is the relatively high channel noise associated with the fully depleted SOS transistors, in particular the excessive flicker noise in the drain current. Measurements show that the flicker noise from a 0.5μm fully depleted SOS NMOS device is worse than that of a 0.5μm standard bulk silicon NMOS device by a factor of 8 [111]. In addition, the flicker noise of SOS NMOS devices show poor correlation with

the gate area, suggesting possible existence of more than one contributing noise process. The noise model does not exactly conform to the noise model of bulk transistors [111].

The following brief descriptions of the process characteristics are taken from the process manual of the SOS process [107], unless otherwise stated.

The process provides six different types of transistors, each of them having different threshold voltages. Table 5.1 summarizes how each transistor type is distinguished from one another.

Table 5.1: SOS transistor types.

Transistor Type	Description	V_{TH} (V)
RN	Regular V_{TH}, n-channel	0.7
NL	Low V_{TH}, n-channel	0.2
IN	Intrinsic n-channel	0.0
RP	Regular V_{TH}, p-channel	−0.7
PL	Low V_{TH}, p-channel	−0.2
IP	Intrinsic p-channel	0.0

The maximum unity-current-gain frequency (f_T) and the maximum unity-power-gain frequency (f_{max}) for the RN type device are 13GHz and 53GHz respectively. This implies the theoretical maximum frequency of oscillation achievable is as high as 53GHz.

The process provides three aluminum metal layers for routing. Starting form the bottom layer, metal-1 (M1), metal-2 (M2), and the top metal (MT) have thickness of 0.85μm, 1.08μm, and 3.1μm respectively. The low sheet resistance of the MT layer makes it ideal for spiral inductor implementation.

MIM capacitors offered in this process are created by selectively reducing the oxide thickness between MT and M2 from 1.1μm to 60nm. The oxide breakdown voltage for the MIM capacitors is greater than 10V. Capacitance density is $0.575fF/\mu m^2$. The low sheet resistances of MT and M2 allow for high Q of approximately 70 and 33 at 2.4GHz and 5GHz respectively.

Various resistor types are offered. Their sheet resistances range from $12\Omega/\square$ of polycide resistor to $1.9k\Omega/\square$ of lightly doped n-type silicon resistor.

5.3 EXPERIMENTAL 5GHZ VCOS

As mentioned earlier, the four 5GHz VCOs presented in this section of the chapter are experimental. They were designed to investigate the multi layer spiral inductor efficiency, the topological advantages, the feasibility of switched capacitor bank for wider frequency tuning range, and most of all, the feasibility of the SOS technology for high performance 5GHz VCO implementation.

The high performance VCO design methodology described in Chapter 4 was not developed at the time of design of these VCOs. Nevertheless, the resulting operating points of the VCOs are calculated, and located on their bias space, and the phase noise space to see where they stand.

5.3.1 VCO Designs

The first VCO, or VCO1 is the base design for the other three. It is a typical NMOS-only topology, using inversion mode MOS varactors for frequency tuning and triple metal layers for the spiral inductor construction.

VCO2 is identical to VCO1, except its inductors are utilizing only the top metal layer. The purpose of VCO2 is to investigate the effects of multiple metal layers on the VCO performance.
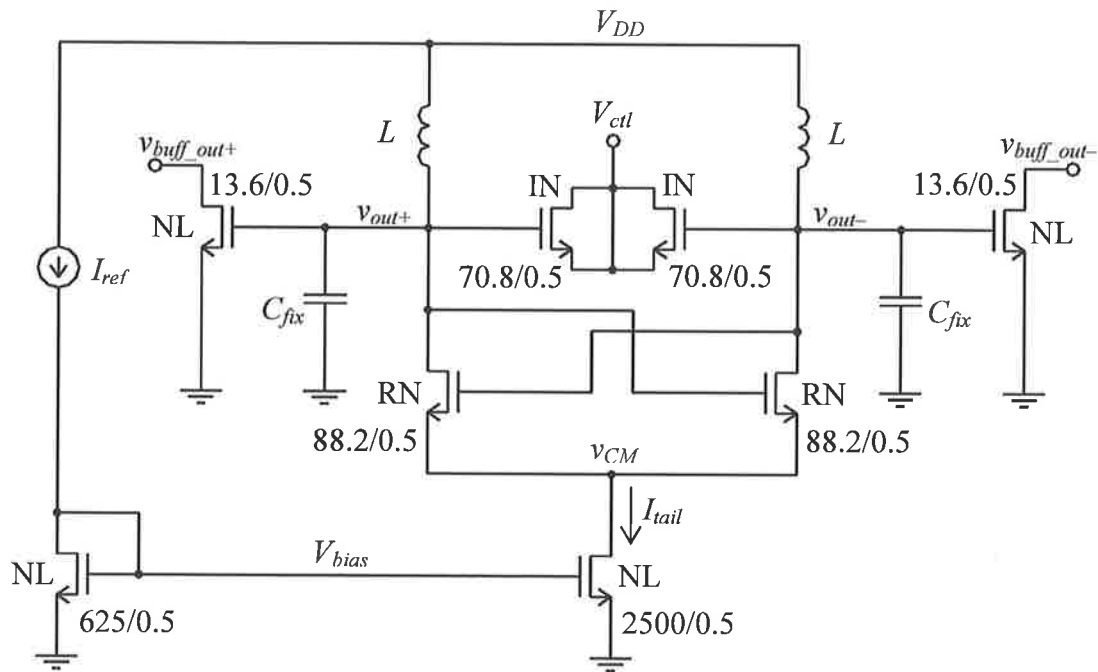
Fig. 5.1: Schematic diagram of VCO1 and VCO2.

The schematic diagram for VCO1 or VCO2 is shown in Fig. 5.1. The transistor type, and gate width to length ratio (W/L) for each transistor are also shown. The gate dimensions are in μm. The cross-coupled transistors were sized such that the VCO core draws approximately 5mA from a 1.5V supply, and maintains V_{CCP} of around 1.3V.

Other lower threshold NMOS devices were considered as not suitable for the implementation of the cross-coupled pair. Because, for a given R_{tank}, lower threshold devices must lower the oscillation amplitude in order to spend sufficient time in saturation and be able to produce the required gain.

For 5GHz operation with 200MHz of continuous frequency tuning, the minimum and the maximum total tank capacitance required are 805fF and 868fF respectively for L=1.1nH. C_{fix} of 400fF were implemented with a MIM capacitor on both sides. Sum of all unavoidable parasitic capacitances associated with the metal routings and transistors after layout extraction was 350fF. The rest of the tank capacitance was provided by the MOS varactors.

The IN type transistors were used to implement the MOS varactors. As demonstrated in section 3.3.2 with some simulation results, the $C_{v.max}$-to-$C_{v.min}$ ratio, ξ is around 3 for the SOS transistors. With the IN type devices, the frequency control voltage, V_{ctl} is effective throughout the peak-to-peak oscillator output voltage range. Other non-zero threshold voltage devices shift the effective range of V_{ctl} up or down according to the polarity and the size of their V_{TH}. For example, the RN type devices used as varactors would downshift the effective range by 0.7V.

The diode connected reference current generating transistor and the tail current bias transistor were realized with the NL type devices. The NL type devices exhibit lower flicker noise almost by an order of magnitude compared to the RN type devices [107]. A current ratio between I_{ref} and I_{tail} of 1:4 was used. The tail transistor was made as wide as possible to reduce the flicker noise and $V_{DS.sat}$.

The differential output buffer was implemented with two common-source configured NL type transistors. Drains of the buffer transistors were left floating. Two external bias-T's were to be used to bias them in measurements.

VCO3 is another NMOS-only VCO similar to VCO1, except it has a wider frequency tuning range, implemented with a 3-bit switched capacitor bank. The purpose of this VCO is to study the effects of switched capacitor bank on the VCO performance.

Fig. 5.2 shows the schematic diagram of the switched capacitor bank used in VCO3. The rest of VCO3 is similar to the one shown in Fig. 5.1. The three transistors in the middle act as the main switches between the capacitors on both sides, whereas the transistors on the sides are there to ensure low voltages on the source and the drain of the main transistors for proper switching.
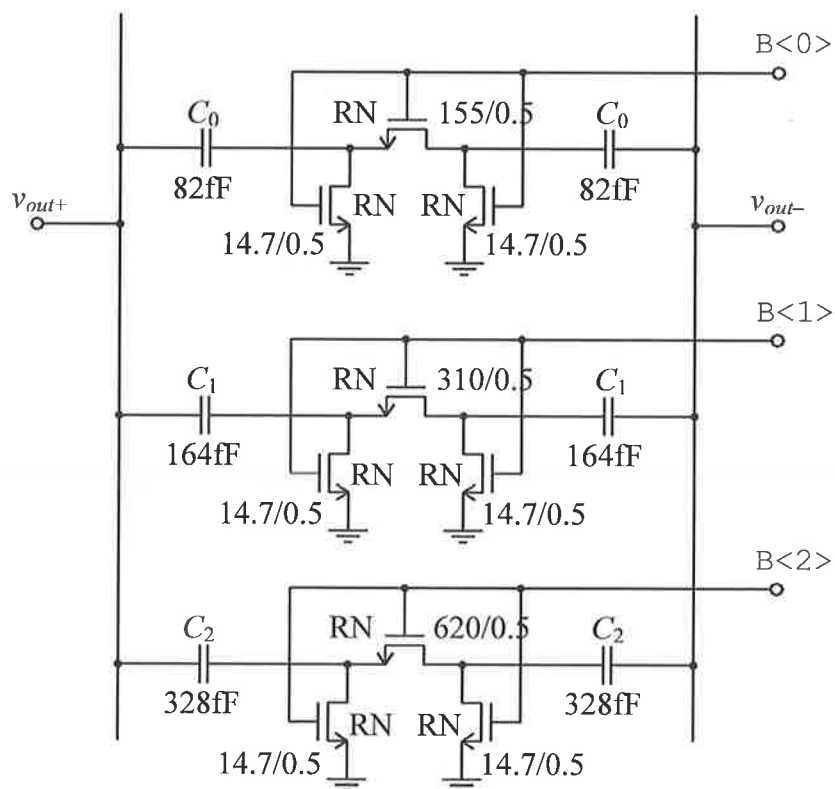
Fig. 5.2: 3-bit switched capacitor bank for VCO3.

When one of the switches is closed, two MIM capacitors on both sides are connected through the main transistor. Since the transistor channel resistance is non-zero, and it adds to the capacitor loss, Q of the capacitor-switch combination during the on state is lower than that of the MIM capacitor alone. Therefore, the main switch transistor is preferably made as wide as possible to lower the channel resistance.

When the switch is opened, large gate-to-drain/source parasitic capacitances provide a capacitive coupling between the two MIM capacitors. The consequence is reduced change in switched capacitance. Simulations showed that switching 529aF of MIM capacitor for every micrometer width of the main switch transistor results in Q of around 10 during the on state, and the resulting change in capacitance is approximately 198aF for every micrometer width of the switch transistor.

Continuous varactor tuning range was adjusted to cover approximately 1.5 times the minimum frequency step covered by the switched capacitor bank. Together with the switched capacitor bank shown in Fig. 5.2, a wider tuning range ranging from 4.7GHz to 5.5GHz, or approximately 15% tuning range was achieved in simulation. At the same time, the minimum capacitor bank Q was kept at 10. Although the maximum capacitance of the switched capacitor bank is only 574fF, the metal routings required to implement the switched capacitor bank was large enough to leave no room for C_{fix}, which is normally implemented with a high quality MIM capacitor.

VCO4 was implemented by the complementary topology. This VCO was designed to operate from double the supply voltage and half the bias current of the NMOS-only VCOs discussed earlier. Therefore, the power consumed is same as in the NMOS-only VCO. The purpose of this VCO is to find out if the complementary

topology has any notable topological superiority over the NMOS-only topology in terms of phase noise performance claimed by many in the literature [9], [18], [20], [24], [41], [51], [55], [72].
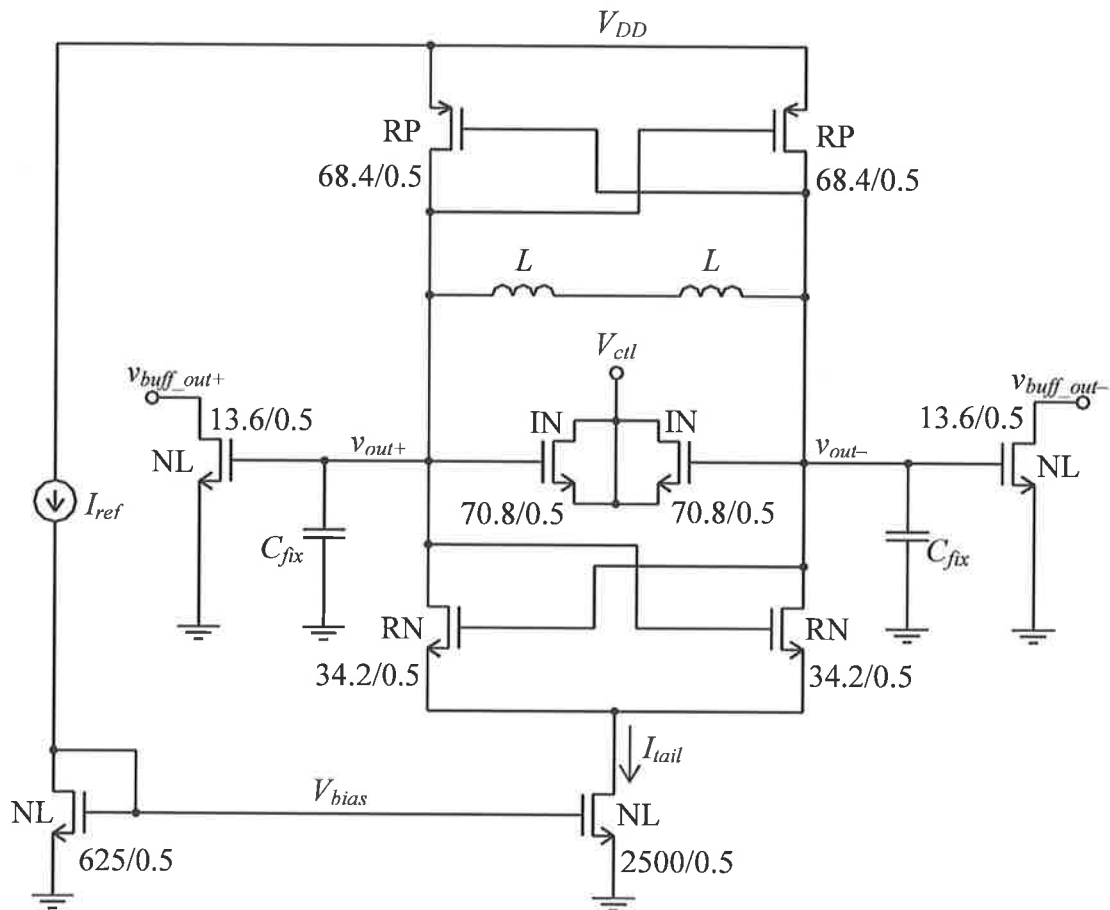
Fig. 5.3: VCO4 schematic diagram.

VCO4 schematic diagram is shown in Fig. 5.3. The NMOS cross-coupled transistors were reduced in width to account for the reduced bias current. PMOS cross-coupled transistors were made twice as wide to compensate for inherent lower gains of the PMOS transistors and to position the mean potential of oscillation at approximately half V_{DD}. The overall parasitic capacitance resulting from the two cross-coupled pairs

was larger than that from the single cross-coupled pair of VCO1 or VCO2, forcing C_{fix} to be reduced down to 220fF.

5.3.2 Inductor Designs

Spiral inductor performance, or its quality factor is proportional to the outer diameter (D_{out}), the conductor width (w), and the number of turns (N), as implied in (4.6) and (4.7). This is assuming the high frequency effects, such as the skin effect and the proximity effect are negligible. Fig. 5.4(a) shows ASITIC simulation results illustrating how Q_L varies with respect to the three aforementioned spiral inductor parameters in the absence of the two major high frequency effects. It is seen from Fig. 5.4(a) that Q_L improves monotonically with D_{out} and w. Also, for given D_{out} and w, larger N gives higher Q_L.

Fig. 5.4(b) shows ASITIC simulation results of Q_L in the presence of the two major high frequency effects. When the high frequency effects are taken into account, Q_L does not increase monotonically with w, or N. As discussed in section 4.3.3, large w, or N can cause Q_L to decrease at high frequencies due to the excessive eddy current generation near the center of the spiral. Therefore, the only parameter for which Q_L can continue to improve is D_{out}, as implied in (4.9), provided the resulting self-resonant frequency is sufficiently higher than the frequency of oscillation.

The high frequency effects also have an influence on the inductance. This is observed from comparing Fig. 5.4(c) with Fig. 5.4(d), where Fig. 5.4(c) shows the

inductance simulation results without the high frequency effects, while the other includes the high frequency effects. As discussed in the previous chapter, this is because the induced eddy currents in the spiral oppose the magnetic field that induced them and results in some reduction in the inductance.
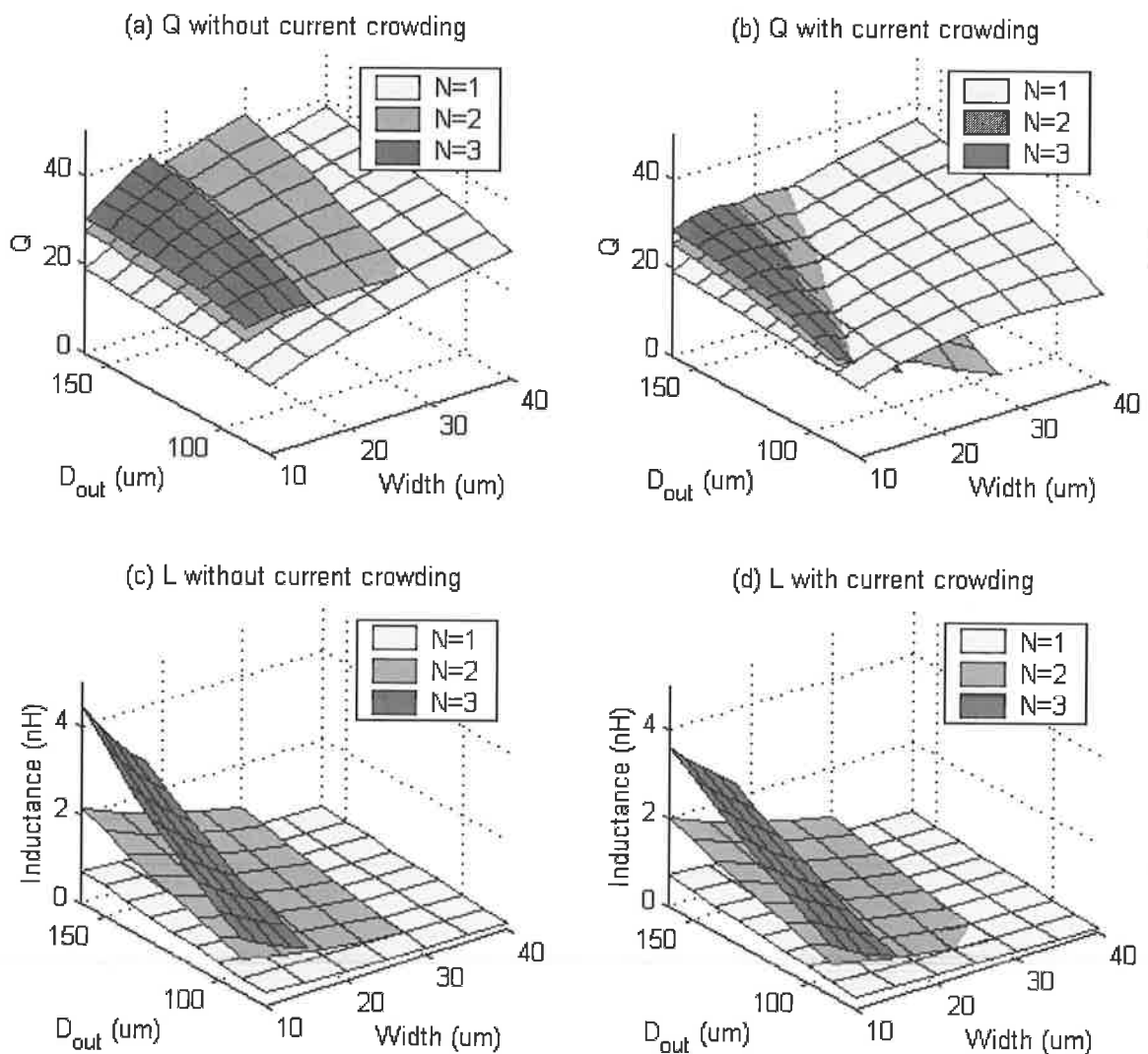
Fig. 5.4: Inductor quality factor simulation results (a) with or (b) without the high frequency effects. Inductance simulation results (c) with or (d) without the high frequency effects.

If sufficient computing resources and time are permitted, contour plots such as the ones shown in Fig. 5.4(b) and Fig. 5.4(d) can be plotted first, and then desired inductance and Q_L can be picked from the plots. Nevertheless, following the flowchart developed in section 4.3.3 for geometric spiral inductor optimization would yield the same result with a lot less number of simulations.

For inductance of 1.1nH per side, spiral geometry of D_{out}=120µm, w=14µm, s=5µm, and N=2.125 was used for the four experimental VCOs. These parameters were obtained from the simulation results in Fig. 5.4(b) and Fig. 5.4(d). The resulting Q_L is approximately 22. Fig. 5.5 shows a layout view of the pair of spiral inductors connected together for differential operation. The metal under path connecting the inner end of the spiral to the outside is implemented by the two lower metal layers connected together with vias.

All three metal layers were used for the spirals, except for the spirals used in VCO2. Simulated Q_L for the single top metal layer spiral with the same geometry is around 25. The difference in Q_L is arising from the difference in series AC resistances calculated by ASITIC. The series resistance for the single layer inductor is 1.42Ω, whereas the series resistance for the multi layer inductor is 1.56Ω. The difference is only around 9%. Nevertheless, unlike one might expect, it is in favor of the single layer inductor. Simulated inductance is around 5% lower for the multi layer spiral. It is thought that extra eddy current generated in lower metal layers is responsible for the extra reduction in the inductance for the multi layer spiral.

The structure shown in Fig. 5.5 was simulated again in HP Momentum, which is able to simulate more complex structures accurately at the expense of much longer simulation time and more computing resources. Due to the extra conductor length

provided by the metal under path and the metal routing that joins the two spirals together, the effective inductance per side was increased to approximately 1.2nH.
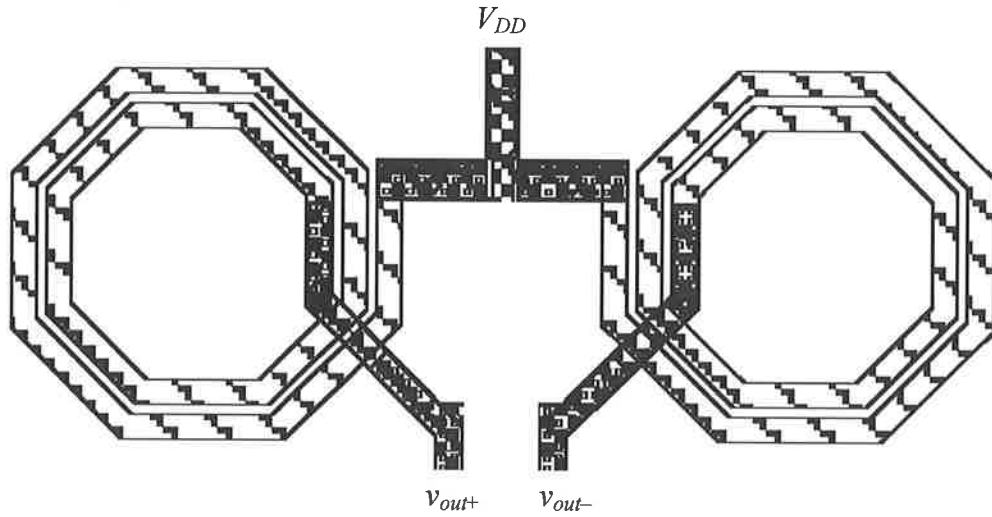
Fig. 5.5: Spiral inductor pair for differential operation.

HP Momentum estimated the self-resonant frequencies of the two different inductors in the vicinity of 34GHz, which is much higher than the frequencies of oscillation. This means Q_L is mostly determined by the series AC resistance of the spiral and not limited by the inductor parasitic capacitors. Therefore, either one of the following two equations can be used to estimate the equivalent parallel tank resistance.

$$R_{tank} = \omega_0 L Q_{tank} \tag{5.1}$$

$$R_{tank} = \frac{Q_{tank}}{\omega_0 C} \tag{5.2}$$

Here Q_{tank} was estimated by (4.1). Estimated R_{tank} for all four VCOs was approximately 550Ω.

The test VCOs were laid out as shown in Fig. 5.6. Total chip area occupied by the four VCOs, including pads is 2.075mm^2.
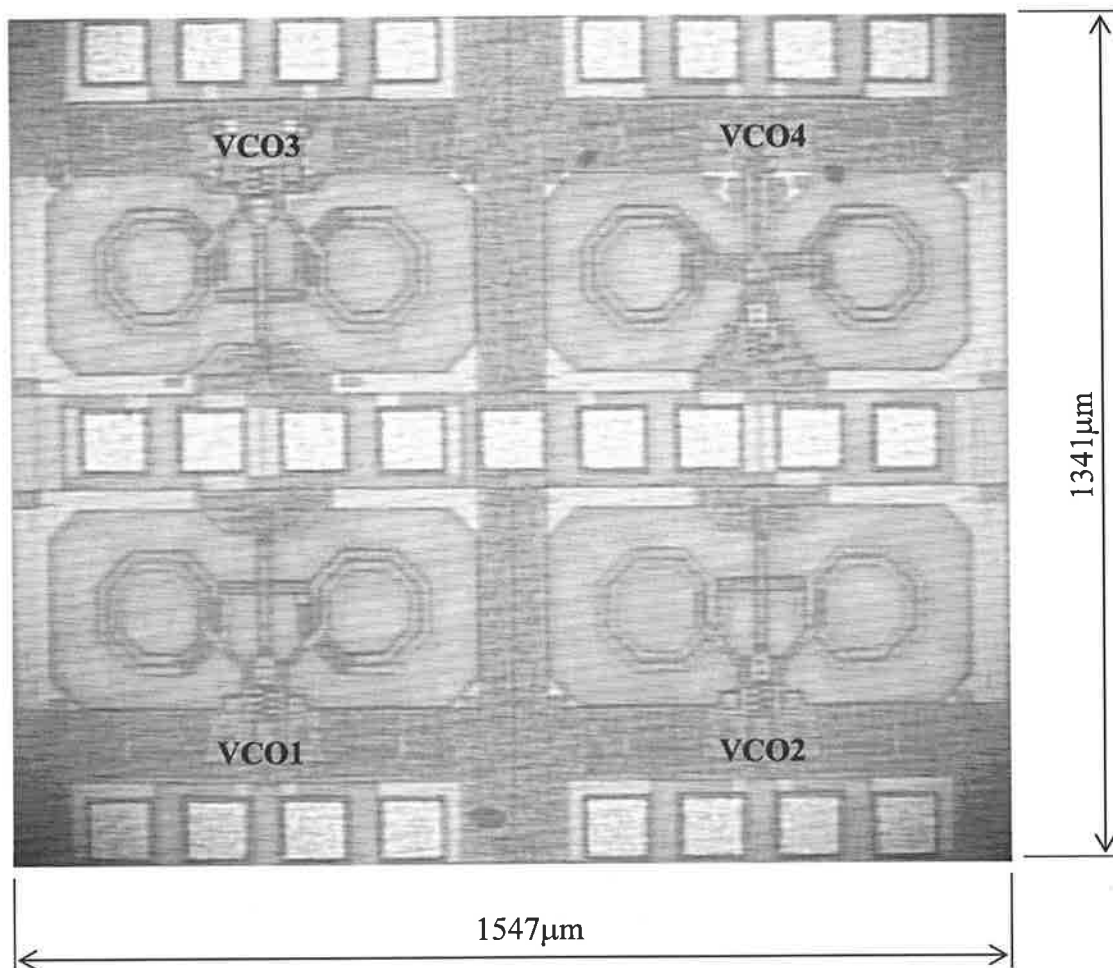
Fig. 5.6: Four experimental 5GHz VCO microphotograph.

5.3.3 Results

The phase noise measurements of the VCOs were made with the measurement setup shown in Fig. 5.7. The VCO test chip was biased with a 6-pin needle probe, while

the output was probed with a Ground-Signal-Signal-Ground (GSSG) air coplanar 40GHz probe. Bias voltages and currents required by the VCO circuits were generated by a custom built bias and control signal generator. The buffered differential output from a VCO was firstly fed to a 180° hybrid, through two bias-T's. This provided an identical loading condition on each end of the differential VCO outputs. The combined signal was then split into two by another 180° hybrid. One end was fed to a spectrum analyzer, while the other was fed to the phase noise measurement set, PN9000.
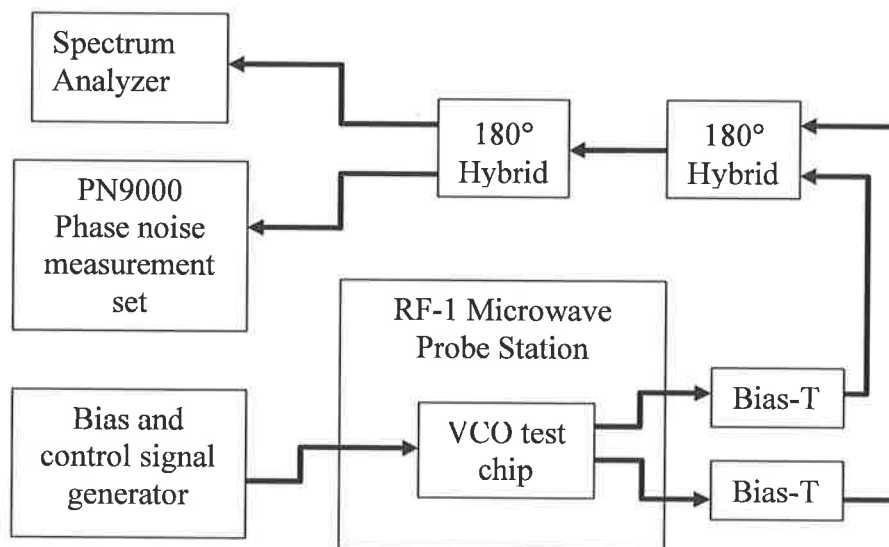
Fig. 5.7: Phase noise measurement setup for experimental 5GHz VCOs.

PN9000 uses a delay line that acts as a frequency discriminator. It is able to measure phase noise of a free running VCO without needing to lock the oscillation frequency with a PLL. This instrument requires its input signal power to be maintained between −5dBm and +5dBm. The spectrum analyzer was there to monitor the signal

power level for PN9000. At the same time, the spectrum analyzer measured the frequency of oscillation.

VCO1 and VCO2 showed almost identical phase noise performance. The only notable difference between the two VCOs was that VCO1 oscillated slightly faster with a constant offset frequency of around 130MHz for all I_{tail}. The same frequency offset was observed for every test chip tested. The difference could not be attributed to the process variation, because the VCOs were fabricated next to each other. The frequency offset was around 2.5%, which may be explained by the 5% reduction in inductance for the multi layer spiral inductors.

Fig. 5.8(a) shows the frequency variation with respect to the control voltage at various tail bias currents for VCO2. The frequency tuning curves can be used to estimate the amplitude of oscillation at different tail bias currents.

VCO1 and VCO2 were almost identical in terms of phase noise performance. Fig. 5.8(b) shows the phase noise variation with respect to V_{ctl} for VCO2 with I_{tail}=1.1mA. 1.1mA is the minimum bias current that ensured a sustained oscillation for VCO2. The VCO constant, or K_V is maximum under this bias condition, because A_0 is minimum. Therefore, the phase noise plotted in Fig. 5.8(b) represents the worst-case phase noise. A slight increase in phase noise was observed near the center of the tuning range, where K_V is maximum because V_{ctl} is at its halfway point, V_{DD}.
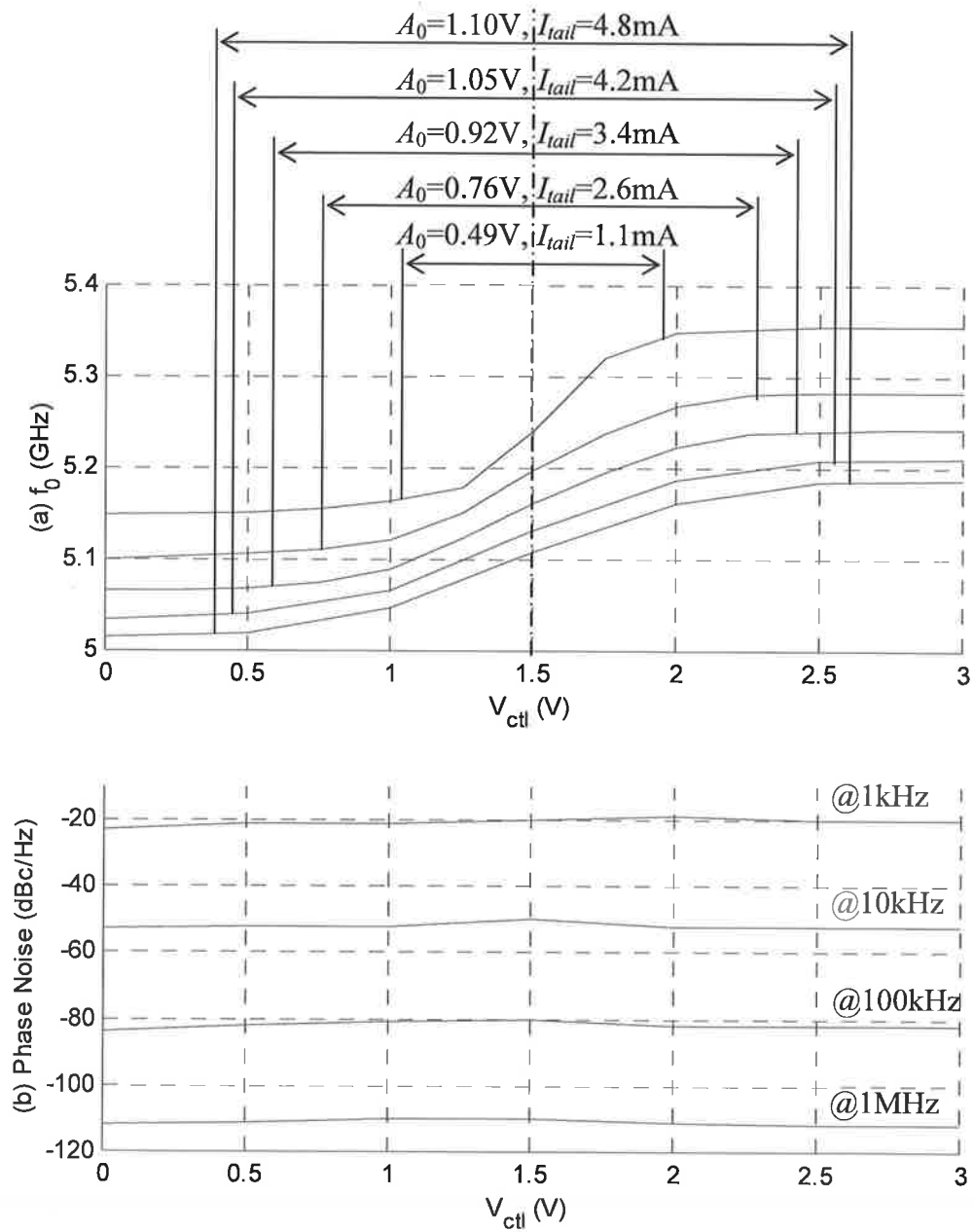
Fig. 5.8: (a) f_0 versus V_{ctl} at various I_{tail} and (b) phase noise across full tuning range for VCO2 with I_{tail}=1.1mA.
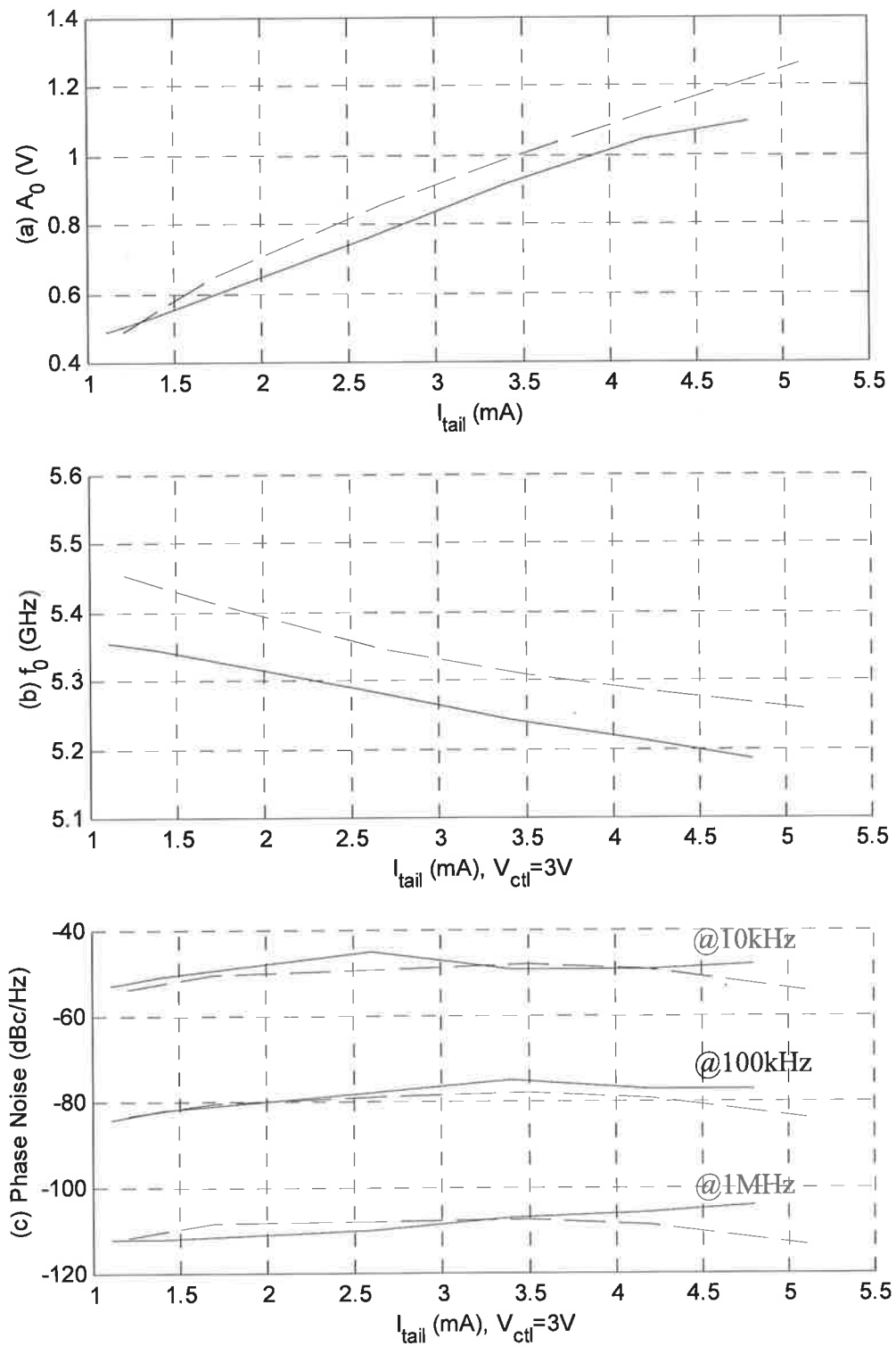
Fig. 5.9: Measured (solid) and simulated (dashed) (a) A_0, (b) f_0, and (c) phase noise versus I_{tail} for VCO2 with V_{ctl}=3V.

The oscillation amplitudes estimated from Fig. 5.8(a) are plotted in Fig. 5.9(a) along with simulated A_0 over a range of I_{tail}. The two curves show a good match. Fig. 5.9(b) shows how the frequency of oscillation varies with respect to I_{tail}. The negative slope is attributed to the variation in the parasitic gate capacitance of the cross-coupled transistors as explained in section 3.4.2.

Simulated and measured plots of phase noise are shown in Fig. 5.9(c). According to the LTI theory of phase noise, the phase noise should decrease quadratically with increasing A_0. However, the measurements showed increasing phase noise with respect to I_{tail} or A_0. This counterintuitive behavior was also observed in phase noise simulations. Fig. 5.10 explains this unusual behavior of the VCO phase noise. Simulations showed that as I_{tail} was increased, noise contribution from the tail bias network was rapidly increased, especially the flicker noise components from the tail transistor and the diode-connected transistor. Since the simple LTI model does not account for the flicker noise upconversion, the phase noise behavior of these VCOs cannot be explained by the LTI model within the flicker noise dominated close-in frequency offset region.
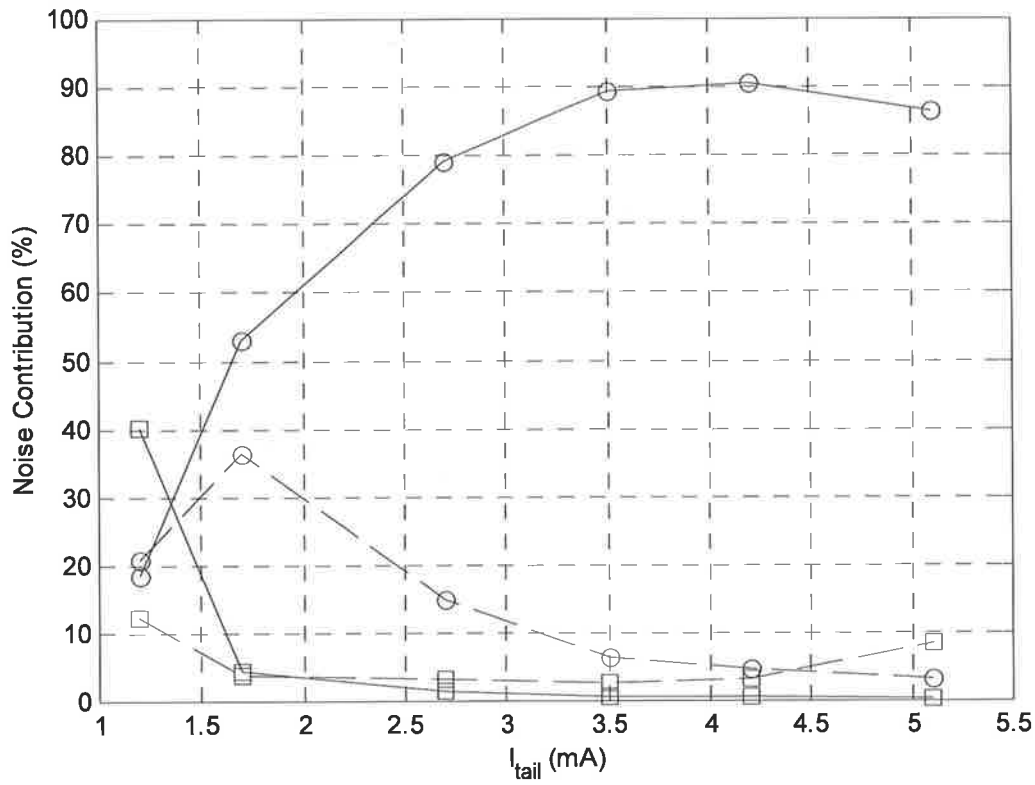
Fig. 5.10: Simulated flicker noise (solid) and white noise (dashed) contributions from tail current bias network (O) and cross-coupled pair (□) versus I_{tail} for VCO2 at 1MHz offset.
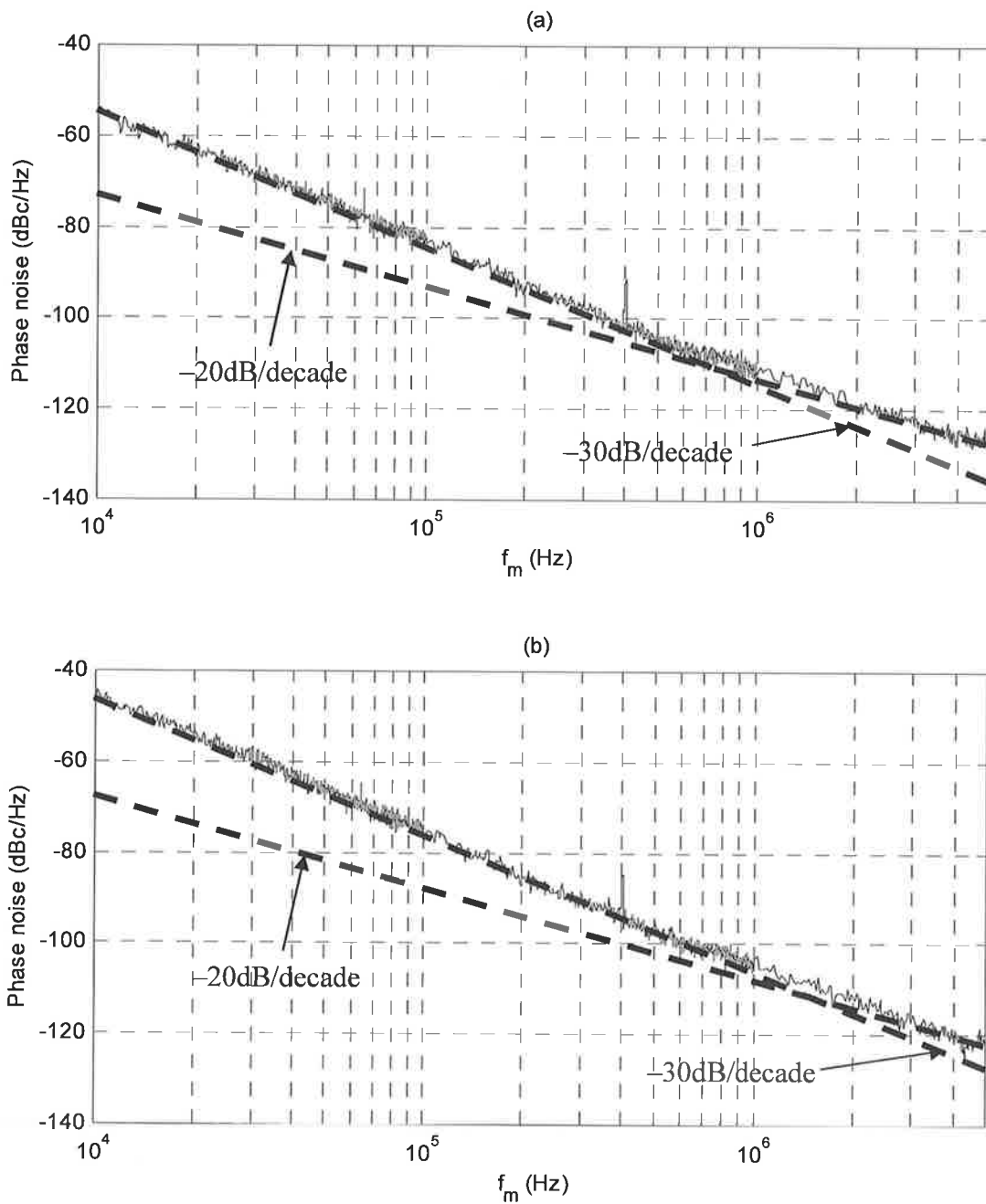
Fig. 5.11: Spectral plots of measured phase noise of VCO2 at (a) I_{tail}=1.1mA, and (b) I_{tail}=4.8mA.

Two spectral plots of phase noise for VCO2 are shown in Fig. 5.11. The corner frequency between the −30dB/decade region and the −20dB/decade region is located at

around 800kHz offset from the carrier when I_{tail}=1.1mA, whereas the corner frequency

is at around 1.7MHz when I_{tail}=4.8mA. This means that the flicker noise is increased

faster than the white noise as I_{tail} is increased. This is in agreement with the phase noise

simulation result shown in Fig. 5.10.
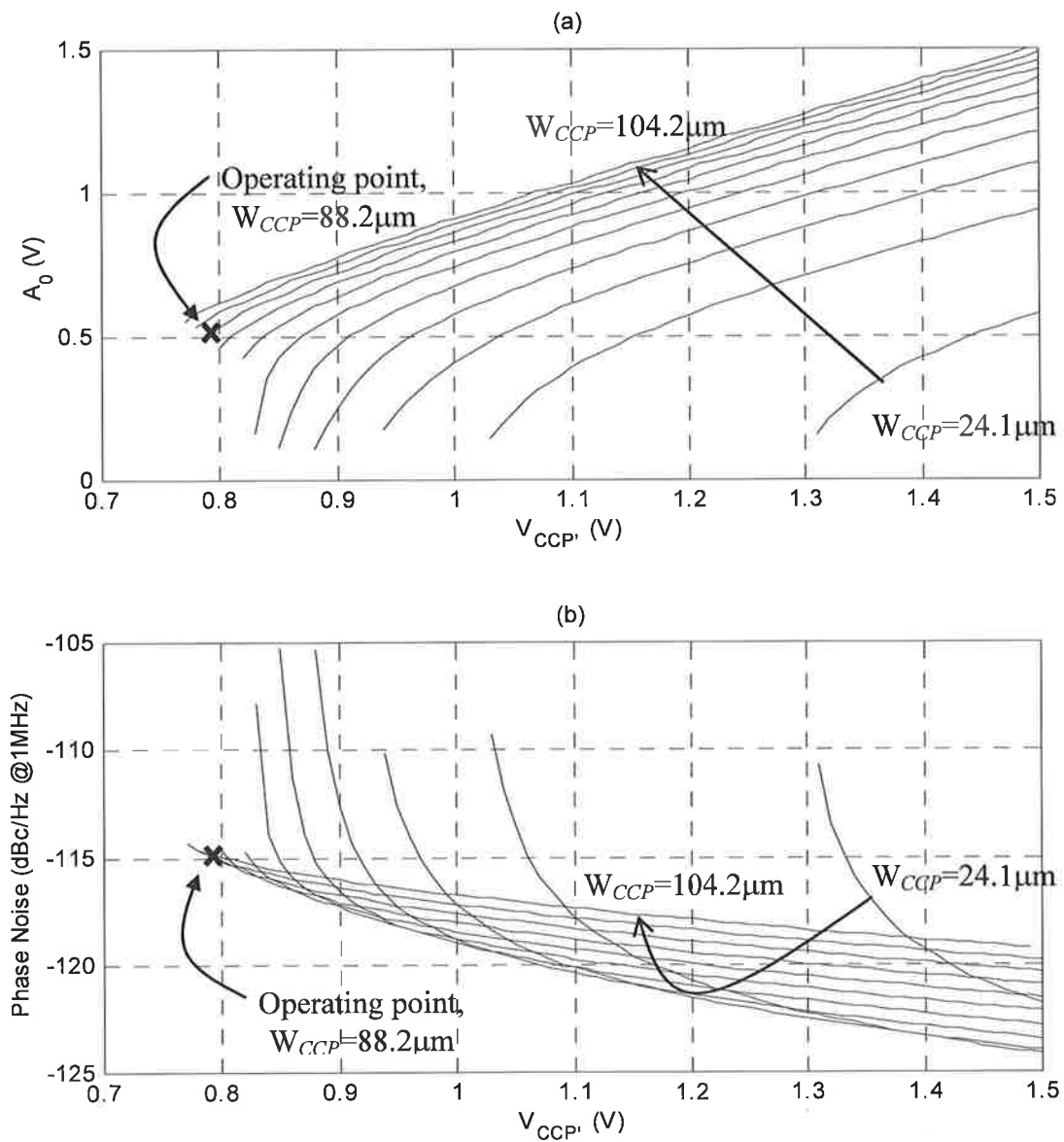
Fig. 5.12: VCO2 (a) bias space, and (b) phase noise space with constant R_{tank} of 550Ω.

The bias space and the phase noise space are plotted for VCO2 with R_{tank}=550Ω in Fig. 5.12(a) and Fig. 5.12(b) respectively. The operating points of VCO2, when biased with I_{tail}=1.1mA are marked with crosses on the two operating spaces.

The actual phase noise measured at 1MHz offset is around −110dBc/Hz while the LTI model estimation is as low as −115dBc/Hz. The difference of 5dB can be attributed to the upconverted flicker noise of the cross-coupled pair and the noise folded down from higher order harmonics due to the oscillator nonlinearity. These are not modeled in the simple LTI model.

Unfortunately, as I_{tail} or V_{CCP} was increased, the flicker noise contribution from the tail current bias circuit became the dominant source of the phase noise. Therefore the phase noise space plotted based on the simple LTI model rapidly loses its accuracy.
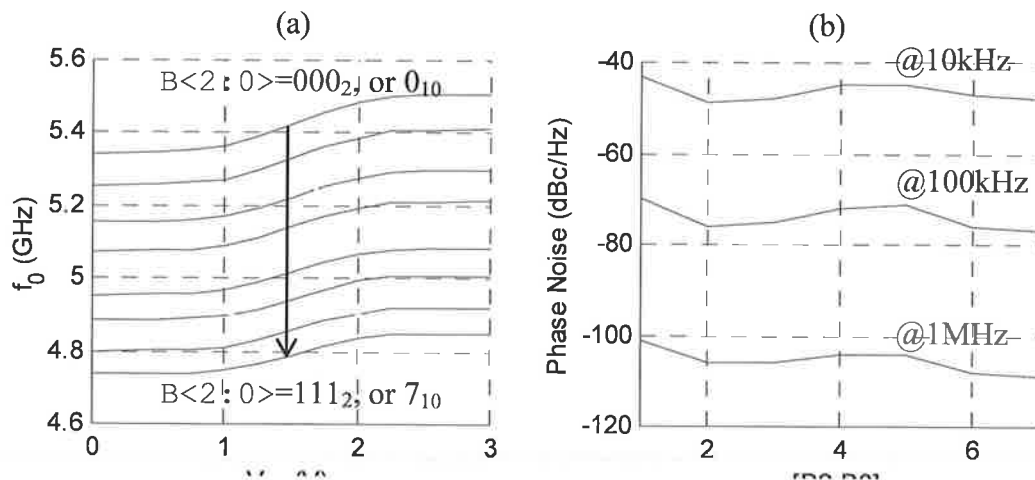
Fig. 5.13: (a) Measured f_0 versus V_{ctl} across full tuning range and (b) measured phase noise versus 3-bit digital frequency control input for VCO3.

The frequency of oscillation and the phase noise measurement results for VCO3 are plotted in Fig. 5.13(a) and Fig. 5.13(b) respectively. The total frequency tuning range spans from 4.75GHz to 5.5GHz. This is approximately 14.6% tuning range.

Compared to 3.8% tuning range achieved by VCO1 or VCO2, it is a significant improvement. The phase noise is somewhat worse than that of VCO1 and VCO2 on average. This may be attributed to the fact that Q of the capacitor bank is lower than that of a MIM capacitor.
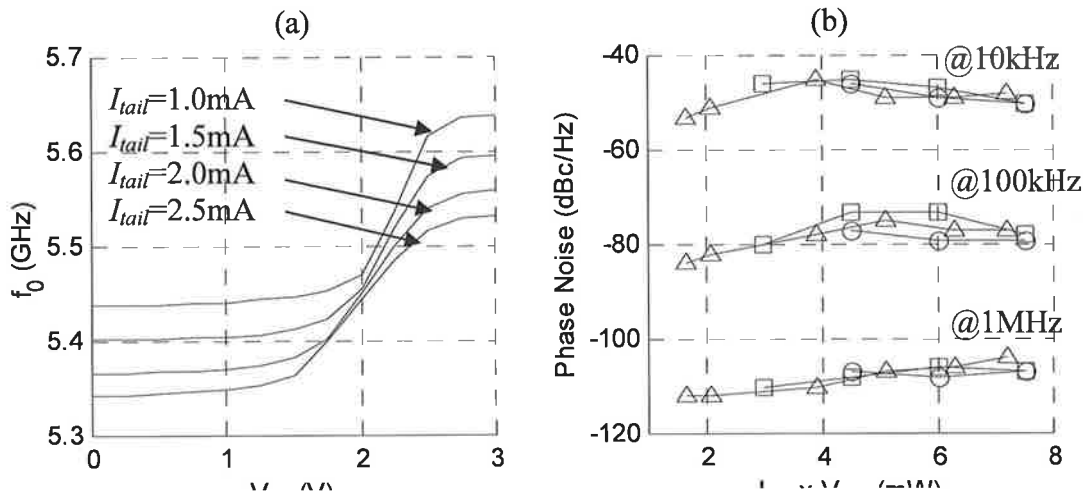
Fig. 5.14: (a) f_0 versus V_{ctl} at various I_{tail} for VCO4, and cross comparison of phase noise of VCO2 ($\triangle$), VCO3 ($\square$), and VCO4 (O) over a range of DC power consumption.

The frequency tuning curves of VCO4 at different tail bias currents are plotted in Fig. 5.14(a). Although the DC bias potential of the output waveform was targeted to be half V_{DD} or 1.5V in design, unpredictable transconductance mismatch between the NMOS and the PMOS devices caused the output DC bias potential to drift with the tail bias current as can be seen from Fig. 5.14(a). Note that the center frequency of oscillation corresponds to V_{ctl}=2V when I_{tail}=2.5mA, whereas the center frequency of oscillation corresponds to V_{ctl}=2.3V when I_{tail} is reduced to 1.0mA. This drift in the mean potential of the output provides a ground for the CMM-to-FM noise upconversion process discussed in section 3.4.2.

The phase noise performance of VCO4 is comparable with that of VCO1 or VCO2. Fig. 5.14(b) shows phase noise plots of VCO1, VCO2, and VCO4 with respect to their power consumption. No significant difference in phase noise is observed between the two different topologies. Therefore, as discussed in section 3.2, there exists no obvious topological advantage between the two topologies in terms of phase noise performance. One should choose the topology based on power supply condition.

With the complementary topology, the complementary cross-coupled pairs must be sized carefully to set the bias potential of the output waveform near the half V_{DD} potential to avoid premature amplitude clipping by hitting the supply rails. Also, it should be noted that the drifting output bias potential could potentially increase the upconverted flicker noise contribution in the phase noise through the CMM-to-FM conversion process.

Table 5.2: VCO2 phase noise performance comparison.

Reference	f_0 (GHz)	V_{DD} (V)	I_{tail} (mA)	Power (mW)	Phase Noise (dBc/Hz @1MHz)	FOM (dBc/Hz)
[23]	4.00	2.5	7.5	18.8	−117	−176.3
[10]	5.50	1.5	4.6	6.9	−116	−182.4
[24] w/ tail	5.00	2.5	2.0	5.0	−110	−177.0
[24] wo/ tail	5.00	2.5	2.9	7.3	−117	−182.4
VCO2	**5.25**	**1.5**	**1.1**	**1.65**	**−110**	**−182.2**

The phase noise performance of VCO2 compares well against other recently published 5GHz CMOS VCOs. VCO2 was first published in year 2003 [112]. Although the phase noise is not the lowest reported, the power consumption is the lowest among the 5GHz VCOs reported to the date of publication [112]. Also, the low FOM of −

182.2dBc/Hz is quite comparable to other high performance VCOs at the time of publication. Table 5.2 compares the performance of VCO2 against some of the high performance VCOs reported in the literature. Comparison against further VCOs is made at the end of Chapter 6.

5.4 EXPERIMENTAL 17GHZ VCOS

A set of experimental 17GHz VCOs was fabricated on the same test chip containing the four experimental 5GHz VCOs of the previous section. The purpose of implementing these 17GHz VCOs was to investigate the effects of multi layer inductors on the performance of VCOs operating in the Ku band (12–18 GHz), and the feasibility of 17GHz operation with the SOS technology under investigation.

The effects of multi layer inductors observed in the 5GHz VCOs were minimal. The only notable difference was the slight decrease in f_0 due to the increased inductance of the single layer inductors in VCO2. Apart from that, no other observable difference was noted in measurements. However, at higher frequencies, the high frequency effects on multi layer inductors are expected to be more pronounced and hence become observable in measurements.

It is interesting to note that the frequency of oscillation under interest for these VCOs is actually higher than the unity-current-gain frequencies of transistors available in this technology. Nonetheless, because the unity-power-gain frequencies of the devices are still higher than the frequency of oscillation, 17GHz oscillation should be possible, at least in theory. The VCOs were laid out with extra care to minimize

parasitic thermal losses associated with metal routings, otherwise the VCOs may not oscillate.

5.4.1 VCO Designs

Four 17GHz VCOs are designed and fabricated. They are based on the NMOS-only topology, and use inversion mode MOS varactors for continuous tuning.
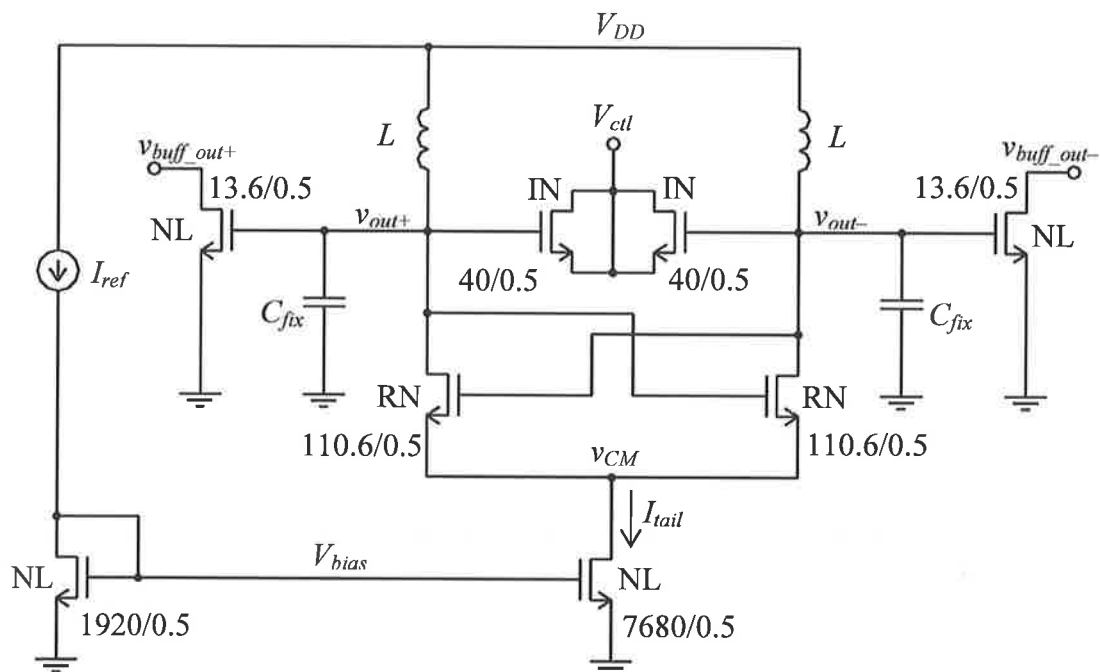
Fig. 5.15: Schematic diagram of VCO5 and VCO6.

The first two VCOs, VCO5 and VCO6 are identical except for the number of metal layers used in their inductors. VCO5 used all three metal layers, whereas VCO6 used only the top metal layer. Fig. 5.15 shows the schematic diagram for VCO5 and

VCO6. The other two VCOs have reduced tuning ranges. Since they do not have any new academic significance, their analysis is omitted in this thesis.

Extracted parasitic capacitance from the layout, arising from the cross-coupled transistors, the MOS varactors, and the metal routings was around 550fF per side. This was rather high for 17GHz operation, and forced L to be at around 0.1nH. Targeted tuning range was around 600MHz, starting from 16.8GHz to 17.4GHz. This left very small margin on C_{fix}. C_{fix} is only 57fF in this case. Therefore there the tuning range expandability is very small, unless L is reduced below 0.1nH.

Reducing L to incorporate larger varactors for larger tuning range would reduce the L/C ratio, and it must not accompany increased transistor width of the cross-coupled pair to limit the parasitic capacitance. Doing so implies reduced oscillation amplitude due to reduced parallel equivalent tank resistance at resonance. Therefore, wider tuning range is difficult to achieve at high frequencies, where parasitic capacitance dominates the tank capacitance.

One way to increase the tuning range would be to have multiple VCOs with different center frequencies to cover the required tuning range and switch between them during operation. However, this approach is considered highly area inefficient.

Another approach would be to use one or more frequency doublers to achieve the target frequency with a VCO running at a fraction of the target frequency. Low-frequency VCOs can have wider tuning range owing to relatively larger capacitance in the tank, and relatively smaller percentage contribution from the parasitic capacitors.

5.4.2 Inductor Designs

Following the guidelines developed for the design of high Q inductors in section 4.3, a single turn inductor geometry was found for the two 17GHz VCOs. Since the inductance required was relatively small, a single turn, differential inductor could be realized while occupying a reasonably small chip area.

Fig. 5.16 shows the microphtograph of VCO5 and VCO6, occupying around 1.12mm^2. The octagonal ring inductor with outer diameter of 220µm and metal width of 35µm is center-tapped in the middle to V_{DD} for differential operation.
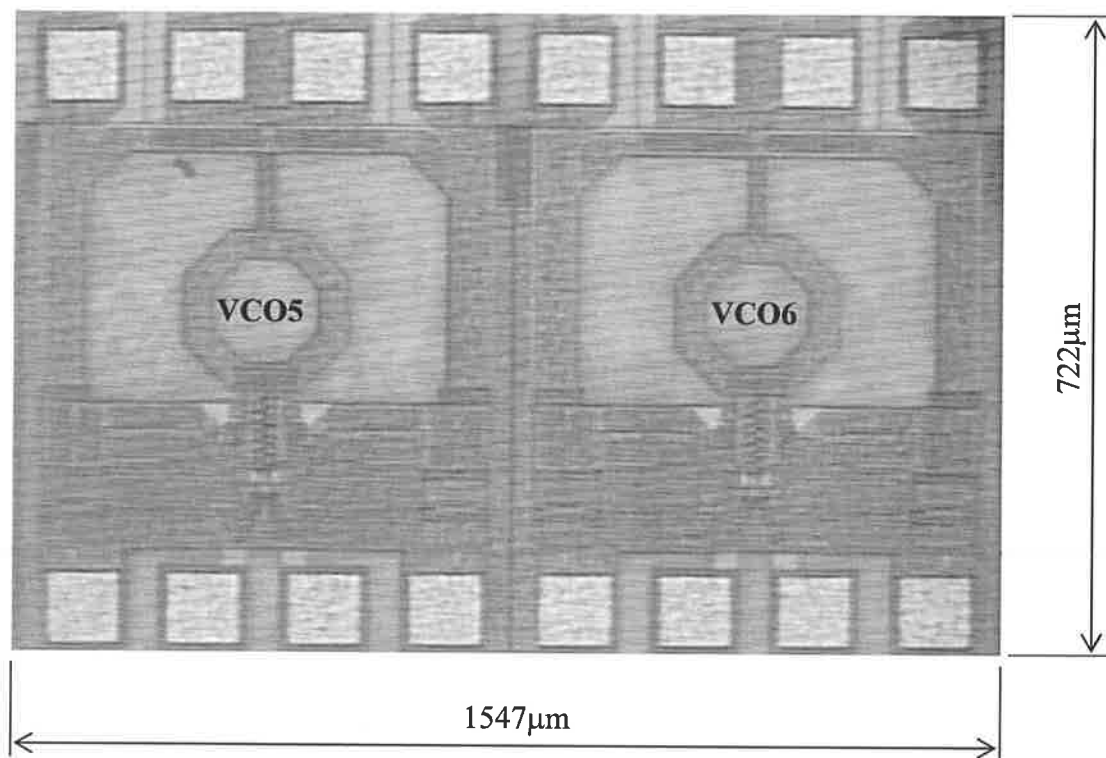
Fig. 5.16: Microphtograph of VCO5 and VCO6.

The simulated inductance of the octagonal ring was around 0.224nH for the multi layer structure, providing around 0.112nH per side. The single layer structure showed a little higher inductance of 0.116nH per side.

While the two simulated inductors showed a small difference in inductance, the simulated Q_L of the multi layer inductor and the single layer inductor were 24 and 48 respectively. Estimated self-resonant frequencies of both inductors were in the vicinity of 80GHz. Therefore, the difference in Q_L is mostly due to the difference in AC series resistance of the two structures. Again, it seems counterintuitive that the multi layer inductors are lossier than the single layer inductors.

5.4.3 Results

Measurements were carried out with the measurement setup shown in Fig. 5.17. Because 180° hybrid operating around 17GHz was not available at the time of measurements, two identical RF power amplifiers (PA) were used to provide a balanced loading condition on each end of the differential output of the VCO under test. Each PA has a gain of 25dB.

The phase noise measurement set, PN9000 accepts input frequencies between 2GHz to 5.9GHz. The VCO output was mixed with a clean sinusoidal 13GHz signal from a signal generator, and downconverted to the acceptable input frequency range of PN9000. The PA provided a sufficient gain before the passive mixer to minimize the SNR degradation of the VCO output.

The designated power consumption of each VCO was to draw 12mA from a 1.5V supply. In simulations, the VCOs oscillated even at half the designated current. In measurements however, neither of the VCOs oscillated under the designated supply condition. VCO5 only started to oscillate with 2.2V supply voltage, while drawing 16mA. The starting supply condition for VCO6 was 13mA from a 1.8V supply.

The lower minimum power required to start implies higher resonator Q. It is interesting to note that the difference in the minimum power required for oscillation between the two VCOs is arising solely from the difference in their inductor construction.
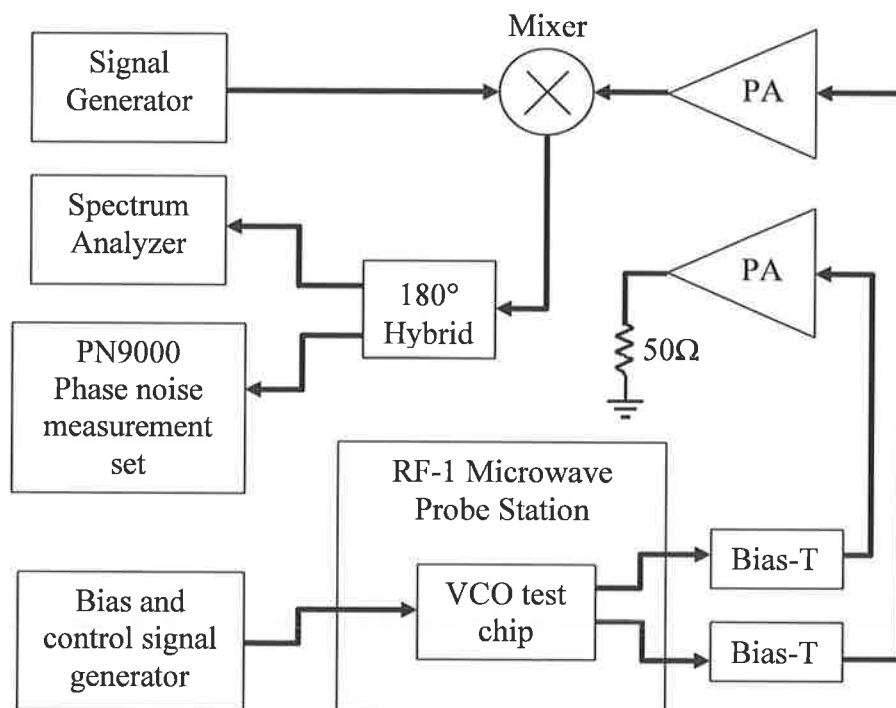
Fig. 5.17: Phase noise measurement setup for experimental 17GHz VCOs.

Another discrepancy between the simulation and measurement results is the frequency of oscillation. Fig. 5.18(b) shows the frequency tuning curves of the two

VCOs. Both VCOs were designed to oscillate from 16.8GHz to 17.4GHz. However, not only the two VCOs oscillated with a large frequency offset (>700MHz) from each other, the average frequency of oscillation is shifted up by around 1.4GHz for VCO5, and 700MHz for VCO6.
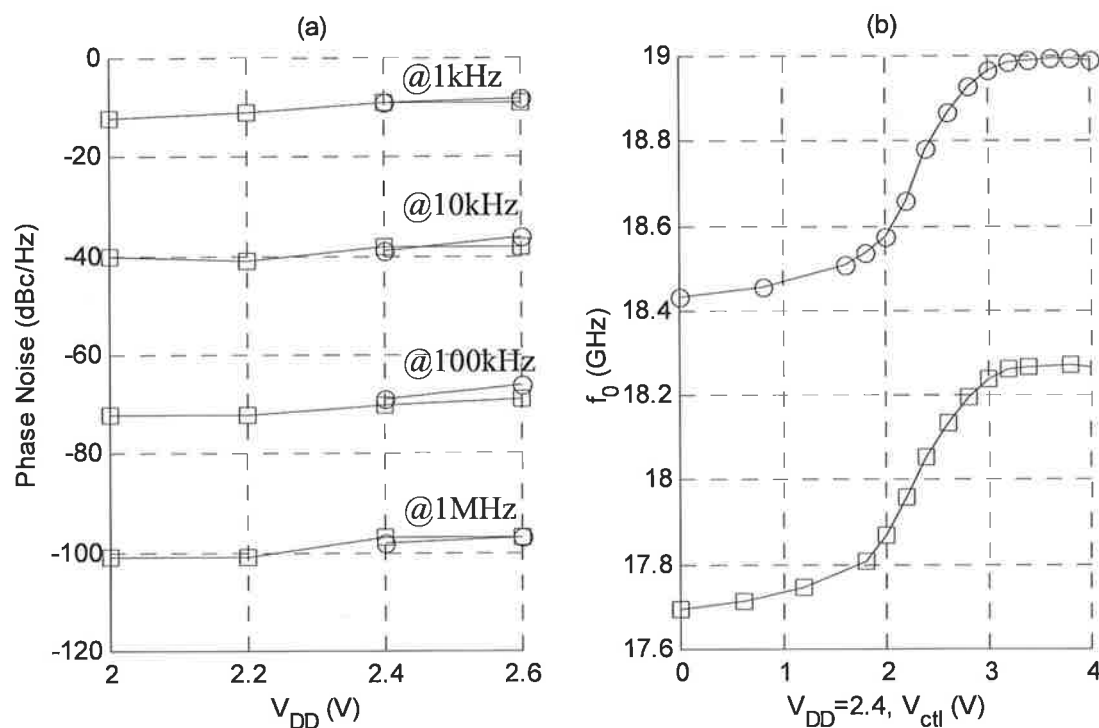
Fig. 5.18: (a) Phase noise plot and (b) frequency tuning curves of VCO5 (□) and VCO6 (O).

Since VCO5 and VCO6 were fabricated on the same wafer as the experimental 5GHz VCOs of the previous section, the process variation in capacitance must have been the same as in the 5GHz VCOs. VCO2 showed around 2% difference in f_0 between simulation and measurement. On the other hand, the difference observed is around 8% for VCO5, and 4% for VCO6. The 2% error in 5GHz VCOs included the process spread of capacitance, as well as errors in the inductance simulations. Because

the process spread of capacitance was same for all VCOs, the excessive frequency offset observed in VCO5 and VCO6 must have come from their inductance simulations.

In Ref. [113] it is states that both the magnitude and phase of current inside a conductor are functions of the depth into the conductor at high frequencies. At π skin depths into a conductor, the current phase is 180° to that of the surface current. As a result the overall current is reduced because of current direction change inside the conductor [113]. There exists a conductor thickness where the ohmic loss is minimum. This was first reported in [114], and experimentally confirmed in [115]. The optimal conductor thickness of a microstrip line that minimizes the minimum AC series equivalent resistance is reported to be between $\pi/2$ and 3 skin depths depending on the conductor width [115], [116].

The skin depth at 17GHz is around 0.64μm for aluminum. That means 3.1μm thick top metal made of aluminum is around 4.8 skin depths thick, which is somewhat thicker than the possible optimal thickness range of $\pi/2$ to 3 skin depths. The multi layer inductor has an overall thickness of 7.53μm. This multi layer structure is similar to having a single metal layer with thickness of 7.53μm, and somewhat reduced effective conductance due to the low fill ratio. This multi layer conductor is more than 10 skin depths thick, which is far from the optimal thickness.

Current flowing deep inside the conductor with phase offset of 180° to that of the surface current means reduced net current. This not only means increased ohmic loss, but also means reduced inductance. That is why the VCOs with multi layer inductors, such as VCO1, or VCO5 are oscillating at higher frequencies, because the multi layer

inductor structures contain more antiphase current components than the single layer ones.

Since the amount of thermal loss in the multi layer structure is greater, VCO5 requires a higher starting V_{DD} and I_{tail} than VCO6. Therefore, it is important to note that unnecessarily thick conductor actually degrades the inductor performance at very high frequencies.

This particular high frequency effect is taken into account in ASITIC only to a certain extent. The vertical separations between metal layers are used to calculate different current density for each metal layer, but the current distribution across the thickness of each conductor is not calculated. As a result, the simulated metal conductance improves monotonically with the metal thickness specified in the simulation despite the fact that there exists an optimal thickness at a given high frequency. ASITIC overestimated the inductances of the two different inductors at 17GHz, and the amount of error is larger with the multi layer inductors.

As it was the case with the experimental 5GHz VCOs, the flicker noise dominated the phase noise of the 17GHz VCOs at least up to 1MHz offset from the carrier. This can be seen from Fig. 5.18(a), where the phase noise of VCO5 and VCO6 are plotted at different frequency offsets that show approximately 30dB decrease in phase noise for every decade increase in the offset frequency.

At 17GHz, the inductors are not the dominant lossy elements. The MIM capacitors in this process have Q of approximately 10 at 17GHz. The parasitic capacitors arising from metal routings are expected to have Q similar to, or lower than that of the MIM capacitor. Also, the MOS varactors certainly have Q lower than that of the MIM capacitor, because of the lower conductances of the transistor gate and the

channel compared to that of the metal layers used as the capacitor plates in the MIM capacitor. Therefore, the resulting Q_C would be lower than the already low Q of the MIM capacitor at 17GHz.

Since Q_L is at least a factor of 2 or 4 larger than Q_C, Q_{tank} is mostly determined by Q_C, while Q_L has a relatively smaller influence on Q_{tank}. This is the reason why the two VCOs oscillate with a similar amplitude size despite the huge difference in the inductor Q values between the two VCOs. The oscillation amplitudes can be estimated from the frequency tuning curves shown in Fig. 5.18(b).

Also, despite the large difference in Q_L, the phase noise performances of VCO5 and VCO6 are quite similar. This can be seen from Fig. 5.18(a). Again, this is because the resulting Q_{tank}, and A_0 for both VCOs are similar.

The phase noise tends to increase slightly with the increased supply voltage or the tail bias current. This is can be attributed to the fact that the excessive flicker noise contribution from the cross-coupled pair and the tail current bias circuit increases faster than the oscillation power as it was the case with the 5GHz VCOs.

Due to the excessive device flicker noise, the phase noise performance of the 17GHz VCOs compare poorly against other previously published bulk CMOS VCOs. For example, the 17GHz VCO reported in [108] is implemented with standard 0.25μm bulk CMOS process. It achieved phase noise of −108dBc/Hz at 1MHz offset while drawing only 7.5mA from a 1.4V supply. Therefore, the 0.5μm SOS technology under investigation does not provide a better alternative for 17GHz VCO implementation, because of the excessive flicker noise in the transistors.

One way to produce improved phase noise at 17GHz with the SOS technology under investigation would be to use a couple of frequency doublers to generate the

17GHz oscillation with a low frequency VCO tuned at around 4.25GHz. At 4.25GHz, Q_C is larger than Q_L. Also, the resulting Q_{tank} is much larger than that of the 17GHz tank. Furthermore, at lower frequencies, the parasitic capacitor contribution towards the total C is lower. Hence, larger varactors can be used, and the resulting tuning range is increased.

Additional advantage of this approach is that it does not require 17GHz prescaler or frequency divider. A prescaler is not a part of a regular VCO, but is required for frequency synthesis with a PLL. A prescaler would be very difficult to implement at frequencies above f_T. Nevertheless, at 4.25GHz, it becomes much easier to implement one.

5.5 LOW-NOISE 5GHZ VCOS

The second and the third 5GHz VCO test chips fabricated with the 0.5µm SOS process are basically aimed to improve the phase noise by lowering the L/C ratio. Although the close-in phase noise of VCOs fabricated in this technology is limited by the flicker noise of the transistors, improvement in phase noise is expected by using a lower L/C ratio and more power. Six low-noise 5GHz VCOs have been fabricated. Of these, two VCOs are presented in this thesis.

Through the investigation of these two VCOs the effectiveness of the low-frequency noise filter reported in [44], [53], and [54] is studied. In addition, the direct upconversion process of the flicker noise originating from the cross-coupled transistors

to the frequency of oscillation in the absence of the Groszkowski effects discussed in section 3.4.3 is demonstrated.

5.5.1 VCO Designs

The previous experimental 5GHz VCOs had an L/C ratio of around 1.1nH/830fF=1325H/F, which is considered relatively high. The VCOs in the second test chip had a much lower L/C ratio of 250pH/3.68pF=68H/F. Although the new VCOs with the lower L/C ratio oscillated well in simulations, they have failed to oscillate in measurements. Higher supply voltages and higher tail bias currents applied did not improve the situation.

It is thought that the parasitic resistance added to the tank circuit may have caused severe degradation in Q_{tank}. A small amount of parasitic resistance added in series with the inductor or the capacitor of a tank with a lower L/C ratio has a greater influence on the loaded Q than the same amount added to a tank with a higher L/C ratio. This is because the tank with a lower L/C ratio has relatively lower series resistance associated with the inductor and the capacitor. Unfortunately, the layout parasitic extraction tool offered by this process technology docs not support the extraction of the parasitic resistance. Therefore, the effects of the parasitic resistance in the VCOs were not fully taken into account in simulations.

The VCOs of the second test chip were carefully revised, and laid out again on the third test chip with a slightly increased L/C ratio of 396pH/2.32pF=171H/F. This is still about an order of magnitude lower than the 5GHz VCOs from the first test chip. Six

VCOs sharing the same tank configuration were fabricated. Of those, two low-noise 5GHz SOS CMOS VCOs are discussed in this section. They are referred to as VCO7 and VCO8 hereafter.

Fig. 5.19 shows the schematic diagram for VCO7 and VCO8. What distinguishes the two VCOs from each other is the absence or the presence of the parallel *LC* filter between the common-mode node (v_{CM}) and the drain of the tail transistor, first introduced by E. Hegazi in [44], [53]. This filter is referred to as the Hegazi's filter hereafter. VCO7 is the one without the Hegazi's filter while VCO8 incorporates the filter.
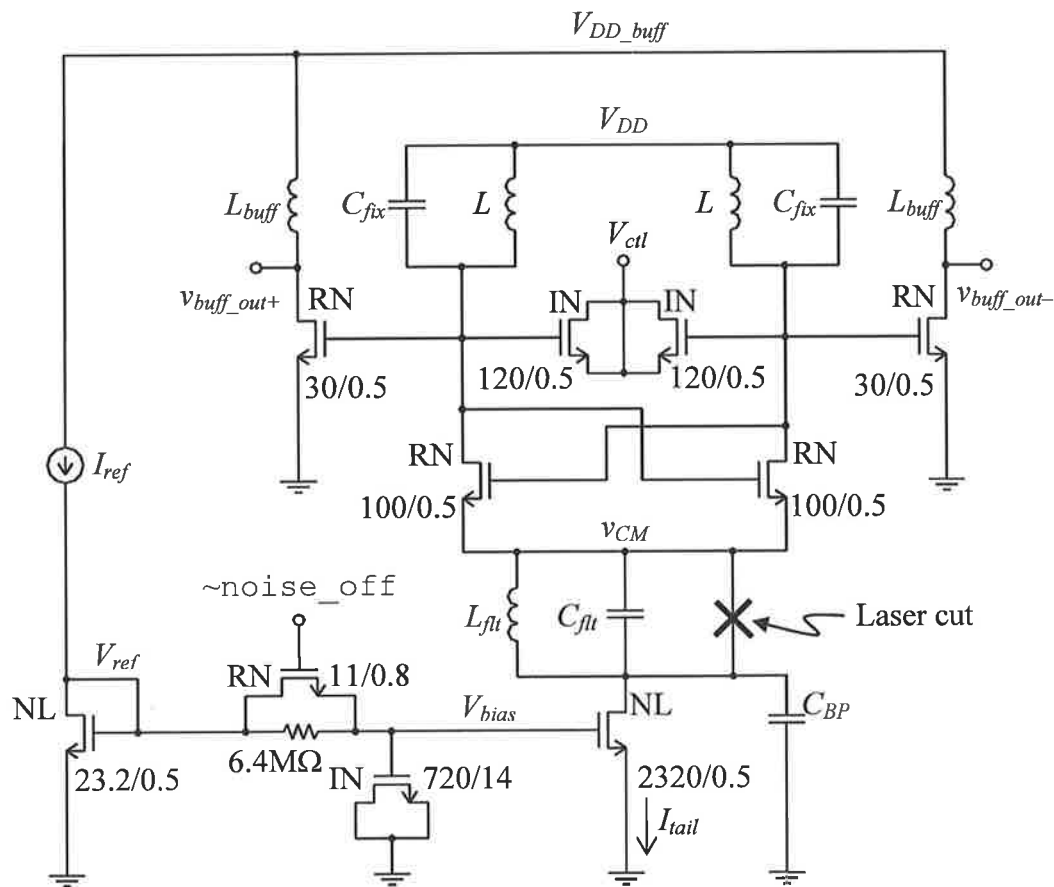
Fig. 5.19: Schematic diagram for VCO7 and VCO8.
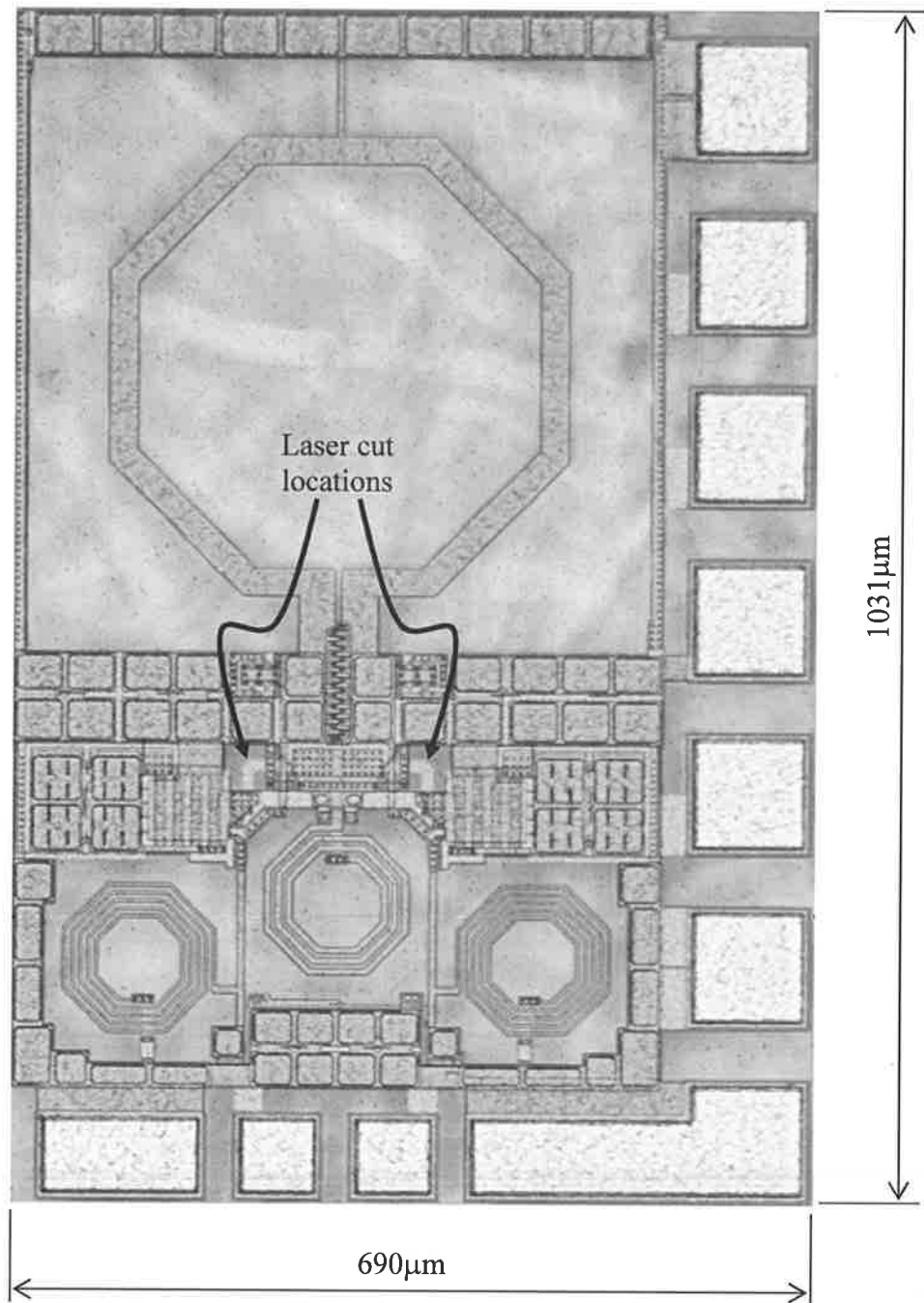
Fig. 5.20: Microphotograph of VCO7 and VCO8.

When the test chip was first fabricated, the Hegazi's filter was not operational

and the resulting VCO was VCO7. If the metal traces bypassing the Hegazi's filter were

cut with precision laser at two places as shown in Fig. 5.20, the parallel LC filter formed

with L_{flt} and C_{flt} becomes operational. This turns VCO7 into VCO8. This way, the same

layout can be used to produce two different VCOs, which conserved chip area.

Separate DC pads were placed for V_{DD} and V_{DD_buff}. V_{DD} feeds the VCO core,

whereas V_{DD_buff} feeds the pair of output buffer. This way, the current consumption of

the VCO core can be monitored separately from the current consumption of the output

buffer.

The output buffer pair is loaded with two on-chip spiral inductors of

approximately L_{buff}=3.3nH each. Simulated quality factor is around 17, and the self-

resonant frequency is at around 26GHz. Q is not critical for buffers, as long as f_{self} is

significantly higher than f_0.

5.5.2 Tank Design

Since the inductance required for VCO7 or VCO8 was much lower than the

inductance of the previous 5GHz VCOs, it was possible to implement a differential

inductor pair with a center-tapped single turn inductor without paying severe area

penalty.

A single turn octagonal inductor, center-tapped to V_{DD} employed here has outer

diameter of 397μm, and conductor width of 25μm. Only the top metal layer was used,

because multi layer inductor at 5GHz is not beneficial, which became evident in section

5.3 and section 5.4.

Inductance simulated with ASITIC was around 0.396nH per side and Q_L predicted was around 32, which was higher than the multi turn inductors used in the previous 5GHz VCOs. This fact supports the argument that lower inductance, lower number of turns, and larger diameter spiral inductor yields higher Q_L in a given process technology.

For the given sizes of L and f_0, the required capacitance per side was around 2.32pF. C_{fix} provided around 709fF, and the rest was provided by the parasitic capacitors and the MOS varactors. The frequency tuning range was to be around 150MHz. Although it was somewhat lower than the tuning range of VCO1 or VCO2, the varactors were made larger than before, because the required change in capacitance was larger than before owing to the lower L/C ratio of the new tank.

Calculated parallel equivalent tank resistance, R_{tank} for VCO7 and VCO8 was around 200Ω. The VCO bias space and the phase noise space for constant cross-coupled transistor gate width of 100μm are plotted in Fig. 5.21.
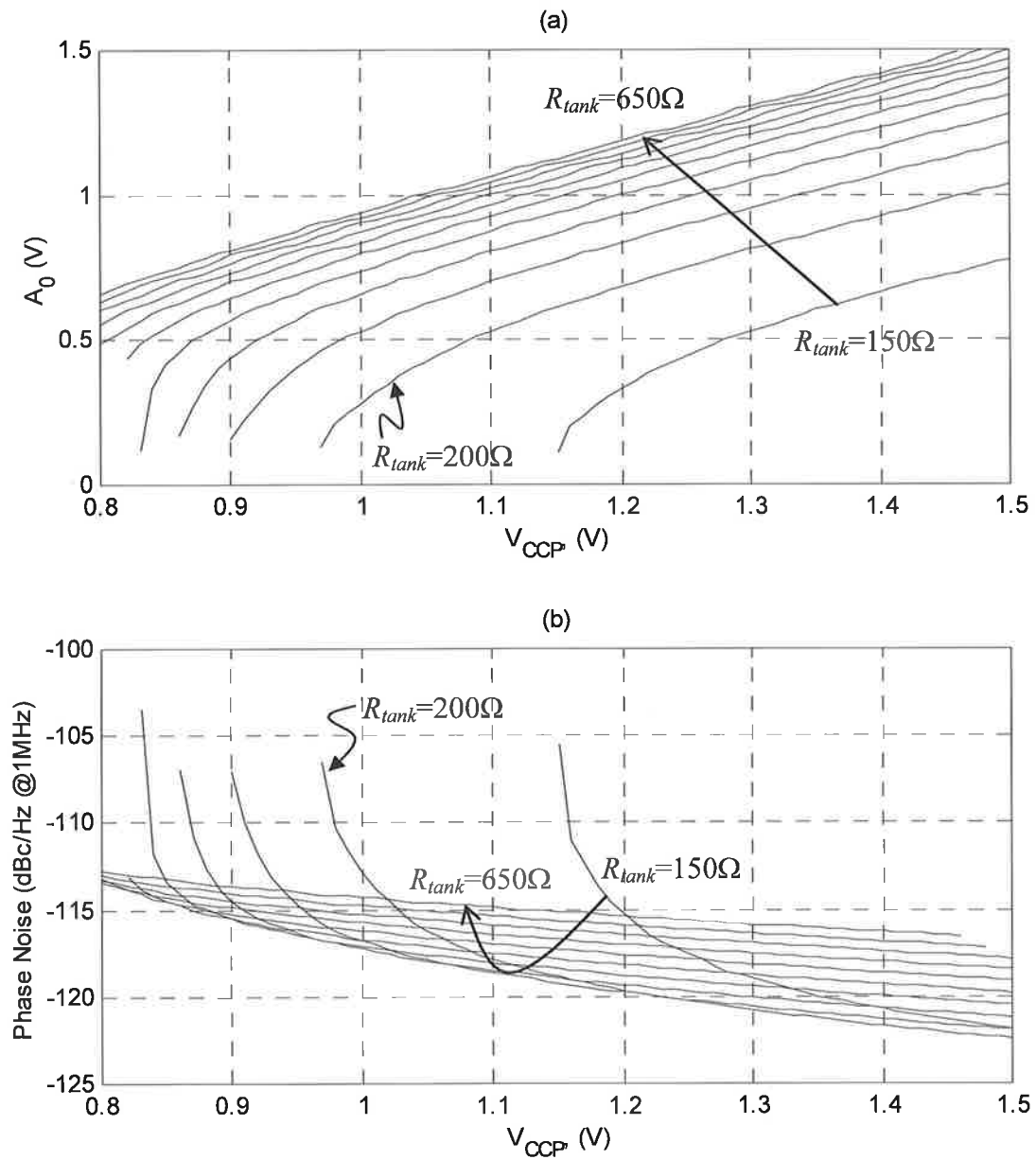
Fig. 5.21: (a) Bias space and (b) phase noise space of VCO7 and VCO8 for W_{CCP}=100µm.

5.5.3 Low Noise Measures

The filtering technique reported in [44] and [53], or the Hegazi's filter involves a parallel LC filter tuned at $2f_0$ that provides a high impedance path from the common-source node of the cross-coupled transistors to ground. Also, a bypass capacitor is placed between the drain of the tail transistor and ground to suppress noise current at $2f_0$.

This filter is claimed to reduce the upconversion of the flicker noise from the tail transistor and the cross-coupled transistors by limiting the two Groszkowski effects reported in [43] and discussed in section 3.4.2 and section 3.4.3. Since the flicker noise is the dominant source of the close-in phase noise in this process technology, a noticeable improvement in phase noise is expected when the filter is made operational. That is, if the filter is truly effective in limiting the flicker noise upconversion processes.

The Hegazi's LC filter was constructed using a three-turn spiral inductor located at the center of the layout shown in Fig. 5.20 and a capacitor consists of a MIM capacitor and parasitic capacitors from metal routings. The inductor has inductance of around 1.2nH and Q of approximately 22 at 10GHz. The required capacitance to tune the filter at $2f_0$ is around 200fF. Of this, 79.3fF was provided by the MIM capacitor and the rest was provided by the parasitic capacitors. Q of the MIM capacitor was only about 20 at 10GHz. The parasitic capacitor was expected to have Q of approximately 20 or below. Therefore, the resulting loaded Q of the filter would have been around 10. This implies a 3dB bandwidth of approximately ± 1GHz centered at 10GHz.

VCO7 and VCO8 have the flexibility to operate with or without the tail current bias circuit, because the drain of the tail transistor is connected to one of the DC pads.

By grounding this pad, the tail current bias circuit can be deactivated. If there is any difference in measured close-in phase noise with or without the tail transistor, it can be said that the close-in phase noise of the VCO is dominated by the flicker noise from the tail transistor and/or the diode-connected transistor. On the other hand, if there is no observable difference in measured close-in phase noise between the two operation modes, it can be concluded that the flicker noise contribution from the cross-coupled pair dominates over the flicker noise from the tail current bias transistors. It should be ensured that when the VCO is operating without the tail transistor, V_{DD} must be adjusted to set the appropriate bias current through the VCO core.

The low-power, low-noise current biasing technique proposed in section 4.6.2 was implemented in VCO7 and VCO8. For the required low-pass RC filter, a lightly doped n^+ resistor is used to provide high resistance of approximately 6.4MΩ and large gate area IN type inversion mode MOS capacitors were used to provide large capacitance of approximately 37pF. The −3dB cutoff frequency of the RC filter is at around 672Hz.

This filter allowed for high current mirror ratio between the diode-connected reference current generating transistor and the tail transistor. The current mirror ratio used in the two VCOs is 1:100. Any noise component above 672Hz originating from the diode-connected transistor is attenuated at a rate of −20dB/decade. A bypass switch was added in parallel with the resistor to bypass the RC filter by asserting the input signal ~noise_off high. This way, the effectiveness of the filter can be observed by toggling the switch on and off. That is, if the flicker noise from the diode-connected transistor is the dominant source of the close-in phase noise.

5.5.4 Results

The measurement setup is quite similar to the one used for the previous experimental 5GHz VCOs. The only difference is that this setup did not involve any bias-T, because the VCOs under test have on-chip buffers with integrated inductive loads. The new measurement setup for VCO7 and VCO8 is shown in Fig. 5.22.

In simulations, the VCOs oscillated with I_{tail} as low as 3mA. It should be noted that although the simulations were run with the extracted netlist from the layout, the lack of parasitic resistance extraction made the simulation results seem more optimistic than the measured results.
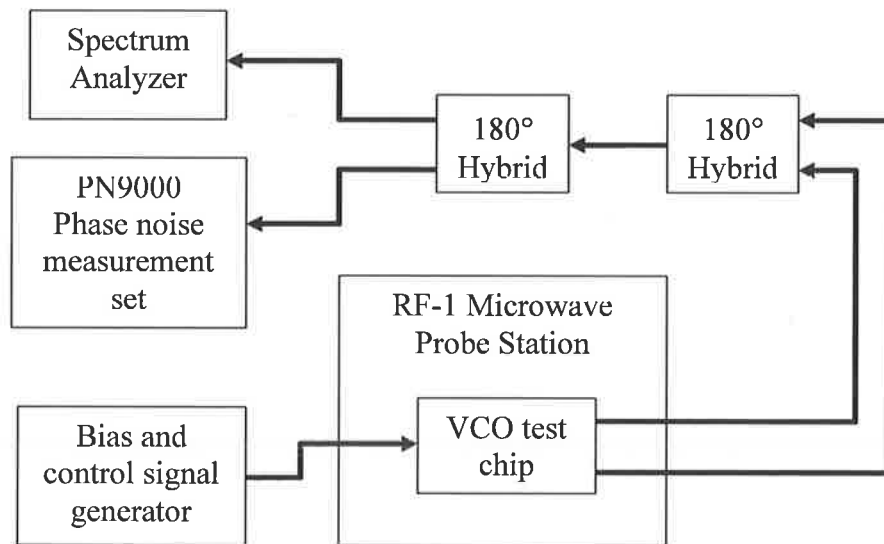
Fig. 5.22: Phase noise measurement setup for VCO7 and VCO8.

In measurements, both VCOs started to oscillate with minimum I_{tail} of around 7mA. With V_{DD} of 1.5V, I_{tail} was able to be increased up to 12mA. Further increase in

I_{tail} was difficult to achieve for constant V_{DD} of 1.5V, because V_{DS} of the tail transistor was approaching 0V and V_{CCP} was approaching its limit, V_{DD}.

Frequency tuning curves of VCO7 are plotted in Fig. 5.23(a). These curves are quite similar for VCO8 as well, because the two VCOs share the same tank configuration and the existence of the Hegazi's filter for VCO8 does not affect the frequency tuning characteristic.

The measured frequencies of oscillation are somewhat higher than expected. It is thought that the difference is caused by the difference between the actual parasitic capacitance and the extracted capacitance in simulations. Parasitic capacitance constitutes the bulk of the tank capacitance, yet its variation over process is not well controlled nor documented. This is typical in most CMOS processes and adds to the difficulty of getting the right frequency of oscillation from the design phase.
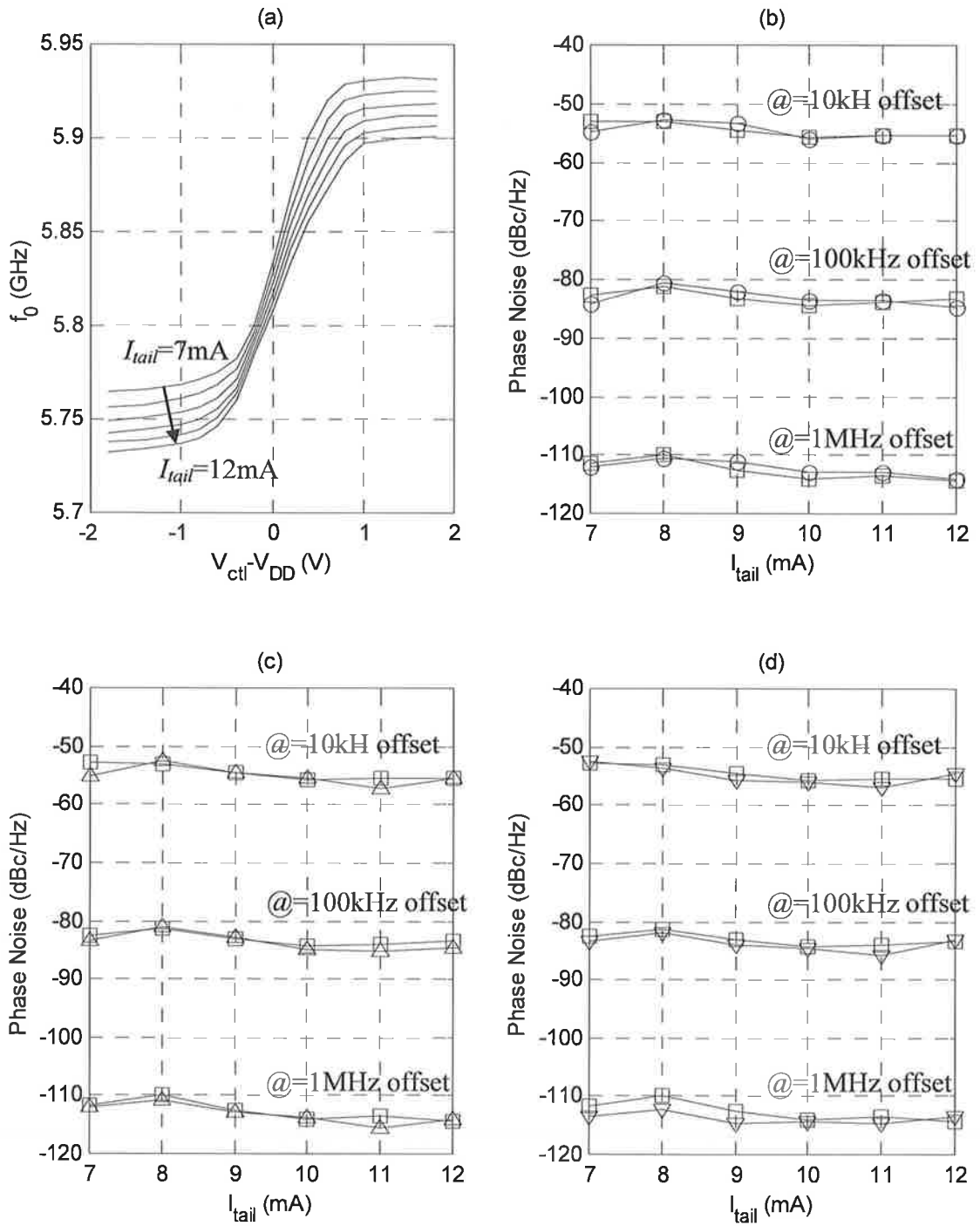
Fig. 5.23: (a) Frequency tuning curves for VCO7, (b) phase noise plots comparing ~noise_off=0 (□) and ~noise_off=1 (O), (c) phase noise plots comparing ~noise_off=0 (□) and no tail transistor (△), and (d) phase noise plots comparing ~noise_off=0 (□) and Hegazi's filter activated (▽).

From the phase noise plots shown in Fig. 5.23(b) and Fig. 5.23(c), it can be concluded that the close-in phase noise of VCO7 or VCO8 is dominated by the flicker noise from the cross-coupled transistors. Because firstly, the phase noise difference between 100kHz offset and 1MHz offset is around 30dB for all phase noise plots, indicating flicker noise dominated phase noise at least up to 1MHz offset. Secondly, the phase noise difference is negligible when the ~noise_off signal is toggled as it can be seen from Fig. 5.23(b). This implies the diode-connected reference current generating transistor's flicker noise is not the dominating source of the close-in phase noise. Lastly, from Fig. 5.23(c), it is observed that the absence of the tail transistor did not cause any notable improvement in the close-in phase noise. This means the tail transistor is not the dominant source of the close-in phase noise either. Therefore, as the only significant sources of the flicker noise left in the circuit are the cross-coupled transistors, it can be concluded that they are the dominant sources of the upconverted flicker noise.

This also proves the fact that the flicker noise from the cross-coupled pair does indeed directly upconvert to the frequency of oscillation as asserted in section 3.4.3. The two flicker noise upconversion mechanisms proposed in [43] with the two Groszkowski effects cannot explain the appearance of the flicker noise induced phase noise when the common-source node of the cross-coupled pair is grounded.

It should be noted that with the previous experimental 5GHz VCOs, the close-in phase noise was dominated by the flicker noise from the tail transistor rather than the cross-coupled pair. It is thought that the reason for increased flicker noise contribution from the cross-coupled transistors for VCO7 or VCO8 is attributed to the fact that the difference between the amplitude of oscillation, A_0 and the cross-coupled pair bias

voltage, V_{CCP} is larger than that of the previous 5GHz VCOs. As it can be seen from Fig. 5.12(a), $V_{CCP}-A_0$ for the previous experimental 5GHz VCOs is around 0.2V, whereas $V_{CCP}-A_0$ for VCO7 or VCO8 is around 0.5V as shown in Fig. 5.21. This means the channels of the cross-coupled transistors in VCO7 or VCO8 are not as fully depleted as those in the previous 5GHz VCOs when cycled between depletion and inversion by the oscillator output swing. The flicker noise reduction by switched biasing becomes less effective as the channel depletion occurs to a lesser extent [82]. This is the reason for the increased flicker noise contribution from the cross-coupled transistors in VCO7 or VCO8.

In Fig. 5.23(d), the presence of the Hegazi's filter made a very small improvement in the phase noise at 1MHz offset near the low end of I_{tail}. However, it is not a sufficient evidence to conclude that the Hegazi's filter actually reduced the flicker noise upconversion. Because the two Groszkowski effects that the Hegazi's filter is designed to suppress are not the dominant flicker noise upconversion processes in these VCOs. The Hegazi's filter at its best can only produce the phase noise equivalent to the phase noise in the absence of the tail transistor or when the common-source node of the cross-coupled pair is directly grounded. However, the experiments with VCO7 with and without the tail transistor showed no notable difference in the phase noise. In other words, the two Groszkowski effects are not the dominant flicker noise upconversion processes in these VCOs. Instead, the direct mixing action of the flicker noise from the cross-coupled pair and the oscillation signal discussed in section 3.4.3 seems to be the dominant low frequency noise upconversion process for these VCOs.

A VCO with smaller V_{CCP}–A_0, such as VCO2, where the flicker noise from the cross-coupled pair is much suppressed may benefit from the Hegazi's filter, if the two Groszkowski effects are the dominant flicker noise upconversion processes.

Unfortunately, it is not possible to determine whether the Groszkowski effects are the dominant flicker noise upconversion processes or not for the previous 5GHz VCOs, because these VCOs do not have the Hegazi's filter with which to experiment. Therefore, the effectiveness of the Hegazi's filter to suppress the two Groszkowski effects could not be validated from the series of experiments conducted in this work. Nevertheless, it is clear that the two Groszkowski effects are not the dominant low frequency noise upconversion processes at least in VCO7 and VCO8.

When stating the phase noise of a VCO, it is important to state the worst measurement recorded across the full tuning range. The worst phase noise measurement is usually recorded when the VCO constant K_V is maximum, because the strong gain of the varactor maximizes the upconversion gain of all low frequency noise. All phase noise measurements plotted in Fig. 5.23 are taken when the varactor control voltage is set to V_{DD} where the VCO gain, K_V is maximum. Hence these represent the worse case phase noise values.

The phase noise prediction by the simple LTI model shown in Fig. 5.21 expects phase noise of –118dBc/Hz and –122dBc/Hz at 1MHz offset for I_{tail} of 7mA and 12mA respectively. However, measurements only show around –111dBc/Hz and –115dBc/Hz at 1MHz offset for I_{tail} of 7mA and 12mA respectively. The excessive flicker noise contribution, especially from the cross-coupled transistors is thought to be responsible for the discrepancy between the phase noise calculated and measured. The phase noise at 1MHz offset is still under influence of the upconverted flicker noise, whereas the

simple LTI model used to calculate the phase noise has no knowledge of the upconversion of the flicker noise. Therefore the estimation by the LTI model is more optimistic than the measurement results.

Unlike the previous 5GHz VCOs, the new 5GHz VCOs exhibit decreasing phase noise with increasing I_{tail}. This is normal in most VCOs. The reason for the increased phase noise with I_{tail} in the previous VCOs is due to the unusual rapid growth of the flicker noise contribution from the tail current bias transistors.

After all, the noise characteristics of the SOS devices are not well understood. The adaptation of the bulk transistor noise models for these devices may not be appropriate for these SOS devices, especially the low frequency flicker noise model [111].

Despite the excessive flicker noise contribution from the cross-coupled pair, the new 5GHz VCOs are able to trade power for improved phase noise performance. Because the flicker noise seems to improve linearly with I_{tail} in the new VCOs. Further improvement in close-in phase noise is expected if wider cross-coupled transistors are used to reduce the difference between V_{CCP} and A_0, which can fully cycle the transistor channels between inversion and depletion and lower the flicker noise.

5.6 CONCLUSIONS

Total of eight VCOs implemented with the 0.5μm SOS CMOS process were presented in this chapter. The first four and the last two VCOs were designed to operate at 5GHz, while VCO5 and VCO7 were designed operate at 17GHz.

VCO1 and VCO2 showed very similar phase noise performance. Although these VCOs do not have the lowest phase noise reported, they showed the lowest power consumption compared to other fully monolithic 5GHz CMOS VCOs reported to the date of publication of VCO2. Also, the FOM calculated is one of the best reported in the literature. This makes these SOS VCOs ideal for applications where low-power operation is the utmost importance, such as battery cell powered handheld wireless mobile devices.

VCO3 successfully demonstrated the feasibility of the switched capacitor bank as an alternative for a wide frequency-tuning scheme. However, some degradation in phase noise was observed due to the degradation in Q_{tank} by the lossy switches.

The complementary topology realized with VCO4 did not prove itself to be superior over the NMOS-only topology. In fact, its design is more complicated than the NMOS-only topology because of the gain mismatch problem between the complementary cross-coupled pairs. This makes it difficult to maintain the bias potential of the output waveform at a desired level in practice. Also, the floating mean potential of the output encourages the CMM-to-AM flicker noise upconversion process.

VCO5 and VCO6 were implemented to examine the influence of the multi layer inductors on the VCO performance and the feasibility of 17GHz oscillation with the SOS process technology under investigation.

Multi layer, or unnecessarily thick single layer inductors are not beneficial at high frequencies, where the total thickness of the inductor structure is larger than few skin depths thick. This is because there exists an optimal conductor thickness at a given frequency of operation. Conductor thickness exceeding the optimal thickness works against and reduces the quality factor and inductance.

The 17GHz oscillators compared poorly against other 17GHz bulk CMOS VCO found in the literature. Nevertheless, the fact that these VCOs oscillated at frequencies well above the f_T of the process is interesting in its own right.

A phase noise improvement scheme to work at 17GHz has been proposed. This scheme also solves the limited tuning range problem of high frequency oscillators and eliminates the need for the high frequency prescalers.

VCO7 and VCO8 operating at 5GHz with a lower L/C ratio were fabricated on the third test chip. These two VCOs only differ from each other by the presence of the Hegazi's filter. By investigating these VCOs, it has been proved that the flicker noise from the cross-coupled pair does in fact directly upconvert to f_0 in the absence of the two Groszkowski effects.

The best phase noise achieved with the new low-noise 5GHz SOS CMOS VCOs, namely VCO7 and VCO8 is –115dBc/Hz at 1MHz offset, while consuming 12mA from a 1.5V supply. Usual FOM comparison against other VCOs from the literature is not appropriate for these two VCOs, because the close-in phase noise is only measured up to 1MHz offset for these VCOs, and at this offset, the phase noise was still dominated by the flicker noise.

The best phase noise performance was obtained from the NMOS-only topology with relatively low L/C ratio. Which were the characteristics of VCO7 and VCO8.

Measured frequencies of oscillations were more or less consistently higher than simulation. This may be partly due to process variation and/or that the parasitic extraction rules used in simulations may have over predicted parasitic capacitances.

In general, the 0.5μm SOS CMOS process investigated is quite adequate for 5GHz oscillators. The insulating sapphire substrate offers excellent environment for

high Q spiral inductor construction. Wide frequency tuning range is achievable with the switched capacitor technique to combat the wide process spread typical in CMOS processes. Phase noise performance compared quite well against other VCOs reported in the literature.

One major down side of the process technology however is that the transistors are noisy at low frequencies. The flicker noise performance is much worse than that of the bulk silicon process with the same feature size. The transistors use the same noise models as those used for the bulk devices in simulations. However, that may not be adequate for the SOS devices, especially at higher current densities as asserted in [111].

The phase noise estimation by the simple LTI model showed poor accuracy for the VCOs fabricated in this technology. This is because the measured close-in phase noise of the VCOs was dominated by the flicker noise in most cases. The phase noise estimation by the simple LTI mode is expected to be more accurate and useful in a process technology exhibiting lower flicker noise, such as the 0.18µm bulk CMOS process investigated in the following chapter.

Chapter 6

HIGH PERFORMANCE BULK CMOS VCOS

6.1 INTRODUCTION

Two 5GHz VCOs fabricated using a 0.18μm bulk CMOS process are presented in this chapter. The first VCO is an experimental prototype of the second VCO. The second VCO is designed as a part of the dual-band 2.4GHz/5GHz radio front-end chipset developed by Wireless Networking Business Unit (WNBU) of Cisco Systems. The first and the second VCOs presented in this chapter are referred to as VCO9 and VCO10 hereafter.

The process technology used for these VCOs is the TSMC's 0.18μm mixed-mode bulk silicon CMOS process. Section 6.2 briefly introduces the main features of this process technology.

VCO9 and VCO10 are presented in section 6.3 and section 6.4 respectively. Since VCO10 is designed based on a set of product level specifications, it is designed by following the high performance VCO design methodology developed in Chapter 4.

Section 6.5 compares the performance of VCO9 and VCO10 against other state-of-the-art 5GHz CMOS VCOs reported in the literature. And section 6.5 concludes the chapter.

6.2 0.18μm BULK CMOS PROCESS

The TSMC's 0.18μm mixed-mode bulk silicon CMOS process is one of the mainstream high-density digital CMOS processes that provide optional analog features to support high performance RF operations. The following brief descriptions of the process technology under investigation are from a set of manuals published by TSMC, unless otherwise stated [106].

A standard 0.18μm logic process offers single polysilicon layer and 6 aluminum metal layers. Each metal layer other than the top metal layer is approximately 0.5μm thick, and the top metal layer is 1μm thick. The mixed-mode process offers 2μm thick top metal for high quality spiral inductor implementation at no extra mask cost.

The substrate used in a logic process is usually an epitaxial substrate, which has a thin layer of lowly doped epitaxial material grown on top of a heavily doped bulk substrate. NMOS devices are implemented on the epitaxial layer and PMOS devices are implemented within n-wells. As mentioned in section 4.3.2, epitaxial substrate is not optimal for monolithic implementation of high performance spiral inductors due to excessive ohmic loss in the substrate.

The mixed-mode process offers a lightly doped non-epitaxial substrate as an alternative. The non-epitaxial silicon substrate has its resistivity in the order of few tens

of Ωcm. Although it is not as good as the insulating substrate of the SOS process discussed the previous chapter, spiral inductors with sufficiently high Q can be realized with the non-epitaxial substrate.

The process supports two different supply voltages. Transistors designed to operate with 1.8V supply voltage have a minimum gate length of 0.18µm, and transistors designed to operate with 3.3V supply voltage have a minimum gate length of 0.35µm. Due to the thicker gate oxide used in 3.3V devices, they have a slightly higher threshold voltage in the case of NMOS devices. Sine the 1.8V devices have smaller feature size and higher gain density, only the 1.8V devices are used in the VCO designs.

In addition to the normal threshold voltage devices, optional lower threshold voltage devices, similar to the NL and IN devices of the SOS process are also available at the expense of extra masks and processing steps. Since there is no advantage in using lower threshold devices in a VCO design, only the standard normal threshold voltage devices are used. The target threshold voltage, V_{TH} of a 1.8V standard NMOS device is 0.42V and for a standard PMOS device, it is –0.50V in this process.

The unity gain frequency of the 1.8V standard NMOS device exceeds 55GHz. Faster transistors means smaller parasitic capacitances associated with the device. This is preferred in high performance VCO implementation, because lower parasitic gate capacitance means the frequency of oscillation is less affected by the variable, low Q parasitic gate capacitance of the cross-coupled pair. Also, it leaves more room for varactors or switched capacitors in the tank to achieve a wider frequency tuning range.

The mixed-mode process also offers optional high quality MIM capacitors for an extra mask and processing step. A MIM capacitor in this process is formed by metal-5 and capacitor-top-metal (CTM) layer separated by 35nm thin oxide dielectric layer. The

CTM layer is then connected to the top metal through vias. Q is as high as 320 at 1GHz. A simple linear extrapolation predicts MIM capacitor Q of approximately 64 at 5GHz. This is a quite plausible approximation as both metal-5 and CTM layers are thinner than the skin depth of aluminum at 5GHz. In other words, conductance degradation due to the high frequency effects can be considered insignificant at 5GHz and the simple linear extrapolation of capacitor Q is considered a valid approximation.

6.3 LOW-NOISE 5GHZ VCO

At the time of the design of VCO9, it was unclear whether the on-chip implementation of a 5GHz VCO could produce phase noise low enough for high performance 5GHz radio front-end operation, when implemented with the mixed-mode 0.18µm bulk CMOS process. The sole purpose of VCO9 is to find out the best phase noise achievable for the given process technology at 5GHz.

The frequency-tuning scheme for VCO9 uses both continuous MOS varactor tuning and discrete switched capacitor tuning. However, because a wide frequency tuning range compromises the phase noise performance, only a narrow frequency tuning range of approximately 200MHz is implemented just to test the functionality of the switched capacitors under the given process technology.

The high performance VCO design guidelines presented in section 4.5.3 are suitable for designing of a VCO with a complete, and real, set of specifications for the final product level quality. However, VCO9 did not have restrictive specifications such as power consumption, tuning range, temperature variation, or process variation.

Therefore, the design of VCO9 did not follow the guidelines strictly. Instead, it used the basic ideas behind the guideline for a low-noise implementation.

6.3.1 Inductor Design

This section starts with the design of a high Q inductor was designed. Unlike the inductors in the SOS process, Q_L in a bulk silicon process can be severely limited by the high frequency substrate effects discussed in section 4.3.2. As a consequence, monolithic spiral inductors implemented in a bulk process often have poor Q_L.

Nonetheless, the inductor optimization guidelines developed in section 4.3.3, and the experimental results obtained in the previous chapter indicated that low N, large D_{out} and wider w would yield higher Q_L. More specifically, a single turn inductor with a large outer diameter and a wide metal width would result in high Q_L.

The self-resonant frequencies are much lower in a bulk process, because of capacitive coupling to the ground through the conductive substrate. Therefore, it is important to use only the top metal for the greatest separation from the substrate. Besides, utilizing additional lower metal layers does not necessarily guarantee better conductivity at 5GHz as indicated in the previous chapter.

As a first step, a similar octagonal ring geometry used in VCO7 and VCO9 was chosen with D_{out} of 400μm. The resulting inductor structure consumed approximately half the chip area allocated for VCO9. Inductance per side, and quality factor were simulated in ASITIC and are plotted in Fig. 6.1, while sweeping conductor width, w from 20μm to 90μm.

The simulated self-resonant frequency was in the vicinity of 22GHz, and it did not vary much with increasing w. This is because, as w is increased, the inductance is decreased and the parasitic capacitance to the substrate is also increased at around the same rate, resulting in approximately constant f_{self}.

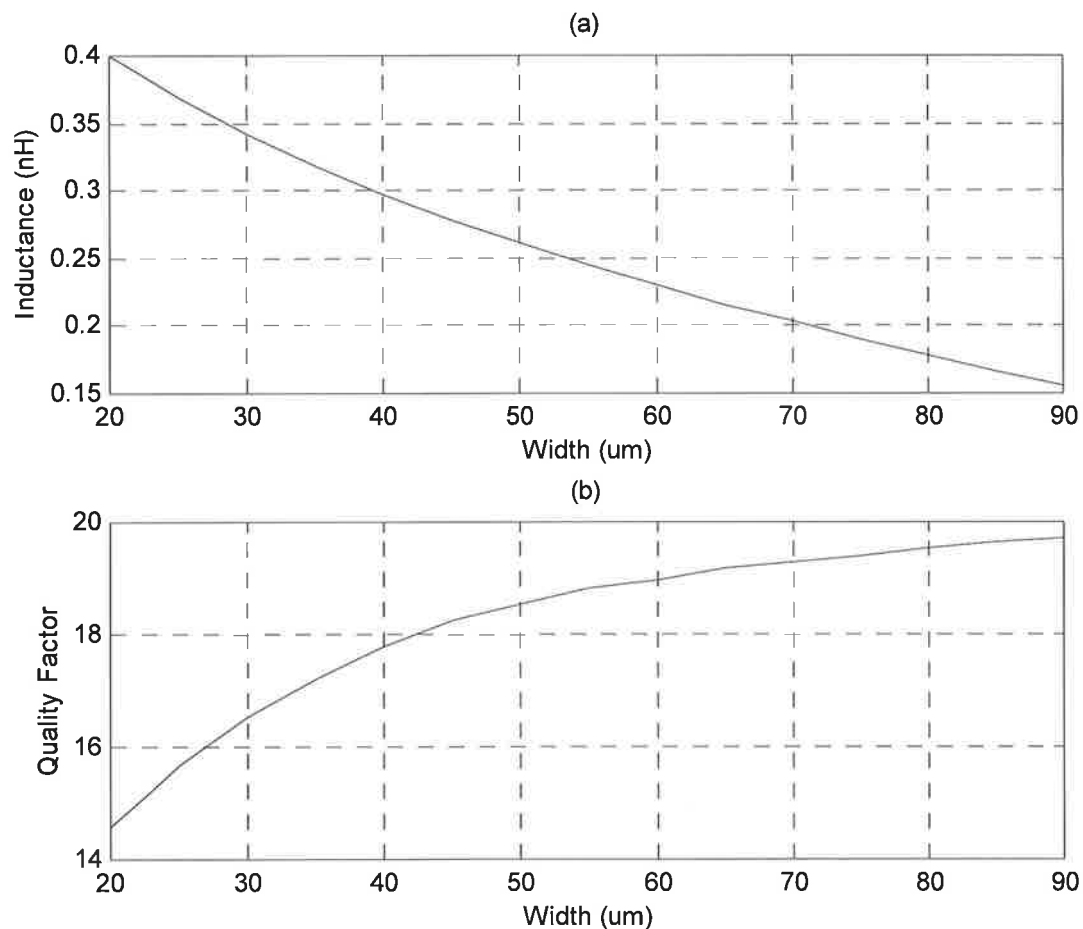Fig. 6.1: Simulated (a) inductance and (b) quality factor of a single turn octagonal inductor with constant D_{out} of 400μm, while varying w.

Q_L increases with w, but its rate of increase slows down as the hollow inductor advantage diminishes with increasing w. At w=65μm, resulting L and Q_L are 0.216nH and 19 respectively. Choosing wider w would result in a very small gain in Q_L, for much

reduced L. 0.215nH is significantly larger than any potential parasitic inductance of metal routings in the tank, yet small enough to yield a low L/C ratio. Therefore, for a given D_{out} of 400μm, conductor width of 65μm is chosen for L=0.215nH and Q_L=19.

The Q_L achieved is higher than any 5GHz on-chip planar spiral inductors reported in the literature. PGS may slightly improve Q_L by shielding out the substrate from the electric field. However, the extra parasitic capacitance introduced by the PGS becomes a part of the tank circuit and affects Q of the tank. Due to the high resistivity of the polysilicon PGS, Q of the parasitic capacitance is expected to be far worse than that of the MIM capacitors. Since the influence of the PGS on the loaded Q of the tank was not experimentally tested for the current process technology, its use was precluded.

6.3.2 VCO Design

The schematic for VCO9 is shown in Fig. 6.2. In addition to the schematic shown below, a 3-bit switched capacitor bank, very similar to the one shown in Fig. 5.2 was implemented with C_0 of 80fF and the switch transistor width of 40μm.

All transistors used in VCO9 are 1.8V standard NMOS transistors with minimum gate length. The output buffer is implemented with inductively loaded common-source differential amplifier to drive external 50Ω load per side.

The continuous frequency tuning range provided by the MOS varactors is around 20MHz. The switched capacitor bank is designed to cover approximately 200MHz, starting from 5.0GHz to 5.2GHz. Because the switched capacitor bank is only 3-bits wide, the entire tuning range is not continuously covered by the varactors.

The tank is designed and laid out to minimize parasitic capacitances, while maximizing C_{fix} portion of the total capacitance in the tank to inherit the high Q of the MIM capacitors. Approximately 81% of the total tank capacitance is provided by C_{fix}, which is 3.8pF in size. The sum of all parasitic capacitances is approximately 0.42fF per side. The resulting Q_C calculated is around 60, which is close to that of a pure MIM capacitor at 5GHz.
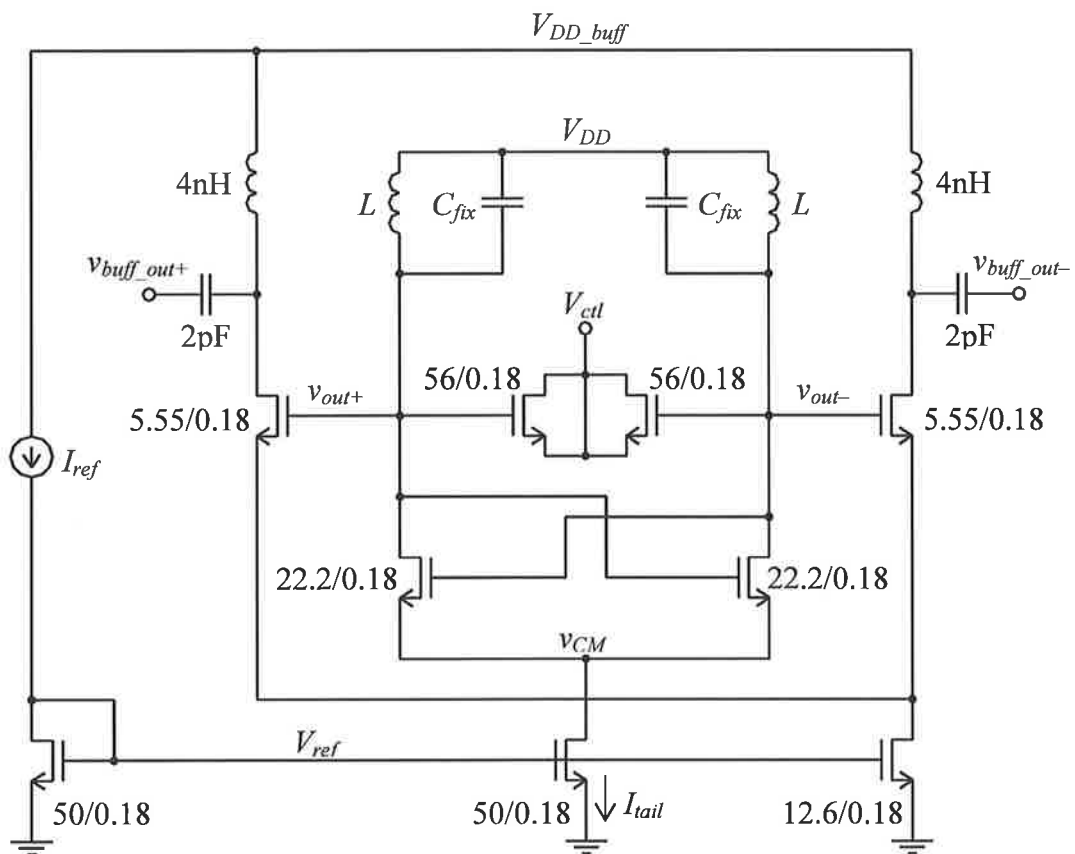
Fig. 6.2: VCO9 schematic diagram.
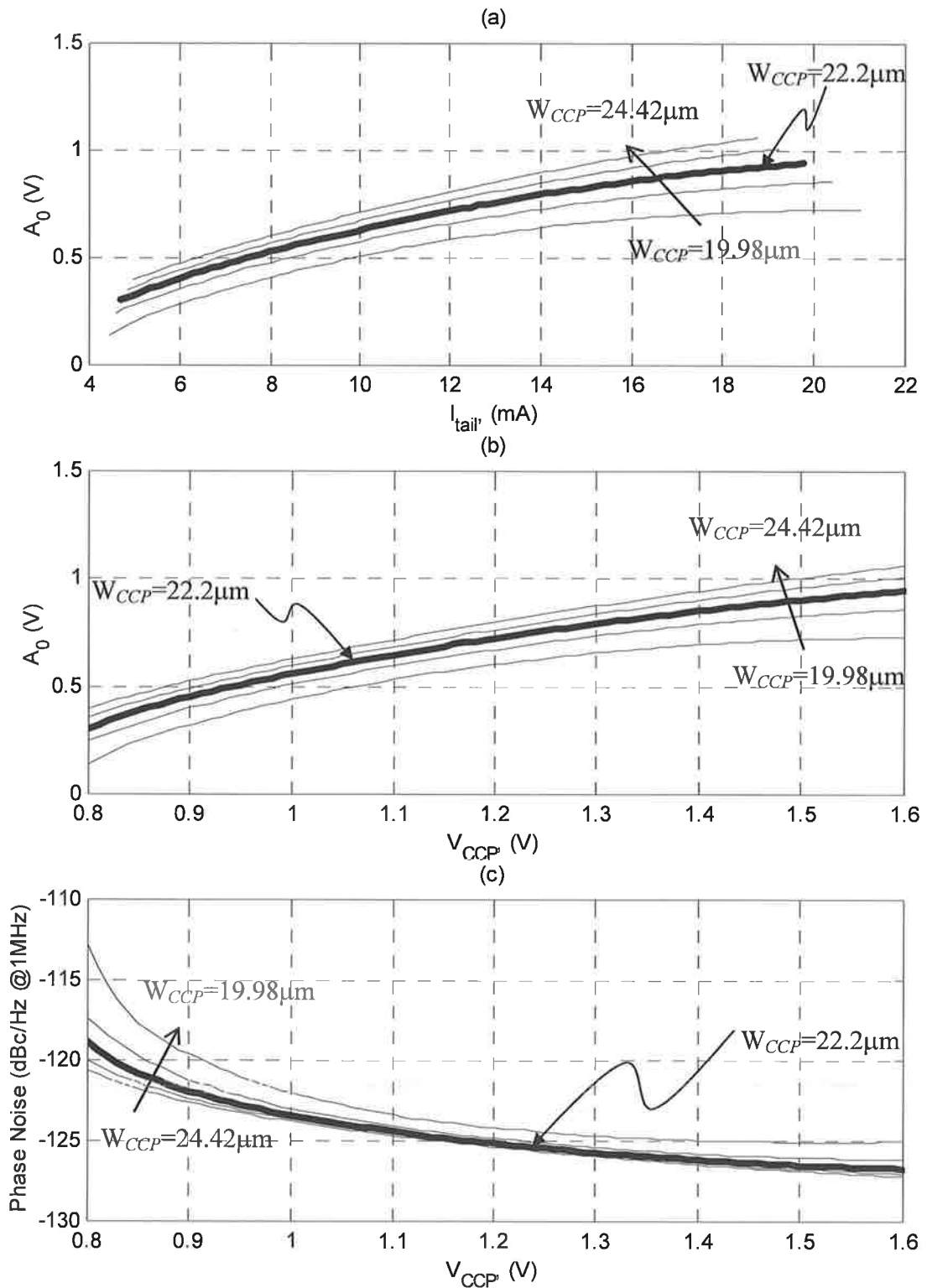
Fig. 6.3: Bias spaces of (a) A_0 versus I_{tail}, (b) A_0 versus V_{CCP}, and (c) phase noise space for constant R_{tank} of 100Ω, while varying W_{CCP} from 19.98μm to 24.42μm.

Based on the Q_L and Q_C found, the loaded Q of the tank, Q_{tank} is calculated to be 14. Using (5.1) or (5.2), the equivalent parallel resistance of the tank at resonance or R_{tank} is calculated to be around 100Ω. From R_{tank} calculated, three operating spaces shown in Fig. 6.3 are plotted. The cross-coupled pair transistors are then sized by choosing the desired operating points from the operating spaces.

The advantage of using wider transistors for the cross-coupled pair does not seem to be of much benefit for low phase noise operation as the cross-coupled pair bias voltage, V_{CCP}, is increased beyond 1.0V. Since unnecessarily a large cross-coupled pair only increases the low quality transistor parasitic capacitance contribution towards the tank capacitance, the transistor width is limited to 22.2μm. The bold lines in Fig. 6.3 correspond to operating the VCO with the cross-coupled pair transistor width, W_{CCP} of 22.2μm.

6.3.3 Results

The microphotograph of VCO9 fabricated is shown below. The VCO consumes around 0.704mm^2 of the chip area, including the pads.
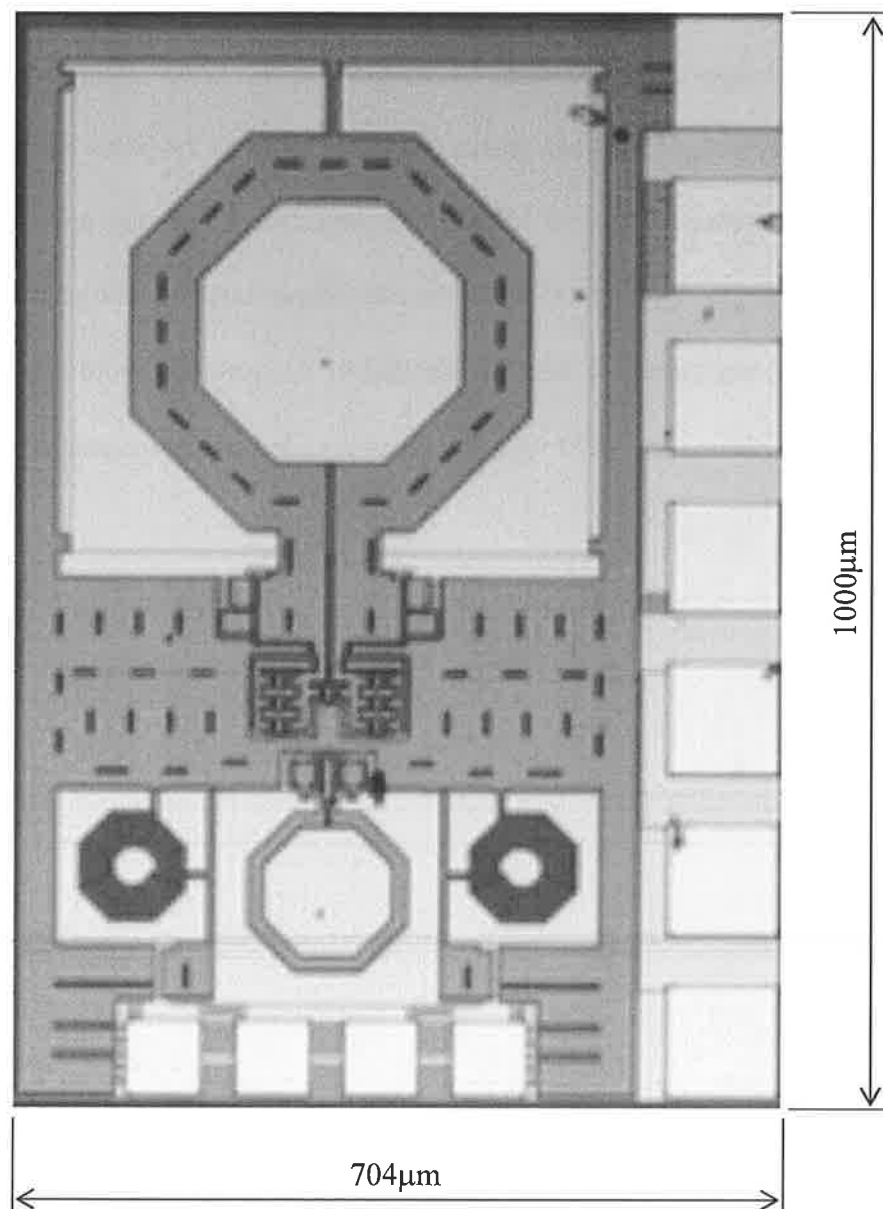
Fig. 6.4: Low-Noise 5GHz bulk CMOS VCO microphotograph.

The same measurement setup used for VCO7 and VCO8 as shown in Fig. 5.22 is used again to test VCO9. Fig 6.5(a) shows the simulation and the measurement results of the oscillation amplitude, while Fig. 6.5(b) shows the LTI model estimation and the measurement results of the phase noise.
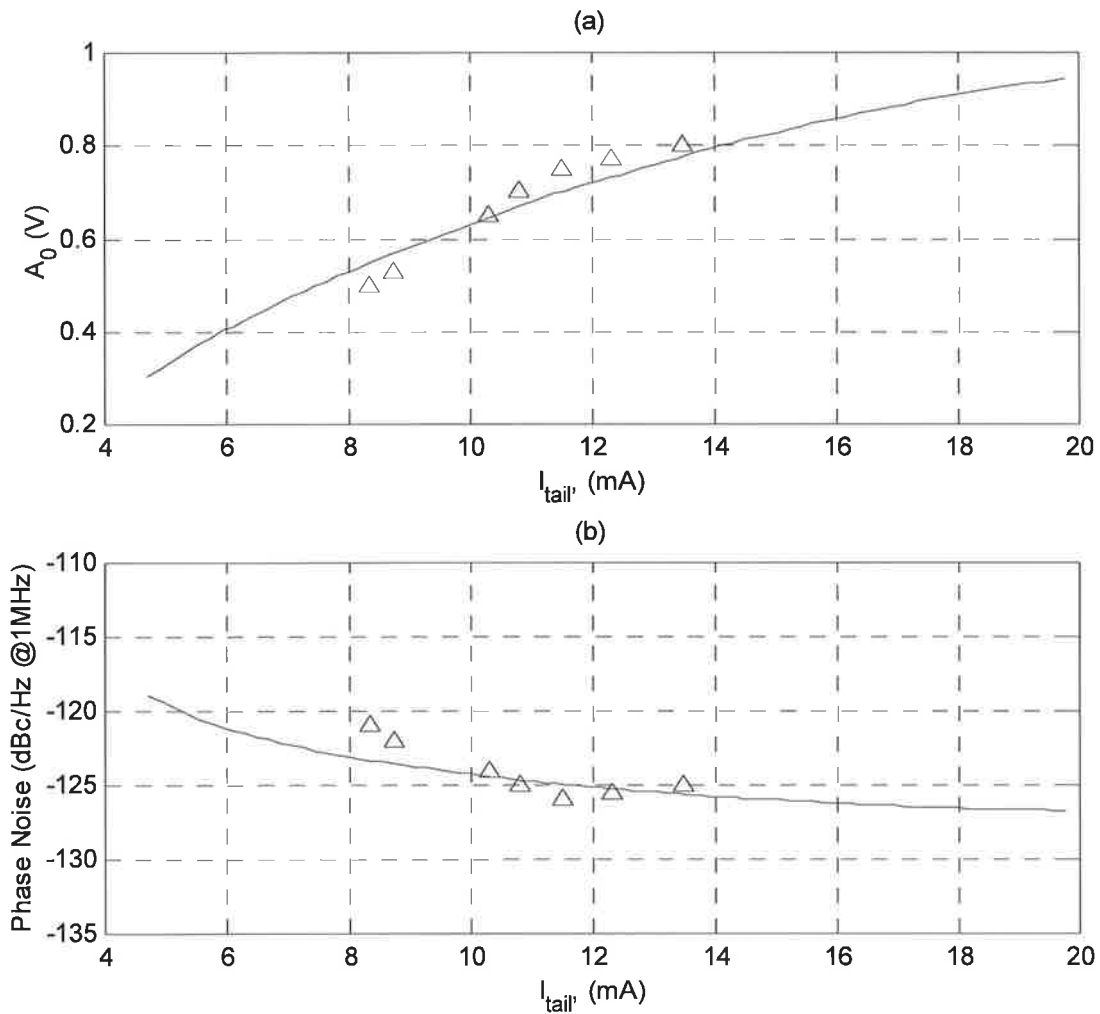
Fig. 6.5: VCO9 simulation (–) and measurement (△) results of (a) oscillation amplitude and (b) phase noise with respect to tail bias current.

In measurement, the oscillation amplitude is indirectly measured by observing the effective range of V_{ctl}, which is equal to $2A_0$. There is a close agreement between the simulated and the measured values of A_0.

The measured phase noise is also in close agreement with the phase noise estimation by the simple LTI model. Unlike the SOS VCOs in Chapter 5, the phase noise of VCO9 is not dominated by the flicker noise at 1MHz offset as can be seen from Fig. 6.6. This is why the simple LTI model is in close agreement with the measured phase noise of VCO9.
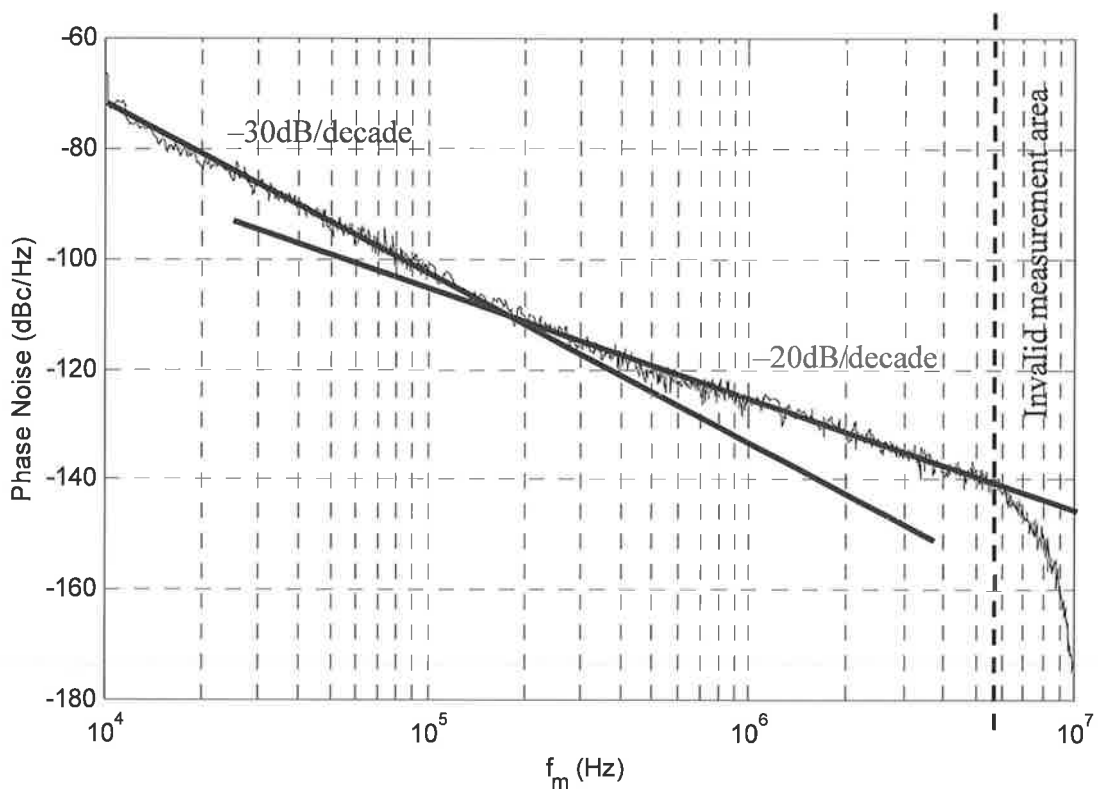
Fig. 6.6: Spectral plot of VCO9 phase noise, when V_{DD}=1.5V and I_{tail}=11.5mA.

Fig. 6.7 shows the measured frequency tuning curves of VCO9. The curves are shifted up by about 150MHz when compared to simulation results. The process spread

is thought to have caused the offset. Although there are frequency gaps that are not completely covered by the continuous MOS varactor tuning, it is sufficient enough to conclude that the discrete frequency-tuning scheme is working as expected in this technology.
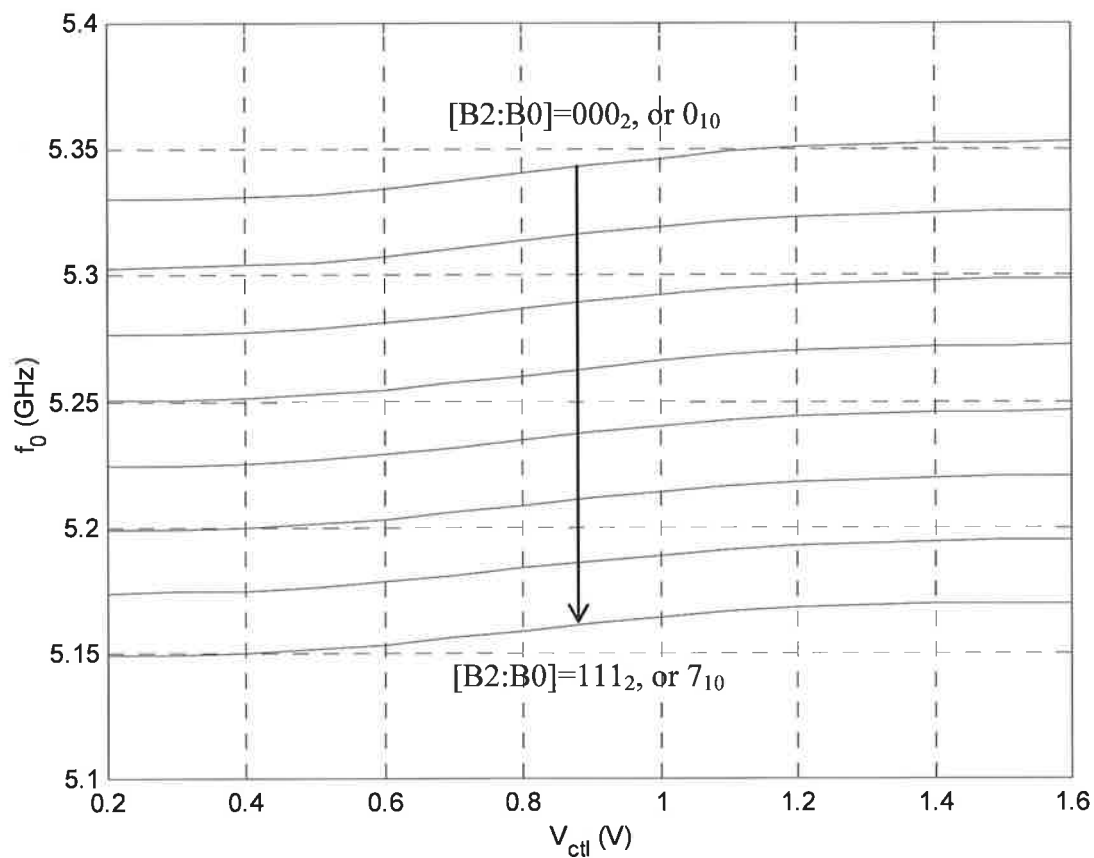
Fig. 6.7: Measured frequency-tuning curves of VCO9.

The phase noise measurements showed no notable variation across the entire tuning range. This is because the tuning range is so small that Q_{tank} stays constant with respect to the switched capacitor bank input and the varactor control input.

The phase noise performance of VCO9 outperforms any other state-of-the-art 5GHz CMOS VCO reported prior to its publication [112]. A detailed performance comparison of VCO9 against other VCOs is made later in this chapter.

6.4 INDUSTRIAL QUALITY 5GHZ VCO

Before VCO9, the best phase noise achieved by the RF design team of WNBU was −112dBc/Hz at 1MHz offset from a 5GHz carrier. While such performance was acceptable for some 5GHz radio chipset developers at the time [14], it was deemed not acceptable for the high performance wireless access point (AP) oriented product lines of Cisco Systems.

Use of a high quality external VCO module was considered as an alternative. Although the external VCO module would deliver the phase noise performance required by the chipset, its use would significantly increased in the chipset cost.

Fortunately, the phase noise performance achieved by VCO9 exceeded the phase noise requirement of the 5GHz radio front-end chipset. Therefore, it was decided to integrate the VCO into the RF chip to be developed for the dual-band operation covering the 2.4GHz band (IEEE 802.11b/g) and the 5GHz band (IEEE 802.11a and HiPERLAN II).

The last VCO presented in this thesis, referred to as VCO10 is used in the wireless AP equipped products of Cisco Systems. Since the VCO10 design was based on a real and practical set of specifications for product level quality, its design process follows the high performance VCO design guidelines developed in Chapter 4.

6.4.1 Specifications

The frequency tuning range as a part of the VCO specifications is closely related to the frequency planning of the dual-band transceiver. The frequency planning part is a company confidential and cannot be disclosed in this thesis. Therefore, the frequency tuning specification is given without any background information as to how the given frequency tuning range is used to cover the entire frequency bands allocated for the IEEE802.11a/b/g and the HiPERLAN II standards. The VCO specifications are summarized in table 6.1.

Table 6.1: VCO10 specifications.

Item	Minimum	Typical	Maximum	Unit
Ambient Temperature	−40		+85	$^\circ C$
Junction Temperature	−40		+125	$^\circ C$
Supply Voltage (V_{DD})	1.6	1.8	2.0	V
Current Consumption			35	mA
VCO Gain (K_V)	100	150	200	MHz/V
Control Voltage (V_{ctl})	0		1.8	V
Phase Noise @1MHz offset	−120			dBc/Hz
Tolerable Capacitance Spread (ΔC)	−15	0	+15	%
Tuning Range for ΔC=0%	3791		4886	MHz
Tuning Range for ΔC=−15%	4113		5299	MHz
Tuning Range for ΔC=+15%	3535		4550	MHz
Guaranteed Tuning Range, ΔC=±15%	4113		4550	MHz

In order to maximize the product yield, the VCO is to maintain the above specifications across all process corners.

In an *LC* tuned VCO design, the most challenging process parameter to deal with is the capacitance variation. Although the required tuning range is only from 4113MHz to 4550MHz or 10%, in the presence of capacitance spread over all process corners, the tuning range of the VCO must be made much larger than the absolute required range.

In the presence of a large switched capacitor bank for wider tuning range, the total capacitance in the tank is dominated by the parasitic capacitors resulting from the metal routings and transistors that form the switches. Because the process spread of the parasitic capacitors is not well controlled nor documented, an estimation for the tolerable capacitance spread is made based on the chip design experience of the RF design team (±15% for the 0.18μm bulk CMOS process).

Given the wide process spread of capacitance, the target frequency range required is from 3791MHz to 4886MHz or 25% at typical. That way, even at the extremes of the capacitance variation, the required tuning range from 4113MHz to 4550MHz is guaranteed.

When the chipset is powered up, it is programmed to undergo a self-calibration phase, and tune all the relevant parameters for the given operating condition. Temperature, supply condition, and the process corner of the chipset are among factors affecting the calibration parameters. The VCO also needs calibration. Although the full tuning range is 25%, only the appropriate 10% is needed for the operation.

The VCO frequency calibration is done through a 5-bit wide frequency control signal that feeds the 5-bit switched capacitor bank. Covering the entire tuning range

with a 5-bit resolution results in a minimum frequency step of approximately 32MHz. The continuous varactor tuning is to cover at least 3 least significant steps of the discrete tuning range. Therefore, the continuous frequency tuning range should be greater than 96MHz.

The lower the current consumption the better. Lower power consumption not only conserves the power, but also helps to reduce the operating temperature of the chip. Because there is a possibility that the target phase noise may be achieved at a lower bias current, it is desirable to have a control over the bias current, so that the system has a flexibility to adjust the current and conserve power. Therefore, a 5-bit wide bias current control signal is allocated to control the VCO bias current. Since the bias current in effect controls the oscillation amplitude, this control signal is referred to as the amplitude control signal.

In order to control the oscillation amplitude automatically, there must be a facility to measure the oscillation amplitude and use it as a feedback. Therefore there is a need for an integrated oscillation amplitude detector.

6.4.2 Tank Design

The design was initiated with the design of the tank. First of all, the required C_{max}/C_{min} ratio or ξ is calculated. For a 25% frequency tuning range, a simple numeric analysis leads to a value of ξ of 1.66.

The capacitor bank quality factor is then estimated based on the quality factors of the MIM capacitor and the parasitic capacitors of the switch transistor. MIM

capacitor Q is around 64 at 5GHz as mentioned earlier. Additional parasitic capacitance resulting from metal routings is assumed to have similar Q values. Parasitic capacitances associated with the transistors are estimated from simulations.

Fig. 6.8(a) shows the schematic diagram of one unit cell of 31 identical switched capacitors that form the 5-bit switched capacitor bank. The 31 switched capacitor cells form 5 binary weighted groups of 1, 2, 4, 8, and 16, as shown in Fig. 6.8(b).
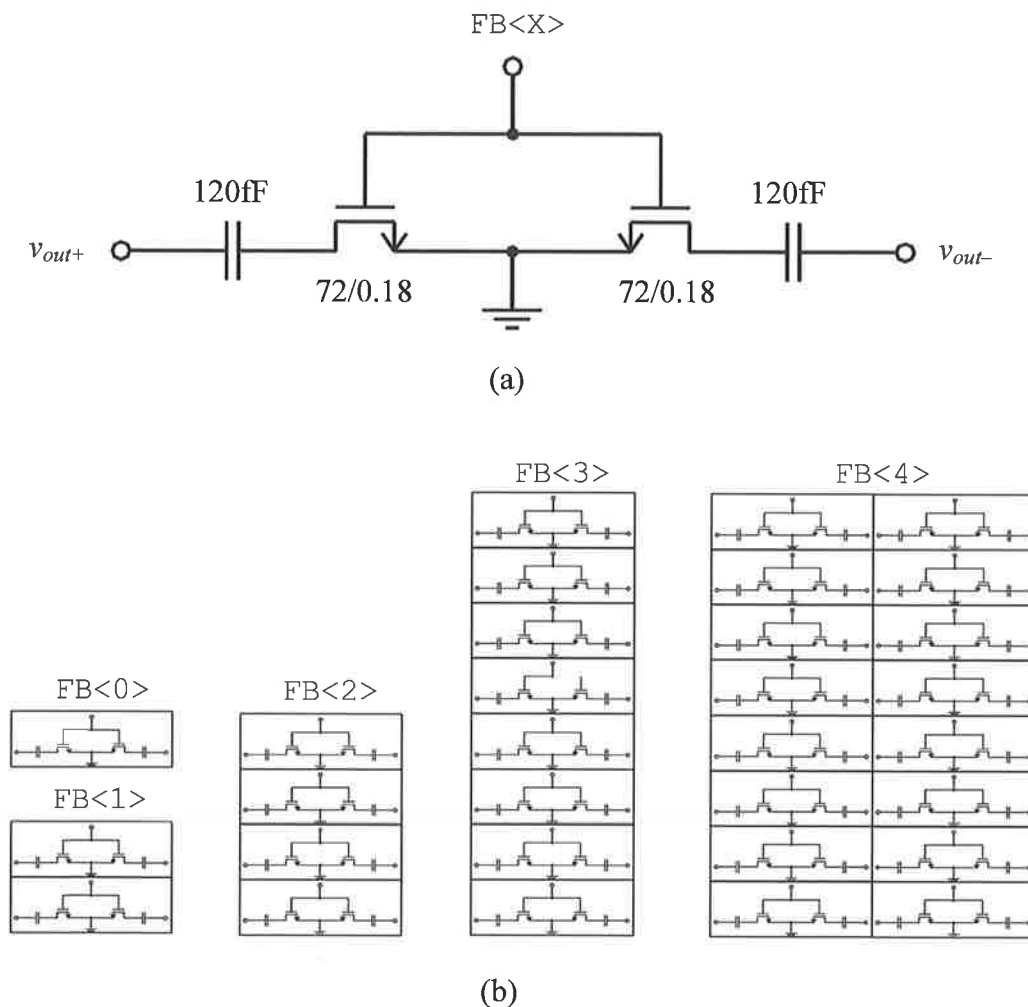

(a)

(b)

Fig. 6.8: (a) Schematic diagram of each switched capacitor cell, and (b) binary weighted grouping of all 31 cells.

Simulations were run with an extracted netlist from the layout, which included the parasitic capacitances as well as the parasitic resistances associated with the metal routings. A series of layout-extracted simulations indicated that switching 1.67fF of MIM capacitor with every micrometer width of switch transistor would result in a Q of 32 when the switch was closed and 64 when opened, while providing the required ξ of 1.66. Therefore, the estimated capacitor bank Q was between 32 and 64 depending on the state of the frequency control signal FB<4:0>. If there is a room for an additional fixed MIM capacitor in the tank, the lower limit of the capacitor Q would increase accordingly.

The next step is to find a realizable low inductance value with high Q_L, but with high enough inductance to provide enough R_{tank} to keep the power consumption within the specification. The L/C ratio used for VCO9 is considered very low in that the oscillation could only be started with the tail bias current as large as 8mA. For VCO10, the L/C ratio was slightly increased to increase R_{tank}. This basically trades some phase noise performance for lower power operation.

D_{out} of the single turn inductor is increased from 400μm to 430μm, and the width of the conductor is decreased from 65μm to 30μm in order to increase the inductance from the value used in VCO9. Fig. 6.9 shows the ASITIC simulation results of L and Q_L of a single turn octagonal inductor. The resulting inductance at w=30 is around 0.38nH, and Q_L is around 16. Some reduction in Q_L is as forecasted. Nonetheless, Q of 16 for an on-chip spiral inductor is still considered outstanding in a bulk CMOS process.

The loaded Q of the tank (Q_{tank}) calculated by (4.1) ranges from 11 to 13, depending on the input state of the capacitor bank. R_{tank} calculated by (5.1) is around 110Ω at typical.
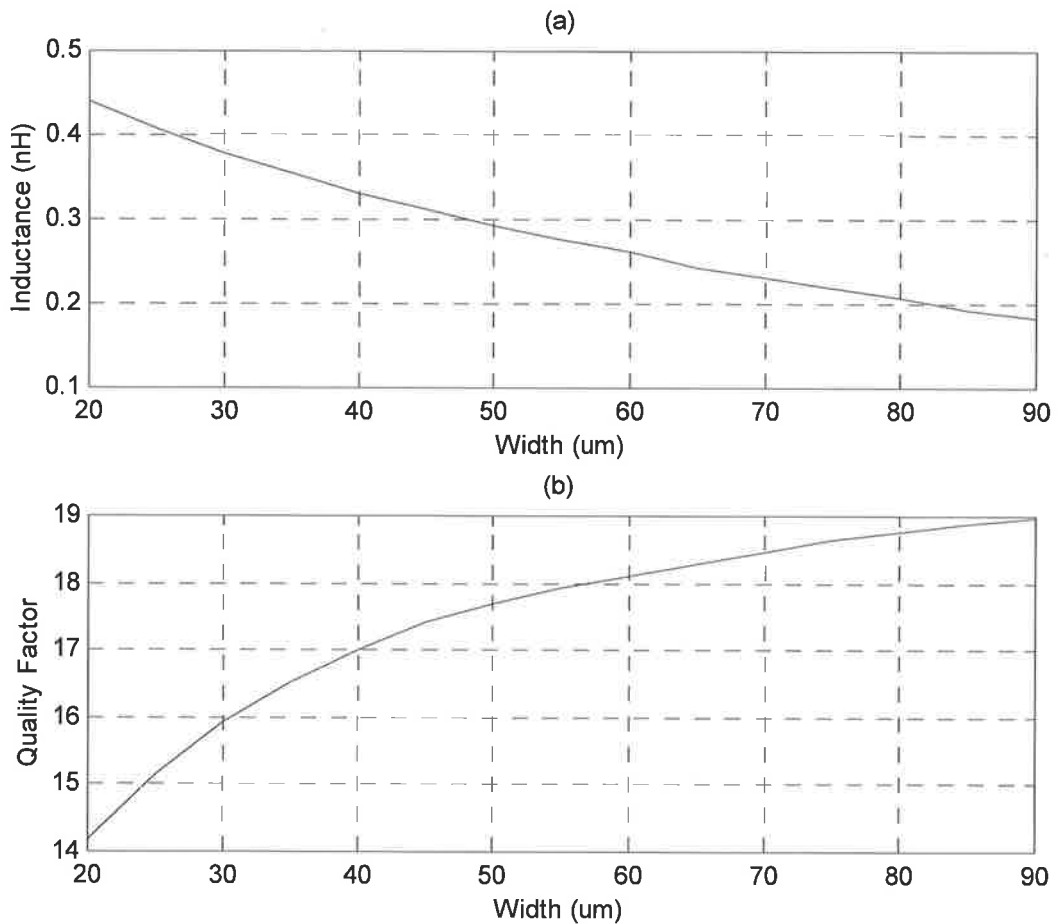
Fig. 6.9: Simulated (a) inductance and (b) quality factor of a single turn inductor with constant D_{out} of 430μm, and varying w.

6.4.3 VCO Design

In order to optimize the size of the cross-coupled pair transistors, three operating spaces shown in Fig. 6.10 are generated based on the estimated values of Q_{tank} and R_{tank}.
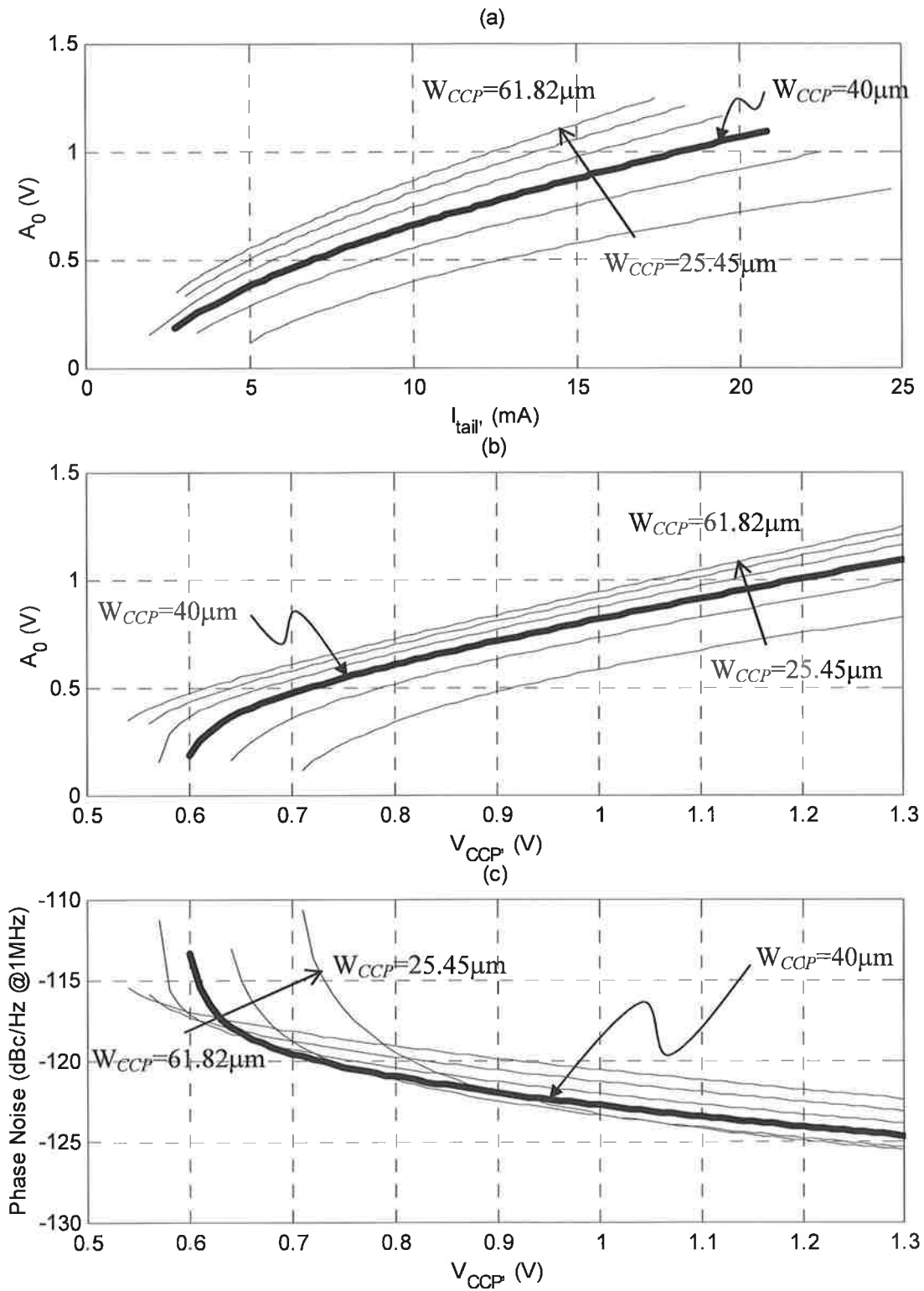
Fig. 6.10: Bias spaces of (a) A_0 versus I_{tail}, (b) A_0 versus V_{CCP}, and (c) phase noise space for a constant R_{tank} of 110Ω, while varying W_{CCP} from $25.45\mu m$ to $61.82\mu m$.

From Fig. 6.10(c), it is observed that W_{CCP}=40μm would ensure operating near the lower bound of the phase noise operating space, which is below −120dBc/Hz at 1MHz offset for most of the bias range. At this value of W_{CCP}, the current sunk by the cross-coupled pair is under 21mA. This leaves around 10mA to be consumed in other parts of the VCO, such as the bias generator and output buffer.

The schematic diagram of the VCO and its output buffer is shown in Fig. 6.11. Transistor sizes are also shown on the schematic diagram. The MOS varactor transistors are sized to provide around 150MHz of continuous tuning. The effective input range of the control voltage, V_{ctl} is designed to be between ground and V_{DD}.
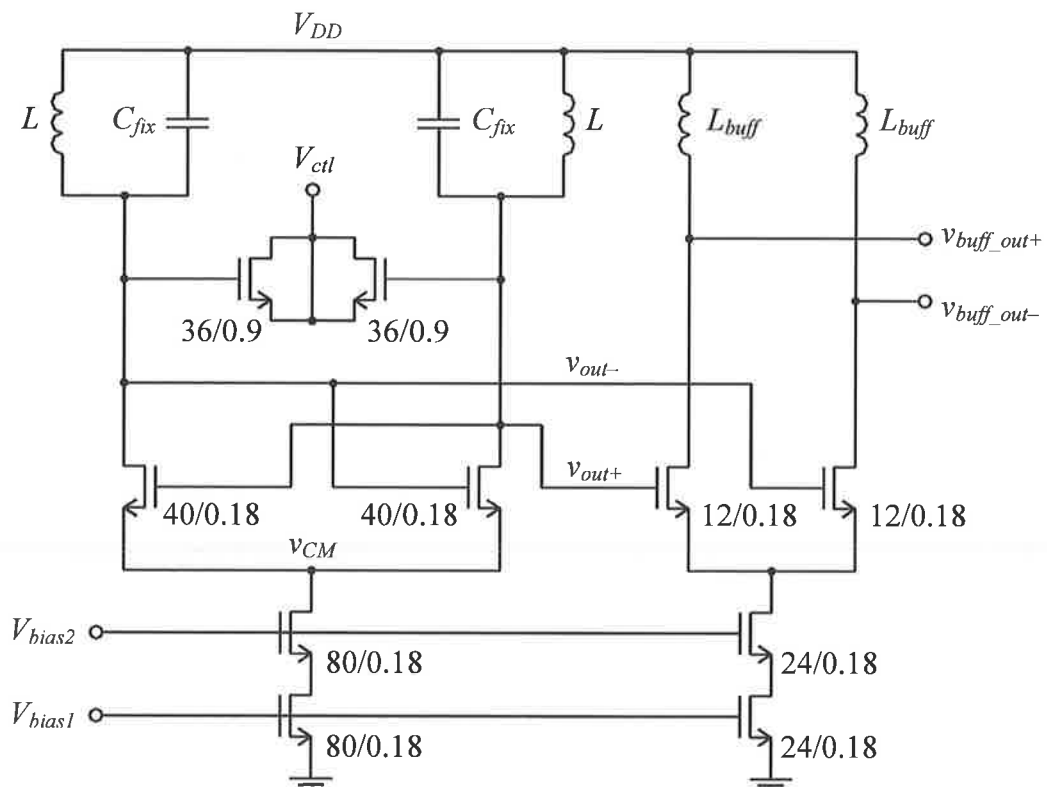
Fig. 6.11: Schematic diagram of VCO10 and its output buffer.

Cascode current sources are used for the VCO and its output buffer, because they provide a much higher output resistance. This helps to control I_{tail} with an improved accuracy.

Although not shown in Fig. 6.11, the 5-bit wide switched capacitor bank of Fig. 6.8 is present across v_{out+} and v_{out-} to provide the discrete frequency tuning range. Because much of the capacitance in the tank is provided by the switched capacitor bank and the parasitic capacitors of the metal routings, there is not much room left for the fixed capacitance. C_{fix} implemented with a high Q MIM capacitor is only 58fF for VCO10.

6.4.4 Bias Current Generator

Looking at Fig. 6.10, for the maximum I_{tail} of 21mA, the cross-coupled pair bias potential, V_{CCP} is 1.3V. That leaves minimum 0.5V for the potential drop across the cascode tail current source.

The bias generator circuit shown in Fig. 6.12 is designed to bias the two cascode transistors with a minimal potential drop of $2V_{DS,sat}$ across the cascode current source. Its design is adopted from the wide-swing current sink illustrated in Fig. 20.27 of [84].
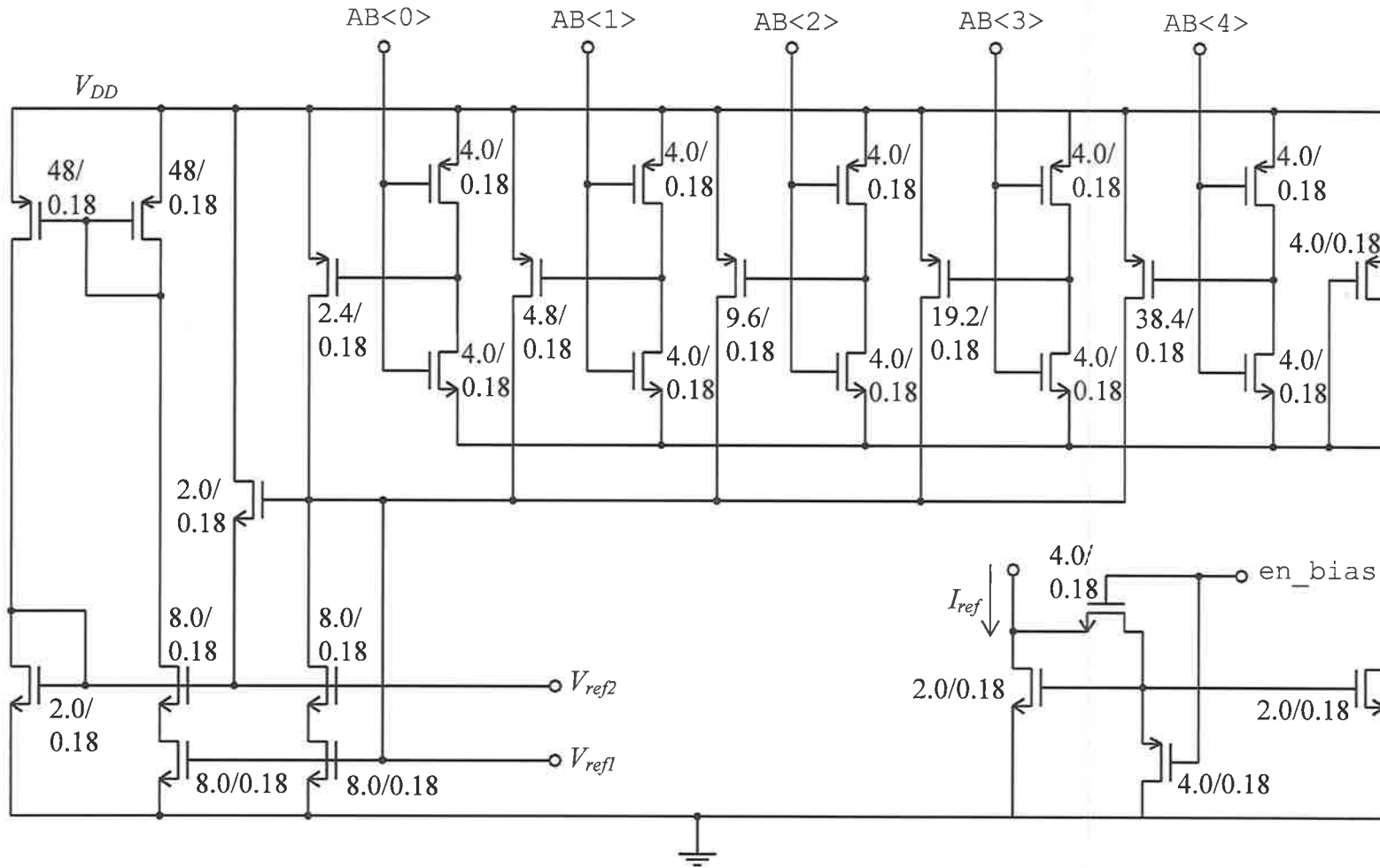
Fig. 6.12: Bias generator for VCO10.

A constant and reliable current of 100μA is provided as a reference current (I_{ref}) to the bias generator. The bias generator uses this reference current to accurately control I_{tail} from 0A to 18.6mA over 31 steps, according to the amplitude control input signal, AB<4:0>. Each bit increment in AB<4:0> corresponds to 0.6mA increment in I_{tail}. This bias scheme limits the maximum I_{tail} to 18.6mA, and V_{CCP} to 1.2V. This gives a little more headroom for the cascode tail current bias transistors.

The input signal en_bias acts as the enable signal for the bias generator. If the bias generator is disabled, the entire VCO is disabled, and draws no current. Therefore, this signal acts as the enable signal for the whole VCO unit.

The nominal current consumption of the bias generator is from 0mA to 5.78mA. The VCO core consumes anywhere between 0mA and 18.6mA. The output buffer is designed to consume anywhere between 0mA and 5.58mA. Therefore, the maximum current consumed by the three circuit modules is 29.96mA, which is just under the target value of 30mA. There exists 5mA margin between the targeted maximum current and the absolute maximum current stated in the specification. This 5mA serves as buffer to deal with an unforeseen increase in I_{ref}.

One potential problem with the current bias scheme is that the current mirroring ratio is very large. For I_{tail} of 18.6mA, the current mirroring ratio between I_{ref} and I_{tail} is as large as 186. As pointed out earlier, any noise present in the 100μA reference current will get amplified by the current mirroring ratio and appear on I_{tail}. Therefore, it is highly desirable to use the low-power, low-noise current biasing technique proposed in section 4.6.2.

Instead of connecting V_{ref1} and V_{ref2} from the bias generator directly to V_{bias1} and V_{bias2} of the VCO core respectively, two low-pass RC filters are placed in between as

shown in Fig.6.13. Two large 2.5MΩ resistors are implemented with two long and narrow non-silicided polysilicon resistors, which has sheet resistance of around $1k\Omega/\square$. High capacitance of around 107pF is realized by each of the MOS capacitor M1 and M2. The *RC* filter has a cutoff frequency of 595Hz. With this filter in place, any noise component with frequency higher than 595Hz coming from the bias generator side will be attenuated at a rate of 20dB/decade.
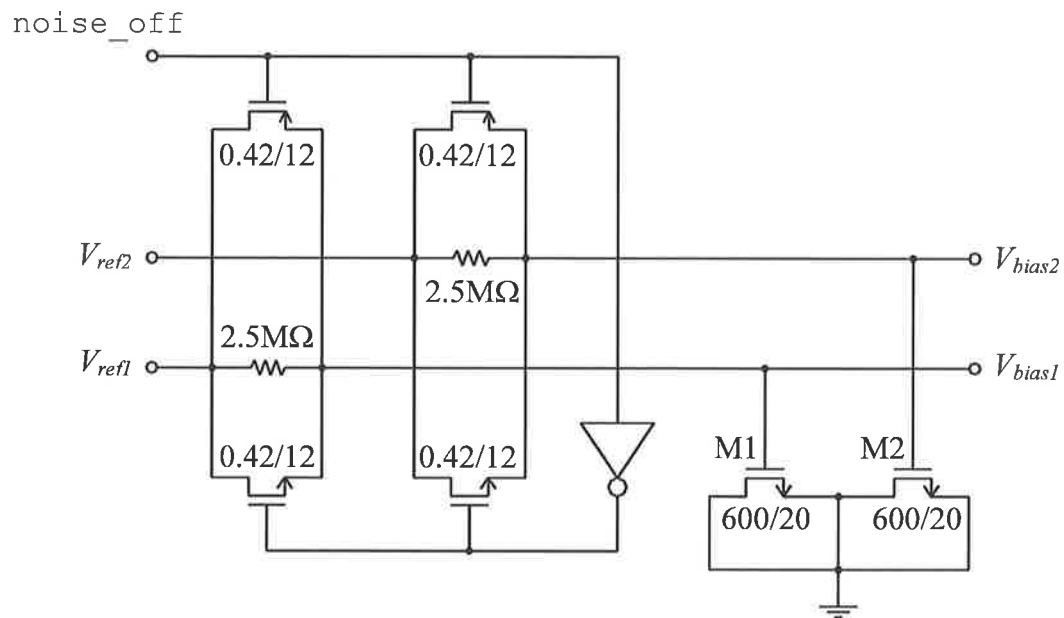
Fig. 6.13: Low-power, low-noise current biasing for VCO10.

A bypass switch is added across each of the resistors to bypass the resistors, in case there is a need for faster settling of V_{bias2} and V_{bias1}. The bypass switch transistors are made long and narrow to ensure high resistance across the drain and source when `noise_off`=1. As a result of the long switch transistors, even when the switches are closed (`noise_off`=0), there exists significant resistance between the input and the output. Nevertheless, it is much lower than 2.5MΩ to allow for much faster settling.

This switch is more of a safety feature, just in case the time constant of the RC filter is much higher than expected.

6.4.5 Amplitude Detector

A simple amplitude detector is designed to monitor the oscillation amplitude of the VCO. Its schematic diagram is shown in Fig. 6.14.
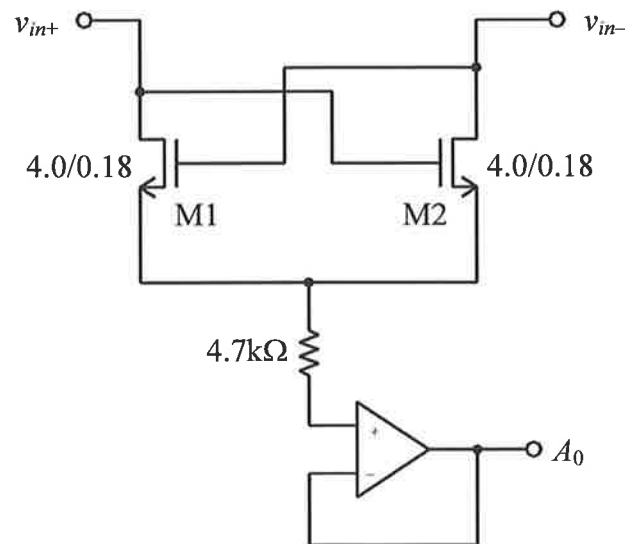
Fig. 6.14: Oscillation amplitude detector.

The differential output of the VCO is connected to the differential input of the detector, v_{in+} and v_{in-}. When v_{in+} is at its peak, v_{in-} is at its minimum and M2 is conducting. At this instance, the source of M2 is at the same potential as v_{in-}. As v_{in+} falls from its peak and v_{in-} rises, M2 gradually stops conducting and M1 starts to conduct. When v_{in+} comes to its minimum, M1 is fully conducting and M2 is cut off. At this instance, v_{in+} appears at the source of M1. Therefore, the common-source of M1 and

M2 always tracks the lower envelope of the oscillation waveform. Therefore, the difference between V_{DD} and the potential at the common-source node is the oscillation amplitude, A_0.

The impedance at the common-source node is preferably kept as high as possible in order not to load the tank unnecessarily. Therefore the detected amplitude signal is coupled to a unity gain buffer, via a high value resistor. The output of the unity gain buffer is then fed to an on-chip 8-bit analog-to-digital converter (ADC) for processing in the digital domain.

6.4.6 Results

The whole VCO unit has been simulated for oscillation amplitude and frequency, and passed all corners of the specification, which includes all process corners, temperature corners, and the supply voltage corners.

Unfortunately, the phase noise simulations did not converge, because of the complexity in the layout-extracted netlist, which included a large number of parasitic elements such as the parasitic capacitors and resistors.

The microphotograph of VCO10 is shown in Fig. 6.15. It occupies approximately 0.473mm^2 of the total chip area of 5mm×5mm=25mm^2.

Measurements were made with the setup shown in Fig. 6.16. The radio chip integrates all the digital control logic required to control every RF circuit module in the chip, including the VCO. The oscillator bias control signal or the oscillation amplitude control signal, AB<4:0>, and the discrete frequency control signal, FB<4:0> are

wired to an internal microprocessor. The oscillation amplitude detected by the amplitude detector is converted to an 8-bit digital signal, and fed to the microprocessor for processing. The internal microprocessor is controlled by a personal computer (PC). A test PCB interfaces the radio chip to the PC.
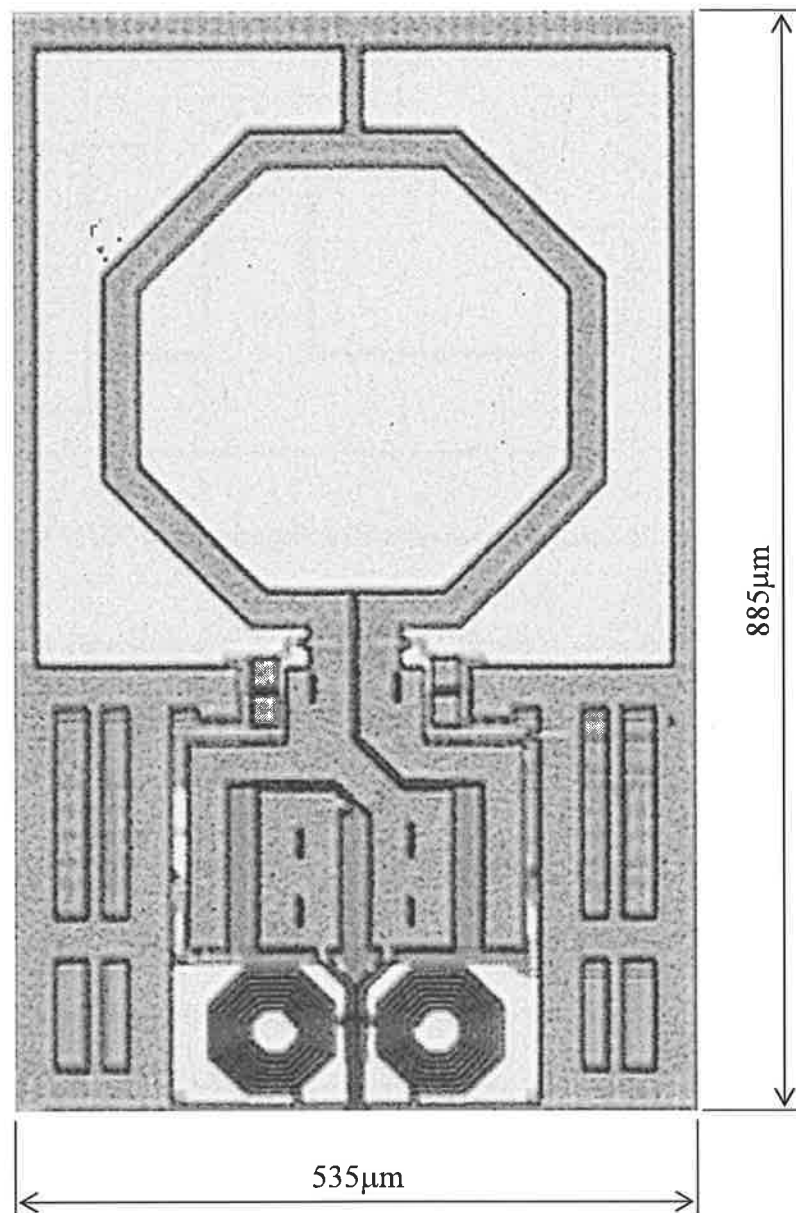
Fig. 6.15: Microphotograph of 5GHz bulk CMOS VCO for IEEE 802.11a/b/g and HiPERLAN II applications.
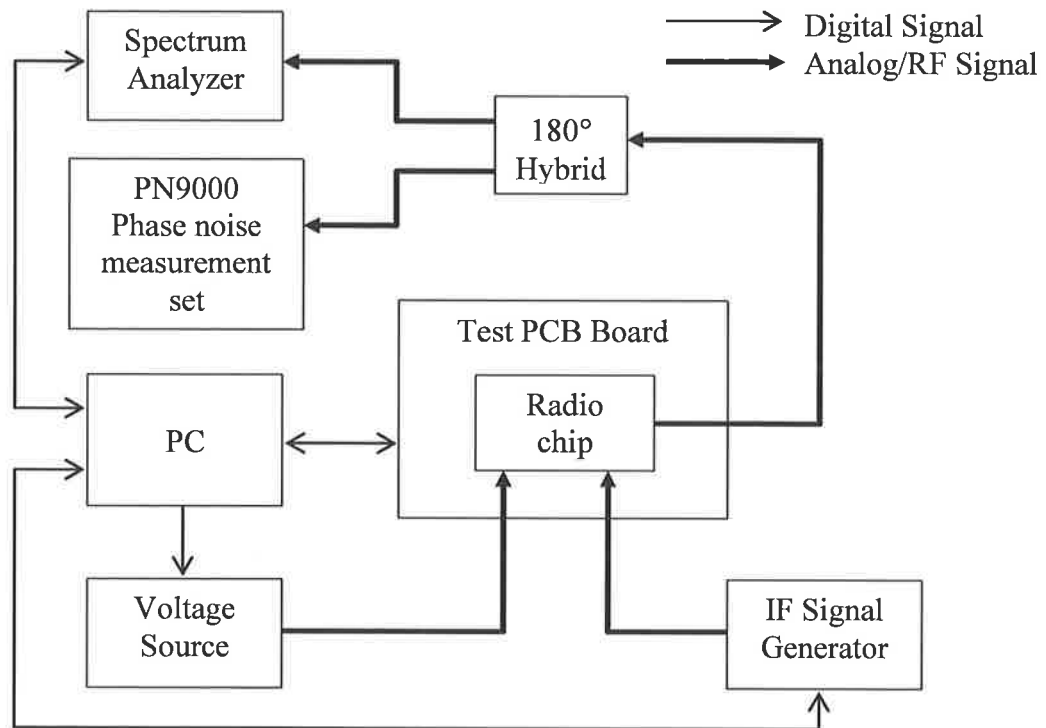
Fig. 6.16: Phase noise measurement setup for experimental 5GHz VCOs.

The continuous frequency control signal, V_{ctl} is generated by an external voltage source. Its output voltage is controlled by the PC through the General-Purpose-Interface-Bus (GPIB) link.

The radio chip is configured to work in the transmit mode during the VCO measurements. A signal generator feeds the radio chip with a single tone IF signal. This signal travels through the transmit path of the radio chip and appears at the output pin. During this process the IF signal is mixed with the internal oscillator signal. Since the IF signal generated by a signal generator is much cleaner than the internal VCO signal, the phase noise of the output signal is basically all due to the internal VCO.

The signal generator, and the spectrum analyzer are also connected to the PC via the GPIB link. This enables automation of most of the measurement process, except the

phase noise measurement. The PN9000 does have the GPIB interface, but unfortunately it lacked suitable software to make use of it.

The first set of measurements involved measuring the oscillation amplitude across the full tuning range, and the full amplitude control range. The continuous frequency control voltage, V_{ctl} is set at its halfway point or 0.9V while the measurements are made. The oscillation amplitude detected is converted to an 8-bit digital signal and read by the PC. Fig. 6.17(a) shows curves of the measured oscillation amplitude across the full amplitude control range. The VCO started to oscillate with AB<4:0>=7. Since each step in AB<4:0> corresponds to 0.6mA change in the tail bias current, the minimum I_{tail} required to sustain oscillation is 4.2mA for this VCO. For a given amplitude control input, the oscillation amplitude does not change much across the full frequency tuning range.

(a) V_{ctl}=0.9V
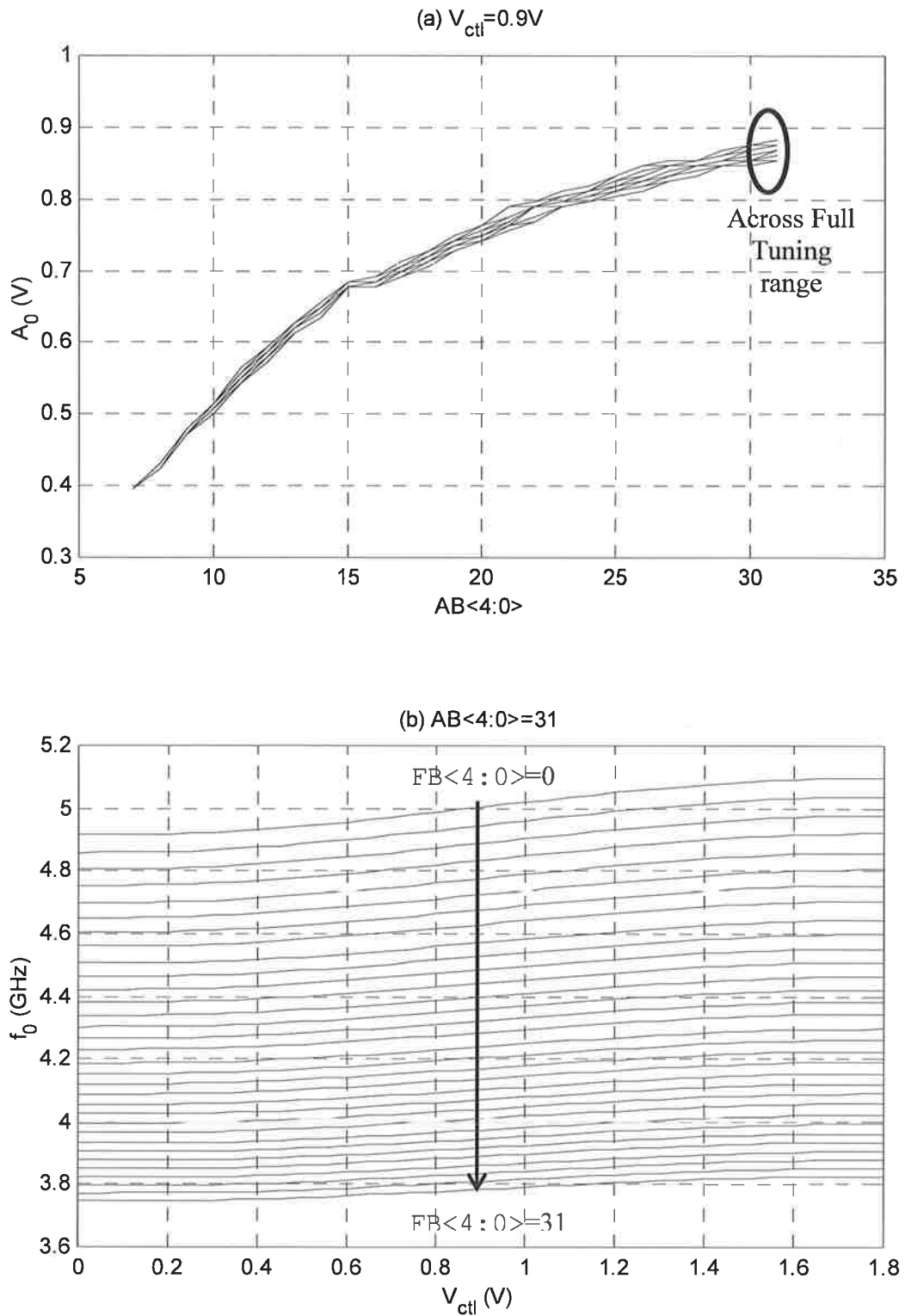
(b) AB<4:0>=31

Fig. 6.17: Measured (a) oscillation amplitude across full frequency tuning range, and (b) entire frequency tuning range of VCO10.

Fig. 6.17(b) shows the measured frequency tuning curves of the VCO for AB<4:0>=31. The discrete frequency control signal, FB<4:0> is varied from its minimum to maximum. For every FB<4:0> control signal, the continuous frequency control signal, V_{ctl} is swept from 0V to 1.8V. The result shows complete coverage of frequency from 3.75GHz to 5.1GHz. This corresponds to approximately 30% tuning range, and it is more than enough to cover the frequency tuning specification for the typical process corner (ΔC=0%). Indeed, the process-control-monitor (PCM) data of the sample chips indicated that the wafers conformed to the typical process corner. Therefore the frequency tuning range should cover the required frequency range of the chipset across all process corners.

Although the amplitude control signal has a negligible impact on the full frequency tuning range, it affects the shape of the frequency tuning curves. Fig. 6.18(a) shows how the oscillation amplitude affects the frequency tuning curves. The frequency tuning curves becomes steeper as AB<4:0> is reduced. A steeper frequency tuning curve means larger VCO constant (K_V). Fig. 6.18(b) shows how K_V changes with respect to AB<4:0>. The peak K_V varies from 340MHz/V to 100MHz/V, as AB<4:0> is varied from 7 to 31. This feature can be used to adjust K_V if desired and provides an extra flexibility in the PLL design.
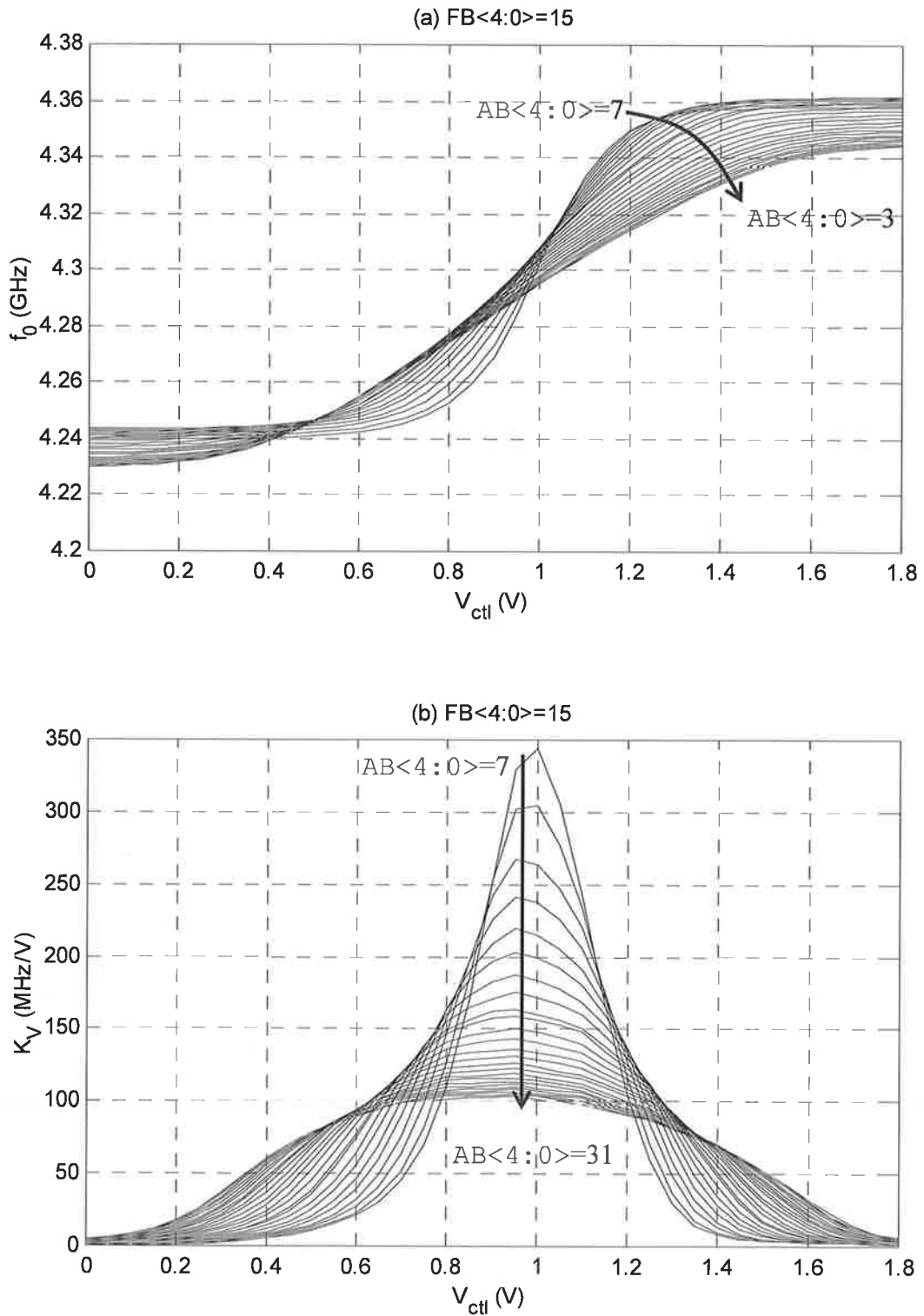
Fig. 6.18: Measured (a) frequency tuning curves and (b) VCO gain curves at different oscillation amplitudes of VCO10.
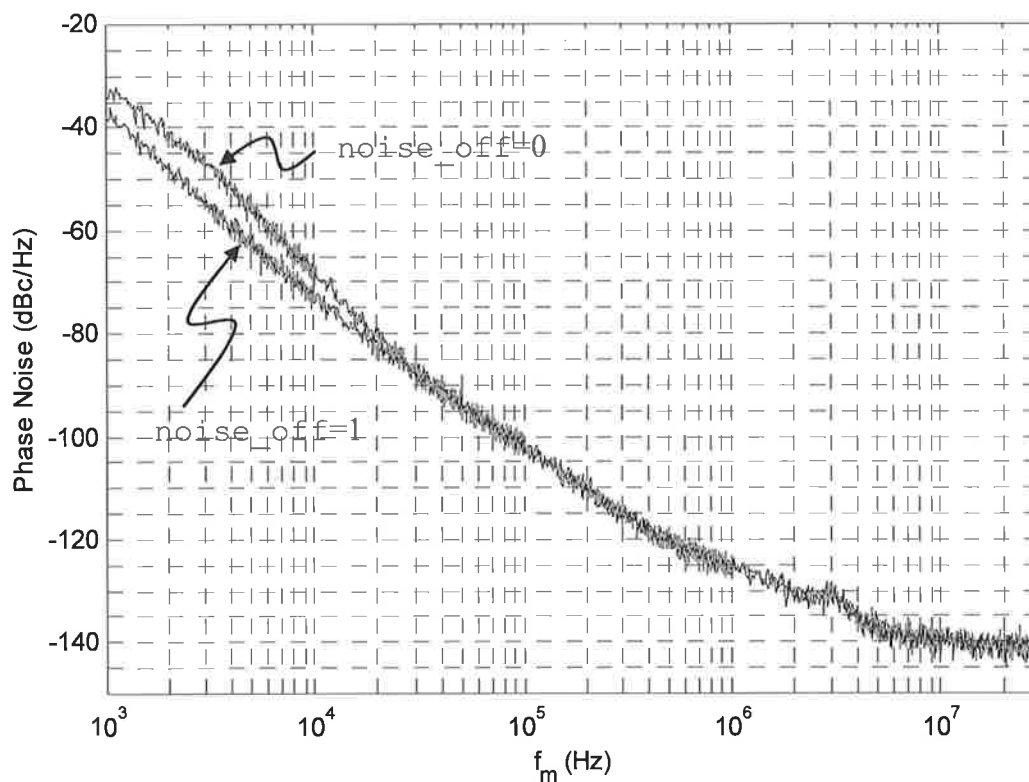
Fig. 6.19: Measured phase noise spectral plots when `noise_off=0` and `noise_off=1`. AB<4:0> and FB<4:0> are held at 27 and 15 respectively, and V_{ctl} is set to 0.9V.

The next set of measurements involved measuring of the oscillator phase noise. Fig. 6.19 shows two measured spectral plots of the phase noise when the tail bias noise filter is turned on or off. The phase noise measurements are made with V_{ctl} set to 0.9V, where K_V is maximum. This corresponds to the point where the phase noise is potentially the worst within the continuous tuning range. The improvement in phase noise when `noise_off` signal is turned on is most noticeable for offset frequencies below 20kHz. The improvement is as much as 8dB. The fact that there is a large

improvement in phase noise when the bias filter becomes active indicates that the filter is effectively filtering out the low frequency noise fed from the bias generator.

At higher frequency offsets, the phase noise performance is indistinguishable between the two input states of the `noise_off` signal. This means, although the pole of the *RC* filter is shifted up in frequency due to the reduced series resistance when the noise filter bypass switch is closed, the filter is still able to filter out the noise components higher than 20kHz to a negligible level. For the best phase noise performance, the `noise_off` signal should be turned on at all times.

Although the VCO oscillates with AB<4:0> signal ranging from 7 to 31, only a part of that range is accepted by the phase noise specification. Fig. 6.20(a) shows how the measured phase noise varies with respect to the amplitude control signal, AB<4:0>. Since the specification asserts that the phase noise to be better than −120dBc/Hz at 1MHz offset, the VCO must be operated with AB<4:0> higher than 12.
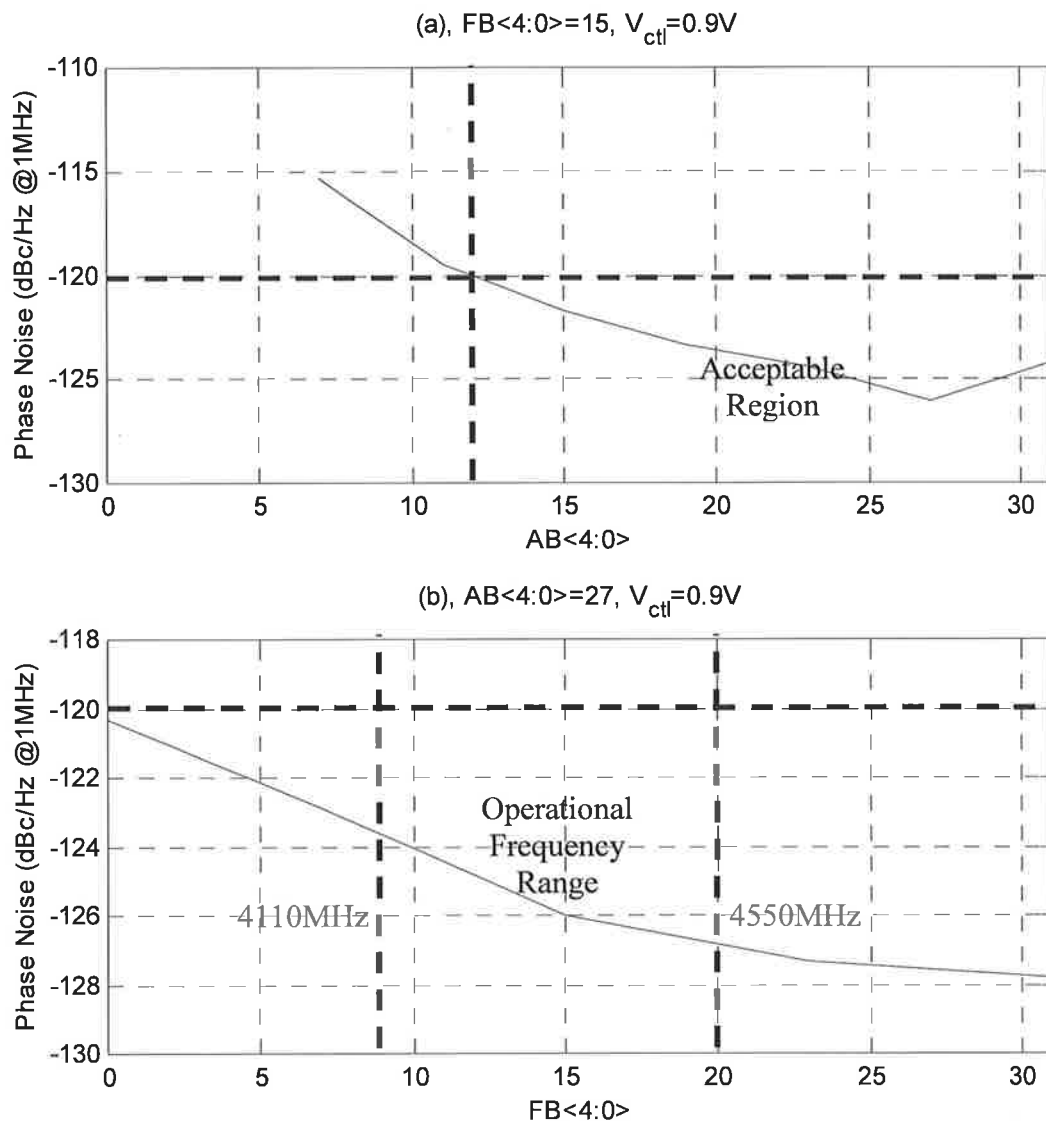
Fig. 6.20: Measured phase noise (a) across full amplitude range, and (b) across full frequency range.

The required frequency range is from 4113MHz to 4550MHz by the specification. For constant V_{ctl} of 0.9V, the discrete frequency control signal, FB<4 : 0> from 9 to 20 covers the required frequency range as shown in Fig. 6.20(b). The measured phase noise within the operational frequency range exceeds the specification.
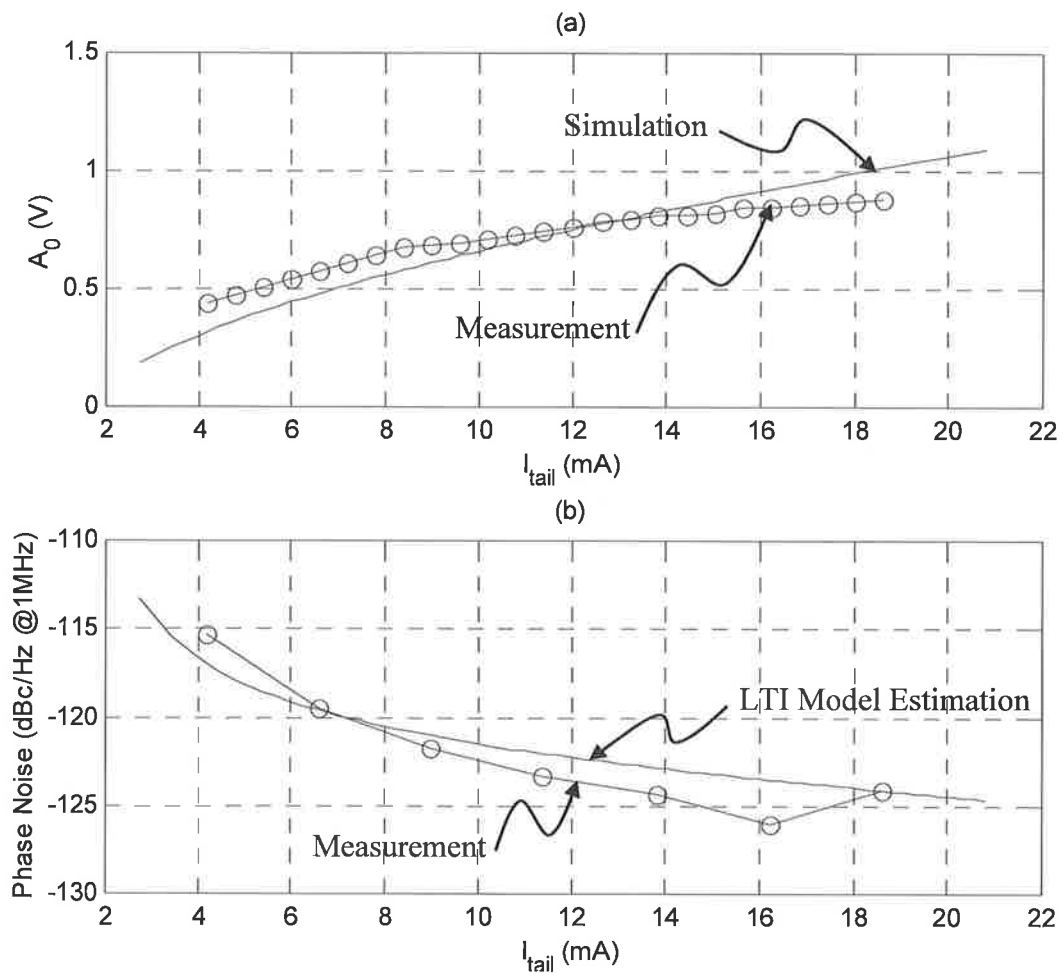
Fig. 6.21: (a) Oscillation amplitude comparison between simulation and measurement and (b) phase noise comparison between LTI model estimation and measurement.

Oscillation amplitudes predicted in simulation were compared against the measured values as shown in Fig. 6.21(a) and close agreement between the two observed.

Looking at Fig. 6.21(b), although the phase noise could not be simulated due to the circuit complexity, the simple LTI model predicted the phase noise performance quite within the –20dB/decade region where the upconverted low frequency noise is negligible compared to the thermal noise of the tank and the cross-coupled transistors.

6.5 VCO PERFORMANCE COMPARISON

As seen from the previous section, VCO10 exceeds the stringent specification of the dual-band radio chip. In this section, the performance of VCO2, VCO9 and VCO10 are compared against other high performance VCOs operating in similar frequency bands as reported in the literature over the past few years.

Table 6.2 shows how the VCOs from this work compares against other state-of-the-art VCOs. Despite the average quality process technology used, VCO9 and VCO10 have achieved the lowest phase noise and the lowest FOM, where the FOM is calculated with (2.15). Some superior process technologies, such as the 0.13μm SOI CMOS used in [20], have advantages such as higher inductor Q (due to the insulating substrate), higher varactor Q and capacitance ratio (due to the lower device parasitics), and higher gain transistors (due to smaller feature sizes and reduced parasitics). Nonetheless VCO9 or VCO10 outperform the VCO reported in [20] in every respect, except for the wider frequency tuning range in [20] (due to the availability of the far superior varactors in the 0.13μm SOI CMOS process).

The bipolar technologies are known to offer lower device flicker noise and larger transconductance compared to CMOS devices. Nonetheless, no bipolar VCOs found in the literature outperformed VCO9 or VCO10.

VCO10 was fabricated and measured in the last quarter of 2003. At the time, the results could not be published due to the company confidentiality. Later, it was released

from the confidentiality and this thesis is able to report the design and results for the

first time.

Table 6.2: VCO performance comparison.

Reference	Process Technology	f_0 (MHz)	Tuning Range (MHz)	P_{DC} (mW)	Phase Noise (dBc/Hz @1MHz)	FOM (dBc/Hz)
[26]	0.25µm CMOS	3945	350	4.08	-99.2	-165.1
[16]	0.5µm BiCMOS	4900	310	57.2	-107.0	-163.2
[26]	0.35µm CMOS	4887	500	9.00	-107.3	-171.5
[17]	Si Bipolar	5765	350	255	-110.0	-161.2
[18]	0.12µm CMOS	3980	1060	1.50	-113.0	-183.2
[17]	SiGe HBT	4765	330	132	-114.0	-166.4
[19]	SiGe HBT	3910	350	17.5	-114.0	-173.4
[20]	0.13µm SOI CMOS	5612	2600	2.50	-114.5	-185.5
[21]	0.35µm BiCMOS	4700	1000	25.0	-115.5	-174.9
[10]	0.25µm CMOS	5462	285	6.90	-116.0	-182.4
[22]	0.25µm CMOS	5230	310	7.05	-116.5	-182.4
[23]	0.25µm CMOS	4000	990	18.8	-117.0	-176.3
[24]	0.25µm CMOS	5000	1100	7.25	-117.0	-182.4
[22]	0.25µm CMOS	5350	354	7.05	-117.0	-183.1
[25]	0.25µm CMOS	4600	230	9.40	-118.1	-181.6
[15]	0.5µm BiCMOS	4405	620	21.6	-119.0	-178.5
[17]	SiGe HBT	4765	270	32.0	-120.0	-178.5
[27]	0.25µm CMOS	4880	780	21.9	-124.5	-184.9
VCO2	**0.5µm SOS CMOS**	**5250**	**200**	**1.65**	**-110.0**	**-182.2**
VCO9	**0.18µm CMOS**	**5330**	**200**	**17.3**	**-126.0**	**-188.2**
VCO10	**0.18µm CMOS**	**4280**	**1350**	**16.2**	**-126.0**	**-186.5**

6.6 CONCLUSIONS

Two high performance bulk CMOS VCOs were presented in this chapter. VCO9 demonstrated a record low phase noise and FOM. VCO10 inherited similar phase noise performance from its predecessor, VCO9, while incorporating much wider frequency tuning range to withstand the process variation and maximize yield. VCO10 exceeded the stringent specifications given for the high performance dual-band wireless AP application in every respect.

The amplitude detector implemented for VCO10 successfully and accurately detected the oscillation amplitude and allows for quick and easy analysis of the oscillation amplitude within the chip.

The low-power, low-noise biasing scheme successfully demonstrated its ability to allow for the large current mirror ratio to be used in a VCO design, while limiting the current noise multiplication engendered by the large current mirror ratio. This technique drastically reduces the power requirement of the bias circuit, which normally requires the same amount of bias current as the VCO core for low noise operation.

Despite the average quality process technology used, the frequency tuning range is outstanding when compared to designs using other 'superior' CMOS technologies (such as the 0.13µm SOI CMOS process). In addition, the phase noise performance achieved is better than any monolithic VCOs reported in the literature to date, including VCOs from various bipolar technologies.

Chapter 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 CONCLUSIONS

New high performance monolithic cross-coupled CMOS VCO optimization techniques have been developed in this thesis. The techniques developed include the geometric optimization of the planar spiral inductors, phase noise performance improvement by the L/C ratio downscaling and the optimal sizing of the cross-coupled transistors. Also, a new low-noise, low-power biasing technique and a simple on-chip oscillation amplitude detector were devised and implemented. The new optimization techniques allow for integration of high performance CMOS VCOs into modern communication chips to help improving the data throughput of the system.

All of this has been achieved through four major steps. Firstly, existing VCO phase noise theories were reviewed. Their properties and usefulness in predicting the phase noise of a VCO were investigated. The simple LTI phase noise estimation equation allowed for quick, simple, and rough estimation of the phase noise in the −20dB/decade region for LC tuned VCOs. This simple LTI model proved itself to be most useful when the more sophisticated modern CAD tools are not able to converge

the phase noise simulations due to the complicated netlist of a VCO that includes all the parasitic elements.

Secondly, the properties of various differential LC tuned VCO topologies were thoroughly investigated. Some of the common misunderstandings of cross-coupled LC tuned oscillators often found in the literature were appropriately addressed. This includes the commonly accepted linear oscillation amplitude expressions as given in (3.1) and (3.2) for the NMOS-only topology. These equations should not be used to estimate the oscillation amplitude of a cross-coupled oscillator, because the assumptions used in the derivation of these expressions are too crude and inaccurate.

The so-called 'voltage-limited region' of a cross-coupled VCO bias region was shown to be nonexistent. The optimal bias point of a cross-coupled VCO based on the belief of the existence of the voltage-limited region frequently reported in the literature must be reviewed as a consequence.

In addition, the topological superiority of the complementary topology over the NMOS-only topology often claimed in the literature was shown to have no solid ground. In fact, the NMOS-only topology is less complex than the complementary topology to implement. Furthermore, the NMOS-only topology is more immune to the CMM-to-FM flicker noise upconversion process than the complementary topology. The complementary topology has an added difficulty of leveling the bias potential of the output waveform at halfway point between the two supply rails to avoid premature amplitude clipping by the supply rails.

As a part of cross-coupled VCO analysis, various frequency-tuning methods available were also investigated. MOS varactors were found to be the most effective way to implement continuously variable capacitances. In order to cover the wide

process spread typical in CMOS processes, switched capacitors or varactors can be used to increase the overall frequency tuning range.

The noise analysis of cross-coupled LC tuned VCOs was then covered. Noise sources internal and external to the VCOs were identified. Low frequency flicker noise upconversion processes, namely AM-to-FM, CMM-to-FM and the Groszkowski effects were discussed.

Thirdly, based on the findings from analyses of cross-coupled VCOs, a new set of VCO optimization techniques were developed. These techniques were developed to design the best performing VCO realizable for a given process technology, chip area, and power budget.

The monolithic planar spiral inductor geometric optimization technique enabled design of high performance inductors for a given process technology and chip area. The technique takes into account most of the high frequency effects namely, the skin effect, the proximity effect, and the substrate effects. In general, smaller inductance, larger inductor outer diameter, lower number of spiral turns, and hollow inductor geometry yield the higher inductor Q.

A technique that allows efficient tradeoff of power consumption for improved phase noise performance by downscaling the L/C ratio of the tank circuit was developed to deliver the phase noise performance needed. Together with the improvement in inductor Q for lower value inductors, it was found that lower L/C ratio results in improved phase noise and FOM.

The cross-coupled transistor size optimization technique developed allowed for the optimal sizing of the cross-coupled pair such that it guaranteed the lowest phase

noise or FOM achievable by a cross-coupled LC tuned VCO for a given process technology and power budget.

In addition, the newly developed low-power, low-noise current biasing technique allowed for power efficient current biasing of the VCO without compromising the phase noise performance.

A simple envelope detector that works at RF frequencies to monitor the oscillation amplitude of a VCO was devised. This amplitude detector allowed for on-chip calibration of oscillation amplitude.

Lastly, the VCO optimization techniques developed were applied and validated by fabricating nine test VCOs and one industrial quality VCO and analyzing their measured performances. Of those ten VCOs built, eight of them were fabricated using Peregrine's SOS 0.5μm CMOS process, and two were built by using TSMC's 0.18μm mixed-mode bulk silicon CMOS process.

The Peregrine's SOS process is shown to be quite adequate for implementing 5GHz VCOs, especially for the low-power mobile applications. The biggest advantage of this process is in the insulating substrate that allows for implementation of very high Q inductors.

The two 17GHz VCOs implemented in this process technology showed that unnecessarily thick conductor used to construct a spiral inductor could in fact degrade the inductor performance due to the increased series resistance of the spiral inductor at high frequencies.

One downside to the SOS 0.5μm CMOS process would be the excessive flicker noise associated with their transistors. Nevertheless, this problem may be alleviated by

using a PLL with a wide loop bandwidth to sufficiently suppress the close-in phase noise dominated by the flicker noise.

The 0.18μm bulk CMOS process was shown to be quite adequate for monolithic implementation of a VCO for the high performance AP quality wireless applications. The first VCO prototype produced in this process technology pushed the boundary of the phase noise performance of fully monolithic VCOs reported in the literature.

Based on the prototype and the set of optimization techniques developed in this work, the second VCO was produced in accordance with the specifications required by the product level radio front-end chip. This VCO exceeded all of the stringent specifications imposed. Realization of such a high quality VCO using the 0.18μm bulk CMOS process had remained questionable until its first appearance in this work.

Based on the measured results of the high performance VCOs designed and fabricated in this work, it can be concluded that the set of optimization techniques developed in this thesis is quite adequate and effective for the design of high performance cross-coupled LC tuned CMOS VCOs.

7.2 RECOMMENDATIONS

In order to advance the academic pursuit of designing high performance CMOS VCOs, the following recommendations can be made. First, there is a tremendous push to operate at higher frequencies to gain access to more frequency channels to meet the explosive demands of the wireless industry. Operating at higher frequencies is difficult to achieve because the phase noise is degrading at a rate of 20dB per every decade

increase in the operating frequency. In order to achieve the phase noise required for high performance wireless communication at higher frequencies, more power consumption seems to be the only way, unless higher transistor gain and faster process technology is used. Therefore, the leading CMOS technologies such as 90nm SOI CMOS process should be actively investigated to push the operating frequencies of monolithic VCOs further up without compromising the phase noise performance.

Secondly, at higher frequencies, it is no longer the inductors that is limiting the quality of the resonator, but it is the capacitors that degrade the quality of the tank as the operating frequency increases. Therefore, high quality varactors operating at higher frequencies must be actively researched.

Thirdly, above certain frequencies where lumped element implementation of the tuned circuit is difficult to achieve, other means of implementing the tuned circuit must be investigated. Optimization of high frequency resonators such as half-wavelength transmission line resonators or cavity resonators using the MEMS technology would be another interesting research area to work on.

Lastly, another low-noise, low-power VCO biasing technique is proposed. By making the diode-connected transistor length much longer than that of the tail transistor while keeping the width the same, low-power biasing becomes possible, while the amount of flicker noise multiplied and mirrored to the tail transistor is virtually unchanged. This is because the amount of current sunk by the diode-connected transistor and the flicker noise of the diode-connected transistor are both inversely proportional to the gate length. Although this is yet to be validated experimentally, the performance is expected to surpass the low-noise, low-power biasing technique implemented in this work.

REFERENCES

[1]   E. Drucker, "Model PLL Dynamics And Phase-Noise Performance," *Microwave & RF*, Feb. 2000.

[2]   *Wireless LAN MAC and PHY Specifications-High Speed Physical Layer in the 5 GHz Band,* IEEE Standard 802.11a-1999, 2000.

[3]   ETSI TS 101 475: "Broadband Radio Access Networks (BRAN); HIPERLAN Type 2; Physical (PHY) layer".

[4]   A. G. Armada, "Understanding the Effects of Phase Noise in Orthogonal Frequency Division Multiplexing (OFDM)," *IEEE Trsns on Broadcasting,* vol.47, No. 2, Jun. 2001.

[5]   T. A. Raju, N. G. Kurahatti, N. M. Dube, and M. K. Roy, "Monolithic surface acoustic wave resonator oscillator," *Journal of Applied Physics,* vol. 54, pp. 1268-1272, Mar. 1983.

[6]   J. Papapolymerou J.-C. Cheng, J. East, and L P. B. Katehi, "A Micromachined High- X-Band Resonator," *Microwave and guide wave letters,* vol. 7, No. 6, Jun. 1997.

[7]   L. Sun, and T. A. Kwasniewski, "A 1.25-GHz 0.35-µm Monolithic CMOS PLL Based on a Multiphase Ring Oscillator," *IEEE J. Solid-State Circuits,* vol. 36, No. 6, pp. 910-916, Jun. 2001.

[8]   S.-J. Song, S. M. Park, and H.-J. Yoo, "A 4-Gb/s CMOS Clock and Data Recovery Circuit Using 1/8-Rate Clock Technique," *IEEE J. Solid-State Circuits,* vol. 38, No. 7, pp. 1213-1219, Jul. 2003.

[9]   T. H. Lee, and A. Hajimiri, "Oscillator phase Noise: A Tutorial," *IEEE J. Solid-State Circuits,* vol. 35, No. 3, pp. 326–336, Mar. 2000.

[10] C. M. Hung, and K. K. O, "A Fully Integrated 1.5-V 5.5-GHz CMOS Phase-Locked Loop," *IEEE J. Solid-State Circuits,* vol. 37, No. 4, pp. 521-525, Apr. 2002.

[11] P. Larsson, "A 2–1600-MHz CMOS Clock Recovery PLL with Low-*Vdd* Capability," *IEEE J. Solid-State Circuits,* vol. 34, No. 12, pp. 1951-1960, Dec. 1999.

[12] P. Nilsson, and M. Torkelson, "A Monolithic Digital Clock-Generator for On-Chip Clocking of Custom DSP's," *IEEE J. Solid-State Circuits,* vol. 31, No. 5, pp. 700-706, May 1996.

[13] P. Zhan *et al.* "A 5-GHz Direct-Conversion CMOS Transceiver," *IEEE J. Solid-State Circuits,* vol. 38, No. 12, pp.2209-2220, Dec. 2003.

[14] M. Zargari *et al.*,"A 5-GHz CMOS Transceiver for IEEE 802.11a Wireless LAN Systems," *IEEE J. Solid-State Circuits,* vol. 37, No. 12, pp. 1688–1694, Dec. 2002.

[15] M. A. Margarit, *et al.,* "A 5-GHz BiCMOS RFIC Front-End for IEEE 802.11a/HiperLAN Wireless LAN," *IEEE J. Solid-State Circuits,* vol. 38, No. 7, pp. 1284-1287, Jul. 2003.

[16] J. van der Tang, P. van de Ven, D. Kasperkovitz, and A. van Roermund, "Analysis and Design of an Optimally Coupled 5-GHz Quadrature *LC* Oscillator," *IEEE J. Solid-State Circuits,* vol. 37, No. 5, pp. 657-661, May 2002.

[17] H. Jacobsson, *et al.,* "Low-Phase Noise Low-Power IC VCOs for 5–8-GHz Wireless Applications," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, No. 12, pp. 2533–2539, Dec. 2000.

[18] J. Maget, M. Tiebout, and R. Kraus, "MOS Varactors With n- and p-Type Gates and Their Influence on an *LC*-VCO in Digital CMOS," *IEEE J. Solid-State Circuits,* vol. 38, No. 7, pp. 1139–1147, Jul. 2003.

[19] M. A. Copeland, *et al.,* "5-GHz SiGe HBT Monolithic Radio Transceiver with Tunable Filtering," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, No. 2, pp. 170–181, Feb. 2000.

[20] N. Fong, J.-O. Plouchart, N. Zamdmer, D. Liu, L. Wanger, C. Plett, and G. Tarr, "A low-voltage multi-GHz VCO with 58% tuning range in SOI CMOS," in *Custom IC Conf.*, Orlando FL, pp. 423-426, May 2002.

[21] N. T. Tchamov, T. Niemi, and N. Mikkola, "High-Performance Differential VCO Based on Armstrong Oscillator Topology," *IEEE J. Solid-State Circuits,* vol. 36, No. 1, pp. 139-141, Jan. 2001.

[22] C.-M. Hung, , *et al.*, "Fully Integrated 5.35-GHz CMOS VCOs," *IEEE Trans. Microwave Theory and Techniques,* vol. 49, No. 1, pp. 17–22, Jan 2001.

[23] J. Maget, M. Tiebout, and R. Kraus, "Influence of Novel MOS Varactors on the Performance of a Fully Integrated UMTS VCO in Standard 0.25-μm CMOS Technology," *IEEE J. Solid-State Circuits,* vol. 37, No. 7, pp. 953–958, Jul. 2002.

[24] S. Levantino, C. Samori, A. Bonfanti, S. L. J. Gierkink, A.L. Lacaita, and V. Boccuzzi, "Frequency dependence on bias current in 5-GHz CMOS VCOs: Impact on tuning range and flicker noise upconversion," *IEEE J. Solid-State Circuits,* vol. 37, No. 8, pp. 1003-1011, Aug. 2002.

[25] R. Fujimoto *et al.,* "4.6 GHz CMOS voltage-controlled oscillator," *IEE Electronics Letters,* vol. 38, No. 13, pp.632-633, Jun. 2002.

[26] A. H. Mostafa, M. N. El-Gamal, and R. A. Rafla, "A sub-1–V 4-GHz CMOS VCO and a 12.5-GHz Oscillator for Low-Voltage and High-Frequency Applications," *IEEE Trans. on Circuits and Systems II,* vol. 48, No. 10, pp. 919–926, Oct. 2001.

[27] S. L. J. Gierkink, *et al.* "A Low-Phase-Noise 5-GHz CMOS Quadrature VCO Using Superharmonic Coupling," *IEEE J. Solid-State Circuits,* vol. 38, No. 7, pp. 1148-1154, Jul. 2003.

[28] B. Razavi, "A 2-GHz 1.6 mW phase-locked loop," *IEEE J. Solid-State Circuits,* vol. 32, No. 5, pp. 730–735, May 1997.

[29] B. Razavi, "A study of phase noise in CMOS oscillators," *IEEE J. Solid-State Circuits,* vol. 31, No. 3, pp. 331–343, Mar. 1996.

[30] A. Hajimiri, S. Limotyrakis, and T. H. Lee, "Jitter and phase noise in ring oscillators," *IEEE J. Solid-State Circuits*, vol. 34, No. 6, pp. 790–804, Jun. 1999.

[31] F. N. Hooge, "1/*f* Noise Sources," *IEEE Trans. Electron Devices*, vol. 41, No. 11, pp. 1926–1935, Nov. 1994.

[32] ERC/REC 70-03E, Relating to the Use of Short Range Devices (SRD); CEPT, Apr. 2002.

[33] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge University Press, 1998.

[34] D. B. Leeson, "A simple model of feedback oscillator noises spectrum," in *Proc. IEEE*, vol. 54, pp. 329–330, Feb. 1966.

[35] J. Craninckx, and M. Steyaert, "Low-Noise Voltage-Controlled Oscillators Using Enhanced *LC*-tanks," *IEEE Trans. on Circuits and Systems II*, vol. 42, No. 12, pp. 794–804, Dec. 1995.

[36] K. A. Kouznetsov, and R. G. Meyer, "Phase Noise in LC Oscillators," *IEEE J. Solid-State Circuits*, vol. 35, No. 8, pp. 1244–1248, Aug. 2000.

[37] A. Hajimiri, and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, No. 2, pp. 179–193, Feb. 1998.

[38] A. Hajimiri, and T. H. Lee, "Design issues in CMOS differential *LC* oscillators," *IEEE J. Solid-State Circuits*, vol. 34, No. 5, pp. 717–724, May 1999.

[39] F. X. Kaertner, "Determination of the Correlation Spectrum of Oscillators with Low Noise," *IEEE Trans. Microwave Theory and Techniques,* vol. 37, No. 1, pp. 90–101, Jan. 1989.

[40] C. Samori, A. L. Lacaita, F. Villa, and F. Zappa, "Spectrum folding and phase nose in *LC* tuned oscillators," *IEEE Trans. on Circuits and Systems II,* vol. 45, No. 7, pp. 781–790, Jul. 1998.

[41] C. Samori, A. L. Lacaita, A. Zanchi, S. Levantino, and G. Calì, "Phase noise degradation at high oscillation amplitudes in *LC*-tuned VCO's," *IEEE J. Solid-State Circuits*, vol. 35, No. 1, pp. 96–99, Jan. 2000.

[42] Q. Huang, "Phase Noise to Carrier Ratio in LC Oscillators," *IEEE Trans. on Circuits and Systems I*, vol. 47, No. 7, pp. 965–979, July. 2000.

[43] J. J. Rael, and A. Abidi, " Physical Process of Phase Noise in Differential *LC* Oscillators," in *Custom IC Conf.*, Orlando, FL, pp. 569-572, 2000.

[44] E. Hegazi, H. Sjöland, and A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, No. 12, pp. 896–908, Dec. 2001.

[45] Oscillator Noise Analysis in SpectreRF: Cadence Design Systems, Inc., 2002.

[46] F. Reif, *Fundamentals of Statistical and Thermal Physics*. New York: McGraw-Hill, 1985.

[47] U. L. Rohde, *Microwave and Wireless Synthesizers: Theory and Design*. New York: Wiley-Interscience, 1997.

[48] W. P. Robins, "Phase noise in signal sources," *IEE Telecommunication series 9*, 1991.

[49] A. L. Lacaita, and C. Samori, "Phase-Noise Performance of Crystal-Like LC Tanks," *IEEE Trans. on Circuits and Systems II*, vol. 45, No. 7, pp. 898–900, Jul. 1998.

[50] F. Herzel, M. Pierschel, P. Weger, and M. Tiebout, "Phase Noise in a Differential CMOS Voltage-Controlled Oscillator for RF Applications," *IEEE Trans. on Circuits and Systems II*, vol. 47, No. 1, pp. 11–15, Jan. 2000.

[51] D. Ham, and A. Hajimiri, "Concepts and Methods in Optimization of Integrated LC VCOs," *IEEE J. Solid-State Circuits*, vol. 36, No. 6, pp. 896–908, Jun. 2001.

[52] A. A. Abidi, G. J. Pottie, and W. J. Kaiser. "Power-conscious design of wireless circuits and systems," *Proceedings of the IEEE*, vol. 88, No. 10, pp. 1528-1545, Oct. 2000.

[53] E. Hegazi, H. Sjöland, and A. Abidi, "A filtering technique to lower oscillator phase noise," in *Proc. ISSCC 2001*, pp. 364-365, Feb. 2001.

[54] K. Hoshino, E. Hegazi,J. Rael, and A.A. Abidi, "A 1.5 V, 1.7 mA 700 Hz CMOS LC Oscillator with no Upconverted Flicker Noise," *Proceedings of the European Solid State Circuits Conference, ESSCIRC'01*, Villach, Austria, Sep. 2001

[55] M. Tiebout, "Low-Power Low-Phase-Noise Differentially Tuned Quadrature VCO Design in Standard CMOS," *IEEE J. Solid-State Circuits,* vol. 36, No. 7, pp. 1018-1024, Jul. 2001.

[56] J. G. Proakis, *Communication Systems Engineering.* New Jersey: Prentice-Hall, Inc., 1994.

[57] A. Kral, F. Behbahani, and A. A. Abidi, "RF-CMOS oscillators with switched tuning," in *Custom IC Conf.*, Santa Clara, CA, pp. 555-558, 1998.

[58] B. D. Muer, M. Borremans, M. Steyaert, and G. L. Puma, "A 2-GHz low-phase-noise integrated *LC*-VCO set with flicker-noise upconversion minimization," *IEEE J. Solid-State Circuits*, vol. 35, No. 7, pp. 1034–1038, Jul.. 2000.

[59] C. Jakobson, I. Bloom, and Y. Nemirovsky, "1/f Noise in CMOS Transistors for Analog Applications From Subthreshold to Saturation," *Solid-State Electron,* vol. 42 No. 10, pp. 1807–1817, 1998.

[60] J. N. Burghartz *et al.*, "RF Potential of a 0.18-μm CMOS Logic Device Technology," *IEEE Trans. Electron Devices*, vol. 47, No. 4, pp. 864–870, Apr. 2000.

[61] H. Tian, and A. E. Gamal, "Analysis of 1/f noise in CMOS APS," in *Proceedings of SPIE*, vol. 3965, pp. 168-176, Jan. 2000.

[62] A. van der Ziel, *Noise in Solid State Devices and Circuits.* New York: Wiley, 1986.

[63] C. H. Chen, and M. J. Deen, "Channel Noise Modeling of Deep Submicron MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, No. 8, pp. 1484–1487, Aug. 2002.

[64] ASITIC   Documentation: Grackle   Release, http://rfic.eecs.berkeley.edu/~niknejad/doc-05-26-02/asitic.html, Sep. 2004.

[65] Harmonic Balance Simulation: Agilent Technologies, Feb. 2004.

[66] Y. Nemirovsky, I. Brouk, and C. G. Jakobson, "1/f noise in CMOS transistors for analog applications," *IEEE Trans. Electron Devices*, vol. 48, No. 5, pp. 921–927, May 2001.

[67] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw-Hill, 2001.

[68] F. Behbahani, *et al.*, "A 2.4-GHz Low-IF Receiver for Wideband WLAN in 0.6-μm CMOS—Architecture and Front-End," *IEEE J. Solid-State Circuits*, vol. 35, No. 12, pp. 1908-1916, Dec. 2000.

[69] Ben G. Streetman, *Solid State Electronic Devices*, Ed. 4, Prentice Hall, New Jersey, 1995.

[70] P. Andreani, and H. Sjöland, "Tail current noise suppression in RF CMOS VCOs," *IEEE J. Solid-State Circuits*, vol. 37, No. 3, pp. 342–348, Mar. 2002.

[71] H.-M. Wang, A. Hajimiri, and T. H. Lee, "Comments on "Design Issues in CMOS Differential *LC* Oscillators"[and reply]," *IEEE J. Solid-State Circuits*, vol. 35, No. 2, pp. 286-287, Feb. 2000.

[72] F. Svelto, and R. Castello, "A Bond-Wire Inductor-MOS Varactor VCO Tunable From 1.8 to 2.4 GHz," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, No. 1, pp. 403–407, Jan. 2002.

[73] C. M. Hung, and K. K. O, "A Packaged 1.1-GHz CMOS VCO with Phase Noise of −126 dBc/Hz at a 600-kHz Offset," *IEEE J. Solid-State Circuits*, vol. 35, No. 1, pp. 100-103, Jan. 2000.

[74] A.-S. Porret, T. Melly, C. C. Enz, and E. A. Vittoz, "Design of High-Q Varactors for Low-Power Wireless Applications Using a Standard CMOS Process," *IEEE J. Solid-State Circuits*, vol. 35, No. 3, pp. 337-345, Mar. 2000.

[75] P. Andreani, and S. Mattisson, "On the Use of MOS Varactors in RF VCO's," *IEEE J. Solid-State Circuits*, vol. 35, No. 6, pp. 905-910, Jun. 2000.

[76] P. Andreani, "A comparison between two 1.8 GHz CMOS VCOs tuned by different varactors," in *Proc. 22nd Eur. Solid-State Circ. Conf. (ESS-CIRC)*, The Hague, the Netherlands, pp. 380-383, Oct. 1998.

[77] C. Leifso, J. W. Haslett, and H. G. McRory, "Monolithic Tunable Active Inductor with Independent Q Control," *IEEE Trans. Microwave Theory and Techniques*, vol. 48, No. 6, pp. 1024–1029, Jun. 2000.

[78] W. M. Y. Wong *et al.,*"A Wide Tuning Range Gated Varactor," *IEEE J. Solid-State Circuits*, vol. 35, No. 5, pp. 773-779, May 2000.

[79] E. Hegazi, and A. A. Abidi, "Varactor characteristics, oscillator tuning curves, and AM-FM conversion," *IEEE J. Solid-State Circuits*, vol. 38, No. 6, pp. 1033–1039, Jun. 2003.

[80] R. L. Bunch, and S. Raman, "Large-signal analysis of MOS varactors in CMOS – G_m LC VCOs," *IEEE J. Solid-State Circuits*, vol. 38, No. 8, pp. 1325–1332, Aug. 2003.

[81] G. F. Zhang, and J. L. Gautier, "Broad-band lossless monolithic microwave active floating inductor," *IEEE Microwave Guided Wave Lett.*, vol. 3. pp. 98-100, Apr. 1993.

[82] E. A. M. Klumperink, S. L. J. Gierkink, A. P. van der Wel, and B. Nauta, "Reducing MOSFET $1/f$ noise and power consumption by switched biasing," *IEEE J. Solid-State Circuits*, vol. 35, No. 7, pp. 994–1001, Jul. 2000.

[83] J. Groszkowski, "The Interdependence of Frequency Variation and Harmonic Content, and the problem of Constant-Frequency Oscillators," *Proc. Of the IRE*, vol. 21, No. 7, pp. 958-981, 1934.

[84] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS circuit design, layout, and simulation*. New York: IEEE Press, 1998.

[85] F. Svelto, S. Deantoni, and R. Castello, "A 1.3 GHz Low-Phase Noise Fully Tunable CMOS LC VCO," *IEEE J. Solid-State Circuits*, vol. 35, No. 3, pp. 356-361, Mar. 2000.

[86] A. Dec, and K. Suyama, "A 1.9-GHz CMOS VCO with micromachined electromechanically tunable capacitors," *IEEE J. Solid-State Circuits,* vol. 35, No. 8, pp. 1231–1237, Aug. 2000.

[87] J. Craninckx, and M. S. J. Steyaert, "A 1.8-GHz Low-Phase Noise CMOS VCO Using Optimized Hollow Spiral Inductors," *IEEE J. Solid-State Circuits,* vol. 32, No. 5, pp. 736–744, May 1997.

[88] J. Craninckx, and M. S. J. Steyaert, "A 1.8-GHz CMOS low-phase-noise voltage-controlled oscillator with prescaler," *IEEE J. Solid-State Circuits,* vol. 30, No. 12, pp. 1474–1482, Dec. 1995.

[89] J. Y.-C. Chang, A. A. Abidi, and M. Gaitan, "Large suspended inductors on silicon and their use in a 2-µm CMOS RF amplifier," *IEEE Electron Device Lett.,* vol. 14, No. 5, pp. 246–248, May 1993

[90] A. Rofourgan, J. Rael, M. Rofougan, and A. A. Abidi, "A 900-MHz CMOS LC-oscillator with quadrature outputs," in *ISSCC Dig. Tech. Papers,* San Francisco, CA, pp. 392-393, Feb. 1996.

[91] R. P. Ribas, *et al.,* "Micromachined Microwave Planar Spiral Inductors and Transformers," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, No. 8 pp. 1326–1335, Aug. 2000.

[92] H. Jiang, Y. Wang, J.-L. A. Yeh, and N. C. Tien, "On-Chip Spiral Inductors Suspended over Deep Copper-Lined Cavities," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, No. 12 pp. 2415–2423, Dec. 2000.

[93] E.-C. Park, *et al.,* "Fully Integrated Low Phase-Noise VCOs With On-Chip MEMS Inductors," *IEEE Trans. Microwave Theory and Techniques,* vol. 51, No. 1 pp. 289–296, Jan. 2003.

[94] P. Basedau, and Q. Huan, "A 1-GHz, 1.5V monolithic LC oscillator in 1-µm CMOS," in *Proc. 1994 European Solid-State Circuits Conf.,* Ulm, Germany, pp. 172–175, Sep. 1994.

[95] J. M. Lopez-Villegas, *et al.*, "Improvement of the Quality Factor of RF Integrated Inductors by Layout Optimization," *IEEE Trans. Microwave Theory and Techniques,* vol. 48, No. 1, pp. 76–83, Jan. 2000.

[96] K. Van Schuylenbergh. *et al.*, "Low-Noise Monolithic Oscillator with an Integrated Three-Dimensional Inductor," in *ISSCC Dig. Tech. Papers*, San Francisco, CA, Feb. 2003.

[97] C. P. Yue, and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE J. Solid-State Circuits,* vol. 33, No. 5, pp. 743–752, May 1998.

[98] D. Halliday, R. Resnick, and J. Walker, *Fundamentals of Physics, 4th ed.*, New York: Wiley, 1997.

[99] H. A. Wheeler, " Simple inductance formulas for radio coils,: in *Proc. IRE*, vol. 16, No. 10, pp. 1398–1400, Oct. 1928.

[100] S. S. Mohan, M. del M. Hershenson, S. P. Boyd, and T. H. Lee, "Simple Accurate Expressions for Planar Spiral Inductances," *IEEE J. Solid-State Circuits,* vol. 34, No. 10, pp. 1419–1424, Oct. 1999.

[101] S. Jenei, B. K. J. C. Nauwelaers, and S. Decoutere, "Physics-Based Closed-Form Inductance Expression for Compact Modeling of Integrated Spiral Inductors," *IEEE J. Solid-State Circuits,* vol. 37, No. 1, pp. 77–80, Jan. 2002.

[102] D. M. Pozar, *Microwave Engineering, 2nd ed.*, USA: John Wiley, 1997.

[103] Y. Cao, *et al.*, "Frequency-Independent Equivalent-Circuit Model for On-Chip Spiral Inductors," *IEEE J. Solid-State Circuits,* vol. 38, No. 3, pp. 419–426, Mar. 2003.

[104] C. P. Yue, and S. S. Wong, "A Physical model for planar spiral inductors on silicon," *IEEE Trans. Electron Devices*, vol. 47, No. 3, pp. 560-568, Mar. 2000.

[105] S.-M. Yim, T. Chen, and K. K. O, "The Effects of a Ground Shield on the Characteristics and Performance of Spiral Inductors," *IEEE J. Solid-State Circuits,* vol. 37, No. 2, pp. 237–244, Feb. 2002.

[106] TSMC 0.18μm mixed-mode CMOS process manual, 2003.

[107] Peregrine SOS 0.5μm FC CMOS process manual, 2002.

[108] C. De Ranter, and M. Steyaert, "A 0.25μm CMOS 17GHz VCO," *ISSCC Digest of Technical Papers*, pp. 370-371, San Francisco, Feb. 2003.

[109] Y.-H. Cho, S.-C. Hong, and Y.-S. Kwon, "A novel active inductor and its application to inductance-controlled oscillator," *IEEE Trans. Microwave Theory and Techniques*, vol. 45, No. 8, pp. 1208–1213, Aug. 1997.

[110] E. Xiao, J. S. Yuan, and H. Yang, "Hot-Carrier and Soft-Breakdown Effects on VCO Performance," *IEEE Trans. Microwave Theory and Techniques*, vol. 50, No. 11 pp. 2453–2458, Nov. 2002.

[111] M. N. Ericson, J.M. Rochelle, C.L. Britton, B.J. Blalock, A. Wintenberg, and D.M. Binkley, "Flicker Noise Behavior of MOSFETs Fabricated in 0.5-micron Fully-Depleted (FD) Silicon-on-Sapphire (SOS) CMOS In Weak, Moderate, and Strong Inversion," *IEEE Trans. on Nuclear Science*, vol. 50, No. 4, pp. 963-968, Aug. 2003.

[112] T. Y. Kim, A. Adams, and N. Weste, "High performance SOI and bulk CMOS 5 GHz VCOs" *in 2003 IEEE RFIC Symp. Dig.*, pp. 93-96, Jun. 2003.

[113] J. C. Rautio, and V. Demir, "Microstrip Conductor Loss Models for Electromagnetic Analysis," *IEEE Trans. Microwave Theory and Techniques*, vol. 51, No. 3 pp. 915–921, Mar. 2003.

[114] R. Horton, B. Easter, and A. Gopinath, "Variation of microstrip losses with thickness of strip," *Electron Lett.*, vol. 7, No. 17, pp. 490–491, Aug. 1971.

[115] M. Konno, "Conductor loss in thin-film transmission lines," *Electronics and Communications in Japan*, pt. 2, vol. 82, No. 10, pp. 83–91, 1999. translated from *Denshi Joho Tsushin Gakkai Ronbunshi*, vol. J81-C-1, No. 8, pp. 466–473, Aug. 1998.

[116] W. Heinrich, "Full-wave analysis of conductor losses on MMIC transmission lines," *IEEE Trans. Microwave Theory and Techniques*, vol. 38, No. 10, pp. 1468–1472, Oct. 1990.

APPENDIX

Calculation of g_{ds} and $G_{ds.eff}$

The transistor drain current i_{DS} in Fig. 3.2 is a sum of a DC bias drain current component (I_{DS}) and a small-signal AC component (i_{ds}) as in the equation below.

$$i_{DS} = I_{DS} + i_{ds} \tag{A.1}$$

Likewise, the drain-source potential of the transistor can be written as

$$v_{DS} = V_{DS} + v_{ds} \tag{A.2}$$

v_{ds} is in most cases is quite sinusoidal, because the waveform distortions caused by the transistor nonlinearity is readily suppressed by the LC tuned circuit. Therefore, V_{DS} is very close to the arithmetic time-average of v_{DS} in most cases.

However, i_{DS} is not always sinusoidal. Its harmonic content is strongly affected by the transistor nonlinearity, especially at larger bias voltages. Therefore, I_{DS} is not always equal to the time-average of i_{DS}, as it can be seen from Fig. 3.2.

Therefore, when calculating the single-sided g_{ds} of a cross-coupled pair with (A.3), it is important that the value for I_{DS} is taken from the value of i_{DS} when v_{DS} is equal to V_{DS} rather than taking the time-average of i_{DS}.

$$g_{ds} = \frac{i_{ds} - I_{DS}}{v_{ds} - V_{DS}} \tag{A.3}$$

For the calculation of the $G_{ds.eff}$, the following fact is acknowledged that the energy lost per cycle in the passive tank must equal to the energy restored by the cross-coupled pair.

$$E_{lost/cycle} = E_{restored/cycle} \qquad (A.4)$$

where

$$E_{lost/cycle} = \int_0^T \frac{v_{ds}^2(t)}{R_{tank}} dt \qquad (A.5)$$

and

$$E_{restored/cycle} = \int_0^T v_{ds}^2(t) g_{ds}(t) dt \qquad (A.6)$$

Therefore,

$$\int_0^T \frac{v_{ds}^2(t)}{R_{tank}} dt = \int_0^T v_{ds}^2(t) g_{ds}(t) dt \qquad (A.7)$$

$$\Rightarrow \frac{1}{R_{tank}} \int_0^T v_{ds}^2(t) dt = \int_0^T v_{ds}^2(t) g_{ds}(t) dt \qquad (A.8)$$

$$\Rightarrow \frac{1}{R_{tank}} = \frac{\int_0^T v_{ds}^2(t) g_{ds}(t) dt}{\int_0^T v_{ds}^2(t) dt} \qquad (A.9)$$

Realizing $G_{ds.eff} = 1/R_{tank}$, (A.9) is the correct expression for $G_{ds.eff}$ rather than simply time-averaging g_{ds}.