Memristive Devices and Circuits for Computing, Memory, and Neuromorphic Applications

by

Omid Kavehei

- B. Eng. (Computer Systems Engineering, Honours) Arak Azad University, Iran, 2003
- M. Eng. (Computer Architectures Engineering, Honours) Shahid Beheshti University, Iran, 2005

Thesis submitted for the degree of

Doctor of Philosophy

in

School of Electrical & Electronic Engineering Faculty of Engineering, Computer & Mathematical Sciences The University of Adelaide, Australia

December, 2011

Supervisors:

Dr Said Al-Sarawi, School of Electrical & Electronic Engineering Prof Derek Abbott, School of Electrical & Electronic Engineering

> CENTRE FOR HIGH PERFORMANCE INTEGRATED TECHNOLOGIES AND SYSTEMS



© 2011 Omid Kavehei All Rights Reserved

Contents

Conten	ts	iii
Abstrac	ct	vii
Statem	ent of Originality	ix
Acknow	vledgements	xi
Conven	itions	xv
Publica	tions	xvii
List of	Figures	xxi
List of	Tables	xxv
Chapte	r 1. Introduction	1
1.1	Definition of memristor	3
1.2	Applications of memristor	5
1.3	Prospects for memristors	7
1.4	Thesis outline	8
1.5	Summary of original contributions	11
Chapte	r 2. Memristor and Memristive Devices	13
2.1	Introduction	15
2.2	Memristor and memristive devices	15
	2.2.1 Memristive devices within Chua's periodic table	16
	2.2.2 Properties and fundamentals	16
2.3	Emerging non-volatile memory technologies	22
	2.3.1 Significance	22
	2.3.2 Phase change memory (PCM)	23

Contents

	2.3.3	Magnetic RAM	23
	2.3.4	Resistive RAM (RRAM)	23
	2.3.5	Discussion of memory technologies	25
2.4	A revi	iew of the memristor	25
2.5	Concl	usion	30
Chapte	r 3. M	emristor's Basic Characteristics and Early Modelling Approaches	31
3.1	Introd	luction	33
3.2	Linea	r drift model	33
3.3	Nonli	near drift model	39
	3.3.1	Window function	41
3.4	Basic	SPICE macro-model of memristor	44
3.5	Concl	usion	50
Chapte	r 4. M	aterials for Memristive Devices	51
4.1	Introd	luction	53
4.2	Mater	ials	53
4.3	Pt/Ti	O_2/Pt memristor	54
	4.3.1	Layer definitions for a $Pt/TiO_2/Pt$ memristor $\ldots \ldots \ldots$	58
4.4	Ag/T	iO_2/ITO memristor	59
4.5	Concl	usion and potential extensions	63
Chapte	r 5. M	emristive Macromodel and SPICE Implementation	65
5.1	Introd	luction	67
5.2	Memr	istor modelling and characterisation	67
5.3	Progr	ession of memristor modelling	70
5.4	Propo	sed model for memristor dynamic behaviour	73
	5.4.1	Comparison of models	77
	5.4.2	Analogue characterisation	82
5.5	Measu	rements and <i>I-V</i> modelling	82
5.6	Comp	lementary resistive switch	85
	5.6.1	Complementary resistive switch modelling	90
	5.6.2	CRS measurement using Ag/TiO ₂ /ITO memristor $\ldots \ldots$	95
5.7	Concl	usion and potential extensions	95

Chapte	r6. Sy	rstem Overview	99
6.1	Introd	luction	01
6.2	CMOS	S image sensor	02
	6.2.1	Pulse-width modulation sensor	04
	6.2.2	Pulse-frequency modulation sensor	08
6.3	Patter	n matching system	16
6.4	Concl	usion and extensions	18
Chapte	r 7. M	emristors from Architectural Overview 12	21
7.1	Introd	luction	23
7.2	Cross	oar memory array	24
7.3	Simul	ations of the crossbar array 13	30
	7.3.1	Statistical analysis	33
7.4	Discu	ssion	35
7.5	Concl	usion and potential extensions	39
Chapte	r 8. As	ssociative Memory 14	41
Chapte 8.1	r <mark>8. A</mark> s Introd	uction	41 43
Chapter 8.1 8.2	r 8. A s Introd Conve	ssociative Memory 14 luction 14 entional CAM and MCAM structures 14	41 43 43
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1	ssociative Memory 14 luction 14 entional CAM and MCAM structures 14 Conventional content addressable memory 14	41 43 43 44
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2	ssociative Memory 14 huction 14 entional CAM and MCAM structures 14 Conventional content addressable memory 14 Generic memristor-nMOS circuit 14	41 43 43 44 45
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3	ssociative Memory 14 luction 14 entional CAM and MCAM structures 14 Conventional content addressable memory 14 Generic memristor-nMOS circuit 14 MCAM Cell 14	 41 43 43 44 45 47
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4	ssociative Memory 14 luction 14 entional CAM and MCAM structures 14 Conventional content addressable memory 14 Generic memristor-nMOS circuit 14 MCAM Cell 14 Simulation results analysis and comparison 14	 41 43 43 44 45 47 48
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5	ssociative Memory 14 luction 14 entional CAM and MCAM structures 14 Conventional content addressable memory 14 Generic memristor-nMOS circuit 14 MCAM Cell 14 Simulation results analysis and comparison 14 Simulation results analysis 14	 41 43 43 44 45 47 48 52
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6	ssociative Memory14luction14entional CAM and MCAM structures14Conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis14A 2 × 2 MCAM structure verification15	 41 43 43 44 45 47 48 52 54
Chapte 8.1 8.2	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6 8.2.7	ssociative Memory14luction14entional CAM and MCAM structures14Conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis14A 2 × 2 MCAM structure verification15Physical layout15	 41 43 43 44 45 47 48 52 54 54
Chapter 8.1 8.2 8.3	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6 8.2.7 CRS-b	associative Memory14Auction14entional CAM and MCAM structures14Conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis14A 2 × 2 MCAM structure verification15Physical layout15wased B/TCAM15	 41 43 43 44 45 47 48 52 54 54
Chapter 8.1 8.2 8.3	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6 8.2.7 CRS-b 8.3.1	ssociative Memory14luction14entional CAM and MCAM structures14Conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis15A 2 × 2 MCAM structure verification15Physical layout15vased B/TCAM15Memristive arrays and scalability15	 41 43 43 44 45 47 48 52 54 54 54 56
Chapte 8.1 8.2 8.3	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6 8.2.7 CRS-b 8.3.1 8.3.2	associative Memory14Auction14entional CAM and MCAM structures14Conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis15A 2 × 2 MCAM structure verification15Physical layout15wased B/TCAM15Memristive arrays and scalability15CRS read-out methods and material implication15	 41 43 43 44 45 47 48 52 54 54 56 57
Chapter 8.1 8.2 8.3	r 8. As Introd Conve 8.2.1 8.2.2 8.2.3 8.2.4 8.2.5 8.2.6 8.2.7 CRS-b 8.3.1 8.3.2 8.3.3	ssociative Memory14Juction14entional CAM and MCAM structures14conventional content addressable memory14Generic memristor-nMOS circuit14MCAM Cell14Simulation results analysis and comparison14Simulation results analysis14A 2 × 2 MCAM structure verification15Physical layout15Memristive arrays and scalability15CRS read-out methods and material implication15Proposed CRS-based CAM cell15	 41 43 43 44 45 47 48 52 54 54 54 56 57 59

Contents

Chapter	9. Computing with Memristive Devices	165
9.1	Introduction	167
9.2	Digital in-situ computing	168
	9.2.1 CRS-based logical operations	168
9.3	Analogue memory and computing	171
	9.3.1 Memristor device characteristics for analogue computing	171
	9.3.2 Muti-stable state memory	174
	9.3.3 Existence of a threshold-like switching	175
	9.3.4 Memristive, plasticity, and learning	175
	9.3.5 Programmable analogue circuits	176
9.4	Conclusion and future work	178
Chapter	10.Summary and Future Work	181
10.1	Part I—modelling and fabrication	183
10.2	System overview	189
10.3	Part II—nanocrossbar array properties and memristive-based memory	
	and computing	191
Append	ix A. Electromagnetic Theory of Memristors	197
A.1	The link to Maxwell's equations	199
	A.1.1 Resistance in the Maxwell picture	200
	A.1.2 Questions surrounding the 4^{th} element $\ldots \ldots \ldots \ldots \ldots$	200
A.2	Quasi-static expansion of Maxwell's equations	201
	A.2.1 Derivation of memristor category	203
A.3	Quasi-static expansion of Maxwell's equations using geometric algebra .	204
Referen	ces	207
Glossary	/	223
Acronyr	ns	225
Index	:	229
Biograp	hy	233

Abstract

A memristor, *memory resistor*, is a two-terminal nanodevice that can be made as thin as a single-atom-thick that has become of tremendous interest for its potential to revolutionise electronics, computing, computer architectures, and neuromorphic engineering. This thesis encompasses two major parts containing original contributions, (**Part I**) modelling and fabrication, and (**Part II**) circuit application and computing. Each part contains three chapters. The fundamentals necessary for understanding the main idea of each chapter are provided therein. A background chapter revolving around memristors and memristive devices is given. A system overview links the two parts together. A brief description of the two parts is as follows:

- **Part I—modelling and fabrication** is relevant to modelling and fabrication of memristors. A basic modelling approach following the early modelling by Hewlett-Packard is presented and tested with several simple circuits. Memristor fabrication process and materials are discussed and two different fabrication runs along with initial measurement results are presented. SPICE modelling for two memristive devices, (i) the memristor and (ii) the complementary resistive switch are also provided.
- **Part II—nanocrossbar array and memristive-based memory and computing** provides an analytical approach for crossbar arrays based on memristive devices. Proposed designs for memristor-based content addressable memories and their analysis are given. This part provides a binary/ternary content addressable memory structure based on a new complementary resistive switch. A number of fundamental building blocks for analogue and digital computing are also presented in this section. The observation of implementing a learning process based on a pair of spikes is also shown and an extension of such a process to a relatively large scale structure based on SPICE simulation is reported.

In addition to these original contributions, the thesis offers an introductory background on memristors, in the area of materials and applications. The thesis also provides a system overview of the targeted system (a CMOS-memristor imager system), which provides a the link between the two parts of the thesis. In addition to the original contributions in the area of modelling and characterisation, an overview on the understanding of the memristor element via the quasistatic expansion of Maxwell's equations is discussed.

Statement of Originality

This work contains no material that has been accepted for the award of any other degree or diploma in any university or other tertiary institution to Omid Kavehei and, to the best of my knowledge and belief, contains no material previously published or written by another person, except where due reference has been made in the text.

I give consent to this copy of the thesis, when deposited in the University Library, being available for loan, photocopying, and dissemination through the library digital thesis collection, subject to the provisions of the Copyright Act 1968.

I also give permission for the digital version of my thesis to be made available on the web, via the Universitys digital research repository, the Library catalogue, the Australasian Digital Thesis Program (ADTP) and also through web search engines, unless permission has been granted by the University to restrict access for a period of time.

December 28, 2011

Signed

Date

Acknowledgements

The research presented in this thesis has been carried out in the School of Electrical and Electronic Engineering at the University of Adelaide. The path towards this thesis spans three years of a multidisciplinary research covering nanoelectronics, materials engineering, and circuit design. It has been an honour and great privilege to be the first Ph.D. student on the emerging topic of memristive devices and systems in Australia at a university with a solid and strong background in microelectronics. From the outset, many people have been involved and have contributed to the presented ideas and understanding gained. I gratefully acknowledge those who have helped along the way and influenced the formation of the understanding and the approach to representation of materials presented in this thesis.

First and foremost I would like to express my gratitude to my principle supervisor, Dr Said Al-Sarawi. He greatly helped with his open and respectful attitude toward science and technology. He provided me with his quick, thoughtful, effective, and also critical comments upon the drafts. I would like to gratefully acknowledge enthusiastic supervision and encouraging attitude of my co-supervisor, Prof Derek Abbott, who inspired me with his wide range of interests and unconventional thinking, which most of the time turn 'impossible' to be feasible. I appreciate all their contributions, time, ideas, strict requirements, funding, and answering quickly all questions I had about topics of their expertise to make my Ph.D. experience productive and stimulating.

Another key person whom I am strongly indebted to is Prof Kamran Eshraghian. He has been a great influential mentor to my scientific career throughout the past three years. His way of thinking inspires me to approach problems in different ways. I wish to express my deep gratitude for his continued encouragement and invaluable suggestions during this work. He provided me with direction, technical support and became more of a mentor and friend, than an advisor. I would also like to include my gratitude to Profs Kyoungrok Cho, Younggap You, Yeong-Seuk Kim, and Sung-Jin Kim, at Chungbuk National University, Cheongju, South Korea, who have enabled part of this research work together with Prof Eshraghian.

I wish to express my warm and sincere thanks to Drs Sharath Sriram, Madhu Bhaskaran, and Prof Arnan Mitchell at the Functional Materials and Microsystems Research Group at RMIT University, Melbourne, Australia, for their fabrication support and thoughtful discussions.

I am indebted to Drs Azhar Iqbal and Nicolangelo Iannella, outstanding scholars at the University of Adelaide, for their kindness, passionate, and patience in discussing long hours around different research issues and also their critical suggestions. I also benefited by works of Drs Azhar Iqbal and James M. Chappell on electromagnetic theory of the memristor. I owe to other great scholars at the university, including Prof Reg Coutts, Assoc Profs Christophe Fumeaux, Cheng Chew Lim, and Drs Withawat Withayachumnankul, Yingbo Zhu, Akhilesh Verma, Thomas Kaufmann, Andrew Allison, Shaghik Atakaramians, Gretel M. Png, and Ajay Tikka for their useful scientific and technical discussions. Drs Jegathisvaran 'Jega' Balakrishnan, Don Wenura Dissanayake and Mr Muammar Kabir also provided me with their Ph.D. thesis IAT_EX style files, which has tremendously helped me in preparing this dissertation. I would like to, again, thank Mr Muammar Kabir for his tremendous help for assisting for printing of this thesis while I was in Melbourne.

I also acknowledge help and support Prof Sung Mo Kang and Dr Sangho Shin at the University of California, Merced, through answering questions and providing valuable comments on several topics related to memristive devices. I also acknowledge Profs Yael Nemirovsky and Amine Bermak help and openness in answering my questions regarding image sensors.

Looking back at my *alma mater*, I am surprised and at the same time very grateful for all I have achieved. I can by no means thank Assoc Prof Keivan Navi enough for all the hope he has put on me, before I thought I could do any research at all. It has certainly shaped me as researcher and has led me where I am now. Other scholars who contributed to my academic background are Drs Omid Hashemipour, Tooraj Nikoubin, Ali Zaker-Alhosseini, Islam Nazemi, Mohammad Eshghi, Mohammad Javad Sharifi, Namdar Saniei, Ramak Ghavami Zadeh, Farshad Safaei, Ali Jahanian, Ali Movaghar Rahimabadi, Mohammad Taghi Manzuri Shalmani, Somayeh Timarchi, Ebrahim Afjei, and Fereidoon Shams. A very special thanks goes out to Mr Ron Seidel for his invaluable suggestions, motivation, encouragement, scientific discussions, and sharing his life experiences, and Mrs Marilyn Seidel for her kindness and general support.

During my candidature, administrative work has been assisted by Rose-Marie Descalzi, Colleen Greenwood, Ivana Rebellato, Stephen Guest, Danny Di Giacomo, Philomena Jensen-Schmidt, and Gail Hemmings. Other supporting people include the technical officers, Ian Linke and Pavel Simcik, and the IT support officers, David Bowler, Greg Pullman, Ryan King, and Mark J. Innes. It became normal for David to receive an email from me every day and I am deeply indebted to his supportive attitude and patience in providing and setting up all the CAD tools used in this dissertation.

I would also like to thank friends and colleagues, including Sang Jin Lee, an incredible friend who provided so much help during my visit to South Korea, Soon-Ku Kang, for his help on memristive-based content addressable memory, Shiva Balendhran, Charan Manish, and Guanrong Xu, for their support during my visit from RMIT and providing technical fabrication support, Seok-Man Kim, Hyeon-Seok Na, and Kyung-Chang Park, for their useful discussions around technical issues, Shahar Kvatinsky, for his critical review on the crossbar structure, Robert Moric, Benjamin Ung, Hungyen Lin, Ali Karami, Henry Ho, Shaoming Zhu, Hui Min Tan, Darryl Bosch, and Yik Ling Lim, for making such a friendly research environment. I should also thank Hossein Pishgar for his effective collaboration in building a technical ground for CAD tools at my *alma mater*, which helped me a lot.

I recognise that this research would not have been possible without the financial assistance of Australian Government via Endeavour International Postgraduate Scholarship (EIPRS) and the University of Adelaide Scholarship for Postgraduate Research. Travel grants and awards were from the School of Electrical & Electronic Engineering (the University of Adelaide), the D.R. Stranks Postgraduate Travelling Fellowship, Research Abroad Scholarship, World Class University program (South Korea) through the Chungbuk National University, and the Australia's Defence Science and Technology Organisation (DSTO) through the Simon Rockliff Supplementary Scholarship.

Beyond memristors, my wife and I are in indebted to our lovely Australian friends, in particular, Marie and Peter Wood, and Anne Spencer. We are extremely grateful for everything they have done to us. It is just impossible to put into words how much energy and happiness they have brought into our lives.

Acknowledgements

My endless appreciation goes to my family, my mother, my father, and my brothers, who always endow me with infinite support, wishes, continuous love, encouragement, and patience. I would like to thank my mother- and father-in-law for their guidances and wishes.

Last but not least, the warmest thank to my dear wife, *Taraneh*. I dedicate this dissertation to her not just because she has given up so much to make my career a priority in our lives, but for being a truly wonderful friend during the entire amazing journey with me.

O. Kavehei

Conventions

- **Referencing** The Harvard style is used for referencing and citation in this thesis.
- **Spelling** Australian English spelling is adopted, as defined by the Macquarie English Dictionary (Delbridge 2001).
- **System of units** The units comply with the international system of units recommended in an Australian Standard: AS ISO 1000—1998 (Standards Australia Committee ME/71, Quantities, Units and Conversions 1998).
- **Physical constants** The physical constants comply with a recommendation by the Committee on Data for Science and Technology: CODATA (Mohr and Taylor 2005).

Publications

Journal publications

- **KAVEHEI-O.**, AL-SARAWI-S.F., CHO-K.R., ESHRAGHIAN-K., AND ABBOTT-D. (2011). An analytical approach for memristive nanoarchitectures, *IEEE Transactions on Nanotechnology*, (Accepted on 28th October, 2011), *arXiv preprint: 1106.2927.**
- **KAVEHEI-O.**, IQBAL-A., KIM-Y.S., ESHRAGHIAN-K., AL-SARAWI-S.F., AND ABBOTT-D. (2010). The fourth element: characteristics, modelling and electromagnetic theory of the memristor, *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Science*, **466**(2120), pp. 2175–2202.*
- ESHRAGHIAN-K., CHO-K.R., KAVEHEI-O., KANG-S.K., ABBOTT-D., AND KANG-S.M.S. (2011). Memristor MOS content addressable memory (MCAM): Hybrid architecture for future high performance search engines, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 19(8), pp. 1407–1417.*
- ESHRAGHIAN-K., **KAVEHEI-O.**, CHO-K.R., CHAPPELL-J., IQBAL-A., AL-SARAWI-S.F., AND ABBOTT-D. (2012). Memristive device fundamentals and modeling: Applications to circuits and systems simulation, *Proceedings of the IEEE*, accepted.*
- LEE-S., **KAVEHEI-O.** HONG-Y., CHO-T., YOU-Y., CHO-K.R., AND ESHRAGHIAN-K. (2007). 3-D system-on-system (SoS) biomedical-imaging architecture for health-care applications, *IEEE Transactions on Biomedical Circuits and Systems*, **4**(6), pp. 426–436.*
- NAVI-K., **KAVEHEI-O.**, RUHOLAMINI-M., SAHAFI-A., MEHRABI-S., AND DADKHAHI-N. (2008). Low-power and high-performance 1-bit CMOS full-adder cell, *Journal of Computers*, **3**(2), pp. 48–54.
- MOLAHOSSEINI-A.S., NAVI-K., DADKHAH-C., **KAVEHEI-O**. AND TIMARCHI-S. (2010). Efficient reverse converter designs for the new 4-moduli sets $\{2^n 1, 2^n, 2^n + 1, 2^{2n+1} 1\}$ and $\{2^n 1, 2^n + 1, 2^{2n}, 2^{2n} + 1\}$ based on new CRTs, *IEEE Transactions on Circuits and Systems I: Regular Papers*, **57**(4), pp. 823–835.
- NAVI-K., MAEEN-M., FOROUTAN-V., TIMARCHI-S., AND **KAVEHEI-O.** (2009). A novel low-power full-adder cell for low voltage, *Integration, the VLSI Journal*, **42**(4), pp. 457–467.
- TIMARCHI-S., **KAVEHEI-O.** AND NAVI-K. (2008). Low power modulo $2^n + 1$ adder based on carry save diminished-one number system, *American Journal of Applied Sciences*, **5**(4), pp. 312–319.
- NAVI-K., FOROUTAN-V., AZGHADI-M.R., MAEEN-M., EBRAHIMPOUR-M., KAVEH-M., AND KAVEHEI-O. (2009). A novel low-power full-adder cell with new technique in designing logical gates based on static CMOS inverter, *Microelectronics Journal*, **40**(10), pp. 1441–1448.

- MOAIYERI-M.H., MIRZAEE-R.F., NAVI-K., NIKOUBIN-T., AND **KAVEHEI-O**. (2010). Novel direct designs for 3-input XOR function for low-power and high-speed applications, *International Journal of Electronics*, **97**(6), pp. 647–662.
- NAVI-K., SAJEDI-H.H., MIRZAEE-R.F., MOAIYERI-M.H., JALALI-A., AND **KAVEHEI-O.** (2011). Highspeed full adder based on minority function and bridge style for nanoscale, *Integration, the VLSI Journal*, 44(3), pp. 155—162.
- AZGHADI-M.R., **KAVEHEI-O.** AND NAVI-K. (2007). A novel design for quantum-dot cellular automata cells and full adders, *Journal of Applied Sciences*, 7(22), pp. 3460–3468.

Conference publications

- **KAVEHEI-O.**, KIM-Y., IQBAL-A., ESHRAGHIAN-K., AL-SARAWI-S.F., AND ABBOTT-D. (2009). The fourth element: Insights into the memristor, *IEEE International Conference on Communications, Circuits and Systems, ICCCAS*, pp. 921–927.*
- **KAVEHEI-O.**, CHO-K.R., LEE-S., KIM-S., AL-SARAWI-S.F., ABBOTT-D., AND ESHRAGHIAN-K. (2011). Fabrication and modeling of Ag/TiO₂/ITO memristor, *54*th *IEEE International Midwest Symposium on Circuits and Systems, MWSCAS*, pp. 1-4.*
- KAVEHEI-O., AL-SARAWI-S.F., CHO-K.R., IANNELLA-N., KIM-S., ESHRAGHIAN-K., AND ABBOTT-D. (2011). Memristor-based synaptic networks and logical operations using in-situ computing, International Conference Series on Intelligent Sensors, Sensor Networks and Information Processing, ISSNIP, (Accepted on 26th September, 2011), arXiv preprint: 1108.4182.*
- KAVEHEI-O., LEE-S., CHO-K.R., AL-SARAWI-S.F., ESHRAGHIAN-K., AND ABBOTT-D. (2011). Integrated Memristor-MOS (M²) Smart Sensor for Basic Pattern Matching Applications, International Conference on Advanced Electromaterials, ICAE, (Accepted on 5th August, 2011).*
- KAVEHEI-O., LEE-S., CHO-K.R., AL-SARAWI-S.F., AND ABBOTT-D. (2011). Analysis of Pulse-Frequency Modulation CMOS Image Sensors, International Conference on Advanced Electromaterials, ICAE, (Accepted on 5th August, 2011).*
- **KAVEHEI-O.**, AL-SARAWI-S.F., ABBOTT-D., AND NAVI-K. (2008). High-performance bridge-style full adder structure, *Proceedings of SPIE*, **7268**, pp. 72680D.
- KAVEHEI-O., AZGHADI-M.R., NAVI-K., AND MIRBAHA-A.P. (2008). Design of robust and highperformance 1-bit CMOS Full Adder for nanometer design, *IEEE Computer Society Annual Symposium on VLSI, ISVLSI*, pp. 10–15.
- KAVEHEI-O., NAVI-K., NIKOUBIN-T., AND ROUHOLAMINI-M. (2006). A novel DCVS tree reduction algorithm, IEEE International Conference on Integrated Circuit Design and Technology, ICICDT, pp. 1–7.
- **KAVEHEI-O.**, MIRBAHA-A.P., DADKHAHI-N., AND NAVI-K. (2006). Novel architecture for IEEE-754 standard, *IEEE Conference on Information and Communication Technologies, ICTTA*, **2**, pp. 2601–2606.
- KAVEHEI-O., AL-SARAWI-S.F., AND ABBOTT-D. (2009). An automated approach for evaluating spatial correlation in mixed signal designs using synopsys HSpice, Synopsys Users Group, SNUG Conference, Singapore. http://tinyurl.com/snugsing09
- ROUHOLAMINI-M., KAVEHEI-O., MIRBAHA-A.P., JASBI-S.J., AND NAVI-K. (2007). A new design for 7:2 compressors, IEEE/ACS International Conference on Computer Systems and Applications, pp. 474–478.
- NAVI-K., **KAVEHEI-O.**, ROUHOLAMINI-M., SAHAFI-A., AND MEHRABI-S. (2007). A novel CMOS full adder, *International Conference on VLSI Design*, *VLSID*, pp. 303–307.

- TIMARCHI-S., NAVI-K., AND **KAVEHEI-O.** (2009). Maximally redundant high-radix signed-digit adder: new algorithm and implementation, *IEEE Computer Society Annual Symposium on VLSI*, *ISVLSI*, pp. 97–102.
- MIRBAHA-A.P., **KAVEHEI-O.**, ASADI-P., AND NAVI-K. (2006). High-speed arithmetic algorithms for multiple-valued logics in mixed-mode, *IEEE Conference on Information and Communication Technologies*, *ICTTA*, **1**, pp. 1682–1687.
- NAVI-K., **KAVEHEI-O.**, HELMI-M., AND MORAVEJI-R. (2006). Multiple-valued Interconnection Network, *IEEE Conference on Information and Communication Technologies, ICTTA*, **3**, pp. 3151–3155.
- AZGHADI-M.R., **KAVEHEI-O.**, AL-SARAWI-S.F., IANNELLA-N., AND ABBOTT-D. (2011). Tripletbased spike-timing dependent plasticity in silicon, *The 21st Annual Conference of the Japanese Neural Network Society, JNNS*, P3-35.
- AZGHADI-M.R., KAVEHEI-O., AL-SARAWI-S.F., IANNELLA-N., AND ABBOTT-D. (2011). Novel VLSI Implementation for Triplet-based Spike-Timing Dependent Plasticity, International Conference Series on Intelligent Sensors, Sensor Networks and Information Processing, ISSNIP, (Accepted on 26th September, 2011).

Note: Articles with an asterisk (*) are directly relevant to this thesis.

List of Figures

1.1	The 4 th fundamental circuit element	4
1.2	Number of publications with memristor as a keyword	6
1.3	Thesis outline	10

2.1	Periodic table of the fundamental passive circuit elements	17
2.2	A simple schematic for the memristor and illustrating memristive be-	
	haviour	19

3.1	Two bipolar memristors in series	37
3.2	Memristor model and its angular frequency response	38
3.3	RMI simulation	39
3.4	Nonlinear <i>I-V</i> characteristics of the memristor	40
3.5	Window function $f(\cdot)$	42
3.6	Basic SPICE macro model	45
3.7	Basic memristor characteristics of switching between two high and low	
	resistances	46
3.8	Response of the memristor to a step voltage input	46
3.9	Response of the memristor to a sine voltage input	47
3.10	Parallel and serial connections of memristors	48
3.11	Interaction of the memristor with other fundamental elements	49
3.12	An integrator circuit using memristor	50

4.1	Periodic table	55
4.2	Masks for $Pt/TiO_2/Pt$ memristors	56
4.3	Fabrication steps for $Pt/TiO_2/Pt$ memristor	57
4.4	Current-voltage characteristics of the $Pt/TiO_2/Pt$ memristor	58

4.5	Layer definitions for a Pt/TiO ₂ /Pt memristor	59
4.6	Ag/TiO ₂ /ITO memristor	60
4.7	Forming and switching mechanism	62
4.8	Current-voltage characteristics of the Ag/TiO ₂ /ITO memristor \ldots .	63

5.1	Memristor's physical representation	69
5.2	Exponential relation between memristor's conductance and junction	
	width	74
5.3	Proposed model under test	77
5.4	Investigating the impact of the parameter n on the nonlinearity \ldots	78
5.5	Proposed model <i>I-V</i> characteristics in a log-log scale	78
5.6	Memristor response to a number of successive triangular voltages	83
5.7	Memristor operation in its analogue regime	84
5.8	Memristor modelled and measured characteristics	86
5.9	Existence of the metallic filament	89
5.10	Memristor measurement and its model approximation	91
5.11	CRS <i>I-V</i> characteristics	93
5.12	CRS resistance behaviour	94
5.13	CRS response to a sequence of pulses	96
5.14	Three-terminal memistor acting as a CRS	97

6.1	System overview
6.2	PWM CMOS imege sensor
6.3	PWM CMOS imege sensor FPN and output code simulation 107
6.4	Generic schematic of a PFM pixel and circuit implementations 113
6.5	Power consumption analysis of the PFM pixels
6.6	Frequency response of the PFM pixels
6.7	A system overview of the feature generation algorithm
6.8	Projected principal-edge distribution (PPED) algorithm

7.1	Crossbar array and its simplified models	6
7.2	Crosspoint memory element between two plates of bit and word lines . 13	0
7.3	CRS resistance switch from a logic state to ON 13	2
7.4	Voltage pattern across a CRS array 13	2
7.5	Crosspoint cell and patterns for simulations	4
7.6	Variation analysis of memristor and CRS arrays	6

Architecture for content addressable memories
Conventional CAM cell structure and SRAM cell
Memristor-nMOS cell and characteristics
MCAM circuits
MCAM write simulation
MCAM read simulation
Small array of MCAM cells
Layout implementations of memristor-based and SRAM-based CAM cells156
CRS device possible state configuration
CRS-based B/TCAM
Simulation of a 64×8 CRS-based B/TCAM

9.1	CRS-based logic gates and PLA structures
9.2	Peripheral CMOS circuitries for multiplexing
9.3	Two sample gate simulations for CRS-based logic
9.4	Multi-stable state memory existence in the memristor device 174
9.5	Sharp switching behaviour of the memristor
9.6	Synaptic weight evolution in an array of memristors
9.7	A memristor-based multiply-accumulate module for biomimetic appli-
	cations

List of Tables

1.1	Number of patents on RRAM applications 8
2.1	Performance of emerging memory technologies
4.1	RRAMs compared with other major emerging technologies
4.2	Parameters for sputtering 59
5.1	Subcircuit model for memristor
5.2	Memristor models comparison 81
5.3	Parameters for the model
5.4	Physical parameters for filamentary-based modelling of the memristor . 89
5.5	CRS logic and ON states
6.1	Features of fabricated CIS
6.2	CIS performance comparison
7.1	CRS and memristor device parameters
7.2	Crossbar simulation results
8.1	MCAM cells performance
8.2	CRS states
9.1	CRS-based logic gates
A.1	Fundamental circuit elements