Fault Tolerance in VLSI

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B. Sc., B. E. (Hons.)

A thesis submitted to the
Department of Electrical and Electronic Engineering, the
University of Adelaide, to meet the requirements for award of the degree of
Doctor of Philosphy.

December 1988.

Abstract

A primary goal in microelectronic systems progress is the achievement of yet higher levels of functional integration. Today this is being addressed from two different perspectives: Firstly, introducing more circuitry onto the chips themselves and; secondly, packaging the chips in higher performance media.

Wafer-Scale Integration (WSI), whereby the chip assumes the size of a wafer, is one goal that combines elements from both of these perspectives. A purely advanced packaging approach is Hybrid Wafer-Scale Integration (HWSI), or silicon on silicon thin film hybrids. Both of these approaches offer many potential advantages, in terms of speed, reliability, power consumption, packaging density and cost. The potential advantages, as well as the disadvantages, are discussed in detail before a review of current WSI and HWSI projects is presented.

Currently one factor that limits chip size growth are the defects incurred in the production of any integrated circuit. Defect tolerance provides the means to overcome this limitation and is particularly important for the achievement of WSI.

A critical point in evaluating approaches to defect tolerance for VLSI, WSI and Ultra Large Scale Integration (ULSI) is the yield model used. A correct yield model allows the type and amount of the optimal level of defect tolerance to be determined. A yield model is presented here that takes account of both clustering and the influence of the reconfigurable interconnect. Two different approaches are presented which would be used for different modeling applications: yield, and expected number of connected processors. The latter form has a number of advantages. The model is applied to a VLSI signal processing chip, and to a generalized chip, to determine the kind of chip structures that can best benefit from defect tolerance. It is found that in order to benefit from defect tolerance regular structures covering more than 20% to 30% of the chip are required. The yield model is also applied in a consideration of granularity effects on wafer-scale arrays. As a result of this discussion on granularity a new metric is suggested for evaluating array element architectures.

Using this model as a basis, a number of alternative approaches to WSI are presented and evaluated. After a review of existing approaches, during which a suitable classification system is introduced, a new approach, called the "frame" approach is introduced. The frame scheme is aimed at the WSI implementation of 2D arrays, containing reasonably large elements. The design and implementation of WSI and HWSI examples of the "frame" scheme are presented. Practical lessons learnt about implementing WSI and HWSI designs are also discussed.

Finally a detailed comparison of different approaches to implementing 2D arrays in WSI is undertaken. The relative merits of the frame scheme are affirmed in this section. Examples are presented that demonstrate the relative advantages and disadvantages of the various approaches, indicating the important points to be considered when designing wafer scale arrays.

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Acknowledgements

As no man is an island, no PhD thesis is completed in isolation, and I wish to thank all of those who contributed to the environment in which this thesis was built. As many people contributed in one way or another to my finishing of this task, I am sure that you all are not covered. Apologies to those I have missed.

First of all thanks to my supervisor, Kamran Eshraghian, whose boundless enthusiasm and energy, even in the face of adversity, has always impressed me. His paving of the road to the end of this task is much appreciated. Thanks also to Pat Clarke, of the Australian Defence Science and Technology Organisation, a true scientist, with a deep curiousity for all things mathematical. I am very grateful to Pat for his suggestions. Now to the last, but not least, of the "Big Three", Stu Tewksbury of AT&T Bell Laboratories. Thanks for providing me the opportunity to work at AT&T Bell Laboratories, and thanks also for your ever ready optimism and help, both inside and outside my thesis.

Now to the team efforts. First of all back to AT&T Bell Laboratories in Holmdel, New Jersey. There a multitude of people gave me help, both technically, and also with the day to day problems of living in a foreign land. First, to Bryan Ackland, and his department. Their help was essential for the production of the "frame" wafers and I also thank them for their general stimulus. In particular I wish to thank Bob Clarke, Jo Othmer, Mehdi Hatamian, Glenn Cash, Jay O'Neill and Adriaan Ligtenberg. Others, at Bell Labs, that deserve to be thanked for their many useful discussions include Larry Hornak, Trevor Little, Tom Wik, Dave Beecham and Vijay Kumar. On the personal side I found many Americans helpful in the often difficult experience of living in the United States. As well as Bryan (who is actually Australian) and Stu I wish to particularly thank Miles Murdocca, Teri Lindstrom and Ruth Dossica (not of AT&T) for their help in this area.

Next to my colleagues here at the University of Adelaide. I wish to thank Micheal Liebelt for his invaluable help with the computing facilities here. I would like to also express my gratitude to Warren Marwood, and the TFB team (in particular John Rockliff, Alex Dickinson, Micheal Pope, Greg Zyner and Syd Fensom) for their stimulus and assistance. Additional thanks to the members of the FES for helping me to survive the PhD process.

Funding for this research was provided by AT&T Bell Laboratories and the Australian Defence Science and Technology Organisation and to them I am grateful.

Finally I would like to express gratitude to my family and to Sandra Whittle for

their critical personal support at various stages of this work.

Preface

I hereby declare that this thesis contains no material which has been accepted for the award of any other degree or diploma in any University and that, to the best of my knowledge and belief, this thesis contains no material previously published or written by another person, except where due reference is made in the text of this thesis. I also consent to this thesis being made available for photocopying and loan.

P.D. Franzon
23 December, 1988.